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Acceleration Management: The Semiconductor Industry Confronts the 21st Century

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Abstract

In the recent generations of semiconductor devices, the semiconductor industry has been accelerating towards the limits of the physical sciences. As a consequence, technology managers in that industry face seven major challenges, which will threaten progress: process, complexity, performance, power, density, productivity, and quality / reliability. We believe that confronting these challenges requires a new approach to technology management both within organizations and between organizations that form the backbone of the industry. We call this new approach Acceleration Management.

Acceleration Management first requires that firms cultivate deep technical knowledge and inspire creative solutions to seemingly insoluble technical problems. The second stage of Acceleration Management requires the necessary expertise to be pooled, which often demands inter-organizational cooperation. This paper explores these managerial imperatives and analyzes how new semiconductor firms--particularly in China--have created niches in the value chain even during a tumultuous time in the industry's history.

I. Introduction

The semiconductor industry's uncanny ability to abide by "Moore's Law," whereby computing power has doubled roughly every 18 months, has transported the industry from a laboratory curiosity to a \$150 billion a year industry. In turn, the semiconductor industry has driven the digital revolution of the last fifty years. At junctures along the evolutionary path of semiconductor technology, technological challenges, labeled "show stoppers," have been encountered. Each time such a show stopper threatened to derail the industry's attainment of Moore's Law, scientists and engineers from around the globe devised clever solutions.

However, as the dimensionality of the circuitry has fallen to "nano" proportions (1 nanometer = one-billionth of a meter), the rate of change of technological challenges has increased dramatically as we document in this paper. Additionally, the internal architectures of chips have, in effect, changed direction. Because of these two dimensions—an increase in the rate of technological change and a change in direction of chip architecture—we label this a period of "acceleration" for the semiconductor industry.

In the recent generations of semiconductor devices, the industry is accelerating towards limits of the physical sciences. Moore's Law addresses the physical dimensions of the circuitry—as the circuitry has diminished in size, computing power has increased. This relentless miniaturization had given rise to seven major challenges that are threatening to derail the industry's progress: Process, Complexity, Performance, Power, Density, Productivity, and Quality and Reliability.

We believe that the acceleration of these challenges requires a new approach to technology management both within organizations and between organizations that form the backbone of the industry. We call this new approach to management: Acceleration Management. Acceleration Management first requires that firms cultivate deep technical knowledge and inspire creative solutions to seemingly insoluble technical problems. The second stage of Acceleration Management requires the necessary expertise to be pooled, which often demands inter-organizational cooperation. This paper explores these managerial imperatives and analyzes how new semiconductor firms—particularly in China—have created niches in the value chain even during such a tumultuous time in the industry's history.

II. Literature Overview of High-Velocity Environments

Previous studies have examined how significant strategic decisions are made in "high-velocity" environments (Bourgeois and Eisenhardt, 1988; Eisenhardt, 1989; Weber, 2002). These environments resemble the environment portrayed in this paper—lots of uncertainty attributable to technology change, demand fluctuations, the competitive

landscape, and regulatory decisions. These studies find that, contrary to prior work in low-velocity settings, a greater quantity of high quality information is processed in shorter time periods by the most successful firms. Furthermore, the successful rapid decision makers use rational decision-making processes and exhibit a greater level of innovativeness.

While some of these findings appear paradoxical—more information used in a short time period for more innovative strategic decisions—they reflect the importance of speed and leadership in high-velocity environments. As these authors point out, a number of business strategies—like an imitation strategy or a fast follower strategy—could lead to bankruptcy. Market saturation by close substitutes or time delays in product release can prove detrimental.

III. Defining Acceleration Management

Acceleration is defined as the rate of change of velocity in a particular time interval. For velocity to change, speed can change or direction can change. We find both types of changes in this stage of the semiconductor industry's evolution. To characterize the change in speed, we focus on the change in the rate of technological change. We first describe how the industry's velocity has been characterized by Moore's Law. We then describe the 7 primary dimensions along which the speed of technological change has increased.

As for the other aspect of acceleration—a change in direction—we analyze how new generations of chips contain novel architectures. While these new architectures appear to “change direction” from previous chip generations, they keep the industry on track to achieve Moore's Law. That is to say that chip performance in terms of computing power is not sacrificed even though the inner-workings of the new chips are quite distinctive.

The Bourgeois and Eisenhardt studies in high-velocity environments mentioned above examined strategic decision-making in the early days of the minicomputer industry. In contrast, our setting is a period of maturity in the semiconductor industry. While maturity may connote stability, the technological challenges that are arising have led the industry to be anything but stable. This instability has led to an acceleration of challenges that merit managerial attention and present new opportunities to potential entrants into the industry.

IV. Abiding by Moore's Law Historically

The semiconductor industry's ability to traverse the high-velocity environment of the past is reflected in its adherence to Moore's Law. The semiconductor industry's unique ability to double the electronic function on a chip roughly every two years while profitably selling these chips at approximately the same price has driven the industry since 1970 as illustrated in Figure 1. However a very significant increase in the pace of

change occurred starting in the mid-1990s. This increase occurred even though the complexity of the product design and manufacturing, as well as the costs of equipment and facilities, were also increasing dramatically. We believe the reason the industry was able to profitably abide by Moore's Law has been because of improvements in the way they managed this rapid technological change, what we call acceleration management. The companies best able to accelerate the profitable introduction and volume manufacturing of new technology gained enormous competitive advantage (Appleyard, et al., 2000; Macher, et al., 1998).

Because of the increased rate of new technology introduction since the 1990s, accompanied by the increasing complexity of the manufacturing and design processes, management issues began to become more important relative to technical issues for the industry. A widely accepted process technology roadmap was central to such management and was created and tracked based on the universally recognized Moore's Law illustrated in Figure 1.

Since the early 1990s, this roadmap, the International Technology Roadmap for Semiconductors (ITRS), has provided the schedule for alignment across chip companies, equipment suppliers, and support industries (Kostoff and Schaller, 2001). An additional and unintended effect of the roadmap was impetus for further acceleration as companies recognized the competitive advantage from beating the published schedule. In fact every update to the roadmap since 1994 has seen a further acceleration relative to the previously published one. Some of these roadmaps and their updates are shown in Figure 2.

The rate of increase in chip density reflected in the ITRS roadmap was limited initially by the industry's ability to improve production yield. By the late 1980s the rate of yield improvement in new manufacturing processes and the high mature process yields that were then attained, led to an increasing emphasis on productivity and a corresponding increasing emphasis on reducing the time to introduce new manufacturing processes. These trends gave rise to managerial imperatives namely yield management and pace-setting development activities.

This acceleration of new technology introduction could not occur in isolation within a particular semiconductor company, but required that the semiconductor support and infrastructure segments, such as semiconductor equipment and mask making, to increase their rate of new technology introductions apace.¹ If an equipment company could not keep up with the rapid new process introductions of the chip companies, they would be replaced. Managing multi-firm coordination has, therefore, become a hallmark of acceleration management.

A management trend during the 1980s and early 1990s, was the decision to "in-source" high value-added capabilities like mask making. Chip companies turned away from external mask-making suppliers. Instead, they either began to acquire their own mask

¹ "Masks" contain the picture of the circuitry that is transferred onto the silicon wafer to make the semiconductor device.

shops or create consortia mask facilities with other semiconductor companies with similar needs. The reason for this reversal was that the external mask suppliers found it increasingly difficult to profitably supply leading-edge masks in a timely enough manner to the chip companies during the crucial stage of new process development.

The managerial capabilities noted above—yield management; pace-setting; multi-firm coordination; and in-sourcing—helped to distinguish the leading semiconductor firms. By the 1990s, as acceleration increased, an overarching managerial imperative became how to cultivate “disciplined creativity.” Disciplined creativity was characterized by balancing a long-range plan for technology and manufacturing planning with short-term decisions that were consistent with that plan. Next generation production process development could be made easier and faster if the current chip generation process was constrained for most synergy with the subsequent generation. While the industry generally carried out long-range planning from its inception, the strategy and management implementation of this planning greatly improved at the leading companies since the early 1990s.

Supporting disciplined creativity was the adoption of better methodologies and procedures for developing new processes and introducing them into volume production. The well-known “copy exactly” methodology pioneered by Intel for new manufacturing processes was one example of such a methodology. Equally striking methodological improvements have been implemented at leading companies over the past decade covering design, design aids, mask-making, process development, yield management, process verification/qualification, and testing.

V. The Technological Challenges behind the Shift from a High-Velocity to an Acceleration Environment

The semiconductor industry’s ability to abide by Moore’s Law started to be called into question in the late 1990s largely due to the technological challenges that were on the horizon. Even though the industry successfully cleared technological hurdles in the past, the looming challenges were thought to be increasingly insurmountable.

Seven Scaling Challenges

Miniaturization has reached an inflection point by 2005. Effects of technology acceleration are visible when looking at the exponentially emerging challenges of computer chip design as the semiconductor industry moves from one silicon process generation to the next. Problems with conventional design flows began to emerge with the 0.35 micron process generation. The difficulties arose because of fundamental physical realities that affect design and manufacturing as processes scale to smaller sizes. With each new process generation, factors that were previously only second- or third-order effects have emerged as significant issues. Figure 3 depicts the accelerating emergence of these design issues.

Advancing from one process generation to the next introduced above is only one dimension of semiconductor product scaling. The six other dimensions of scaling, each of which has also significantly compounded the challenge of semiconductor design and product development, are: power consumption management; cost reduction and control; product complexity; performance improvement; development productivity; and quality and reliability. These accelerating challenges analyzed below are changing not only how engineers design and oversee manufacturing but also how companies need to organize and manage to continue bringing successful new products to market.

Product development challenges resulting from process advancement

Imagine an assembly line in a factory. As chip process generations became more advanced over time, the amount of work performed at a “station” increased. At the 0.25 micron process generation, the conveyor belt between stations slowed down (or got longer) because of increasing resistance and capacitance. This resulted in the “interconnect wires” between logic gates leading to as much as 20% to 80% of the delay across the logic path. The net effect starting at 0.25 micron was that many product developments were delayed due to difficulties learning how to compensate for interconnect delays.

In the 0.18 micron process generation, interconnect complexity increased and two other significant design challenges emerged: signal integrity and power integrity. The remedy for overcoming interconnect delays that required modification to the interconnect wires, actually led to a new problem: capacitive coupling. Capacitive coupling between signals meant that one signal could potentially electrically couple to an adjacent signal and corrupt its intended data value. New methods to detect and reduce these signal integrity violations were required.

The increased resistance required to ease the interconnect delays also effected the distribution of power across chips. Without new power integrity checks, semiconductors could suffer power drops that would reduce the intended performance of the design, something akin to a power brown-out.

In the next generation, 0.13 micron, the intensity of the aforementioned design challenges increased. For example, the average number of signal integrity violations for a given design grew from 30 to about 300 for the 0.13 micron process. At the same time, three new significant design challenges emerged: “in-die variation,” increased leakage power, and the corruption of memory cells.

The first new concern at 0.13 micron was in-die variation. Prior to 0.13 micron, designers could be comfortable that all the circuits on one chip, or “die,” would have the same process characteristics. Consistency of operation across the chip yielded benefits to the designer: one could predict consistent assembly time in the “factory.” Starting with 0.13, the process variation of transistor strengths between different portions of the *same* chip started to vary significantly. The assembly line was no longer predictable!

This complicated the design of clock timing trees. Variations in transistor strength across each die made it more challenging to support a common clock domain. Now, the engineer had to design the chip to be tolerant of logic functions being skewed in timing across different areas of the chip. Portions of the chip that logically operate on the same clock had to be broken into separate clock domains and linked via well-controlled timing interfaces.

The second new challenge was the increase of leakage power. Previously, the power consumed by a chip was primarily associated with the speed of operation and amount of logic computation that occurred at one time. This is called the active power. Leakage power is power that is consumed even when a circuit is at rest. Transistor gates act electrically like water faucets providing current to a digital signal line; however, these water faucets never completely turn off. This leakage power had previously been so small that it was not a big concern.

In the 0.13 micron generation, an 8x increase in leakage power occurred. Leakage power became a component of overall chip power—potentially as much as 20 to 30 percent of chip's power consumption. To provide engineers with a means of reducing leakage power, process engineers created two types of transistors: one which scaled performance normally, but leaked a lot of power and another that was slower, but leaked 10 times less power. To manage power consumption during the design process, engineers needed to learn how to optimize power and use slower, low-leakage transistors where appropriate. Only some companies today have effective and efficient means to utilize both types of transistors in a design. Leakage power will continue to increase by a factor of about 8x across future process generations.

The final significant design issue to emerge on the 0.13 micron process generation was due to shrinking on-chip memories. As on-chip memories fell in size, the amount of electrical energy required to sustain the knowledge in a memory cell decreased exponentially. In 0.13 micron and 90 nanometer generations, memory cells contain such a small level of energy that they can be upset and change state if hit by periodic atomic alpha particles that are emitted by most natural materials. The more memory required in a given design, the higher the probability that a memory cell can be hit by one of these particles. This phenomenon is a huge concern because data integrity must be maintained. Engineers need to take measures that enable a design to operate properly even if memory cells become corrupted.

The design challenges mentioned above are side effects of semiconductor process scaling. Their complexity is accelerating and new issues emerge with every process generation. There are six additional dimensions of scaling that are also experiencing acceleration of issues that have to be solved to successfully bring new semiconductor designs to market.

Power consumption management

In the market place for portable devices, the ability to extend battery life is a key

competitive differentiator. The challenge to manage power during the development process is actually much larger. Each new process generation drives reduction of power supply voltage and cuts the power available for a given design virtually in half. At the same time, companies design, develop, and introduce products that are more capable and have many new features. As a result, it is common to see twice the amount of logic in new semiconductor devices. This in turn doubles the power consumed. Designs are also required to be faster. If the frequency is increased 50%, the power required is also increased by 50%. Add the increase in leakage power noted in the previous section and total power may increase another 50%. The challenge of making products more power efficient has dramatically increased the development challenge.

This issue is even more complex. Due to increasing power in smaller spaces, new technology to cool the devices must be continually innovated, applied, and adapted. Significant mechanical engineering capability is required to enable the continued scaling of electronic devices. Many higher performance devices today have exceeded the thermal density of a standard kitchen hot plate in number of watts dissipated per square centimeter. Many people complain about how hot laptop computers feel on their laps. This thermal density will continue to increase over time.

Cost reduction and control

The cost to develop new semiconductor devices has been increasing over time. Managers must manage the risks associated with new product development to ensure adequate rates of return. Today, engineering costs to initially develop a complex product can be in the \$10M ballpark for 0.13 micron products and in the \$20M range for 90 nanometer products. With each new process generation, the chip area needed to implement the same design is reduced in half. This is an obvious benefit. On the other hand, the cost of making a set of masks is roughly doubling every process generation. Mask costs were about \$300K on the 0.18 micron process generation. At 0.13, mask costs were approximately \$600K. 90 nanometer masks cost roughly \$1.3M and 60nm masks started in the \$2.4M range.

Another critical cost consideration has emerged with increasing complexity. The cost of resources required for functionally validating that a design is free from bugs has emerged to be one of the largest burdens on product development. Debugging now commonly takes from one to two times the number of engineers as it does to design the functionality of a semiconductor device. In addition, trends showing that products are less likely to meet performance requirements on the “first silicon.” Bug fixing, revalidation and retooling can cost as much as half the initial design.

Many semiconductor products today have a life span of about three years and generate \$5M to \$10M in revenue with margins ranging from 20% to 60% or more. Over time, fewer products will be economically feasible as processes advance. To make matters more complicated, product life cycles for many consumer products are shrinking. Cell phones are a perfect example of this trend.

Complexity dimension

With the ability to put twice the function and features on the same chip area with each new process generation, design complexity is exponentially growing. One of the challenging questions is how to use this additional silicon floor space to make products more exciting and also how to stay within emerging design constraints and challenges.

For those that are looking at the power issues described above, they ask how exciting products can be built by increasing the ratio of memory on a chip in the place of logic. Doubling logic will tend to double the power, but power does not increase even linearly with the addition of more memory.

A significant driver of processor design overtime has been the focus on how to execute a “single code stream” faster. This led to accelerating complexity for incrementally more performance. It started with reducing the time to execute an instruction from multiple clocks to one clock; then to pipelining multiple memory accesses in parallel; then to executing multiple instructions per clock in parallel; then to hardware support for switching between more than one stream of code; then to even predicting in advance what instructions might be executed and executing them while waiting for a slower operation in case they would be used. All this creates an exponential increase in complexity that has to be validated and adds to development time.

Performance improvement challenges

Increasing a products performance frequency enables a product to do more in the same amount of time, which enables creating new excitement in future products. While each new process generation provides a performance improvement of about 30%, certain types of products try to sustain performance increases of two times over the prior generation. The additional performance gains beyond those offered by a new process generation require even greater tradeoffs and complexity. One type of performance improvement relies on the implementation of a given logic function with less serial logic between logic clocks, in other words more parallelism.

While parallelism shortens time to execute, it can significantly add to the amount of logic to perform a given function, thus adding to the validation effort. In addition, fewer gates between timing clocks result in a host of circuit issues to deal with. One such issues is called “hold time” that adds to the complexity of the low level design. Also, because the amount of logic operating in parallel for a given function, it exacerbates the power consumed by the device. These are only a few examples of the things that are affected by increasing performance. So pushing performance adds to the inflections that are occurring in all of the other scaling dimensions.

Development productivity, time to market, and product lifetime challenges

To minimize the time to turn out ever more complicated products, there are strategic changes that need to be taken by companies. Some previous examples include increasing

use of modules that are designed to be reused on more than one design. This has led to the emergence of a significant 3rd party intellectual property (IP) industry that specializes in making these “IPs.” Because of the existence of this third party industry, small design houses can compete with larger traditional design companies, which have a lot of resources to develop their own modules. Some estimate that by 2007, as much as 80% of an average chip may consist of reusable IP blocks.

The EDA tool industry is continually trying to keep up with capabilities that support automation of best-known techniques. This implies an increasing amount of accumulated tool capability, as well as required maintenance. At the same time neither the number of customers nor the pools of money, which can be extracted from the industry for CAD tools, is increasing rapidly.

Quality, reliability, and design for manufacturability challenges

With the increasing complexity of advance process manufacturing, the yield of good die on a wafer started to be dominated by systematic failures after the 0.25 micron process. A new inflection has emerged in the effort to maximize yield of good die on a silicon wafer. One approach is to distinguish the areas of a design that are critical to performance or operation. In those areas, one uses normal scaled design rules. However, in other areas, relaxing certain design rules can enhance the yield by increasing margins of error. This is one example of new types of “design for manufacturability” methods that need to be adopted to increase competitiveness.

Today, there is significant technology being developed to support improved chip performance by analyzing in-die variation effects on timing via statistical analysis methods. This type of analysis can enable trade-offs between yield and performance.

VI. Change in Direction: the Dual Core Architecture

A company’s strategic direction needs to be reevaluated more frequently as the rate of change of technology accelerates. A salient example of this can be seen in recent changes on how to use silicon to increase microprocessor performance. For 30 years, microprocessor performance has been driven by applying more of the increasing silicon area to speed the execution of a single stream of application code. Initially, microprocessors took several clock cycles to execute a single instruction. Then came Reduced Instruction Set Computer (RISC) technology that proved the performance benefit of executing an instruction in a single cycle. RISC techniques were incorporated in all types of processors.

Then came pipelining memory accesses to reduce the performance impact of slow memory access times and to overcome processor bus bandwidth. This was followed by the execution of multiple instructions in parallel called Superscalar Execution. Out of order execution followed, which enabled instructions to stall briefly while the hardware would make a good guess at the next instruction needed and would go ahead and execute

if not immediately dependent on the stalled result. This is a very simplified list of the advances that propelled each generation's performance at a faster rate than could be delivered through process improvements alone. Each of these advances required more than doubling the amount of transistors in each microprocessor to increase performance.

However, in roughly the last five years, it has been recognized that the resulting power increase to meet this rate of "single stream" performance increase will not be sustainable without running into power limitations that are sometimes referred to as "The Power Wall." Avoiding the Power Wall has led to a recent strategy change across the industry of pushing performance through the faster execution of *multiple* code streams.

Multiple code streams were first implemented with Multi-Treaded execution. More recently this approach is being implemented by putting two or more processor cores on a chip at the same time. The shift from increasing speed through a single code stream to now putting multiple processor cores on a single chip is a significant strategy change motivated by practicality, development efficiency, and technological changes.

VII. Implications of Acceleration: Impact on Business Model Evolution

In the semiconductor industry, the rate of change of technology challenges are driving business model changes at an increasing rate. Companies are focusing on developing their areas of strength and outsourcing other aspects to fulfill their product development requirements in light of the technical demands examined in this article.

For example, a traditional application-specific integrated circuit (ASIC) company used to have its own production facility, its own library of IP, its own reusable IP blocks, and developed its own CAD tools. In the last 15 years, the need for this integrated structure has been dismantled. Instead of building and managing their own production facility, ASIC companies now regularly work with world-class contract manufacturers, or foundries. Foundries have emerged across Asia, including TSMC and UMC in Taiwan and Chartered Semiconductor in Singapore. Independent assembly and test companies also have sprung up to support this new dis-integrated structure.

Also in the last 15 years, independent CAD companies have emerged which could offer smaller companies with the ability to buy/license their own tools and afterward have their products fabricated at an independent foundry. This has given rise to the "fabless" semiconductor industry.

The rise of the foundries and CAD companies opened up business opportunities for a whole new segment of the industry—independent IP companies. These companies follow a business model focused on developing large, predesigned and reusable building blocks (IPs) that a fabless company can purchase to speed the development of a chip.² Many predict that an average chip design in 2007 will be roughly 80% predesigned and

² Reusable means that the building block can be easily integrated into many different designs as compared with the older approach of designing each function into a customized chip.

reusable building blocks. The availability of these building blocks—many of which used to be system level components—has given way to the concept of building a System-On-a-Chip (SOC).

This changing landscape also supported the growth of another complementary industry during the last 10 years—the fabless design house, or “backend” design service. The dynamics leading to the rise of backend design services included the fact that physical design tools became increasingly expensive, as well as the design process becoming increasingly challenging as noted in this article. The backend physical design portion of a product could take on average a few weeks up to a few months to complete. Unless a product company was developing a lot of products each year and could keep a physical design team busy, the cost of the design tools has become prohibitively expensive to support a physical design team in-house. Further, because the technology has been changing so rapidly, if a company does not have their design team doing physical design all the time, they would rapidly become out of date and could not sustain the ability to develop designs with good quality on predictable schedules.

This change paved the way for a more recently expanding industry during the last 5 to 6 years of the fabless backend physical design service industry or fabless ASIC companies. While there were companies of this type before, the last 5 years has seen expanded interest and funding of these types of businesses by venture capital companies. This trend also has been fueled by a view that a decreasing percentage of companies in the future will have the expertise level to keep up with the escalating design challenges outlined in this article. This suggests the possibility of a dramatic increase in demand for these services.

Since the burst of the dot com bubble, companies have looked for ways to cut costs more intensely this has led to outsourcing in lower cost geographies like China and India. Whereas it took Taiwan over a decade to build a world-class semiconductor industry based upon developing the semiconductor foundry business, it may take China only 5 years to develop companies with similar semiconductor manufacturing volumes. With technological capability in China quickly rising due to strong domestic universities, the return of Chinese engineers who had worked internationally, and an expanded venture capital interest, design foundries are on the rise in China. In addition to design services, a design foundry may also provide “turnkey” manufacturing through supply chain management. Design foundries have reduced the design process to a systematic operation—design “art” has given way to “factory-like” science. This increases efficiency, further reduces cost, and allows entry points for new players. In China, one could anticipate that these operations may become quite large based upon the readily available and expanding workforce that is growing in expertise at a very rapid rate. The economics of these design foundries can support a design-only business, allowing the customer to decide among manufacturing options. This will create a disruptive factor in the U.S. market where many product companies are once again wanting to manage the manufacturing supply chain themselves as a way of increasing their product margin in this post dot com era.

With the escalation of technology challenges described in this article, semiconductor companies are increasingly working together through alliances to overcome these roadblocks. One recent example saw four industry powerhouses working together to develop a 90nm generation design flow. TSMC (the leading foundry), Artisan (a leading library supplier), Cadence (one of the top two EDA companies), and ARM (a leading embedded processor and related IP company) worked together to develop this design flow. The flow could then be used by other companies wanting to successfully develop 90nm products that would be fabricated in TSMC's production facilities.

This trend toward specialized firms interacting in a highly collaborative way is consistent with the Open Innovation paradigm (Chesbrough, 2003). In discussions with venture capitalists, we have heard recent acceptance of this multi-party approach to innovation because of the need to combine capabilities required to offer a complete and competitive semiconductor product. We anticipate that the Open Innovation approach will not only be used between companies that offer different parts of a solution, but also by competitors that collaborate to offer improved products that benefit from the synergistic combination of the unique core competencies of each company.

References

Appleyard, Melissa M., Nile W. Hatch, David C. Mowery (2000). "Managing the Development and Transfer of Process Technologies in the Semiconductor Manufacturing Industry." In G. Dosi, R. R. Nelson, and S. G. Winter, eds., *The Nature and Dynamics of Organizational Capabilities*. London: Oxford University Press: 183-207.

Bourgeois, L.J. III and Kathleen M. Eisenhardt (1988). "Strategic Decision Process in High Velocity Environments: Four Cases in the Microcomputer Industry." *Management Science*, 34(7), July: 816-835.

Chesbrough, Henry (2003). *Open Innovation: The New Imperative for Creating and Profiting from Technology*, Boston: Harvard Business School Press.

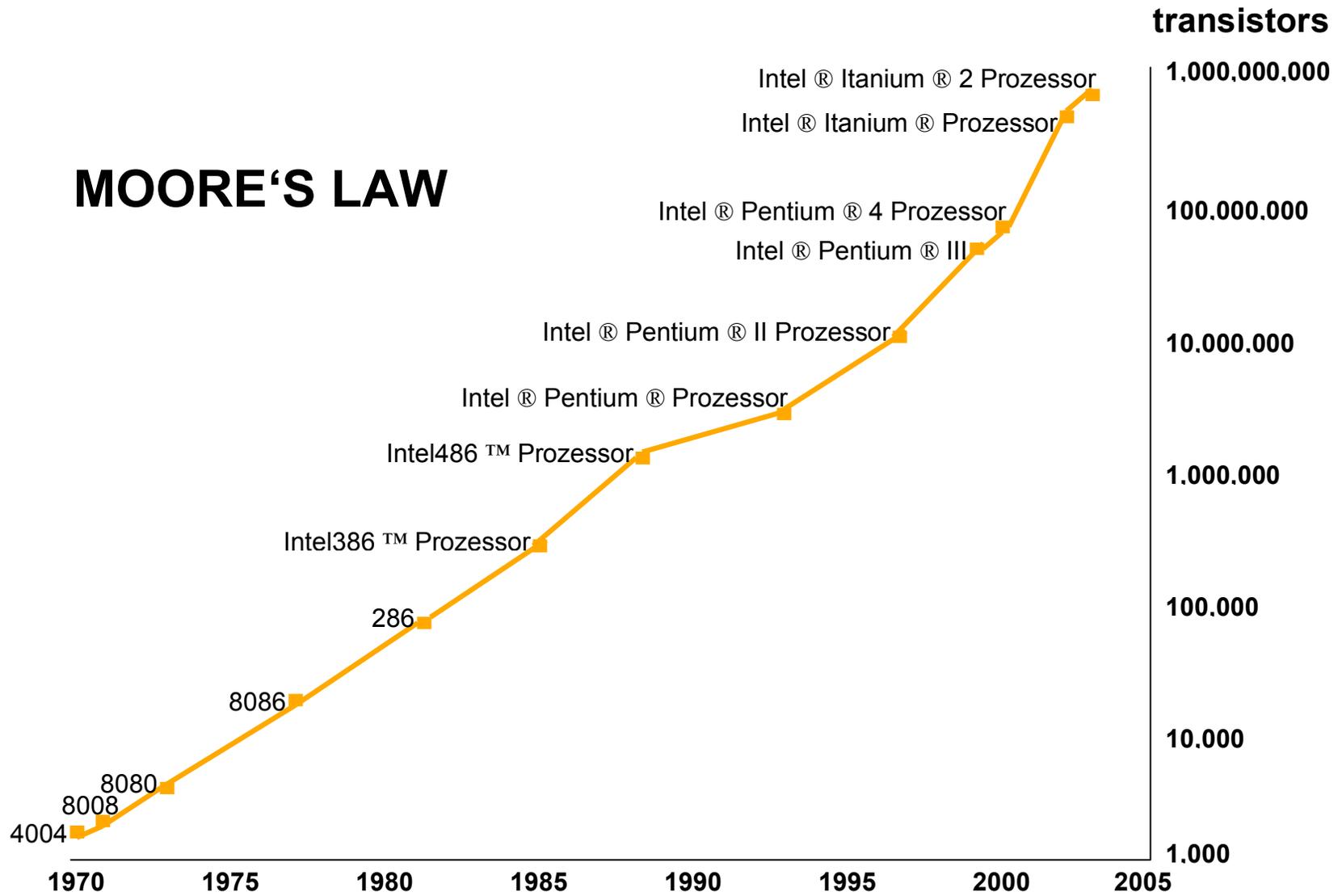
Eisenhardt, Kathleen M. (1989). "Making Fast Strategic Decisions in High-Velocity Environments." *Academy of Management Journal*, 32(3): 543-576.

Kostoff, Ronald N. and Robert R. Schaller (2001). "Science and Technology Roadmaps." *IEEE Transactions on Engineering Management*, 48(2), May: 132-143.

Macher, Jeffrey T., David C. Mowery, and David A. Hodges (1998). "Reversal of Fortune? The Recovery of the U.S. Semiconductor Industry." *California Management Review*, 41(1), Fall: 107-136.

Weber, Charles (2002). "Punctuated Learning as a Source of Profitability in High-Velocity Manufacturing Environments." Working Paper.

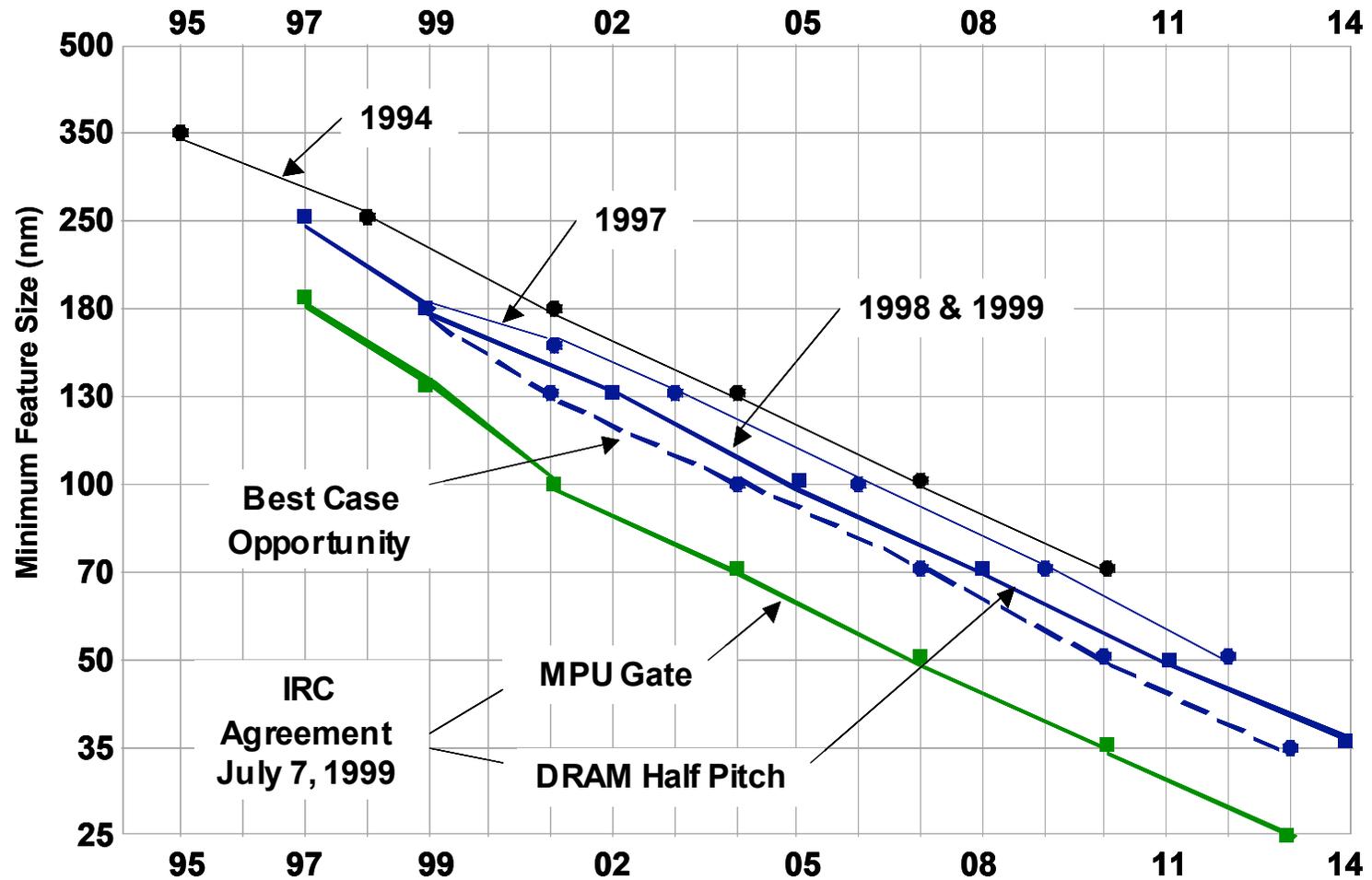
Fig. 1 Trend in the number of transistors on state-of-the-art logic chips from 1970 through 2005



Source: <http://www.intel.com/research/silicon/mooreslaw.htm>

Fig. 2 The ITRS Roadmaps for 1994, 1997, and 1998/99

ITRS Roadmap Acceleration

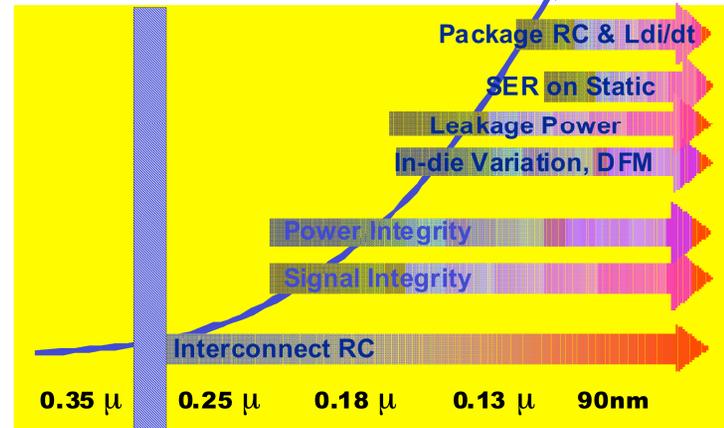


Source: <http://www.sematech.org/resources/ief/meetings/200011/itrs.pdf>

Fig. 3

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**Exponentially Increasing Design Complexity
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