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Fabrication, Field Emission Properties and Theoretical Simulation of Triode-Type
Carbon Nanotube Emitter Arrays

by

Jianfeng Wu

A dissertation submitted in partial fulfillment of the
requirements for the degree of

Doctor of Philosophy
in
Applied Physics

Dissertation Committee:

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ABSTRACT

Carbon nanotubes exhibit excellent field emission properties and will likely be prime candidates as electron sources in future vacuum electronic applications. Recent research has focused on enhancing field emission from traditional diode-type emitters by adding a gate electrode between the anode and the cathode. Since the gate to cathode (emitter) distance in this triode-type structure is small relative to the anode to cathode distance, this structure allows relatively small gate voltages to significantly enhance or dampen field emission. The key challenge for this research is: synthesizing vertically aligned carbon nanotube field emitters inside arrays of triode-type devices.

The most common “top-down”, etch-deposit-synthesis method of synthesizing carbon nanotubes inside gated cavities is discussed here, and a novel “bottom-up” method is presented. This new approach bypasses the lithography and wet chemistry essential to the etch-deposit-synthesis method, instead using a dual-beam focused ion beam (FIB) system to mill cavities into a multi-layered substrate. Here the substrate is designed such that the act of milling a hole simultaneously creates the gate structure and exposes the catalyst from which carbon nanotubes can then be grown. Carbon nanotubes are synthesized using plasma enhanced chemical vapor deposition (PECVD) rather than thermal chemical vapor deposition, due to the superior alignment of the PECVD growth. As dual-beam FIB and PECVD can both be largely computerized, this synthesis method is highly reproducible. The dual-beam FIB also permits a high degree of controllability in gate radius, cavity depth and emitter

spacing. The effects of a host of PECVD growth parameters (initial catalyst thickness, gas concentration, growth temperature, temperature ramping rate, chamber pressure, and plasma voltage) were characterized so that the morphology of the carbon nanotube emitters could be controlled as well. This “bottom-up” method is employed to construct functional, large area carbon nanotube field emitter arrays (CNT FEAs).

The role of the gate layer in field emission is examined experimentally as well as through theoretical models. Field emission testing revealed that increasing gate voltage by as little as 0.3 V had significant impact on the local electric fields, lowering the turn-on and threshold fields by 3.6 and 3.0 V/ μm , respectively, and increasing the field enhancement factor from 149 to 222. A quantum mechanical model of such triode-type field emission indicates that the local electric field generated by a negatively or positively biased gate directly impacts the tunneling barrier thickness and thus the achievable emission current. However, the geometry of triode-type devices (gate height, gate radius, emitter density) can influence the degree to which the gate voltage influences field emission. I demonstrate here an effective method of analytically calculating the effect of various such geometric parameters on the field emission. Results show that gate type (the height of the gate relative the emitter tip) can significantly impact the local electric field and hence the type of applications a device is suitable for. Side gates (gate height < emitter height) induced the highest local electric field, while top gates (gate height > emitter height) provided the greatest controllability. For all gate types, increasing the size of the gate opening increased the local electric field by diminishing the gate-emitter screening effect. However, gate

voltages were able to enhance or inhibit the local electric field much more readily with smaller gate radii. Due to the strength of gate-emitter field screening in the triode-type structure, the spacing between emitters had virtually no impact on the local electric field, allowing relatively high emitter densities. These theoretical results, combined with a highly controllable synthesis method, provide valuable information and methodology for those designing and optimizing triode-type devices targeted at specific applications.

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Chapter 1 INTRODUCTION

Section 1.1 provides an overview of the significance of carbon nanotube (CNT) research, including their structures, properties and applications. Section 1.2 quickly reviews field emission history and several main develop stages. Section 1.3 focuses on the triode-type CNT field emission research, including their advantages and challenges. Section 1.3 also discusses the common triode-type fabrication method. Section 1.4 lists the problems in this project and Section 1.5 is a outline of remaining chapters.

1.1 Significance of CNT Research

Carbon nanotubes (CNTs) are hollow cylinders composed of one or more concentric layers of graphene in a honeycomb lattice arrangement. The discovery of CNTs led to the realization that with graphene tubes parallel to the filament axis, these highly crystallized tubular structures would inherit several important properties of “intra-plane” graphite [1-3]. In particular, a CNT exhibits high electrical conductivity, thermal conductivity, and mechanical strength along its axis.

The large aspect ratio makes the CNT a nearly ideal one-dimensional (1-D) object, and is expected to have unique properties. In addition, depending on the arrangement of the carbon atoms, single-walled CNTs can be metallic or semiconducting [4, 5]. Furthermore, the CNT has high mechanical stability and chemical inertness due to strong C-C bonds.

1.1.1 Structure of CNTs

1.1.1.1 Single-walled CNTs

The structure of single-walled CNT is specified by a chirality vector (C_h) connecting two equivalent point on the two-dimensional graphene sheet. Single-walled CNTs can be described by a pair of integers (n, m) that define their chiral vector. As shown in Fig. 1.1, $C_h = na_1 + ma_2$, where a_1 and a_2 are the unit vectors of the hexagonal honeycomb lattice.

$$a_1 = \frac{\sqrt{3}a}{2}x + \frac{a}{2}y \quad \text{and} \quad a_2 = \frac{\sqrt{3}a}{2}x - \frac{a}{2}y, \text{ where } a=2.46 \text{ \AA}.$$

The chiral angle θ can be calculated from:

$$\cos \theta = \frac{2n + m}{2\sqrt{n^2 + m^2 + nm}}.$$

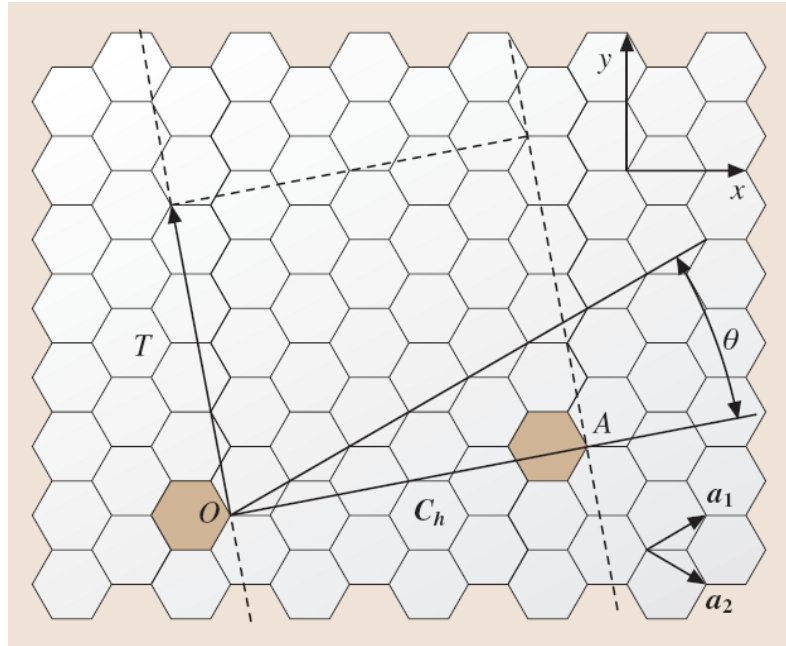


Fig. 1.1 Sketch of the way to make a single-walled CNT [6].

As illustrated in Fig. 1.2, there are many ways to roll a graphene into a single-walled CNTs. Single-walled CNTs can be the zigzag type when $m=0$, the armchair type when $n=m$, and the chiral type when $n \neq m$ and $m \neq 0$. The chiral angle for the zigzag tube and armchair tube are 0° and 30° respectively.

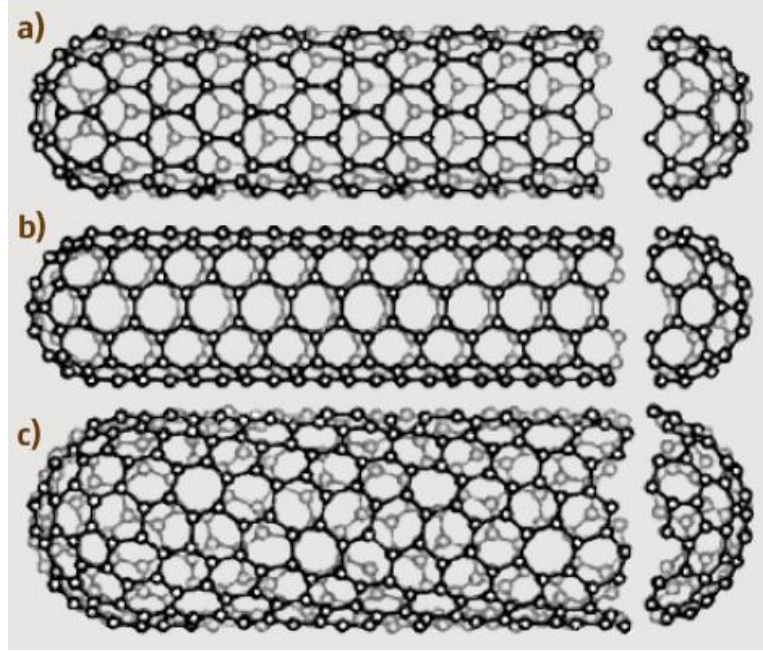


Fig. 1.2 Illustration of three types of single-walled CNTs including (a) zigzag, (b) armchair and (c) chiral [7].

The approximate diameter (D) of the single-walled CNTs can be calculated from the n and m integers.

$$D = \frac{a_{cc} \sqrt{3(n^2 + m^2 + nm)}}{\pi},$$

$$\text{where } \frac{1.41A}{(\text{graphite})} \leq a_{cc} \leq \frac{1.44A}{(C_{60})}.$$

1.1.1.2 Multi-walled CNTs

Multi-walled CNTs consist of multiple rolled layers of graphite. Multi-walled CNTs can be thought of as concentric single-walled CNTs of increasing diameter. There are two models for multi-walled CNTs [8]. The first one is the Russian Doll model that the sheets of graphite are arranged in concentric order. The second one is the Parchment model that a single sheet of graphite is rolled itself.

Depending upon the structure of the concentric CNTs and the presence of imperfections, multi-walled CNTs can exhibit a number of structure formations including herringbone type and bamboo type [8].

1.1.2 Properties of CNTs

1.1.2.1 Mechanical Properties

CNTs' special C-C bonding make them particularly stable against deformations. The tensile strength of single-walled CNTs can be 20 times that of steel [9] and has actually been measured equal to ~45 GPa [10]. The tensile strength is around 150 GPa for perfect multi-walled CNTs [11].

1.1.2.2 Electrical Properties

The electronic band structure of single-walled CNTs can be derived from the electronic band structure of graphene by applying the boundary conditions of the single-walled CNTs. Single-walled CNTs' band structure and hexagonal first Brillouin

zone are shown in Fig. 1.3 [12]. The valence band (π) and conduction band (π^*) touch at six corners (K points) of the Brillouin zone. If one of these sub-bands passes through the K point, the single-walled CNT is metallic (Fig. 1.3b); otherwise it is semiconducting (Fig. 1.3c). In addition, the electric properties (metallic / semiconductor) can be predicted from the (n, m).

All armchair chiralities of CNT display metallic properties. In addition, chiral vectors with: $n-m=3i$ also display metallic properties, where i is an integer value. All other (n, m) single-walled CNTs show semiconductor properties.

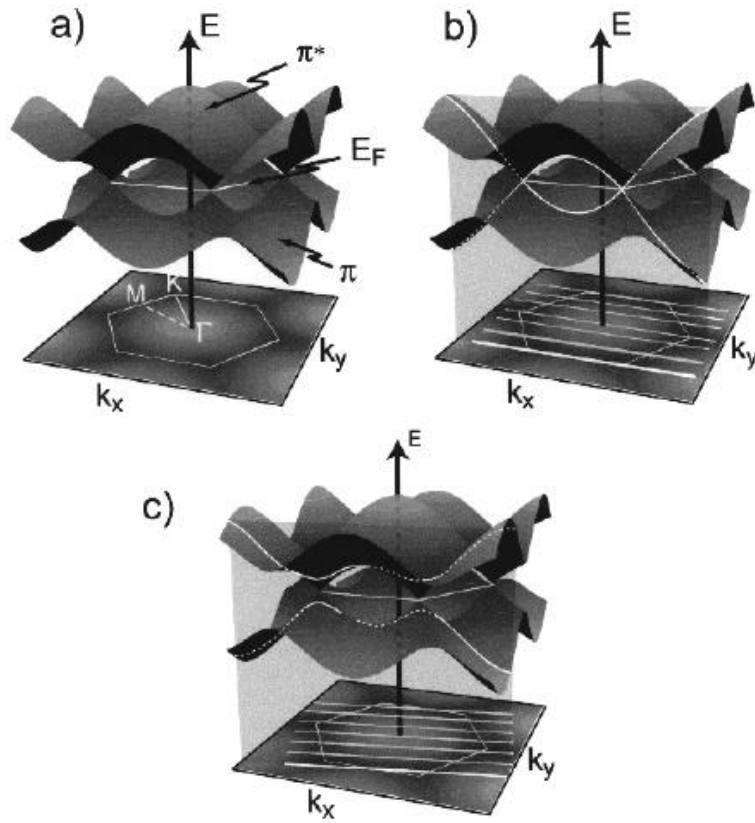


Fig. 1.3 Single-walled CNTs' band structure and first Brillouin zone [12].

(a) Band structure of a graphene sheet (top) and the first Brillouin zone. (b) Band structure of a metallic (3, 3) single-walled CNT. (c) Band structure of a (4, 2) semiconducting single-walled CNT.

Unlike single-walled CNTs, the electrical properties of multi-walled CNTs are more complicated due to their complex structure. For multi-walled CNTs, every carbon shell can have different electronic properties and chirality [13]. At normal conditions, the transport is dominated by outer-shell [14].

1.1.3 Applications of CNTs

CNT's amazing properties make them ideal for a wide range of applications.

1.1.3.1 CNTs in electronics

Since the invention of integrated circuits, size-reduction has meant greater performance, more components per chip, and less power consumption. However, it is now generally accepted that silicon devices will reach some fundamental scaling limits in a decade or so. One promising direction for future transistors involves CNTs because they impose a reduced phase space for scattering of the carriers and open up the possibility of ballistic transport [15, 16]. Furthermore, power dissipation is low; in this regard, CNTs have shown particular promise as the building blocks for future nano-electronic technology. Many of the problems that silicon technology is or will be facing are not present in CNTs.

In addition to being field-effect transistors (FET), CNTs can also function as interconnects due to their metallic properties. As interconnect sizes shrink, the resistivity of current Cu interconnect increases due to surface or grain-boundary scattering [17]. However, CNTs exhibit a ballistic flow of electrons and are capable of large current density [18]. Also, CNTs do not suffer from electro-migration or atomic diffusion like metals [19, 20]. Purcell et al. [21] demonstrated the resistance of the individual multi-walled CNT decreases with temperature increase. This characteristic is different from metal materials. In metals, the resistance increases with temperature, which means more heat is produced.

Another area where CNT's may be useful is on-chip thermal management. High power consumption and the related heat dissipation is one of the biggest issues in today's microprocessors. Efficient cooling can be achieved on silicon chips using aligned CNT arrays [22].

1.1.3.2 CNTs in energy applications

Due to their good chemical stability and high electrical conductivity, CNTs have been utilized as the electrode or the conductive filler for the active materials. With regard to energy generation and storage, CNTs show great promise in Lithium-ion batteries [23, 24], solar cells [25, 26] and fuel cells [27, 28].

1.1.3.3 CNTs sensors

CNTs have been effective as sensing elements utilizing their electrical and electrochemical properties. Single-walled CNTs have been used as gas-sensing

elements due to their 1-D electronic structure. Compared with conventional metal-oxide-based sensors, CNT-based sensors have advantages in power consumption, sensitivity, and reliable mass production [29]. Most CNT sensors are based on a FET structure [30, 31]. The conductance change upon analysis adsorption is monitored via source and drain electrode.

1.1.3.4 CNTs in field emission applications

CNTs have a high aspect ratio and are whisker-like in shape, the ideal morphology for field emission tips [32]. In addition, their graphene walls run parallel to the axis resulting in high electrical conductivity at room temperature. They have been shown to be very stable emitters [20]. Due to these unique structural and electric properties, CNTs are extremely promising candidates for electron field emission applications [33-37], such as field emission displays [38], X-ray tubes [39], and electron sources for microscopy and lithography [40].

In the following two sections, I will discuss the field emission history and more recent triode-type CNT field emitter arrays (FEAs) technology.

1.2 Field Emission History Review and Main Development Stage

An important phase in field emission development was the integration of an electron collector (anode), field emitter arrays (cathode) and a control electrode (gate).

Spindt-type cathodes were developed in the late 1960s, which are micro-fabricated molybdenum (Mo) tips in gated configuration [41, 42]. In 1970, Crost et al. proposed flat panel display technology based on Spindt's FEAs [43]. Later, silicon

(Si) tip arrays with triode structures were fabricated for prototype field emission display application because of the widespread availability of Si fabrication techniques. These developments led to the creation of a new area of research called “vacuum microelectronics”.

Recently carbon based materials have been used as a cathode emission source. In 1972, Baker et al. reported that graphite fibers showed better stability than several metals in a number of environments [44]. In 1991, Wang et al. reported low emission threshold field emission from diamond-based emitter [45].

The discovery of CNT’s high aspect ratio implies an extremely large field enhancement at the apexes of CNTs and provides a great opportunity to obtain electron emission at rather low fields [46]. In 1995, the field emission from a single, isolated, multi-walled CNT was first reported by Rinzler et al. [47]. Subsequently, many experimental studies on field emission from multi-walled CNTs and single-walled CNTs were reported. Experimental results show that CNT emitters need a lower electric field compared with normal emitters. In addition, compared to single-walled CNTs, multi-walled CNTs have been determined as the best emission materials due to their lower threshold voltage and better structural stability [48, 49].

1.3 Triode-type CNT FEAs technology

Currently, FEAs are being intensively studied as candidates for application in flat display panels with high-brightness and low power consumption [50], electro-optical devices with high brightness and small spot size [51], microwave amplifiers and generators [52], and high-speed digital switching devices.

For diode-type FEAs, the high local electric field (LEF) is obtained by placing a probe close to the CNT FEAs. Yet even with this field-enhancing geometry, the anode still typically requires a few thousand volts to generate a LEF sufficient for quantum tunneling to occur.

Diode-type field emission can be further enhanced with the creation of a triode-type configuration in which an integrated gate electrode is added between the anode and cathode. The gate layer allows relatively small gate voltages to control over field emission. In addition, the small voltage reduce the intensity of ion bombardment during field emission, increasing the lifetime of the flat panel display and making the emitter operation more stable. In recent years, researchers have successfully fabricated ordered arrays of metal or semiconductor tip cathodes integrated in a honeycomb of gates [42]. Fabricating such metal or semiconductor field emission cathodes typically involves a multi-step process: anisotropic selective chemical etching, ion beam lithography, and reactive ion etching [53].

For CNT-based triode-type FEAs fabrication, the most common method begins by etching the gated cavities, and then depositing catalyst for CNT growth into the cavities. Lee et al. [54] successfully employed this method using chemical vapor deposition (CVD) to synthesize CNT emitters. Subsequent work by Gangloff et al. [55], and Choi et al. [56] were all based on these processes. Gangloff et al. [55] greatly improved the morphology of the emitters by replacing the CVD method with plasma enhanced CVD (PECVD) and adding additional steps to reduce the size of the deposited catalyst dots until a single CNT emitter was fabricated within each cavity.

Choi et al. [56] increased emission control by adding an additional focusing gate layer. All of these studies relied on the basic etch-deposit-synthesize method to construct their devices; however, novel approaches to device construction have been explored. She et al. [57] synthesized a Si nanowire-gated field emission device using self-assembled nanomask and anisotropic plasma etching. Guillorn et al. [58] created carbon nanofiber emitters using a reversal process, beginning with the deposition of catalyst dots and the synthesis of single, vertically aligned carbon nanofiber emitters using PECVD. They proceeded to bury the emitters in a SiO₂ insulator layer, deposited a metal gate layer on top of the SiO₂, and then re-exposed the CNT emitters using a targeted wet-etching process. However, the aforementioned methods all involve numerous, time consuming steps and often, a lack of controllability. Here, I focused my efforts on designing a more efficient, controllable synthesis process.

1.4 Statement of the Problems

Although several reports demonstrate that triode-type CNT FEAs can reduce the required anode voltage and enable greater control over the emission current, the study of such triode-type CNT FEAs has been a less-publicized effort. The scarcity of reports on fabricating and characterizing triode-type CNT FEAs is largely due to the methodological complexity of situating CNTs properly within gated insulator-cell-arrays. The main objectives of this work were therefore, to:

- (1) Focus on developing a novel technique to fabricate CNTs in a triode-type field emission structure;

(2) Investigate the field emission behavior of triode-type structures in relation to their geometrical configuration and applied fields; and

(3) Develop simulations of the field emission process to guide optimization of next-generation device architectures.

In order to contribute to a solution for the above objectives, this research was designed to seek answers to the following questions:

- How do factors such as temperature ramping rate, growth temperature, catalyst thickness, and gas concentration influence the morphology of CNTs in a plasma environment?
- How can vertically aligned CNTs be synthesized in a triode-type structure?
- How can the problem of short-circuiting between CNT emitters and the gate be solved?
- How can the field emission properties of triode-type CNT FEAs be tested?
- What is the function of a gate layer? What is the relationship between the gate potential and the field emission process?
- How will the different gate types (top gate, standard gate and side gate) change the field emission properties of the triode-type device?
- How does the field screening effect influence field emission from CNT FEAs? How many types of field screening effects do we need to consider in triode-type device?
- How to optimize the geometrical and electrical parameters of triode-type field emission devices for specific applications?

1.5 Outline of Remaining Chapters

In this research, the first key step was to obtain suitable field emitters. Thus, Chapter 2 describes how I determined the best catalyst and growth method to fabricate vertically aligned CNTs. I present an efficient CNT synthesis method and introduce various synthesis processes and growth parameters. Beside these, Chapter 2 also describes two in-situ CNT properties test methods. In the first, horizontally aligned CNTs are synthesized on a special TEM sample holder so they can be directly observed in TEM, avoiding any sample preparation procedures that may alter the structure of the CNTs. This method can be extended to test electric properties of CNTs by fabricating electrodes on either end of CNTs. In addition, a special TEM sample preparation method is discussed to investigate internal structures of devices such as the CNT/substrate interface properties.

Chapter 3 describes two approaches to synthesizing triode-type CNT FEAs: the “top-down”, etch-deposit-synthesize method described above, and a novel “bottom-up” method. In the “bottom-up” method, dual-beam focused ion beam (FIB) milling is used to carve gated cavities and, in the process, expose an embedded layer of catalyst. CNT emitters are then synthesized within the gated holes in PECVD. I compare these two methods and present various improvements to the “bottom-up” method that make it more effective at fabricating large area functional triode-type CNT FEAs devices.

Chapter 4 discusses field emission theory and Chapter 5 presents the field emission properties of synthesized CNT films and triode-type CNT FEAs. A model

for analytically calculating the effect of various gate parameters on triode-type field emission in general is also discussed. In addition, according to the theoretical simulation results, I list some recommend geometric and electric parameters for three kind of specific applications. Finally, Chapter 6 concludes the research.

Chapter 2 EFFECTS OF GROWTH METHOD AND PARAMETERS

Standard methods for synthesizing carbon nanostructures include arc discharge [59], laser vaporization [60], chemical vapor deposition (CVD) [61], and plasma-enhanced CVD (PECVD) [62].

The first two methods synthesize CNTs at high temperatures ($>3000\text{ }^{\circ}\text{C}$) and short time reactions (microseconds \sim milliseconds). In the arc discharge method, an electric spark between two graphite rods sublimates the carbon in the negative electrode because of the high temperature of the discharge. The vaporized carbon then forms CNTs. In the laser ablation method, a pulsed laser vaporizes a graphite target in a high temperature reactor. Inert gas is bled into the chamber while the CNTs forming on the cooler surfaces of the reactor. The CNTs produced from these two methods are often coated in layers of amorphous carbon (70% amorphous carbon for arc discharge, 30% amorphous carbon for laser ablation) [63], so a purification step is required to separate the CNTs from the amorphous carbon. At the same time, arc discharge and laser ablation do not offer control over the spatial arrangement of the produced nanostructures [64], an essential feature for field emission applications.

In comparison with arc discharge and laser ablation, CVD utilizes hydrocarbon gases as carbon sources and transition metal catalyst nanoparticles as “seeds” for CNT synthesis at lower temperatures ($500\text{ }^{\circ}\text{C} \sim 1000\text{ }^{\circ}\text{C}$) and long reaction times (typically from minutes to hours). In addition, CVD allows location-specific synthesis of CNTs. Compared with CVD, PECVD additionally allows the controlled alignment of each individual CNT during synthesis. This alignment function makes PECVD method the

most promising way to actualize the application of CNTs in field emission. Another major advantage of CVD or PECVD is that no purification process is necessary for either method.

Section 2.1 provides an overview of the growth mechanism of CNTs in a CVD environment. Section 2.2 discusses the silicon substrate cleaning and catalyst preparation process. Section 2.3 - 2.5 compares the CNTs grown by CVD and PECVD. Section 2.6 lists the effect of growth parameters of CNTs synthesized in PECVD. Section 2.7 provides two novel in-situ methods of testing CNT properties, including structure properties, electric properties, and CNT/substrate interface properties.

2.1 CNTs Growth Mechanism

Synthesizing CNTs involves passing a gas flow containing hydrocarbon (CH_4 , C_2H_2 , ...) over small transition metal particles (Fe, Co, Ni) in a furnace. The CNT growth mechanisms include three steps [65]:

(1) Adsorption then decomposition of carbon-containing gaseous moieties at the catalyst surface.

(2) Dissolution then diffusion of the carbon species through the catalyst to form a solid solution.

(3) When the catalyst has reached the saturation threshold of its carbon content, the solid carbon precipitates to form the walls of the CNTs. Then the catalyst becomes able to incorporate carbon again until over-saturation is reached, starting the process again.

This reaction is called catalysis-enhanced thermal cracking:

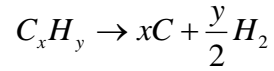


Fig. 2.1 shows a schematic diagram that illustrates the key features of this growth model for a tip-type CNT structure. The precipitation occurs on the bottom surface of the catalyst particle and elevates the particle, which remains at the tip throughout the growth process.

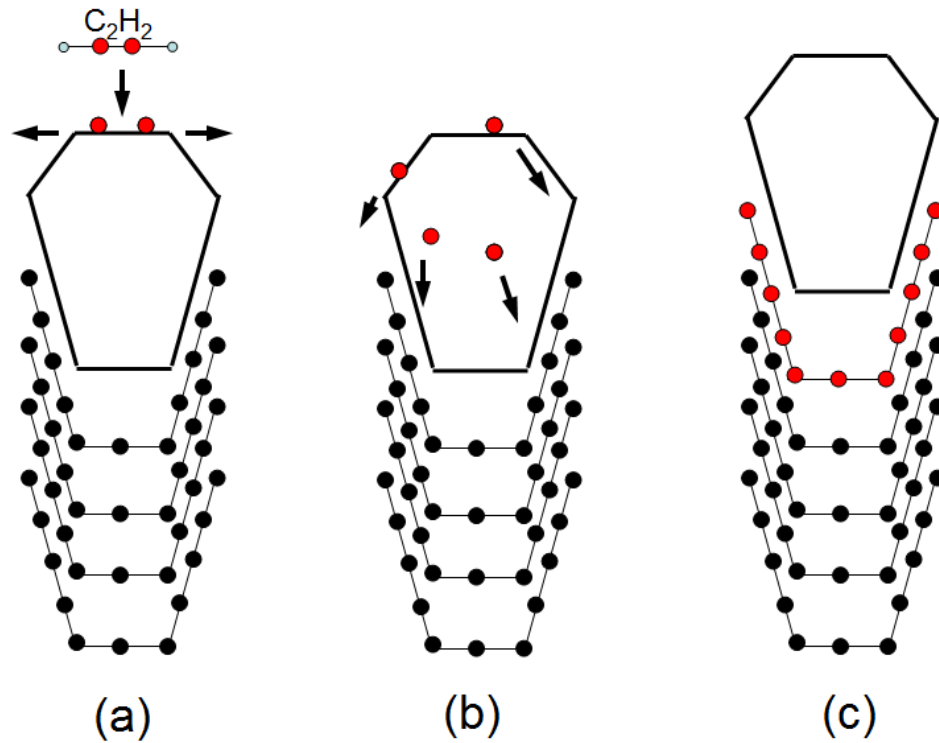


Fig. 2.1 Mechanism of tip-type CNT formation.

(a) Adsorption and decomposition of the reactant C_2H_2 molecule on the surface of catalyst, (b) dissolution and diffusion of carbon species through or around the metal particle, and (c) precipitation of carbon on the opposite surface of the catalyst particle and incorporation into graphene layers.

At the beginning of the CNTs' growth process, the driving force for the bulk diffusion of carbon through the metal particle was due to a temperature gradient [66, 67]. The diffusion of carbon is from the hotter surface on which the exothermic pyrolysis of hydrocarbons occurs, to the cooler trailing surfaces on which carbon is precipitated from the solid solution (endothermic process). Later, concentration gradients drove the carbon diffusion through the catalyst particle, from the metal-gas surface to the metal-graphene surface [68]. Recently, Helveg et al. performed an in-situ transmission electron microscope observation of the formation of CNTs from methane decomposition over nickel catalyst [69, 70].

2.2 Silicon Substrate Cleaning and Catalyst Preparations Process

Prior to use as the growth substrate, silicon wafers were prepared using the piranha clean method. The etching solution contained three parts H_2O_2 to seven parts H_2SO_4 . Because the mixture is a strong oxidizer, it will remove most organic matter, and hydroxylate silicon wafers (add OH groups), making them extremely hydrophilic (water compatible). In the cleaning process, the silicon wafers were kept in the piranha solution for a period of 90 min. After cleaning, the silicon substrate was washed in deionized water and soaked for another 90 minutes; the cleaned silicon wafer could then be kept "fresh" in deionized water for up to two days before use.

Fe, Ni, and Co are the most commonly used catalysts for CNTs synthesis. One of the reasons for choosing these metals as the catalyst for CNT growth is due to the metal-carbon phase diagrams. Listed below are the two kinds of catalysts I used to

synthesize CNTs: sol-gel Fe catalyst for CVD method and Ni thin film catalyst for PECVD method.

2.2.1 Sol-gel Fe catalyst

Sol-gel Fe catalyst was used to synthesize CNTs in a CVD environment. To prepare a sol-gel Fe catalyst, ferric nitrate solution ($\text{Fe}(\text{NO}_3)_3 \cdot 9\text{H}_2\text{O}$, 1.5 M, 15ml) was mixed with tetraethoxysilane (TEOS, 10 ml) and ethanol (10 ml), followed by magnetic stirring for 20 min. Four drops of hydrogen fluoride (HF) were added, and stirred for another 15 min; the sol-gel solution must be continuously stirred to avoid the formation of a gel. An orange solution was obtained. Finally, sol-gel Fe catalyst can be spin coated to form a catalyst film on the wafer.

2.2.2 Ni thin film catalyst

Another common technique for depositing the Ni catalyst is by physical vapor deposition (sputtering or evaporation). The film thickness is usually from a few nanometers to a few micrometers and is monitored during deposition using a quartz oscillator-type film thickness monitor.

The advantage of using thin film catalysts is that they can easily and accurately be patterned using masking or etching techniques such as photolithography, electron beam lithography, or dual-beam FIB milling.

2.3 CVD System and CNT Synthesis Process

CVD utilizes hydrocarbon gases as the carbon sources, and transition metal catalyst particles as “seeds” for CNT growth, which takes place at lower temperatures (500°C ~ 1000°C).

A schematic of a CVD system is shown in Fig. 2.2. The system usually consists of a quartz tube inside a furnace with a controllable source gas flow. The CVD system consists of three main parts:

- Gas supply: the concentrations and flow rates of gases are controlled using a MKS throttling valve, MKS 600 series pressure controller and MKS 4 Channel mass flow controller.
- Temperature control system: the required decomposition temperatures of the hydrocarbon gases used are provided by the Carbolite CTF12/75/700 tube furnace.
- Vacuum system: The evacuation of air from the reaction chamber is accomplished using a mechanical pump while a pressure sensor monitors the vacuum.

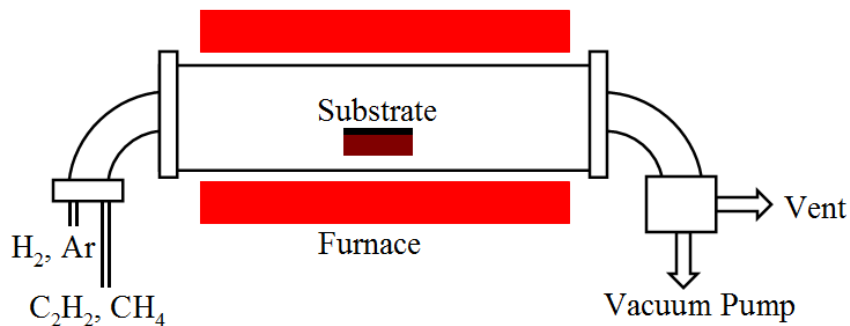


Fig. 2.2 Schematic illustration of the CVD system.

A photo of the above CVD system is shown in Fig. 2.3.



Fig. 2.3 Photo of the CVD system.

Substrates are placed inside the tube, and the atmosphere (temperature, temperature ramping rate, chamber pressure, gas composition, flow rate) is controlled to affect the growth of CNTs. Typically, the synthesis of CNTs consists of two steps:

(1) Catalyst activation, where the catalyst thin film is heated at 700 °C for 15 min in 76 Torr hydrogen (H_2) environment;

(2) Increase the temperature to 800 °C and input acetylene (C_2H_2) carbon source for synthesize CNTs. Keep the chamber pressure at 76 Torr for a further 15 min.

The advantage of CVD method is the ability to grow from a patterned substrate; however, it is hard to generate vertically aligned, free-standing CNTs in this process.

2.4 PECVD System and CNT Synthesis Process

As previously discussed, field emission applications require CNT growth in highly ordered directions and located at specific positions.

The important difference between CVD and PECVD is that in CVD thermal energy is used to activate the gas, whereas in PECVD the molecules are also activated by electron impact. PECVD allows for lower process temperatures because precursor dissociation is affected by high-energy electron impact reactions that would otherwise take place at much higher temperatures when using CVD. However, the most important purpose of using plasma is the outcome of uniform alignment of CNTs due to their interaction with the electric field [71].

A PECVD system consists of four main parts:

- Vacuum chamber, include vacuum pumps and pressure control system;
- Gas flow control system, include mass flow controller and gas shower head;
- Plasma power supply;
- Substrate heater with temperature control system.

There are many methods used to generate plasma, including radio-frequency (RF) plasma [72, 73], microwave plasma [74-76], and direct-current (DC) plasma [77-79]. Regardless of the plasma source used, the key aspect is the generation of electric fields on the wafer surface in the plasma sheath.

In order to understand the mechanisms involved in CNT formation in a PECVD reactor, I briefly review some basic processes that occur in plasmas. In the

simplest case of a DC diode-type reactor, a voltage is applied across a space filled with a low-pressure gas (a few Torr). The glow discharge that is initiated can be divided into four visible regions arranged from cathode to anode: (1) cathode dark space, (2) negative glow, (3) Faraday dark space, and (4) positive column. These regions are shown in Fig. 2.4. The ions are accelerated by the applied voltage and some of them bombard the cathode. The bombardment generates secondary electrons that accelerate away from the cathode. Cathode dark space is a thin region near the cathode with a strong electric field. The electrons are of too low density and/or energy to excite the gas, so it appears dark. The negative glow region has the brightest intensity of the entire discharge. Electrons carry almost the entire current in the negative glow region. Faraday dark space is the region in which the electron energy is low. The positive column is a long, uniform glow.

The current in the dark space is carried primarily by ions, while in the negative glow it is carried by electrons. Thus, the negative glow is a low impedance region and the applied voltage drops mostly over the dark space. Since the dark space varies from a few hundred micrometers to a few millimeters, application of several hundred volts can create electric fields on the order of 10^4 V / cm [80]. Electric fields present in the sheath orient the growth of CNTs normal to the substrate surface, which leads to the growth of individual, freestanding CNTs.

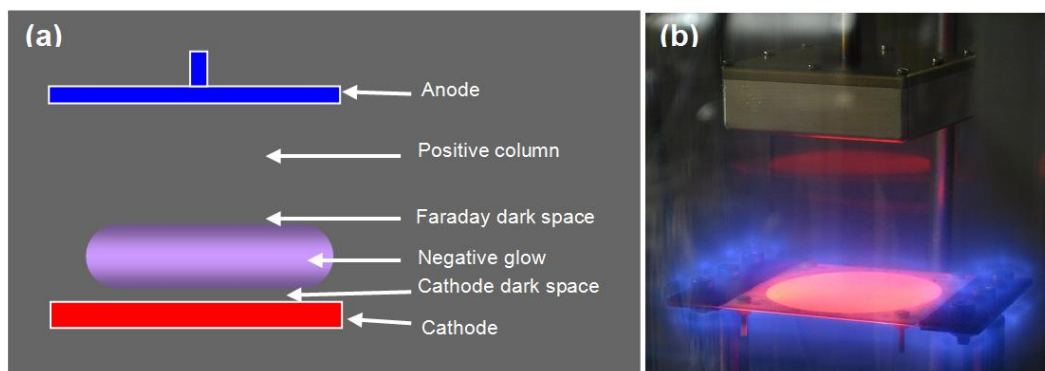


Fig. 2.4 Schematic and photos of DC glow discharge.

In the PECVD system, the substrate is placed on a heater that also serves as a cathode. The gas showerhead, used to produce a uniform gas flow distribution over the entire substrate surface, also serves as the anode. A photo of the PECVD system is shown below in Fig. 2.5.



Fig. 2.5 Photo of the PECVD system.

Unlike CVD reactors in which only temperature, chamber pressure, and gas flow rate govern the nanostructure growth process, the PECVD process must also take into account parameters specific to the glow discharge. Voltage, current, power, and resultant field distributions within the discharge all play a critical role in shaping the outcome of the growth process.

Fig. 2.6 demonstrates the effect of plasma bias voltage on the distribution and density of plasma. As the plasma bias voltage increases, the negative glow region becomes brighter. Also, the cathode dark space is smaller when the plasma bias voltage increases ($d_1 > d_2 > d_3$). As a result, the electric field, generated by plasma sheath, increases and leads to better alignment of the synthesized CNTs.

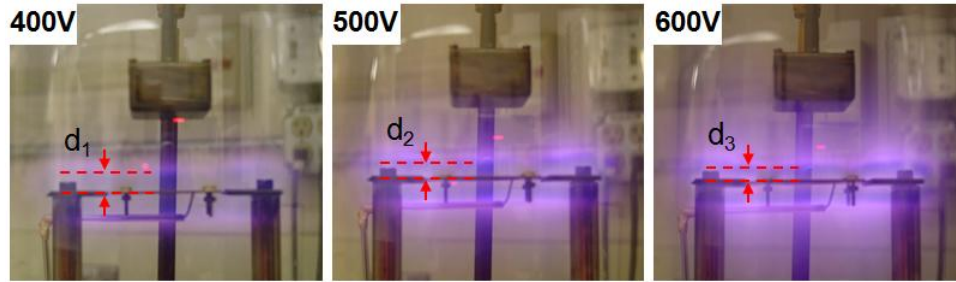


Fig. 2.6 Effect of plasma bias voltage.

Fig. 2.7 demonstrates the effect of chamber pressure on the distribution and density of plasma. As the chamber pressure increases, more gas molecules can be activated into ions, and these ions bombard the cathode and generate more secondary electrons. The plasma distribution and density are charged based on these ions and secondary electrons. As the chamber pressure increases, the negative glow region is

brighter and closer to the cathode, which makes the cathode dark space thinner ($d_1 > d_2 > d_3 > d_4$). As a result, the electric field increases.

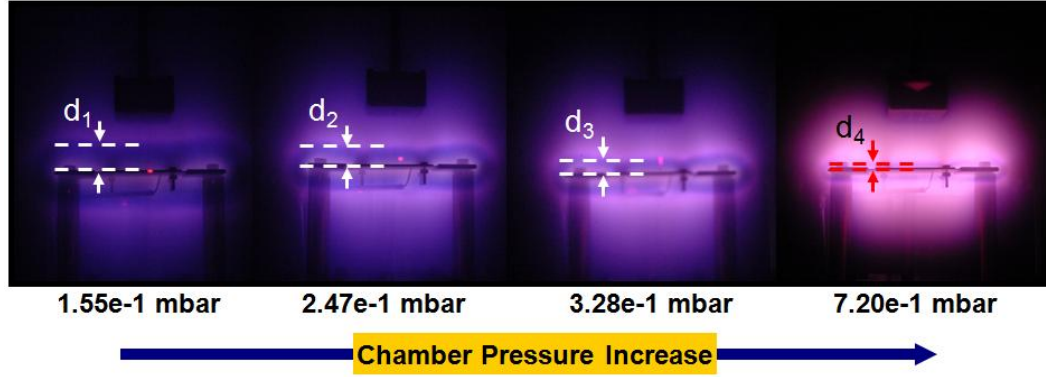


Fig. 2.7 Effect of chamber pressure.

It is important to note that plasma is usually used for deposition and etching, depending on the choice of conditions. Special consideration must be given to finding the balance between etching and deposition to prevent detrimental formation of carbon films and at the same time avoid damage to the sidewalls of growing nanotubes [81].

A typical PECVD CNT growth process occurs as follows: A very thin film of Ni is deposited on a substrate using magnetron sputtering or evaporation. The typical film thickness is a few nanometers (with the thickness monitored by a quartz film thickness detector). In the catalyst activation step, the NH_3 plasma, in addition to the high temperature, anneals/etches the Ni thin film into nanoparticles/nanoclusters due to increased surface mobility and the strong cohesive forces of the metal atoms [82, 83]. These nanoparticles then act as the necessary seeds for the growth of CNTs. The introduction of C_2H_2 (the carbon source) allows deposition to begin, while NH_3 (the

etching/reducing gas) prevents the deposition of amorphous carbon. The whole process is illustrated in Fig. 2.8.

Two growth modes (tip or base growth) are possible based on whether the catalyst metal interacts strongly or weakly with the underlying support material. The interaction of the catalyst with the support can be characterized by its contact angle, analogous to “hydrophobic” (weak interaction) and “hydrophilic” (strong interaction) surfaces [83-85]. For example, Ni on TiN or SiO₂ has contact angle >90° (i.e. “hydrophobic” or weak interaction) and thus tip-growth is favored. On the other hand, Co or Fe on Si [83, 84] favor base growth.

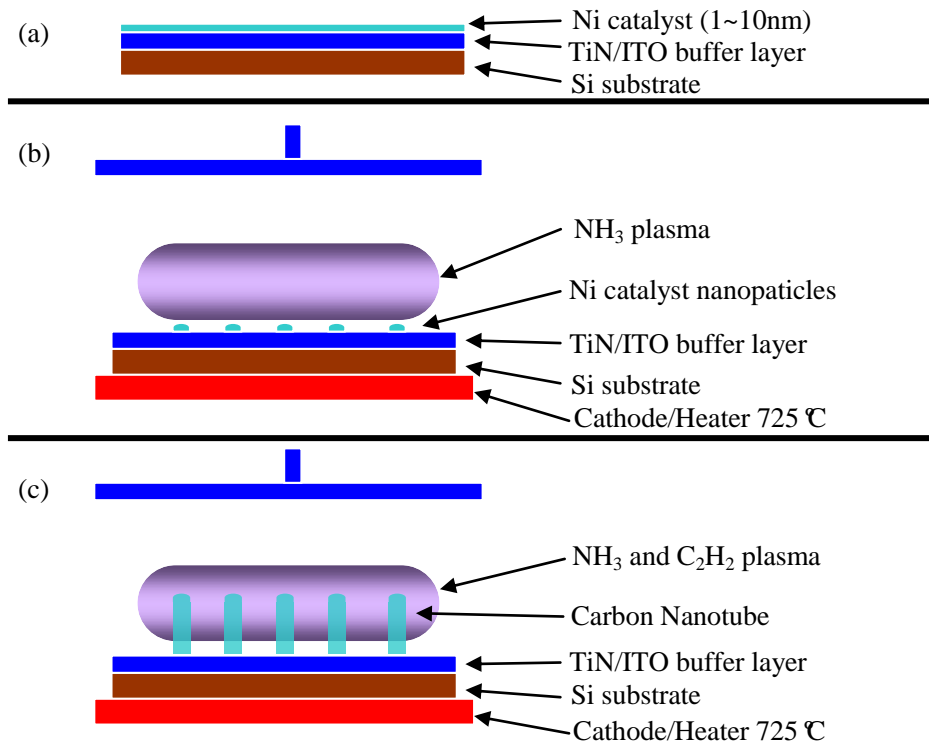


Fig. 2.8 Schematic of the PECVD process for growing vertically aligned CNTs.

(a) Catalyst deposition, (b) catalyst pretreatment/nanoparticle formation, and (c) growth of CNTs.

2.5 Morphology and Internal Structure of CNTs Synthesize in CVD and PECVD

In CVD, the energy required to break down the reactant deposition gases into graphene comes from the heat supplied to the catalyst particle and its environs. There is no alignment of CNTs as a result of the CVD process. As demonstrated in Fig. 2.9a, the resulting CNTs synthesized by CVD are curly and randomly oriented. In contrast to the CVD process, the substrate in the PECVD method is biased by a negative potential of 630 V to form glow discharge plasma. The plasma creates a sheath above the substrate and the electric field is perpendicular to the substrate. The field vertically aligns the CNTs during growth (Fig. 2.9b).

The different growth techniques also lead to differences in the shapes of the tube tips. The nanotubes made by CVD terminated in irregular carbon structures, while the tube tips made by PECVD had a more uniform shape, as indicated in the insets of Fig. 2.9a and Fig. 2.9b, respectively. High resolution TEM images of typical CNTs grown by PECVD are shown in Fig. 2.10.

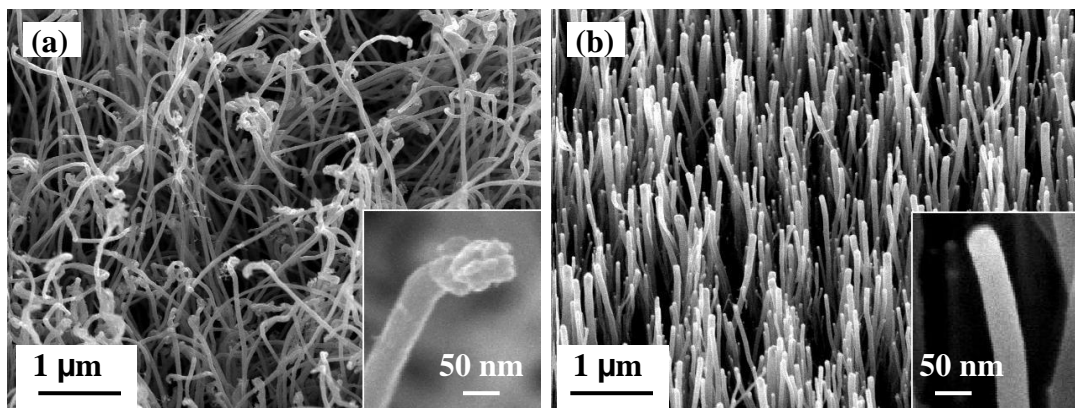


Fig. 2.9 Compared morphology of CNTs grown in CVD and PECVD environment. (a) CNTs synthesized by CVD were curly and randomly oriented. The tubes' tips were an irregular shape; (b) CNTs formed by PECVD were well aligned in a vertical configuration. The tubes' tips have a more uniform shape.

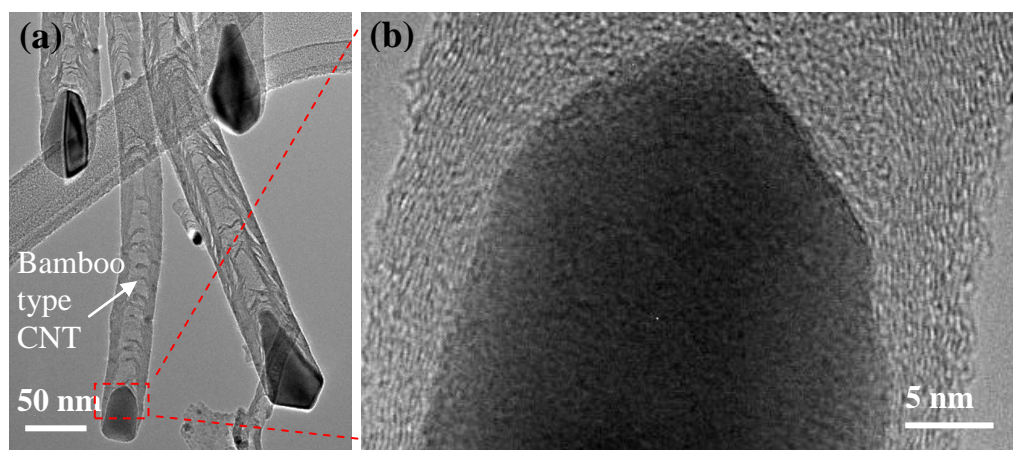


Fig. 2.10 High resolution TEM images of typical CNTs grown by PECVD. (a) TEM image of MWCNTs grown by the PECVD process. The Ni catalyst is located at the tip of each nanotube, while bamboo-type fringes formed inside the nanotubes. (b) An HRTEM image of the nanotube region labeled in Fig. 2.10a.

Note that the Ni catalyst is located at the tip of the CNTs. The CNT length increases with deposition pressure and time as the catalyst is always exposed to the incoming gas/plasma. The internal structures of the PECVD tubes display bamboo-like fringes characterized by periodic curving graphitic bands normal to the tube axis. Small Ni particles are also observed inside the nanotubes, as demonstrated by the STEM image in Fig. 2.11a. The EDX line scan results in Fig. 2.11b indicate the presence of a small Ni particle inside the main body of the nanotube and a large Ni particle within the nanotube tip region.

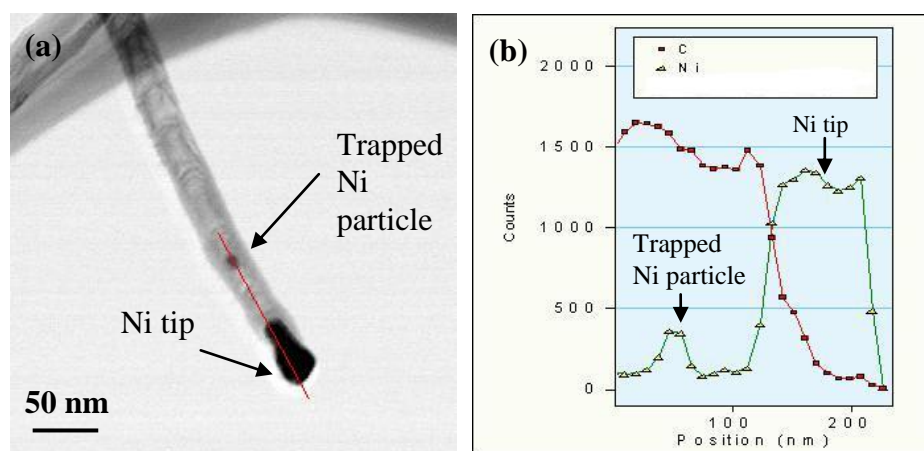


Fig. 2.11 A STEM image and EDX line scan spectrum of typical CNTs grown by PECVD.

(a) STEM image of a nanotube with a Ni particle trapped inside. (b) An EDX line scan spectrum of the nanotube region labeled in (a) shows the distribution of carbon and Ni along the nanotube axis.

High resolution TEM images of typical CNTs grown by CVD are shown in Fig. 2.12. Instead of single Ni catalyst particles on the tip of the CNT, CVD growth produces a lot of small Ni particles at the tip (Fig. 2.12b).

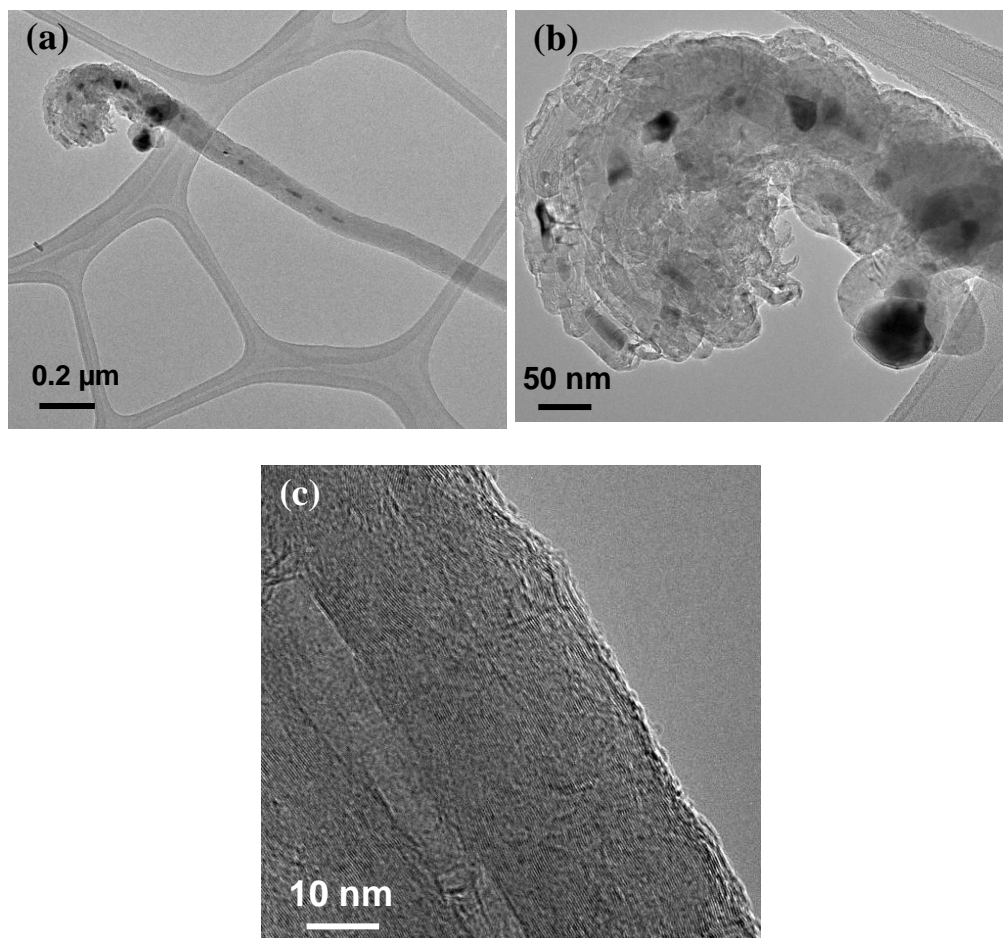


Fig. 2.12 TEM image of multi-walled CNTs grown by CVD process.

- (a) TEM image of multi-walled CNTs grown by the thermal CVD process.
- (b) An HRTEM image of the nanotube tip in (a) demonstrates that there is no single catalyst particle, but there is a mixture of catalyst particles and carbon nanostructures.
- (c) An HRTEM image of the nanotube stem in (a). The hollow stem verifies that this is a CNT.

It is clear that PECVD provides a more desirable and effective method for the synthesis of vertically aligned CNTs, the morphology of which will enhance the field emission properties. In addition, the best field emission tip should be whisker-like, followed by the sharpened pyramid, hemi-spheroidal, and pyramidal shapes in order of desirability [32]. CNTs are whisker-like.

2.6 Effect of Growth Parameters on CNTs Synthesized in PECVD

From the discussion in section 2.5, PECVD provides an easy and effective method for synthesis of the vertically aligned CNTs needed in triode-type FEAs. However, as a variety of growth parameters affect the formation of CNTs, system research is needed to optimize the CNT synthesis process.

2.6.1 Effect of catalyst layer thickness

The Ni catalyst nanoparticle size determines the diameter of the synthesized CNTs. As the Ni catalyst film thickness was increased from 1 to 6 nm, the diameter and the length of the CNTs also increased (Fig. 2.13).

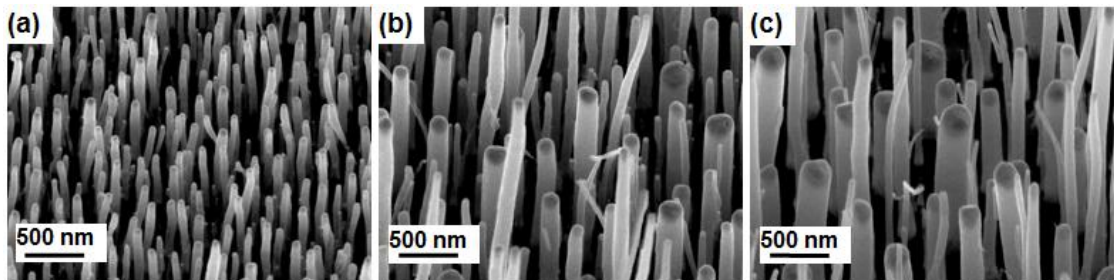


Fig. 2.13 Effect of initial catalyst layer thickness.

(a) 1nm Ni film catalyst. (b) 3nm Ni film catalyst. (c) 6nm Ni film catalyst.

2.6.2 Effect of growth temperature

Increasing the growth temperature of CNTs decreases their average diameter and increases their average height (Fig. 2.14).

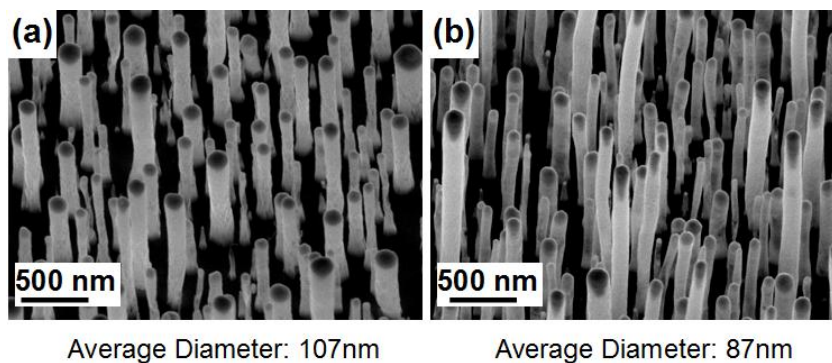


Fig. 2.14 Effect of growth temperature.

(a) CNTs grown at 725 °C. (b) CNTs grown at 825 °C.

2.6.3 Effect of gas concentration

Changing the C_2H_2 to NH_3 ratio influences the morphology of CNTs. A high concentration of NH_3 (Fig. 2.15a) results in diameter variations along the tube axis. Diameter variations across the entire sample (i.e. from tube to tube) also increase.

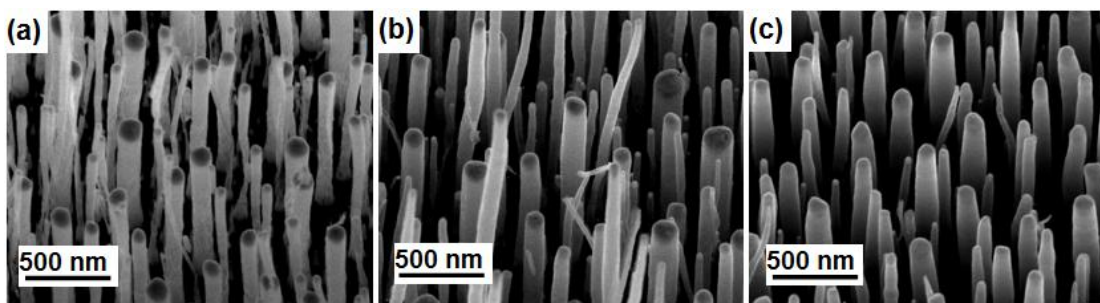


Fig. 2.15 Effect of gas concentration.

(a) 50:200 sccm $C_2H_2:NH_3$. (b) 70:200 sccm $C_2H_2:NH_3$. (c) 90:200 sccm $C_2H_2:NH_3$.

2.6.4 Effect of temperature ramping rate

For the first time in this study, the temperature ramping rate is examined. The ramping rate is the time at which the sample is raised from room temperature to growth temperature (725 °C). As shown in Fig. 2.16, the initial Ni catalyst film is transformed into Ni particles during the temperature ramping process. The size and distribution of Ni particles is dependent on the different temperature ramping rates. A slower temperature ramping rate (420 seconds) yields larger Ni particles on average and gives a wide size distribution, while a faster temperature ramping rate (21 seconds) results in smaller particles on average with a much narrower size distribution.

The strong cohesive forces of the metal atoms make small particles tend to join into bigger particles. When the sample temperature increases slowly, it takes 420 seconds to heat from room temperature to growth temperature, leaving plenty of time for particle merging. If the sample temperature increases rapidly, it only takes 21 seconds from room temperature to growth temperature; in this small period, the cohesive forces do not have enough time for significant particle merging. With the introduction of C₂H₂, the CNTs begin to grow and no further merging occurs. These smaller particles in turn grow a thinner, more uniform CNT at a high temperature ramping rate (Fig. 2.17).

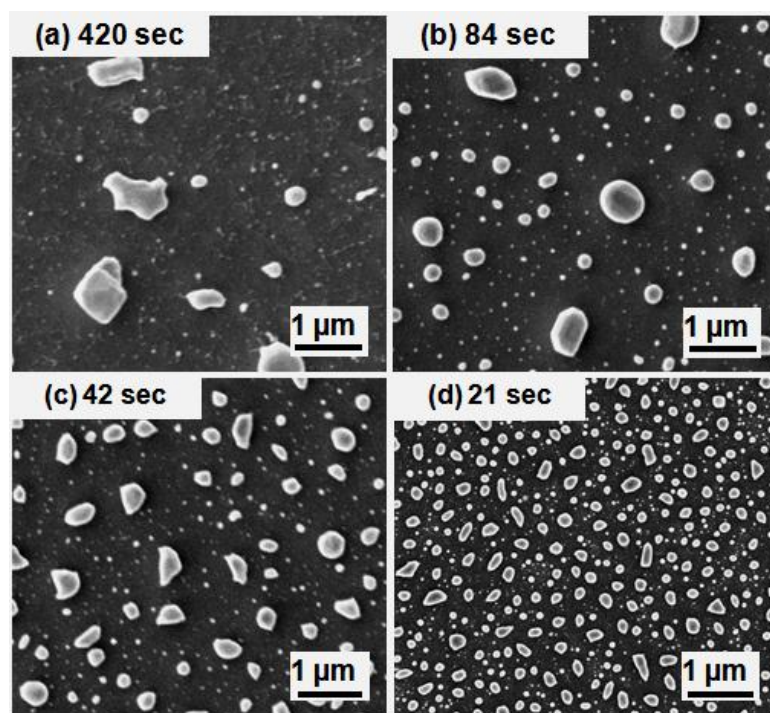


Fig. 2.16 Formation of Ni nanoparticles from 5nm thin films after varying temperature ramping rates.

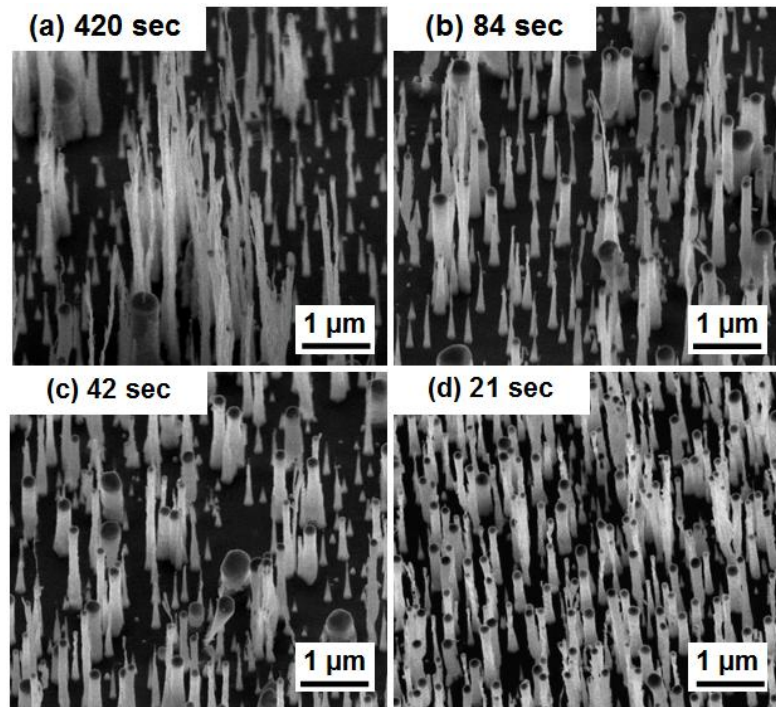


Fig. 2.17 CNTs grown from Ni nanoparticles depicted Fig. 2.16.

Throughout this work, these results were used to select CNT growth parameters that would produce appropriate emitter morphologies. Furthermore, these methods of controlling CNT morphology will allow future researchers to tailor the CNT emitters synthesized to the requirements of their desired applications.

2.7 Methods of Testing CNT Properties In-situ

CNTs are excellent candidates for many applications because of their exceptional electric properties. Many of these properties are determined by the internal structure (single vs. multi walled, chirality etc) of the CNTs. TEM analysis is essential in examining these internal structures. The traditional method for preparing CNTs for TEM analysis involves scraping the CNTs from the substrate, suspending them in a

solvent, and finally depositing them on a TEM grid. This procedure has a number of drawbacks. First of all, only generic observations can be made; if we find an especially interesting region using SEM, it is next to impossible to make a TEM sample of that specific area using this method. In addition, the act of scraping the CNTs from the substrate introduces a reasonably high likelihood of structural damage to the CNTs and makes it impossible to examine the interface between the CNT and the substrate in TEM. In response to these drawbacks, two methods of examining CNTs in-situ are presented.

In the first method, horizontally aligned CNTs are directly synthesized across slits in a special TEM sample holder. This allows for direct observation of well aligned, as-made CNTs by SEM or TEM and avoids any sample preparation procedures that may alter the structure of the CNTs. In addition, by depositing Pt electrodes on either side of the a TEM slit, additional electric properties of these CNTs, including CNT-substrate contact resistance and I-V characteristics, can be studied. Unfortunately, depositing the electrodes introduces some contamination problems. Two methods of Pt deposition, electron beam and ion beam induced deposition (EBID and IBID), were tested and relative contamination levels assessed in TEM.

The first method is ideal for characterizing the electric and morphological properties of CNTs themselves, but it does not allow study of CNTs incorporated into devices. In device development, it would frequently be desirable to examine the CNT-substrate interface or the interior gate structure. SEM is often in sufficient for such

observation. In the second method, a desired sample spot is identified in SEM and then FIB technology is used to excise sufficiently thin vertical slices of the device for TEM analysis. While this method inevitably contaminates the sample, it offers a unique opportunity to examine aspects of a device not visible in SEM.

2.7.1 CNTs Structure properties

As mention above, a special TEM sample was used to synthesize horizontally aligned single-walled CNTs and investigate their internal structure through TEM. A Si_3N_4 membrane window TEM grid was fabricated with a window thickness of 50 nm and a surrounding silicon support thickness of 200 μm . A thin film catalyst consisting of Al (15 nm)/Fe (1 nm)/Mo (0.3 nm) was deposited onto the Si_3N_4 membrane grid via a sputter coater [86]. The thickness of these catalyst layers was controlled with a quartz-oscillator thickness monitor. The dual-beam FIB was then used to mill a series of slits completely through the Si_3N_4 window membranes, creating the TEM grid (Fig. 2.18a). This substrate was placed in a CVD chamber with a base vacuum of ~ 0.1 mbar. The temperature was ramped to 950 $^{\circ}\text{C}$ at a rate of 300 $^{\circ}\text{C}/\text{min}$. Once the desired temperature was reached, acetylene was fed into the chamber at a flow rate of 200 SCCM as a carbon source. The nanoparticles produced from melting the thin film reacted with the gaseous C_2H_2 , leading to the formation of single-walled CNTs [87].

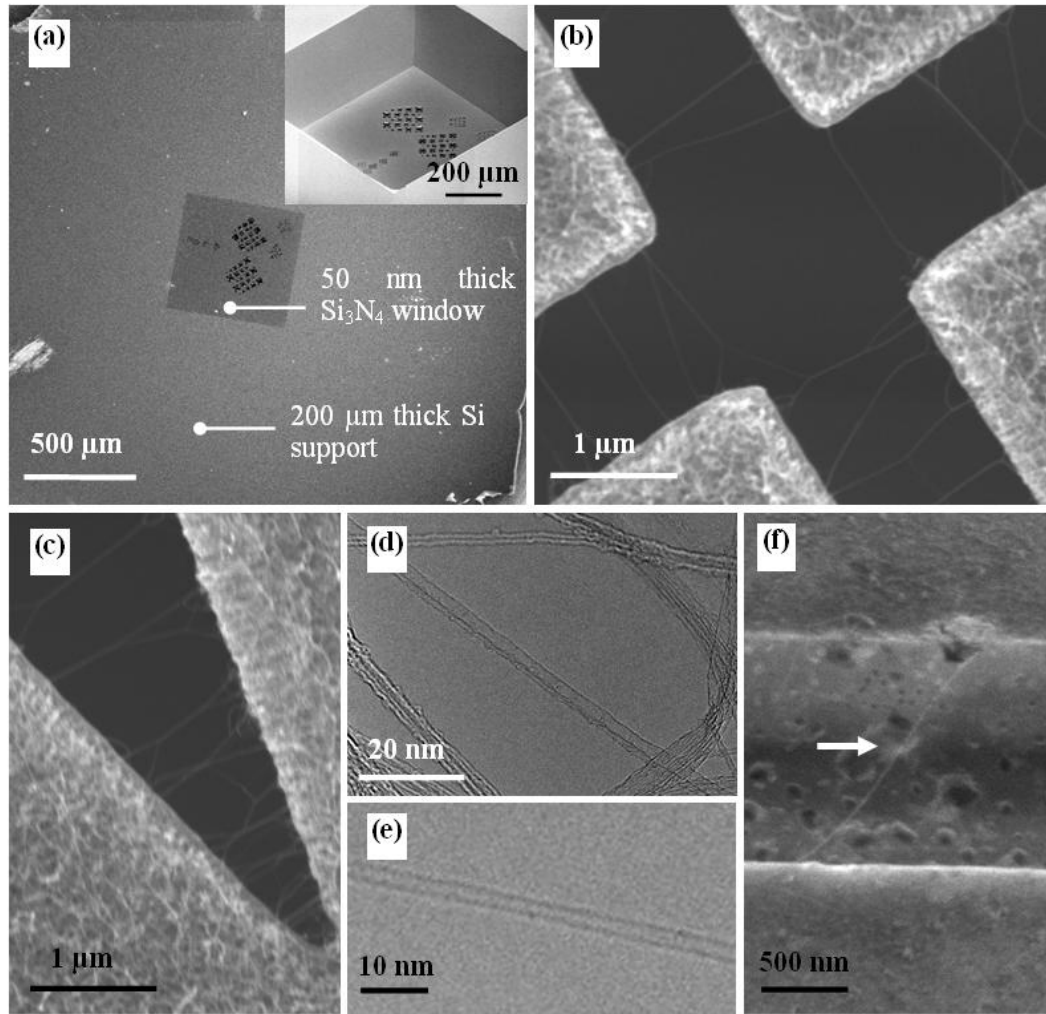


Fig. 2.18 Synthesized horizontally aligned single-walled CNTs.

(a) SEM image of the pattern of slits milled in the Si_3N_4 membrane window with surrounding silicon support. The insert image shows the reverse side of this TEM grid. (b)-(c) Suspended networks with well-defined orientations grown across the slits shown in (a). (d) TEM images showing bundles of single-walled CNTs and (e) isolated single walled CNTs. (f) SEM image of single-walled CNTs grown across two electrodes in Si substrate.

Suspended CNT networks with well-defined orientations grew across these slits, as visible in Figs. 2.18b and c. As the gap width was increased, the nanotube density decreased and the maximum growth distance was approximately 2.5 μm . In this growth process, although the CNTs were well aligned horizontally from one side of the trench to the other, no external driving force such as plasma or an electric field was applied to the growth process. It is plausible that the growth direction of the CNTs was driven by van der Waals forces [88].

The CNTs synthesized by this method could be directly characterized in TEM. In the high-resolution TEM images in Figs. 2.18d and e, the wall structure of an individual single-walled CNT can be clearly observed. These suspended bridges are individual or bundled single-walled CNTs with diameters of approximately 1–3 nm. These results are consistent with those reported by Choi et al. [89], whose work featured the fabrication of CNTs on a micro-machined silicon grid using thermal oxidation, an ion-implanted catalyst, and wet etch and dry etch methods.

The method introduced here can be used to synthesize both multi-walled CNTs and single-walled CNTs. To verify the morphology of the CNT samples of either multi-walled or single-walled CNTs with high growth density, Raman spectroscopic analysis was performed using an excitation line at 488 nm. Fig. 2.19 shows the Raman spectra of MWCNTs and SWCNTs grown at 750 and 950 $^{\circ}\text{C}$, respectively. The SWCNT spectrum revealed a typical radial breathing mode (RBM) peak around 186 cm^{-1} , corresponding to the disordered carbon band (D band, around 1344 cm^{-1}) and highly ordered graphite band (G band, around 1593 cm^{-1}). The G:D peak ratio of

SWCNTs (5.4) was larger than that of MWCNTs (1.3), which confirmed that the quality of SWCNTs was better than that of MWCNTs. The G peak high wave number shift (30 cm^{-1}) of SWCNTs with respect to MWCNTs further validated the high quality of the SWCNTs.

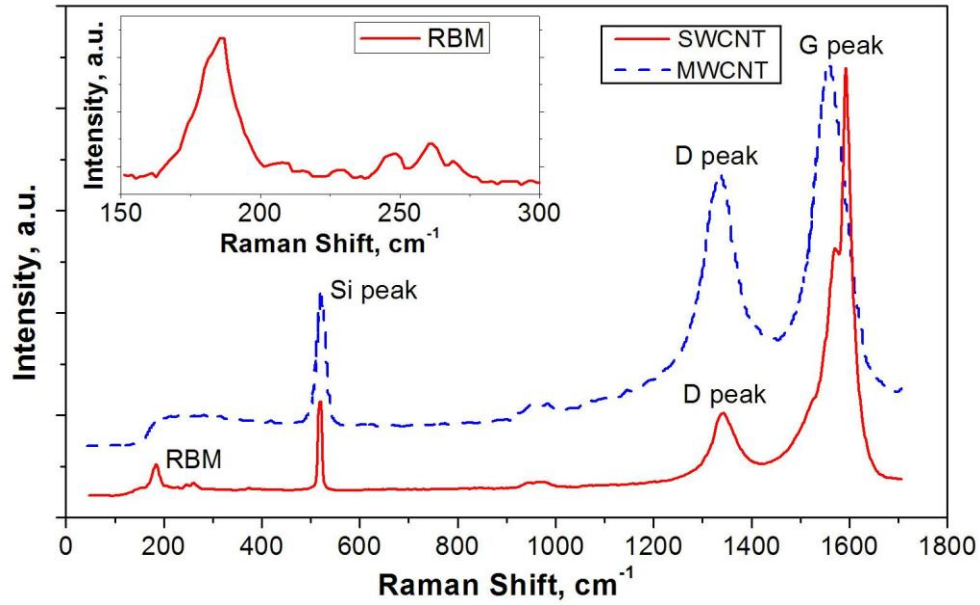


Fig. 2.19 Raman spectrum of single-walled CNTs and multi-walled CNTs on Si substrate. The inset shows a high resolution RBM peak around 186 cm^{-1} .

This method could be extended to test the properties of directly fabricated CNT field-effect transistors (FET). Electrodes were deposited at either end of a horizontally aligned CNT like that shown in Fig. 2.18f. This allowed testing of contact resistance, as well as the effect of adsorbates and substrate temperature on the reduction of the contact resistance. It is expected that the direct growth of CNTs should be able to minimize the substrate-to-CNT contact resistance (typically on the

order of kilohms or megaohms), a factor that frequently interferes with tests performed in the traditional dispersion and alignment methods [90, 91].

2.7.2 CNTs Electric Properties

Since the demonstration of the CNT FET in 1998, intensive efforts have been made to fabricate CNT-based devices and to characterize their electronic properties [92]. CNTs have unique ballistic transport characteristics and high carrier mobility which have attracted a great deal of attention [93, 94]. However, the techniques used to grow single CNTs usually result in wide variations of the shape, size and internal structure on which their electronic properties are based. It is this variation that necessitates a methodology to connect those electronic properties to their observed structure.

The horizontal CNT fabrication process is already discussed in Section 2.7.1. In order to fabricate CNTs FET, I use an electron beam and ion beam induced deposition method (EBID and IBID) to deposit a Pt electrode on two ends of CNTs to test the CNT's electric properties, including contact resistance and I-V characteristics. This deposition method can deposit on almost any solid surface with very high spatial precision and is currently used for deposition of conductors in integrated circuit editing.

In order to deposit the Pt electrodes, I use a gas injection system (GIS) to deliver methylcyclopentadienyl platinum trimethyl $(\text{CH}_3)_3(\text{C}_5\text{H}_4\text{CH}_3)\text{Pt}$ metallorganic molecules to the deposit location. The ion beam or the electron beam decomposes the gas molecules into volatile parts, which are pumped away, and nonvolatile Pt metal

residues remain to form the deposit (Fig. 2.20) [95]. All deposited films contain not only the desired Pt metal, but also incorporate impurities from the incompletely decomposed metallorganic molecules and Ga from the ion beam. The deposited film is an admixture of Pt, C, Ga and O with a ratio of 45:24:38:3 and may vary depending on different deposition conditions [96].

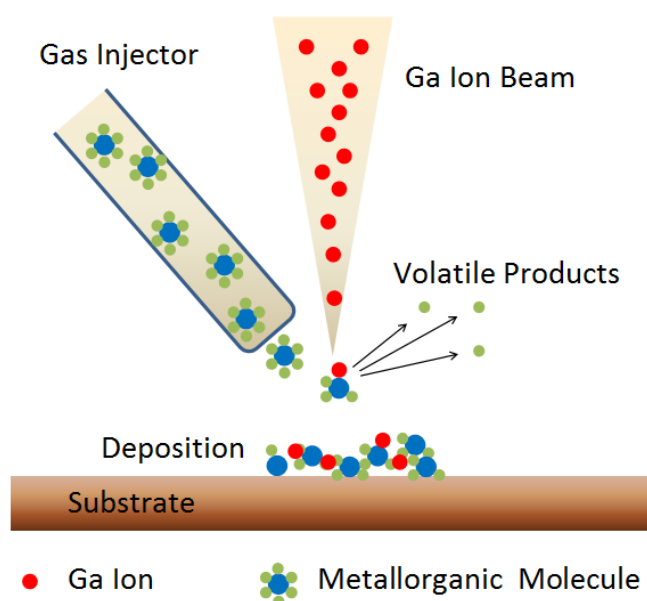


Fig. 2.20 Schematic drawing of ion beam induced deposition process.

The advantage of beam-induced deposition is that by using nanometer scale scanning beams, various features can be modified with nanoscale precision in size and position. Fig. 2.21a presents Pt electrodes deposited at either end of a CNT by Ga ion beam induced deposition.

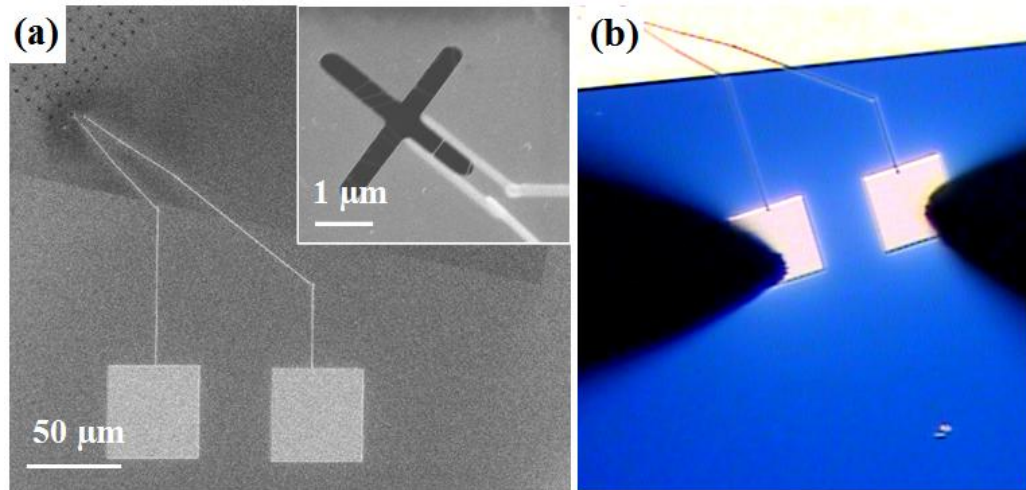


Fig. 2.21 Fabricated electrodes at the end of CNTs.

(a) Electrodes are deposited at the two ends of CNTs to allow electronic properties to be tested. The insert image shows details of the electric contact. (b) A CCD image of two probes that are used to test the electronic properties.

The electrical contacts leading to a single CNT circuit were easily located by the tungsten tip of the probe station (Cascade Microtech Summit MicroChamber). They are shown touching down in Fig. 2.21b. The source-drain current (I_{ds}) through the CNTs as a function of the bias voltage (V_{ds}) was measured at room temperature with an Agilent 4156C semiconductor parameter analyzer.

SEM and TEM were used to characterize the morphology and internal structure of the fabricated CNTs. An isolated, horizontal, single walled CNT of $\sim 2 \mu\text{m}$ in length suspended across a membrane window is shown in Fig. 2.22a. Note that the TEM image in Fig. 2.22b-c shows that the majority of CNTs were single walled with a diameter of 1~3 nm.

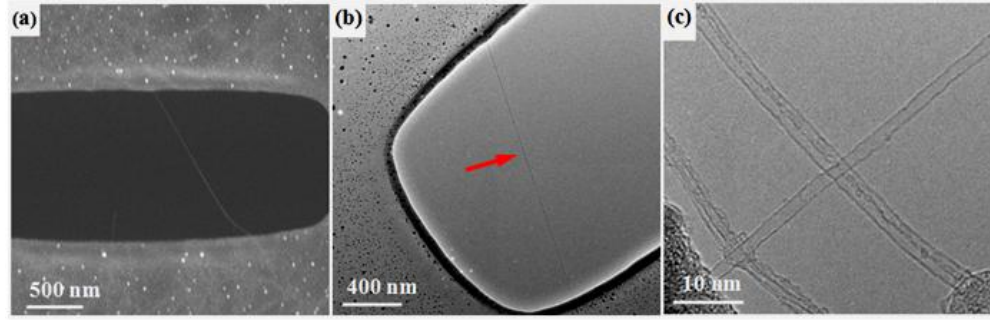


Fig. 2.22 SEM and TEM characterize the fabricated CNTs.

(a) SEM image of suspended CNTs grown within gaps. (b) A low magnification TEM image of a CNT. (c) High resolution TEM image showing isolated and bundled SWCNTs.

As shown in Fig. 2.23, the I-V curve indicates that the aligned single walled CNT test subject possesses metallic characteristics. During the electronic measurement, V_{ds} was swept from -3 to 3 V with a 0.1 V step size. The contact resistance was measured several times and was found to remain constant at 75.1 k Ω over the duration of the tests. This suggests a good contact between the CNT and the Pt electrodes.

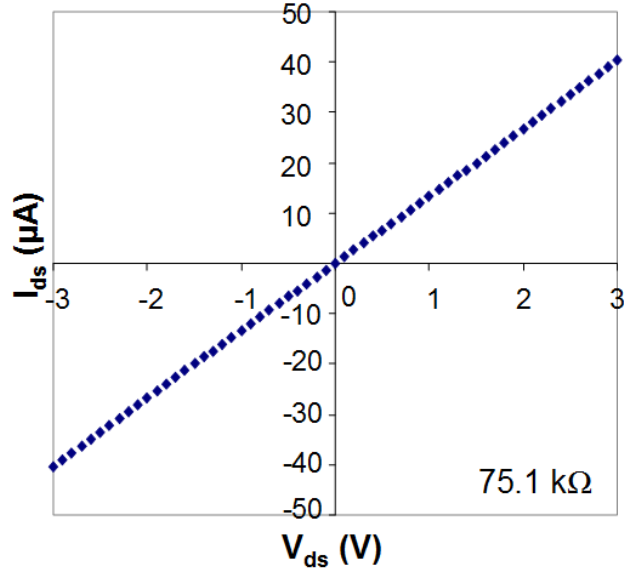


Fig. 2.23 Dependence of current on drain voltage in a single-walled CNT contaminated by Pt deposition.

After conducting the electrical tests, the samples were removed from the probe station and placed back into the TEM in order to observe the nanotubes after the I-V measurement. The electrodes that are connected to the CNT can be seen in Fig. 2.24a. The image in Fig. 2.24b shows that the CNT under test was coated with a layer of Pt approximately 7 nm thick. EDX spectroscopy confirmed that the coating was, indeed, Pt [Fig. 2.24c]. This contamination is caused by the ion beam induced metal deposition. During the deposition of the electrodes, the ion beam caused an aura of metal contamination around the target area. This evidence of contamination puts the metallic character of the CNT into question. On the other hand, since the CNT FETs were synthesized on this special TEM grid, it was easy to detect the contamination and determine its extent, which verifies the benefit of in-situ TEM analysis.

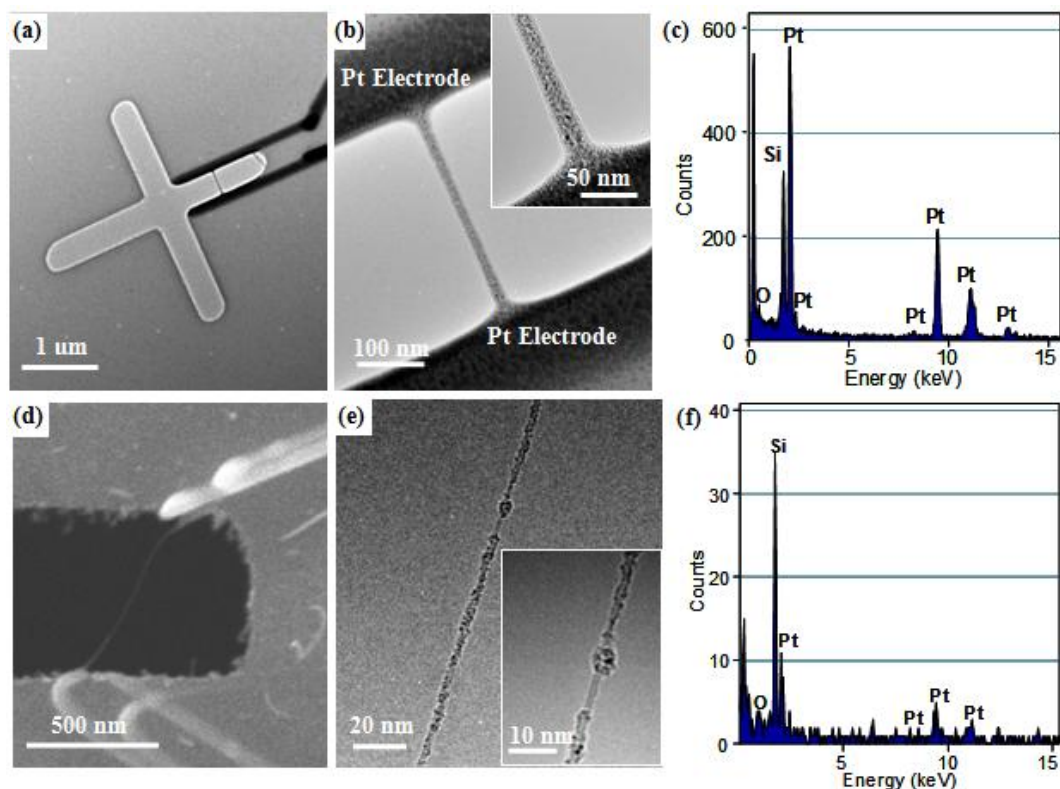


Fig. 2.24 IBID and EBID under TEM.

(a) TEM image of CNT bridging two electrodes. (b-c) TEM shows CNT after IBID of Pt. This is confirmed by EDX. (d) SEM image CNT after EBID of Pt. (e-f) TEM and EDX of CNTs after EBID showing less Pt contamination than after IBID.

In addition to contaminating the CNTs with Pt, IBID can damage the substrate on which deposits are formed and the gallium ion beam also may result in unintended ion implantation and contamination. The electron beam does not significantly damage the substrate and causes less contamination than the ion beam. EBID of the Pt electrodes [Fig. 2.24d] was attempted using the same metal compound deposition source. The image in Fig. 2.24e shows that part of the tube is contaminated by the Pt

as well, which is confirmed by the EDX spectrum in Fig. 2.24f. The coating, however, is very thin and less uniform. The single walled CNT can still be seen between the gaps. The electron beam is well known to have a smaller probe size than the ion source. This may be the reason for reduced contamination in comparison to the IBID.

In summary, in order to fabricate single-walled CNT FEAs, IBID and EBID were employed to fabricate electrodes. However, the process contaminated the CNT and surrounding area due to an aura of Pt. The nanotube was coated by the metal which made it appear to have metallic properties. This suggests that using dual-beam FIB may not be an effective way to fabricate electric contact for CNT FETs. Electron beam lithography may be one solution to this type of contamination. Regardless, the in situ methodology introduced here will provide an alternative method for the characterization of internal structures of as-made CNTs. This may also help us to understand the effect of processing parameters for the electronic properties of CNT devices.

2.7.3 CNT/substrate interface properties

During my research, it is essential to be able to closely examine individual device structures, like the gate layer of a CNT FEAs or the CNT-substrate interface of a CNT bundle. SEM microscopy does not offer suitable resolution when imaging structures on the 100 nm scale. The TEM is appropriate for analysis on this scale. However, the traditional method for preparing these samples in TEM is insufficient for a number of reasons. As discussed above, traditional scrape-suspend-deposit methods

are insufficient to fully characterize even structures like uniform CNT growth. It cannot possibly be used to study a device in a CNT FEA.

Dual-beam FIB technology offers a solution. The dual-beam FIB allows one to locate the lift-out site with SEM resolution and then use the ion beam to excise the sample. The dual-beam FIB can then thin the extracted sample to the 100 nm thickness required for TEM microscopy. In addition, the dual beam saves time because it polishes and grinds in one machine.

I did find that Ga contamination from the ion beam affected the quality and reliability of the process wafer and CNTs. Ga deposition can be observed on the surface of the effected nanotubes and the rapid ion beam appears to have fused some of the nanotubes together. However, we identified a number a steps to decrease the contamination and damage to the CNTs sample. Lower beam current cutting (30 pA) was used to minimize damage, see Fig. 2.25a. For further cleaning, we tilted the sample 1.5 °so that the contaminated edge was partially exposed from above. We then used low-current line cutting to shave the contaminated face off of the bundle. The length of time spent on each line cut varied depending on the thickness of the sample at that point, minimizing new contamination or overheating of the sample. The result is shown in Fig. 2.25b.

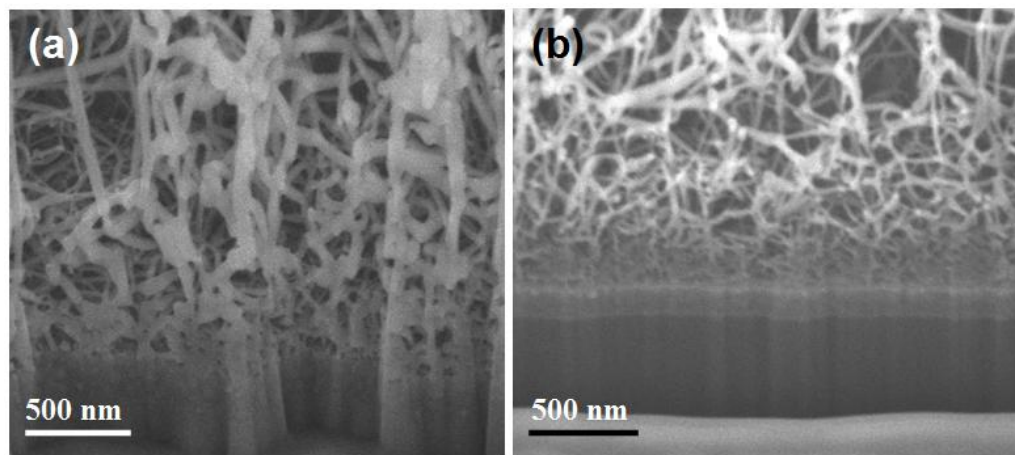


Fig. 2.25 Lower beam current cutting and cleaning step to minimize damage to the CNTs bundles.

(a) High magnification of the root area of CNTs bundle to research the density and the interface between Si wafer and CNTs bundle. Ion contamination is still clearly present on the surface of the vertical trench.

(b) After the cleaning cross section steps, the ion-induced contamination is decreased and the CNT root area and Si-bundle interface are visible.

I demonstrated this method of TEM sample fabrication on a 15 μm bundle of CNTs, shown as Fig. 2.26a. The detailed structure at the base of the CNTs where they interface with the substrate, which contains the essential information on nucleation and growth, is usually disregarded in the literature. The substrate-CNT interface was traditionally ignored because it is too small to be observed using SEM, and only dispersed CNT samples, which do not include the interface, are usually characterized using TEM. I cross-sectioned the CNT bundle and used TEM to analyze the interface between the silicon substrate and the CNTs bundle.

Initially, the CNTs in the bundle were inclined to fall over during TEM sample preparation. We used the ion beam metal deposition technology to deposit a Pt ring around the base of the bundles to support the nanotubes, as shown in the insert image of Fig. 2.26a. The “in-situ lift-out” method of TEM sample preparation can be simplified into three successive steps. In the first we excised the lift-out sample using FIB milling, extracted the sample from its trench with two rapid ion-milling steps, or “cuts,” and fixed the probe to the released sample through ion beam metal deposition. The sample was then removed from the wafer by the nanomanipulator. The second step is the “holder-attach” step, during which the sample is translated on the probe tip to the TEM sample holder (the lift-out grid) and attached (again, typically with ion beam-induced metal deposition). The sample is later detached from the probe tip point using FIB milling. These two steps are shown in Fig. 2.26b. The third and final step is the thinning of the wedge into an electron-transparent thin section using FIB milling. After the thinning step, the wedge is about 100 nm thick, as shown in Fig. 2.26c.

The CNT bundle, and particularly the bundle/substrate interface, was studied in TEM. A cross-section TEM of the CNTs and the CNT/substrate interface is shown in Fig. 2.26d. As shown in Fig. 2.26e, the CNTs do not directly adhere to the substrate as proposed in many growth models. The tubes are, instead, anchored to the substrate via a silicon-iron film, approximately 250 nm thick, also shown in Fig. 2.25b and Fig. 2.26f. Small particles (5~30 nm) were present inside the silicon-iron film, which the EDX results in Fig. 2.27a–b shows are rich in iron, silicon and oxygen. The EDS line scan from the silicon substrate to the CNT base growth in Fig. 2.27c–d shows that the

silicon signal decreases sharply while the carbon signal increases and the iron signal increases briefly and then decreases. The data indicates that there are three distinct layers: silicon substrate, silicon-iron layer, and CNT base growth. In addition, the TEM imaging showed that individual CNTs do not grow directly from the substrate. The tiny catalyst nanoparticles initially produce very thin, dense CNT growth. These CNTs appear to merge, resulting in increasingly thicker CNTs that eventually level out. This final thickness and density then remains constant throughout the bundle.

This type of fundamental research is essential to later understanding how the various components of a device function and interact.

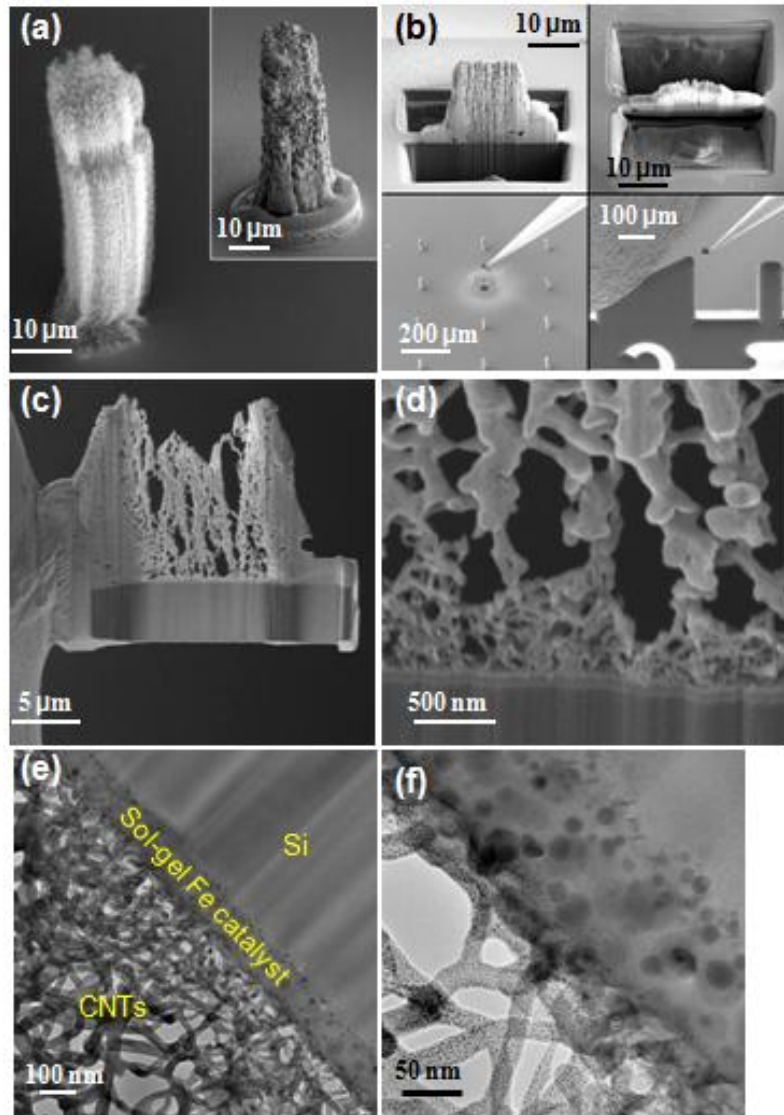


Fig. 2.26 TEM sample preparation by using dual-beam FIB.

(a) A 15μm CNTs bundle for TEM sample preparation. In order to prevent bundles from falling apart, we deposited a Pt ring to support the CNTs bundle, shown in the inserted images.

(b) “In-situ lift-out” method for TEM sample preparation. Side view and top view of CNT sample after FIB milling of the sample. We can see the CNT bundle has a little

warping. The TEM sample is lifted from the silicon wafer using an omniprobe and mounted on the TEM sample holder.

(c) Overview of the TEM sample after it has been mounted to the TEM sample holder.

(d) High magnification SEM image shows the CNT/substrate interface.

(e) The CNTs do not directly adhere to the substrate as proposed in many growth models. The CNTs are, instead, anchored to the substrate via a silicon-iron film with a thickness in the range of ~250nm.

(f) Small $(\text{Fe,Si})_3\text{O}_4$ particles (5~30nm) were present inside the sol-gel catalyst film.

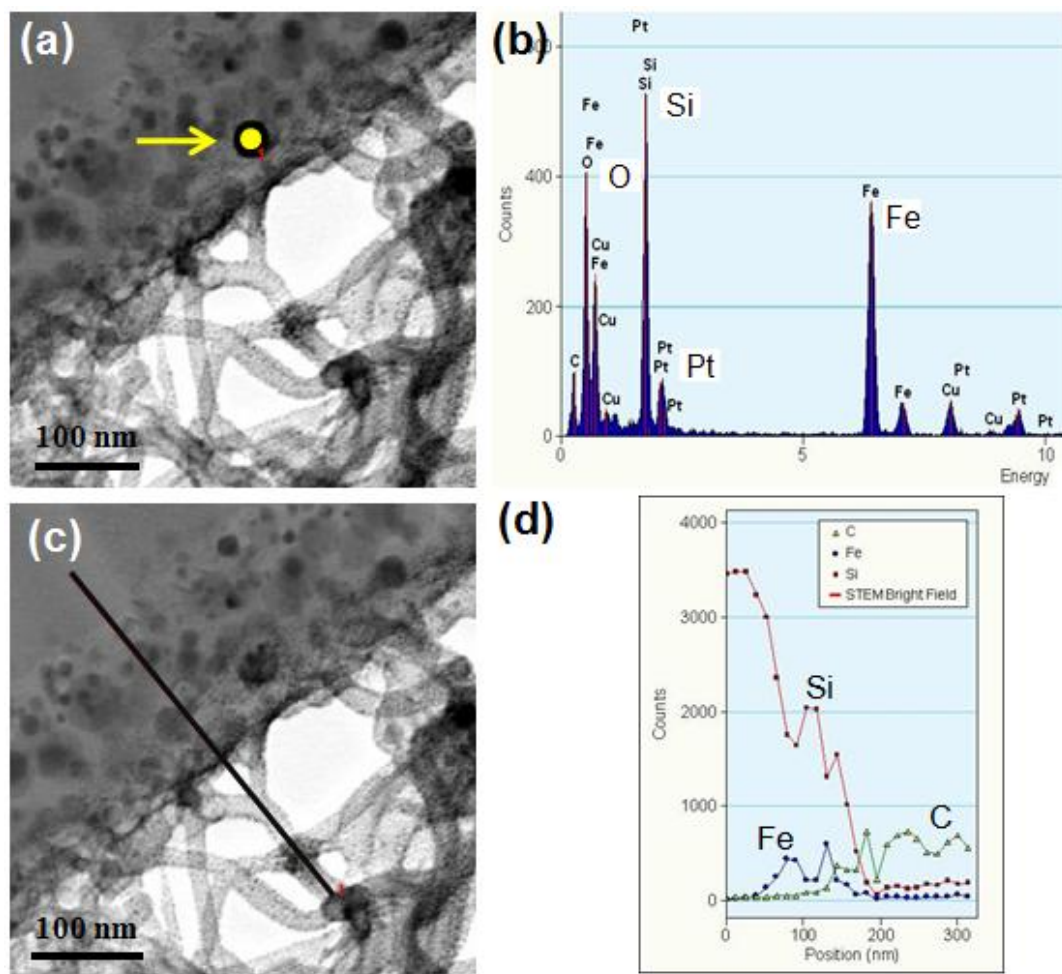


Fig. 2.27 STEM image and EDX scan spectrum.

(a) STEM image of the CNT/substrate interface. (b) An EDX spot scan spectrum of the nanoparticle region labeled in (a). (c) – (d) An EDX line scan spectrum of the CNT region shows the distribution of carbon, iron and silicon along the CNT/substrate interface.

Chapter 3 FABRICATION OF TRIODE-TYPE CNT FEAs

The key challenge for fabricating triode-type FEAs is how to accurately grow emitters inside of the gated cavities. In this chapter, two methods for the fabrication of triode-type CNT FEAs, the commonly used “top-down” approach and a new “bottom-up” method, are compared. Various improvements to the “bottom-up” method are also studies to make it more effective at fabricating large area functional triode-type CNT FEAs devices.

3.1 “Top-down” Method

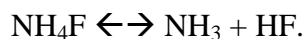
The “top-down” method is the most common method to fabricate triode-type FEAs, which can be summarized in four steps: open the gate layer, wet etch the insulator to form cavities, deposit the catalyst into cavities, and synthesize the emitters into each cavities. My experimental approach for “top-down” method is based on the previous research: fabricate CNTs at desired locations by controlling the catalyst location. Below is the detailed fabrication process.

In this study, I created a sandwich structure consisting of a stack of multi-layers, where a Pt thin film of 120 nm (serving as the gate electrode) was fabricated on top of a SiO₂/Si substrate. A TiN adhesion layer of 50 nm was deposited between the Pt and SiO₂. Then a layer of photoresist was spin coated onto the top of the Pt surface to protect the surface from contamination. To avoid charging during electron microscopy characterization, a thin Au layer (40 nm) was then deposited on top of the photoresist layer (Fig. 3.1a). An FEI 611 FIB was used to mill arrays of holes into

SiO₂ of this multi-layer substrate (Fig. 3.1b). In order to form cavities and expose the Si substrate, the substrate was put into a buffered hydrofluoric acid (BHF) solution (Fig. 3.1c). The BHF used was an admixture of HF (49%), water, and ammonium fluoride (NH₄F) with a ratio of 1:6:4. The etching rate for SiO₂ was about 1000 Å/min. The overall reaction for etching SiO₂ with BHF is:



The function of NH₄F (the buffering salt) was to control the pH of the mixture in order to minimize the photoresist removal by HF. The buffering reaction was:



Without the buffering salt, the photoresist layer peeled off from the substrate very easily.

To deposit catalyst into the cavities, I investigated two different deposition methods and two different types of catalysts. The first method was the spin coating of sol-gel Fe catalyst into the arrays of cavities (Fig. 3.1d). The second method was sputter coating Ni thin film catalyst into the cavities (Fig. 3.1e). After catalyst deposition, the photoresist on the surface of the substrate was removed, leaving only the catalyst inside of each cavity.

After completing these processes, the whole substrate was placed in a ceramic boat and put into a CVD reactor for CNT synthesis (Fig. 3.1f).

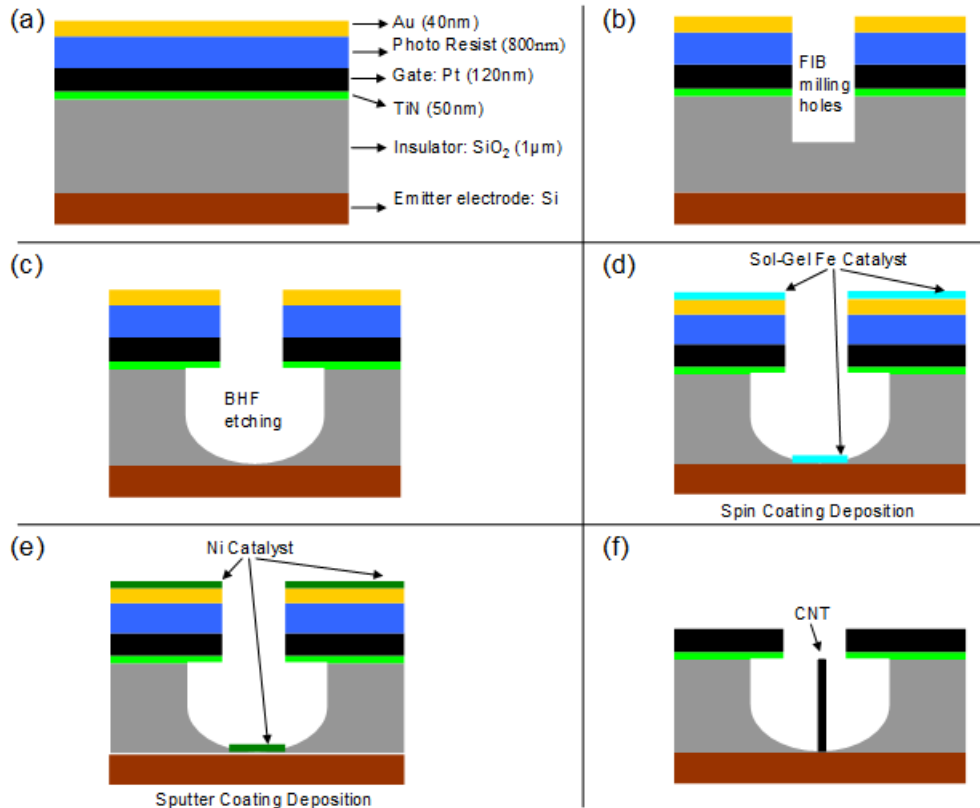


Fig. 3.1 Schematic of fabricating triode-type CNT FEAs by “top-down” method.

SEM was used to characterize the sample before and after BHF etching and photoresist lift off. Fig. 3.2a shows an array of cavities after BHF etching. The inserted image in Fig. 3.2a shows one of the holes before BHF etching, suggesting that FIB milling creates holes with a column-like shape. Therefore, it is necessary to use BHF to etch the holes to a cavity shape as illustrated in the inset of Fig. 3.2b. A SEM image of a specific cavity created to demonstrate the cavity structure before and after photoresist lifting is shown in Fig. 3.2b. Note that half of the cavity is covered with the photoresist, and another half reveals the Pt surface. These results demonstrate the successful fabrication of triode-type substrate.

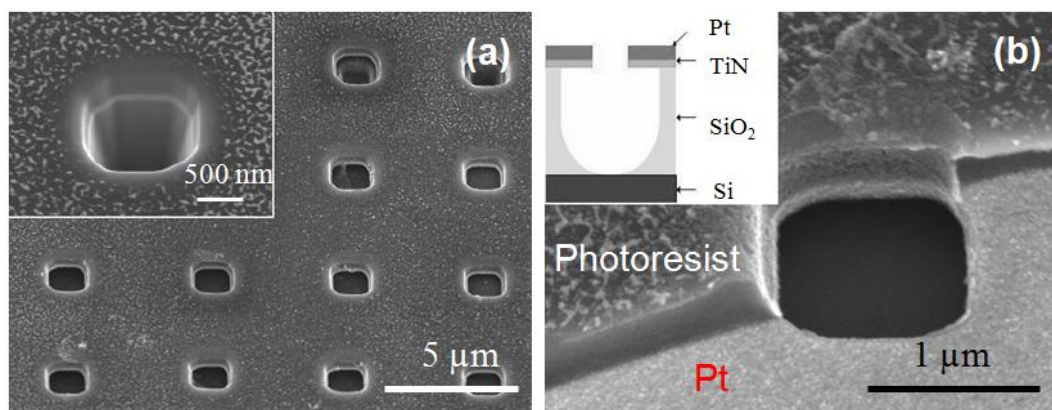


Fig. 3.2 SEM image of the holes before and after BHF etching.

(a) Arrays of cavities after BHF etching. The inserted image shows one of the holes before BHF etching. (b) A specific cavity demonstrating the structure before and after the photoresist lift off. Note that half of the cavity is covered with the photoresist, and the other half reveals the Pt surface of the cavity. The inserted illustration shows the structure of the wafer after the BHF etching and photoresist lift off.

A set of SEM images obtained from the samples after CNT synthesis is shown in Fig. 3.3a-b. Note that although CNTs were formed in almost every cavity, the morphologies of the CNTs were quite different. The average diameter of the CNTs from Ni catalysts (Fig. 3.3b) was smaller than that of CNTs from the sol-gel Fe catalyst (Fig. 3.3a). CNTs from both catalysts were curly and randomly oriented.

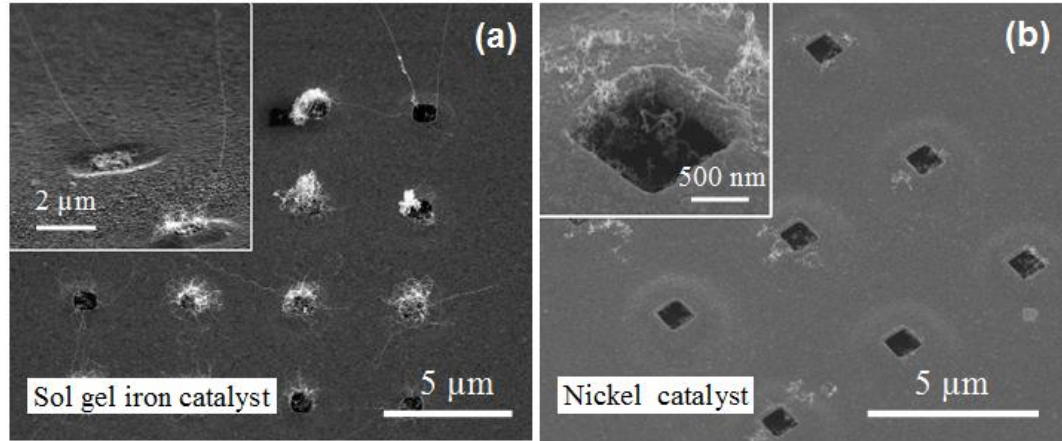


Fig. 3.3 SEM images of CNTs synthesized by different catalyst.

(a) CNTs grew from arrays of devices using sol gel Fe catalyst. The inserted image shows two standing CNTs from two devices.

(b) CNTs grew from arrays of devices using sputter coated Ni as the catalyst. The inserted image of CNTs was taken at a higher magnification.

However, the “top-down” method presented some significant problems. One of the largest problems is cathode-gate short circuiting. The random growth shown in Fig 3.3 would almost inevitably result in contact between CNT emitters and the Pt gate, resulting in cathode-gate short circuiting. Substituting PECVD growth for CVD growth would result in aligned, non-random growth, but even then, CNTs growing from the deposited catalyst will often come into contact with the rim of the gate layer. In addition, since the gate layer forms the roof of the cavity, any CNTs that do not make it through the gate opening are likely to touch the gate layer. This short circuiting problem is exacerbated if one tries to address one of the other key issues, the number of CNTs synthesized. The usual method for reducing the number of CNTs

grown is to reduce the area of catalyst they grow from. However, in this method, the only way to reduce the area of the catalyst would be to reduce the radius of the gate opening, increasing the likelihood that CNTs would contact the gate layer. Finally, this method relies on lithography and wet chemical etching procedures which make the whole process hard to control.

In order to solve the problems discussed above, I designed an effective and more controllable, “bottom-up” method for the fabrication of a large number of triode-type CNT FEAs. My technique employs dual-beam FIB technology to carve gated holes from a multilayer embedded catalyst substrate and PECVD to synthesize CNT emitters in these microgated holes, avoiding the lithography and wet chemistry procedures conventionally used to fabricate such structures.

3.2 “Bottom-up” Method

Instead of depositing the catalyst into milled holes (a common practice in other reports [97–99]) a multilayer structure with an embedded catalyst layer was used. To construct this structure, an indium tin oxide (ITO) adhesion layer of 15 nm was deposited on a silicon substrate, and a 10 nm thin film of Ni, serving as the catalyst for CNT growth, was sputter coated over it. A 1 μm thick layer of insulating SiO_2 was deposited onto the Ni catalyst by PECVD with N_2O and SiH_4 precursors at 280 $^\circ\text{C}$. Following this, another 15 nm ITO adhesion layer and a 120 nm thin film of Pt were deposited on top of the SiO_2 by sputtering. The Pt layer served as the gate electrode. A schematic diagram of the substrate design is shown in Fig. 3.4a. An FEI dual-beam

SEM/FIB was then used to mill arrays of holes to expose the Ni catalyst for the CNT growth, as illustrated in Fig. 3.4b-c.

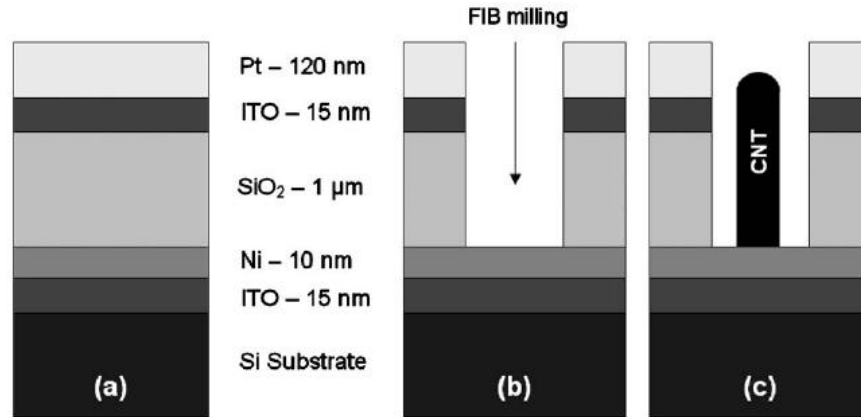


Fig. 3.4 Schematic of fabricating triode-type CNTs FEAs by “bottom-up” method. (a) Triode-type CNT FEAs substrate design including Pt gate, SiO₂ insulating layer, embedded Ni catalyst, and ITO adhesion layers. (b) Preparatory FIB milling and (c) result of CNT synthesis.

In this “bottom-up” method, I utilized the FIB to selectively expose the predeposited catalyst. This procedure has proven to be significantly easier than the deposition of a catalyst into pre-etched regions through sputtering, evaporation, or electrochemical deposition. In this process, control over the milled depth and geometry as it pertained to the exposed catalyst became the single crucial factor in substrate preparation. Determining mill depth proved a challenge since each layer of materials has a different milling rate (detail investigation in Section 3.2.2 and Section 3.3.2). It was therefore necessary to calibrate the settings (beam current and milling time) for a particular pattern to achieve the desired depth. Irregularities in the depth of

emitter holes in array can be reduced by milling for a longer time at a reduced beam current.

3.2.1 Effect of gate opening and milling depth

Once the gates had been fabricated and the catalyst exposed, vertically aligned CNTs were synthesized in each gated cavity using the PECVD. During synthesis, the substrates were heated to 725 °C and exposed to 50 SCCM of C₂H₂ and 200 SCCM of NH₃ gas for approximately 30 min.

SEM characterization of this variation in CNT morphology can be seen in Fig. 3.5. The results displayed three distinct morphological variables: bundling vs. individual growth, CNT diameter, and height. These morphological variables are impacted by milling parameters (hole depth and diameter) and growth parameters (duration).

Firstly, bundling vs. individual growth is determined by hole depth. In Figs. 3.5(I-II), I compare CNTs synthesized under the same growth parameters from holes of equal diameter but differing depth. The first, which produced individual thick nanofibers (Fig. 3.5I), was produced by milling to the exact depth of the Ni layer. Accurately milling to the catalyst layer allows tip growth from the entire exposed Ni surface. On the other hand, penetrating the catalyst layer, rather than just uncovering it, sputters Ni particles onto the inner walls of the hole, resulting in bundles of thin CNTs, grown from the redeposit catalyst (Fig. 3.5II).

Secondly, In Figs. 3.5(I, III) I see the diameter of individual CNTs correspond to the diameter of the milled holes they are grown in. In Fig. 3.5III the hole diameter

was reduced from $\sim 1\ \mu\text{m}$ to $\sim 300\ \text{nm}$ with hole depth and growth parameters held constant. Thin CNTs, grown individually, appear most promising as field emitters.

Finally, the height of the CNT in relation to the gate layer can be controlled by limiting the plasma exposure time during PECVD growth. A reduced plasma time (and therefore overall growth time) of approximately 15 min will allow the CNTs to attain heights slightly below the gate layer (Fig. 3.5IIIId). For the gate potential to exert a significant effect, I want the CNT emitters more or less level with the gate layer (for further discussion of the effects of relative emitter-gate heights see Section 5.5.1). However, it is much easier to image, characterize, and determine the yield of taller CNTs.

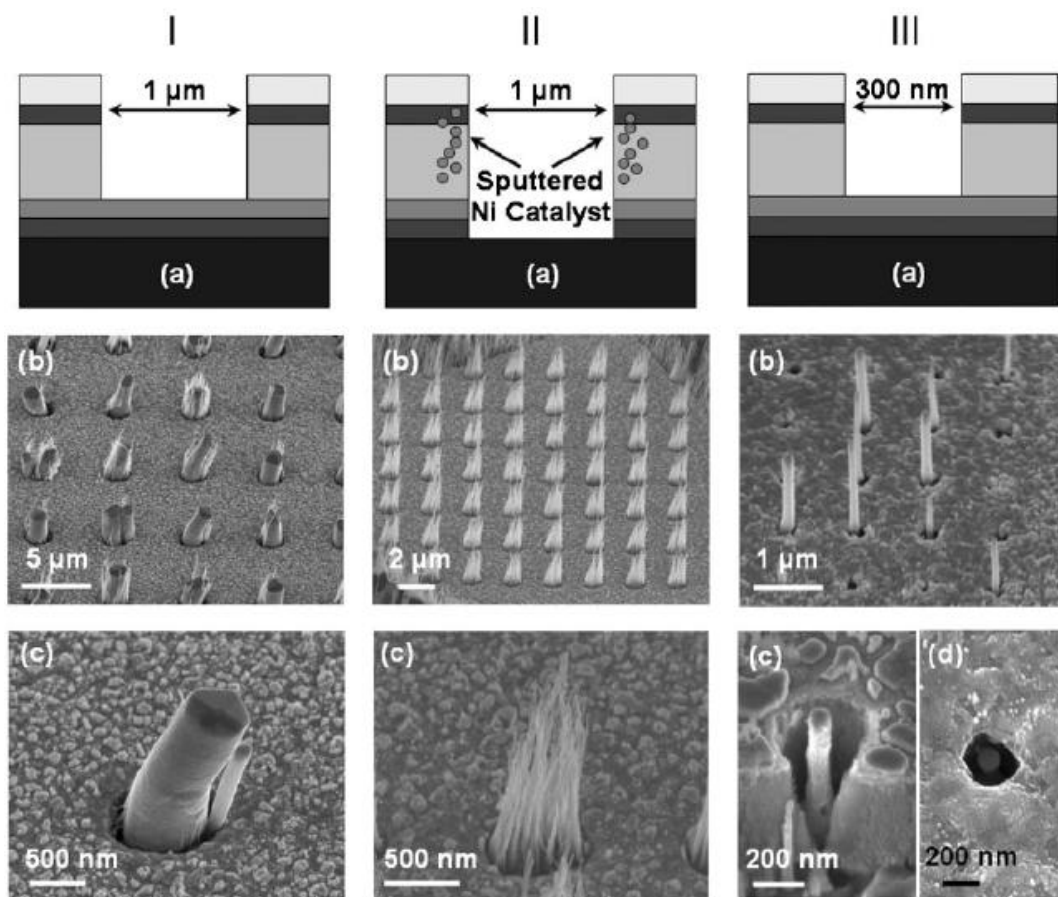


Fig. 3.5 Triode-type CNT FEAs fabricated by dual-beam FIB.

Nanofibers and CNTs fabricated within (I) 1 μm wide, triode-type, FIB-milled holes. Here the holes are milled to uncover but not penetrate the catalyst layer, (II) 1 μm holes milled through the catalyst, and (III) 300 nm wide holes that do not penetrate the Ni layer. (III)(d) Shorter CNTs produced by reduced plasma exposure during synthesis.

3.2.2 Control milling depth by step milling

A challenge in the fabrication process was control over the milling depth to accurately expose the amount of catalyst required for the CNT's growth. The milling depth is an important parameter in the fabrication process; insufficient milling will not expose the Ni catalyst at all, while over milling will damage or destroy it. Both extremes result in little or no CNT growth. Accurate milling can be difficult for a number of reasons.

First of all, the Ni catalyst layer is thin (10 nm) compared with the whole milling depth (Pt + SiO₂, >1.1 μm), which makes the appropriate milling depth harder to gauge.

Second, this is a multilayer milling process: different materials have different density and sputtering yields, which means various milling rates. The sputtering yield is defined as the number of ejected particles per incident ion. Table 3.1 lists the sputter yield of 30 keV Ga ion at 0 degrees incident angle [100]. The sputter rate of metal is higher than other materials, which means metals are easy to mill compared with Si. Due to the different sputtering yields for different materials, I cannot figure an average milling rate and simply use milling time to control the milling process (Fig. 3.6).

Table 3.1 Sputter yield of 30 keV Ga ion at 0 degrees incident angle.

<i>Pt</i>	<i>Ni</i>	<i>Si</i>	<i>O</i>
9.76	9.69	2.78	4.75

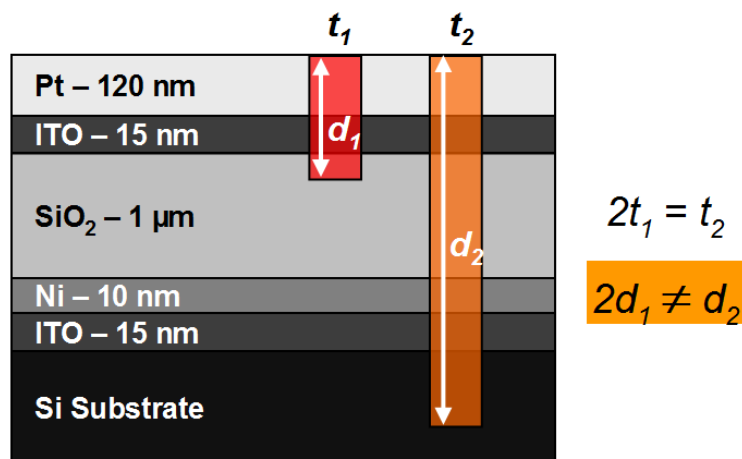


Fig. 3.6 Schematic of multilayer substrate milling.

Based on the above discussion, I designed a step milling method which used Autoscript software to optimize the milling procedures for control of the milling depth. In an initial trial, I milled an array of successively deeper rows of holes and then synthesized CNTs in each of them (Fig. 3.7). The results suggest that when the Ni layer was barely exposed, very few CNTs grew (Fig. 3.7a). Partially exposing the Ni layer resulted in low CNT density and non-uniform growth (Fig. 3.7b). However, when the Ni layer was completely exposed within the hole, the CNT grew uniformly along the perimeter of the hole, as in Fig. 3.7c. The characterization of subsequent rows suggests that if ion beam had milled too deep, it would result in reduced numbers of CNTs (Fig. 3.7d). From these results I selected the optimal milling time for catalyst exposure. In the two-hole case, the outer hole was formed within 44s of milling time with a beam voltage of 30kV and beam current of 300pA. An additional 5s of milling with the same parameters was used to create the inner hole to expose the catalyst.

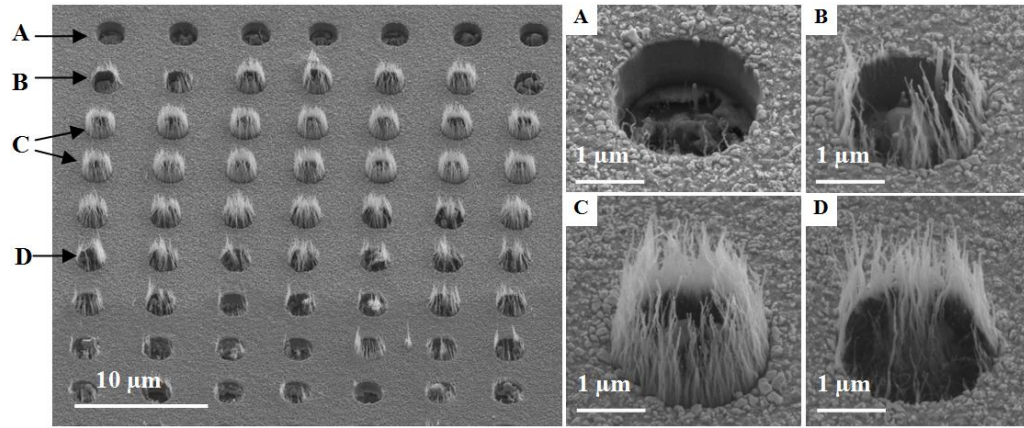


Fig. 3.7 SEM image of triode-type CNT FEAs synthesized from different depths. In the left image, hole depth increases as I go down each column. Shallow holes failed to uncover the catalyst layer (a) or only partially uncovered it (b) resulting in irregular growth. Uniform CNT growth (c) indicated optimum milling time, while subsequent rows of irregular growth (d) indicated overmilling of the catalyst layer.

3.3 Improvements to the “Bottom-up” Method

As discussed in Section 3.2, the “bottom-up” method avoids the lithography and wet etching process to fabricate triode-type structures. However, during the fabrication and field emission process, I met several problems which either affected the function of the gate layer, or influenced the fabrication yield of the triode-type structure. Here I list several improvements to the “bottom-up” method to solve these problems.

3.3.1 “Two-hole” milling steps to prevent CNTs from shorting the gate layer

I successfully used the method discussed in section 3.2 to fabricate the triode-type CNT FEAs as shown in Fig. 3.8I. However, when I attempted to perform field emission tests on these arrays, they naturally resulted in a short circuit between the substrate and the gate layer. To overcome this obstacle, I modified the fabrication design by milling one hole inside of another (Fig. 3.8IIa,b) to prevent the CNTs from short-circuiting with the gate layer. In this case, the first hole was milled into the insulating SiO₂ layer, and then a second hole of smaller diameter was milled further, exposing the catalyst layer. The CNTs now formed around the inner wall of the smaller hole (Fig. 3.8IIc). The CNTs consistently grew around the perimeter of the holes because the dual-beam FIB significantly milled the catalyst layer and the sputtered catalyst particles tended to redeposit on the adjacent walls [101]. This new two-hole structure not only solved the short circuit problem but lent me a new control parameter; I can now vary the distance between the CNTs and the gate layer by varying the radius of the outer and inner holes. In Fig. 3.8II I examine triode-type CNT FEAs with an outer hole radius of 1.5 μm and an inner hole radius of 0.5 μm .

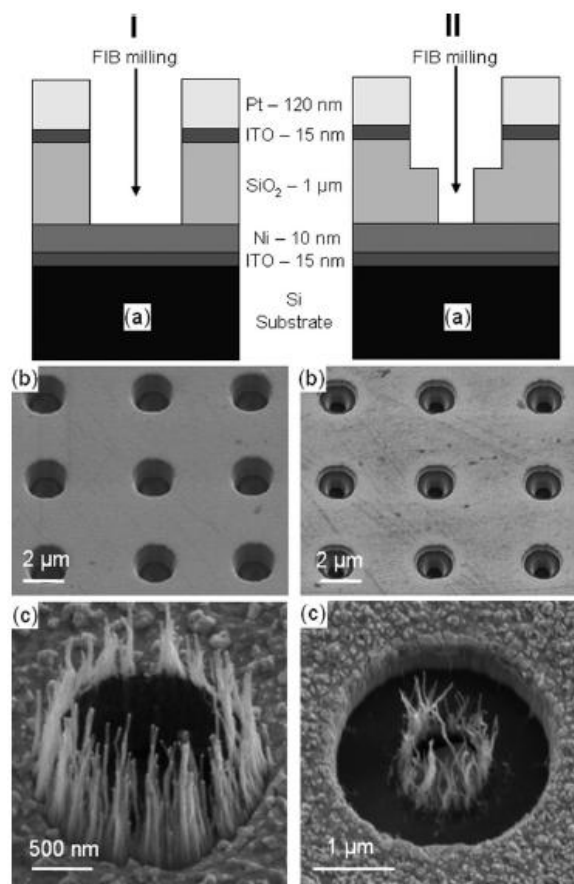


Fig. 3.8 “Two-hole” milling steps to prevent CNTs from shorting the gate layer. Schematics of the multilayer substrate with embedded Ni catalyst. Dual-beam FIB was used to mill holes and expose the catalyst layer using I(a) the single-hole method, and II(a) the two-hole method, in which an initial hole was milled into the SiO₂ insulating layer, followed by a smaller, concentric hole milled to the catalyst. This second method prevented short circuiting between the gate and cathode layer. SEM images of milled arrays are shown in I(b) and II(b). I(c) and II(c) demonstrate one of the completed triode-type CNT FEAs on the substrate generated by the single-hole method and the two-hole method, respectively.

3.3.2 Control milling depth by stage current graph

Although the above “step milling” method (section 3.2.2) can successfully control the milling depth to reach the Ni catalyst, this method is inefficient. Milling the depth test pattern alone requires several hours and it must be followed by PECVD CNT synthesis and SEM sample analysis. In addition, the step milling parameters/settings/time is related to one kind of wafer with a series of coatings. If the wafer design changes, for example: SiO₂ insulator thickness increase from 1 μm to 1.5 μm, or the gate layer material change from Pt to Au, the whole step milling test need processing to get another “sweet” milling point. The milling parameters/settings/time for old wafers cannot be easily adjust to make it work for new wafers.

In order to easily find the right milling depth, here I demonstrate another method to control the milling depth of multi-layers substrate by using end point detection (EPD) technique. The EPD technique monitors the interaction of the ions with the multi-layer substrate through a plot of the stage current as a function of ion milling time.

The sample charging is defined by ion beam current, secondary electron current and secondary ion current. Since in the generic case these currents are not balanced, the imbalance is compensated by the “stage current,” flowing between the sample and the grounded stage of the system.

The equation to describe the stage current is

$$I_{sc} = I_{IB} + I_{SE} - I_{SI},$$

where I_{SC} is the stage current, I_{IB} is the ion beam current, I_{SE} is the secondary electron current, and I_{SI} is the secondary ion current. Fig. 3.9 illustrates the different beam currents in a FIB system.

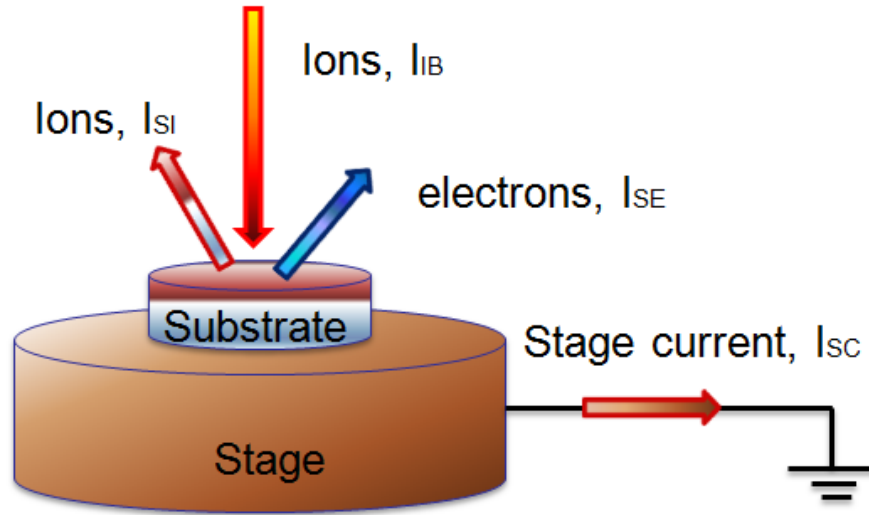


Fig. 3.9 Schematic diagram illustrate the different current in a FIB system.

Based on a picoammeter's low noise and high resolution, I can detect the variation of the stage current for endpoint information. The possibility of using the stage current plot for hole milling endpoint purposes was verified experimentally (Fig. 3.10). I mill a $3 \times 3 \mu\text{m}$ pattern at 300 pA beam current on my multilayer substrate. In Fig. 3.10, the plot can be divided into four segments based on the transition between different materials. The first segment (time: 0 ~ 20 second), Ga ion beam milling the top Pt gate layer and the ITO adhesion layer. The second segment (time 20 ~ 126 second), Ga ion milling the SiO_2 insulator layer. When the Ga ion beam reaches the Ni catalyst layer and the ITO adhesion layer, the stage current has a big jump from ~250

pA to ~550 pA. Since the Ni + ITO is pretty thin (10 + 15 nm), the stage current falls back to around 430 pA when the Ga ion beam reaches Si substrate.

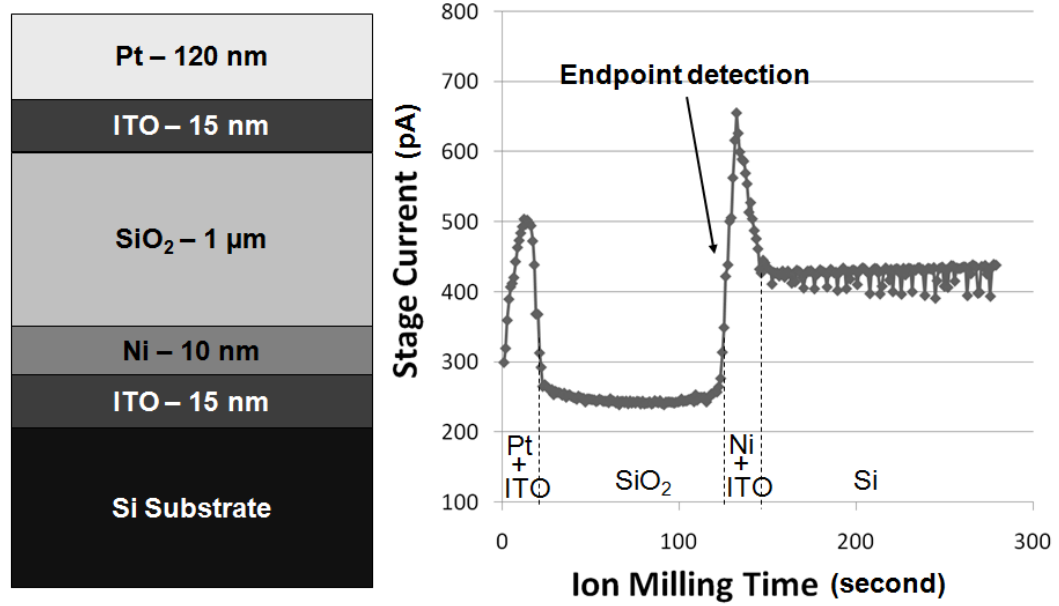


Fig. 3.10 Plot of stage current, associated with the hole milling endpoint detection.

3.3.3 Large area triode-type CNT FEAs Fabrication

Having dealt with the issues of short circuiting and optimal milling depth, I was able to scale up fabrication. Using the optimized DB-FIB milling conditions, I was able to synthesize over seven hundred uniform CNT emitters within a relatively large area ($300\ \mu\text{m} \times 300\ \mu\text{m}$) with a packing density of 2.5×10^6 devices/ cm^2 (around 10 ~ 30 tips/device), as shown in Fig. 3.11a. Note that each triode-type emitter has a similar microstructure to the one shown in Fig. 3.11b. Fig. 3.11c-d are cross-section views of one of these microstructures, showing the locations of the gate electrode, SiO₂ insulator, Ni catalyst layer, Si cathode, and vertically aligned CNT emitters.

These images reveal CNT emitters formed from the inner walls of the smaller hole, where the sputtered Ni catalyst is located. Note that the thickness of the CNTs in Fig. 3.11c is increased due to the substrate re-deposition during the dual-beam FIB milling process to create this cross-section view. By increasing the Ga ion beam current, I was able to program the dual-beam FIB to fabricate a large area emitter array to the millimeter scale. This advancement from single device synthesis to large-scale array is critical for achieving mass production of triode-type CNT FEAs.

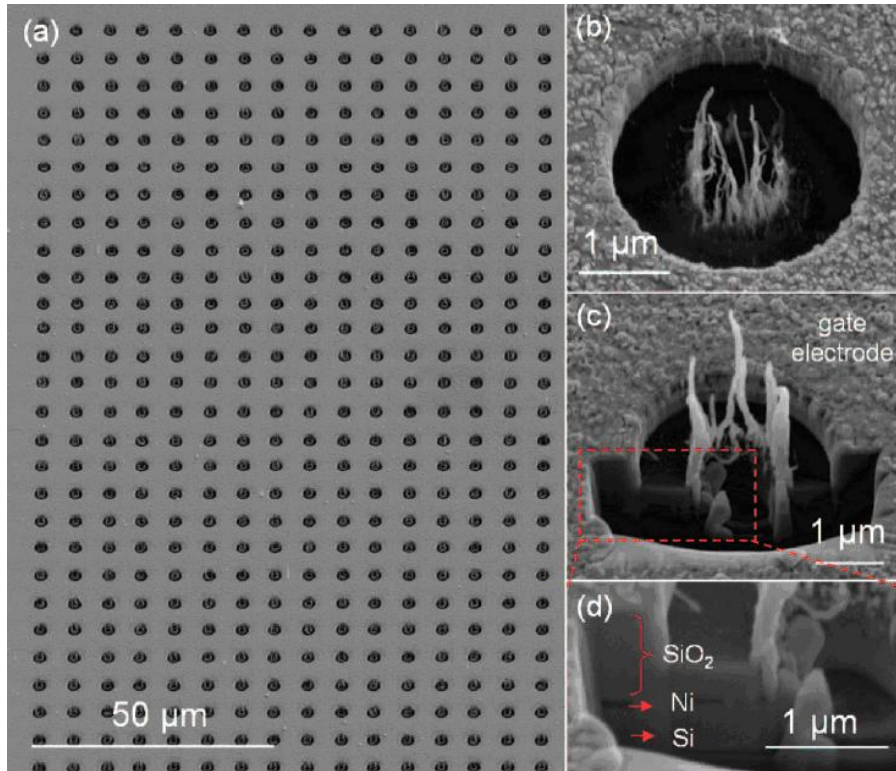


Fig. 3.11 Large area triode-type CNT FEAs fabrication.

(a) A large area triode-type CNT FEAs fabricated by a combination of DB-FIB and PECVD techniques. (b) One of the fabricated triode-type CNT FEAs devices from panel a. (c,d) Cross-section views of one of these devices.

3.3.4 Lower the capacitance between gate and cathode

During field emission testing of the large area CNT FEA described above, I found that the capacitance between the gate and cathode layer due to their small separation distance (1 μm) limited high frequency operation. The issue of capacitance is important for two reasons. First, because the energy stored in emitter arrays ($E = CV_g^2/2$) increases with the increase of capacitance (C), the larger capacitance could cause leakage current and perhaps break down the SiO_2 isolating layer [102]. The dielectric breakdown of the insulation layer usually results in a short circuit at the breakdown voltage. Second, for the modulation of the emission, the power required to drive the emitters is proportional to the capacitance squared [103]. Thus, it is important to keep the capacitance as low as possible. In general, capacitance (C) can be described as

$$C = \epsilon_r \epsilon_0 \frac{A}{d},$$

where A is the area of each plate, d is the separation between the plates, ϵ_r is the relative static permittivity of the SiO_2 (3.9) [104], and ϵ_0 is the permittivity of free space (8.85×10^{-12} F/m).

The easiest way to decrease the capacitance is to decrease the area (A) of the gate layer. As shown in Fig. 3.12a, I was able to significantly reduce the relevant gate area by using dual-beam FIB to cut through the Pt layer in a rectangle around the triode-type CNT FEAs test area ($400 \mu\text{m} \times 220 \mu\text{m}$), separating it from the rest of the

gate layer ($2\text{ mm} \times 2\text{ mm}$). In my field emission testing, this small section of the gate layer, rather than the whole substrate surface, was biased as desired. Calculations indicate this step significantly reduced the gate-cathode capacitance from approximately 138 to 3.1 pF.

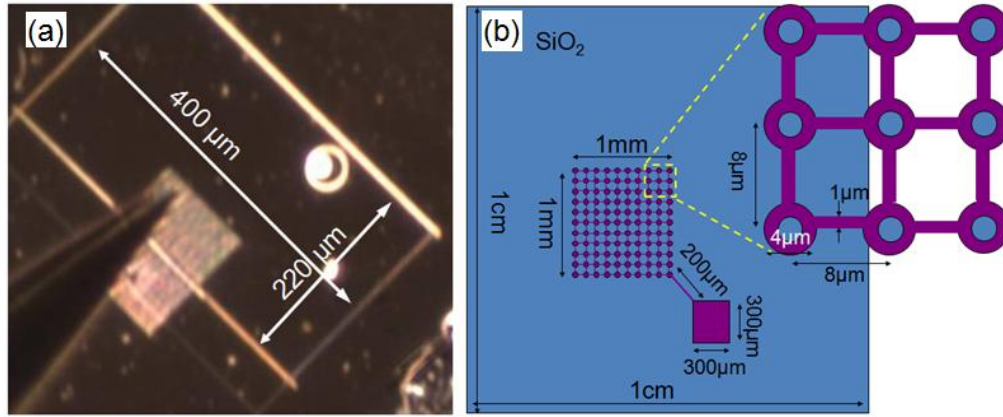


Fig. 3.12 Lower the capacitance between the gate and cathode.

(a) Decrease the area of the gate layer by using dual-beam FIB to cut through the Pt gate layer. (b) Schematic of ring-shaped gate.

In order to further decrease the capacitance, I designed a ring-shaped gate (Fig. 3.12b) to replace the plain gate and further reduce the gate-cathode capacitance from 3.1 pF to 1.25 pF. To construct the ring-shaped gate, a multilayer silicon wafer with an embedded catalyst layer was fabricated (Fig. 3.13a). The initial wafer consisted of an ITO adhesion (15 nm), Ni catalyst (10 nm), SiO_2 insulation (1 μm), and standard 950k polymethyl methacrylate (PMMA) positive e-beam resist (in that order) on the Si

wafer. The PMMA spin coating speed is 3000 rpm and the resist thickness is around 150 nm. Then these wafers are baked at 160 °C for 1 hour. Wafers are load in the ZEISS Ultra-55 field emission scanning electron microscope equipped with Nabity NPGS electron beam lithography system. For positive PMMA resist, the e-beam exposure will break many of the bonds of the large PMMA molecular chains, and the smaller chains will be more soluble in the developer than the unbroken (unexposed) chains. After ring-shaped pattern exposure, I dissolve these wafers in a 1:3 MIBK:IPA developer (MIBK is Methyl Isobutyl Ketone and IPA is Isopropyl Alcohol) for 1 min. After development, I evaporate the final Cr gate electrode (120 nm) layers deposited. For lift-off, I put the wafer in acetone, which will dissolve the PMMA, causing most of the metal to float away. Only the Cr deposited onto the substrate in the patterned areas will remain for a round gate (Fig. 3.13b). An FEI dual-beam FIB was then used to mill arrays of holes to generate the ring-shaped gate and expose the Ni catalyst for further CNT emitter growth (Fig. 3.13c).

I could also decrease capacitance by increasing the thickness of the SiO₂ layer. Since CNTs can be grown to a range of heights, I have a degree of flexibility in my choice of gate-cathode distance, d .

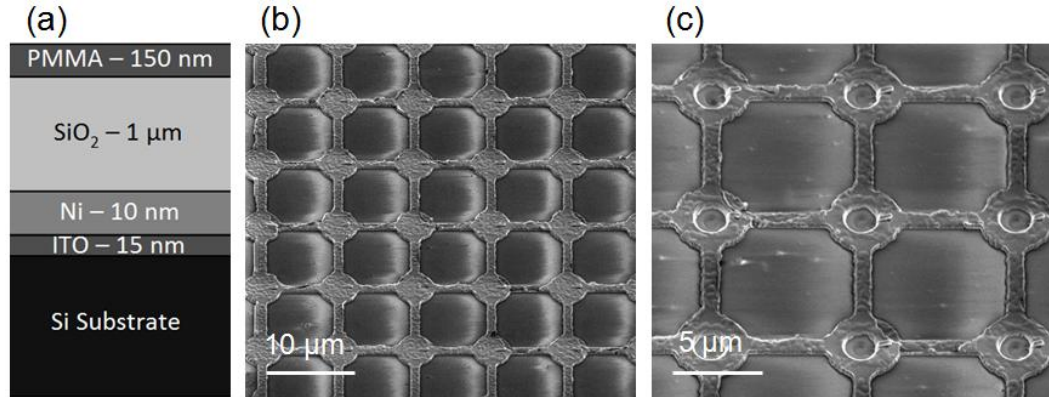


Fig. 3.13 Further decrease the gate area by patterning ring-shaped gates around individual holes.

(a) Schematic of the multilayer substrate for ring-shaped gate fabrication. (b) SEM images of round gate. (c) Mill arrays of holes to generate ring-shaped gate and expose the Ni catalyst for further CNT emitters growth.

In order to simulate the effect of the ring-shaped gate, I use the finite element method (details in section 5.4.1) to calculate the variation in electrostatic potential energy and plot the electric field equipotential lines (represented as a color spectrum in Fig. 3.14). The local electric field intensity at the CNT tips increase from 4.90 to 5.48 V/nm when the gate settings are changed from plain gate to ring-shaped gate. In general, the larger the local electric field, the easier it is to initiate field emission.

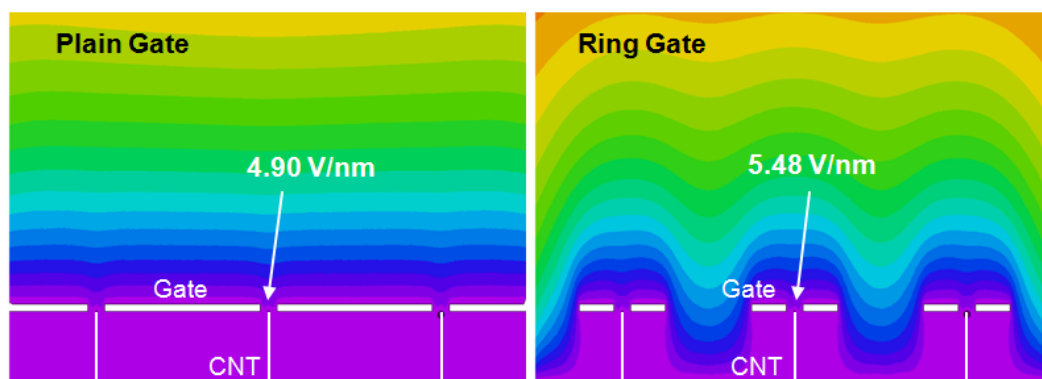


Fig. 3.14 Model simulation equipotential lines for plain / ring gate settings.

Chapter 4 FIELD EMISSION THEORY

Field emission, also known as Fowler-Nordheim tunneling, is a form of quantum mechanical tunneling in which electrons pass through a barrier in the presence of a high electric field (10^7 - 10^8 V/cm) [105]. In order to produce such a high electric field the emitter is usually formed into a tip with small apex radius. Sections 4.1 and 4.2 provide a brief overview of thermionic and field emission respectively. Section 4.3 discusses the Fowler-Nordheim Theory. Section 4.4 discusses quantum tunneling and the role of reducing barrier thickness in increasing field emission.

4.1 Thermionic Emission

Thermionic Emission is the technology used in many current applications. The basic equation of thermal emission can be derived for metal, where the energy levels are occupied up to the Fermi level, which in this case lies in the conduction band [106]. If the metal is heated to a temperature T , some of the electrons in the conduction band acquire sufficient energy to overcome the work function (potential energy difference between the fermi-level and the vacuum level) of the material.

For the ideal case of a metal with uniform surface and zero extraction field at the surface, the emission current density is given by:

$$J_s = A_R T^2 e^{-\frac{\phi}{kT}},$$

where A_R is the Richardson constant.

During thermionic emission, the space charge limited current I_{SCL} is independent of the temperature, but depends on the field strength in front of the cathode:

$$I_{SCL} = KU_a^{3/2}.$$

The geometry factor $K = 2.33 \times 10^{-6} A_k/D^2$, where A_k is the emitting cathode surface area and U_a is the anode voltage.

For a thermionic emission cathode, a clean metal must give sufficient emission current density at a temperature where it does not evaporate too rapidly. Table 4.1 lists the properties of tungsten (W) metal [107].

Table 4.1 Properties of tungsten (W) in thermionic emission.

<i>Melt Point (K)</i>	<i>Temperature (K) for Thermionic emission</i>	<i>Work function ϕ (eV)</i>	<i>Js (A/cm²)</i>
3640	2520	4.54	0.4

However, the disadvantage of thermionic emission is the high requisite heating power (~ 2500 K) and hence the high energy consumption of thermionic devices. Field emission presents the possibility of a more energy efficient emission technology.

4.2 Field Emission

Field emission occurs when an electric field of 10^7 V/cm or more is applied to a metallic surface. Such field strengths can be generated by low voltages at sharp edges and very fine tips. One common field emitter is formed by electrolytically etching a tungsten wire with ~ 150 μm diameter, resulting in a ~ 100 nm radius tip. The current density emitted from such tips and edges can reach very high values (e.g. 10^8

A/cm²). However, the emission currents are generally small (μA, due to the fact that metals segregate at high current densities). In addition, at such current densities an extreme heating of the emitter tips can occur, vaporizing the emitter tips [108].

To release electrons from a metal surface, the extracting field must be sufficiently strong that electrons can tunnel with a high probability through the potential wall in front of the tip. This wall is thinnest close to the tip. At a temperature of 0 K electrons fill the bands in the metal up to the Fermi energy level: tunneling requires a field strength of > 0.4 V/nm. Thermo field emission uses increased temperature to decrease the field strength required. However cold field emission, while more energy intensive, results in the brightest cathode and hence is most valuable for applications like microscopy and materials analysis [108].

4.2.1 Thermo field emission

Electrons can reach energy levels above the Fermi level by operating the field emitter at elevated temperatures. These electrons begin to contribute to the emission current. Field emission at elevated temperatures is called thermo-field emission or Schottky emission. The current obtainable is given by [109]

$$J_{es} = J_s \frac{\pi q}{\sin(\pi q)},$$

where

$$q = \frac{h^{1/4} F^{3/4}}{\pi} \sqrt{2mkT} \text{ and } J_s = 120T^2 e^{\frac{-\phi + \sqrt{e^3 F}}{kT}},$$

with T the absolute temperature in Kelvin, ϕ the work function and F the electric field.

Fig. 4.1 shows the potential distribution and the electron distribution in metal at elevated temperatures. Since electrons at $T = 0 \text{ K}$ fill the metal potential well up to the Fermi level, a high field is required to release them by tunneling through the potential into the vacuum. Since in a heated metal the electrons above the Fermi level have a Maxwellian energy distribution, they can tunnel at lower field strength and deliver an emission current in thermo-field emission [110].

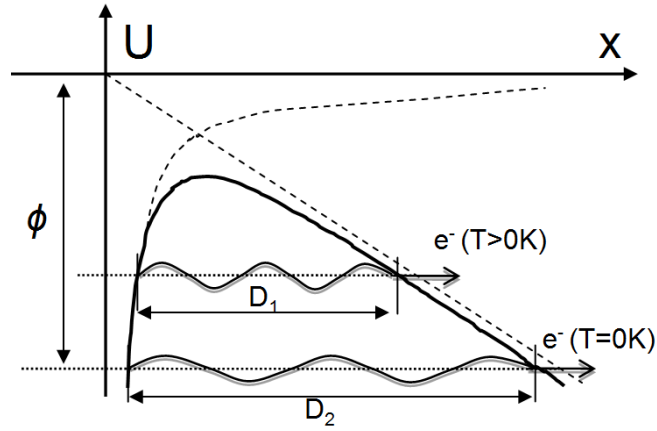


Fig. 4.1 Thermo field emission.

4.2.2 Cold field emission

Consider a metal occupying the half-space from $x = -\infty$ to $x \approx 0$. According to the free-electron theory of metals, an electron inside the metal sees a constant (zero) potential, and the potential energy $U(x)$ of the electron on the vacuum side of the metal-vacuum interface is asymptotically given by:

$$U(x) = E_F + \phi - \frac{e^2}{4x},$$

where E_F is the Fermi level, ϕ is the work function, and $-\frac{e^2}{4x}$ is the image force. The image force is the interaction due to the polarization of the conducting electrodes by the charged atoms of the sample. The potential threshold for field emission of electrons is essentially lowered by the image force.

When an external electric field F is applied to the surface, a term $-eFx$ is added. Here x is the distance to the surface:

$$\begin{aligned} U(x) &= E_F + \phi - \frac{e^2}{4x} - eFx & \text{for } x > 0 \\ &= 0 & \text{for } x < 0 \end{aligned} .$$

The potential barrier for a typical value of $E_F + \phi$ and for a value of the applied field is given in Fig. 4.2. The thinning of the potential barrier allows for electrons to tunnel out of the emitter.

The electron energy at the Fermi level is $E_F = -\phi$.

$$U(x) = -\frac{e^2}{4x} - eFx$$

The width of the image force barrier is [111]:

$$\Delta x = |x_2 - x_1| = \frac{\sqrt{\phi^2 - e^3 F}}{eF} .$$

The location of maximum barrier height is:

$$x_m = \frac{1}{2} \sqrt{\frac{e}{F}} ,$$

and the maximum height of the barrier is:

$$H_m = \phi - \sqrt{e^3 F} .$$

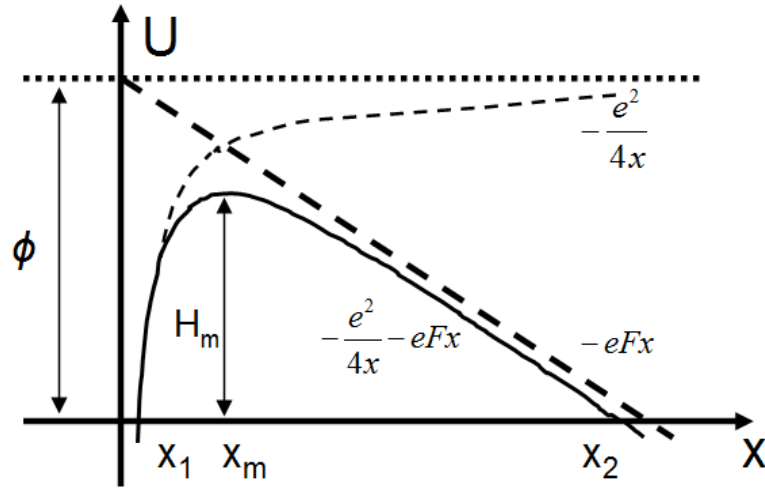


Fig. 4.2 Potential energy of electron U as function of the distance X .

4.3 The Fowler-Nordheim (F-N) Theory

Quantifying the field emission process requires calculating the field emission current density as a function of the electric field. To calculate the probability of electron tunneling through the potential barrier, the barrier transparency and the incident electron flow need to be considered and integrated. Fowler-Nordheim theory is based on the following assumptions:

(1) The emitter is assumed to obey the free electron model with Fermi-Dirac statistics.

The free electron model is a simple model for the behavior of valence electrons in a metallic solid. Valence electrons are assumed to be completely detached from their ions and form an electron gas. In the free electron model electron-electron interactions are completely neglected.

(2) The potential with the emitter is considered constant. Outside the metal the potential barrier is due to the image force $U(x) = -\frac{e^2}{4x}$. The external electric fields do not affect the electron states inside the emitter.

(3) The calculation is performed for the temperature $T = 0$ K.

Under these assumptions, the current density is given by:

$$J = e \int_0^{\infty} n(E_x) D(E_x, F) dE_x,$$

Where e is the electron charge, E_x is the electron kinetic energy, F is applied electric field, $n(E_x)$ is the number of electrons with energy between E_x and $E_x + dE_x$, incident on 1cm^2 barrier surface per second.

The barrier transparency D is calculated using the semi-classical method of Wentzel-Kramers-Brillouin (WKB) approximation [112].

$$\text{At the Fermi level } E_F = -\phi, \quad U(x) = -\frac{e^2}{4x} - eFx.$$

The transparency D is given by:

$$D(E_x, F) = \exp\left[-\frac{8\pi(2m)^{1/2}}{3he}\right] \frac{|E_x|^{3/2}}{F} \mathcal{G}(y),$$

Where $\mathcal{G}(y)$ is the Nordheim function:

$$\mathcal{G}(y) = 2^{-1/2} [1 + (1 - y^2)^{1/2}]^{1/2} \{E(k) - [1 - (1 - y^2)^{1/2}]\} K(k),$$

$$y = \frac{(e^3 F)^{1/2}}{\phi},$$

and

$$E(k) = \int_0^{\pi/2} \frac{1}{(1 - k^2 \sin^2 \alpha)^{1/2}} d\alpha, \quad K(k) = \int_0^{\pi/2} (1 - k^2 \sin^2 \alpha)^{1/2} d\alpha$$

are complete elliptic integrals of the first and second kinds, with

$$k^2 = \frac{2(1 - y^2)^{1/2}}{1 + (1 - y^2)^{1/2}}.$$

Using the above equation, the field emission current density J (Ampere/cm²) follows the classic Fowler-Nordheim formula:

$$\begin{aligned} J &= \frac{I}{A} = \frac{e^3}{8\pi\hbar} \frac{F^2}{t^2(y) \phi} \exp\left[-k_2 \frac{\phi^{3/2}}{F} \mathcal{G}(y)\right] \\ &= k_1 \frac{F^2}{t^2(y) \phi} \exp\left[-k_2 \frac{\phi^{3/2}}{F} \mathcal{G}(y)\right] \end{aligned} \quad (*)$$

where $k_1 = 1.54 \times 10^{-6} \text{ A eV V}^{-2}$ and $k_2 = 6.83 \times 10^7 \text{ eV}^{-3/2} \text{ V cm}^{-1}$. I is the emission current (Ampere), A is the emission area (cm²), β is the enhancement factor, F is the applied electric field in V, and ϕ is the work function in eV. The $t(y)$ is close to unity and varies weakly, representing the influence of the image force. In many cases it is justifiably set to unity [113]. The $\mathcal{G}(y)$ varies significantly with y and correspondingly F [114]. However, it does not significantly affect the linear behavior of the current-voltage characteristic because $\mathcal{G}(y)$ is very close to a parabolic curve of the form $\mathcal{G} = 1 - by^2$ ($b = \text{const}$) [115].

Formula (*) gives an excellent description of the experimentally observed exponential dependence of the emission current on applied electric field F and work function ϕ . For better evaluation of the emission characteristics, a logarithmic display

of the current density divided by the square of extraction voltage over the reciprocal value of the extraction voltage (generally called the Fowler–Nordheim plot) is used:

$$\ln J = f(1/F) \text{ or } \ln I = f(1/F).$$

The correction to the slope of the FN characteristic $\ln (J/F^2) = f(1/F)$ is given by the expression:

$$S(y) = \mathcal{G}(y) - \frac{y}{2} \frac{d\mathcal{G}(y)}{dy},$$

which is very close to unity, so:

$$\frac{d [\ln (J / F^2)]}{d (1 / F)} = -k_2 \phi^{3/2} S(y),$$

where ϕ in eV, F in V, and J in Ampere/cm².

4.4 Quantum Tunneling Theory and Simulation

When a high electric field is applied on a solid surface with a negative electrical potential, electrons inside the solid are emitted into the vacuum as a result of the quantum mechanical tunneling effect. Quantum tunneling is a wave coupling effect and particles behave in accordance with Schrödinger's wave equations.

4.4.1 Step potential barrier

The Schrödinger equation for the wave function is:

$$H\psi(x) = \left[-\frac{\hbar^2}{2m} \frac{d^2}{dx^2} + V(x) \right] \psi(x) = E \psi(x),$$

where H is the Hamiltonian, \hbar is the Plank constant, m is the mass, E is the energy of the particle and $V(x)$ is the potential step. The step divides the space in two parts ($x < 0$,

$x > 0$), shown in Fig. 4.3 [116]. The solution of the Schrödinger equation can be written as left and right moving waves:

$$\psi_L(x) = \frac{1}{\sqrt{k_0}} (A_R e^{ik_0 x} + A_L e^{-ik_0 x}) \quad x < 0$$

$$\psi_R(x) = \frac{1}{\sqrt{k_1}} (B_R e^{ik_1 x} + B_L e^{-ik_1 x}) \quad x > 0$$

where $k_0 = \sqrt{\frac{2mE}{\hbar^2}}$, $k_1 = \sqrt{\frac{2m(E - V_0)}{\hbar^2}}$.

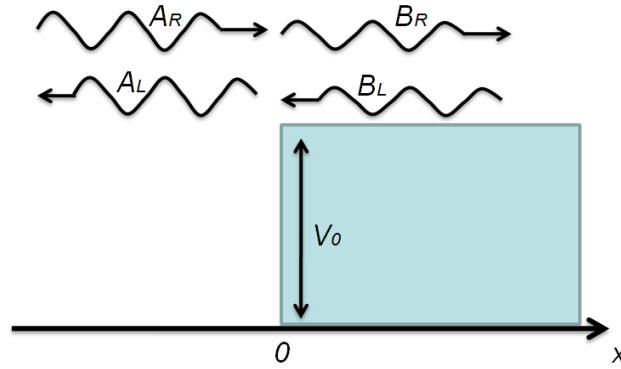


Fig. 4.3 Scattering at a finite potential step of height V_0 .

The coefficients A, B have to be found from the boundary conditions of the wave function at $x=0$. The wave function and its derivative have to be continuous, so

$$\psi_L(0) = \psi_R(0),$$

$$\frac{d}{dx}\psi_L(0) = \frac{d}{dx}\psi_R(0).$$

Combining the wave function and the boundary conditions gives the following restrictions on the coefficients:

$$\sqrt{k_1}(A_R + A_L) = \sqrt{k_0}(B_R + B_L),$$

$$\sqrt{k_0}(A_R - A_L) = \sqrt{k_1}(B_R - B_L).$$

When a particle is incident on the barrier from the left side it may be reflected or transmitted. Assume $E > V_0$. I put in the above equation $A_R=1$ (incoming particle), $A_L=r$ (reflection), $B_L=0$ (no incoming particle from the right) and $B_R=t$ (transmission).

So

$$t = \frac{2\sqrt{k_0 k_1}}{k_0 + k_1}, \quad r = \frac{k_0 - k_1}{k_0 + k_1}.$$

Step potential barrier simulation (Fig. 4.4) show the propagation of a Gaussian wavepacket when it hits a step potential [117]. The initial kinetic energy is 200meV. In classical mechanics, when the step height is larger than the particle energy, a total reflection can be observed. In quantum mechanics, when the step height is larger than the particle energy, the particle is partially transmitted. The probabilities of transmission and reflection can be obtained by integrating the area of the transmitted or reflected wavepacket.

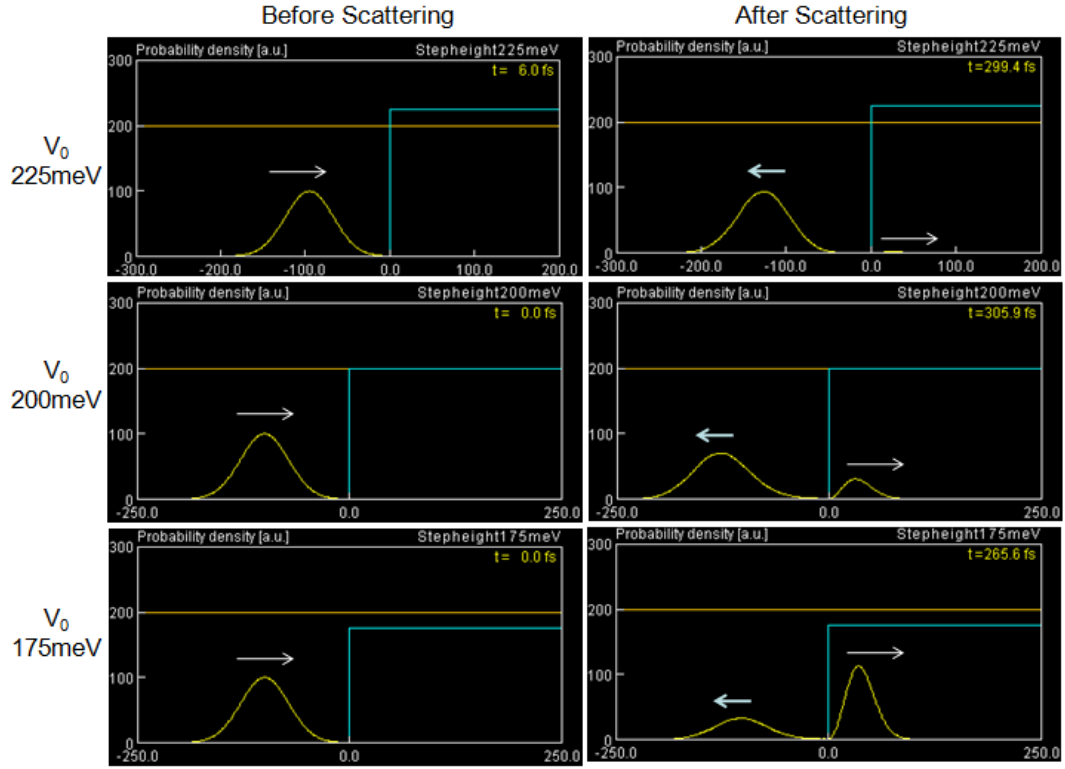


Fig. 4.4 Simulation of scattering at different potential height (225, 200, 175 meV).

4.4.2 Rectangular potential barrier

Let us consider a particle incident on a rectangular potential barrier positioned between $x=0$ and $x=a$. The likelihood that a particle will pass through a barrier is given by the transmission coefficient, while the likelihood that it is reflected is given by the reflection coefficient, where both coefficients are calculated using Schrödinger's wave-equation.

The barrier divides the space in three parts ($x<0$, $0<x<a$, and $x>a$), shown in Fig. 4.5 [118].

1. If $E>V_0$,

$$\psi_L(x) = A_R e^{ik_0 x} + A_L e^{-ik_0 x} \quad x < 0,$$

$$\psi_C(x) = B_R e^{ik_1 x} + B_L e^{-ik_1 x} \quad 0 < x < a,$$

$$\psi_R(x) = C_R e^{ik_0 x} + C_L e^{-ik_0 x} \quad x > a.$$

where

$$k_0 = \sqrt{\frac{2mE}{\hbar^2}} \quad x < 0 \text{ or } x > a,$$

$$k_1 = \sqrt{\frac{2m(E - V_0)}{\hbar^2}} \quad 0 < x < a.$$

Note if $E < V_0$, k_1 becomes imaginary and the wave function is exponentially decaying with the barrier. The case $E = V_0$ is discussed below.

The coefficients A, B, C have to be found from the boundary conditions of the wave function at $x=0$ and $x=a$. The wave function and its derivative have to be continuous, so

$$\psi_L(0) = \psi_C(0),$$

$$\frac{d}{dx} \psi_L(0) = \frac{d}{dx} \psi_C(0).$$

$$\psi_C(a) = \psi_R(a),$$

$$\frac{d}{dx} \psi_C(a) = \frac{d}{dx} \psi_R(a).$$

Combining the wave function and the boundary conditions gives the following restrictions on the coefficients:

$$A_R + A_L = B_R + B_L,$$

$$ik_0(A_R - A_L) = ik_1(B_R - B_L),$$

$$B_R e^{iak_1} + B_L e^{-iak_1} = C_R e^{iak_0} + C_L e^{-iak_0},$$

$$ik_1 (B_R e^{iak_1} - B_L e^{-iak_1}) = ik_0 (C_R e^{iak_0} - C_L e^{-iak_0}).$$

2. If $E = V_0$,

$$\psi_C(x) = B_1 + B_2 x \quad 0 < x < a,$$

Matching wave functions and their derivatives at $x=0$ and $x=a$ gives the following restrictions on the coefficients:

$$A_R + A_L = B_1,$$

$$ik_0 (A_R - A_L) = B_2,$$

$$B_1 + B_2 a = C_R e^{iak_0} + C_L e^{-iak_0},$$

$$B_2 = ik_0 (C_R e^{iak_0} - C_L e^{-iak_0}).$$

To find the amplitudes for reflection and transmission for incidence from the left, I put in the above equation $A_R=1$ (incoming particle), $A_L=r$ (reflection), $C_L=0$ (no incoming particle from the right) and $C_R=t$ (transmission). So

$$t = \frac{4k_0 k_1 e^{-ia(k_0 - k_1)}}{(k_0 + k_1)^2 - e^{2iak_1} (k_0 - k_1)^2},$$

$$r = \frac{(k_0^2 - k_1^2) \sin(ak_1)}{2ik_0 k_1 \cos(ak_1) + (k_0^2 + k_1^2) \sin(ak_1)}.$$

Rectangular potential barrier simulation (Fig. 4.6) shows the propagation of a Gaussian wavepacket when it hits a step potential [117]. The thinner the barrier thickness, the higher the probability of the tunneling effect. As the goal of field emission is to maximize and control the rate of tunneling (i.e. the emission current), it

is necessary to understand the pertinent factors impacting barrier thickness. Section 5.3 will provide a more complete model of this.

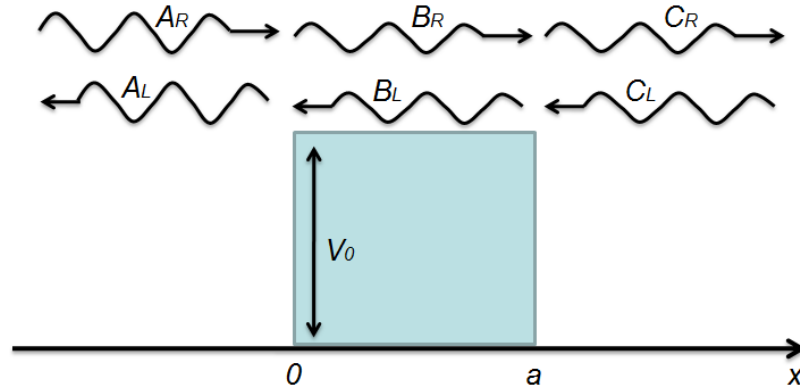


Fig. 4.5 Scattering at a rectangular potential barrier of height V_0 .

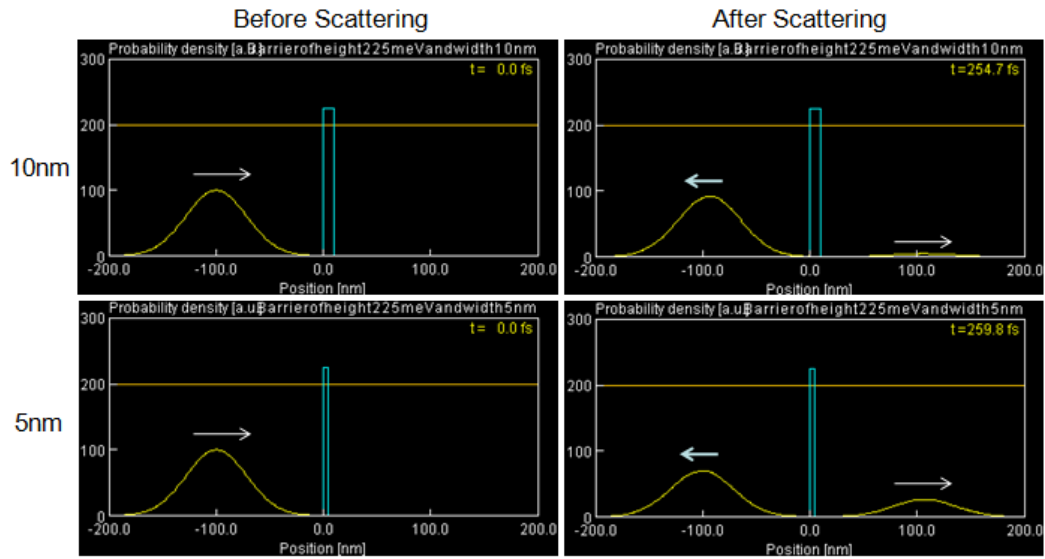


Fig. 4.6 Simulation of scattering at 10 nm / 5 nm rectangular potential barrier thickness.

Chapter 5 FIELD EMISSION PROPERTIES AND THEORETICAL SIMULATION OF TRIODE-TYPE CNT FEAs

Section 5.1 introduces the field emission test systems (field emission probe station). Section 5.2 discusses the impact of initial catalyst thickness on field emission properties of CNT film. Section 5.3 focuses on the field emission properties of triode-type CNT FEAs. Sections 5.4-5.5 present theoretical simulations method, model details and the effect of geometric and potential parameters. Section 5.6 discusses the recommend configurations and parameters for three specific applications.

5.1 Field Emission Measurements System and Method

To test field emission properties, I loaded the triode-type CNT FEAs into a three-probe ultra-high vacuum (UHV) probe station chamber with a base pressure of 10^{-9} Torr. I heated the sample to 200 °C for 24 h to eliminate water vapor or other possible residual adsorbates on the emitters. The experimental setup for the field emission measurements is shown in Fig. 5.1. I positioned the 25 μm diameter tungsten anode probe so that the gap between the anode and the sample was 50 μm . All three probes could be moved in the x, y, and z directions. During field emission, the anode was driven positively using a variable dc voltage power supply to extract electrons from the triode-type CNT FEAs. The emitted electrons were measured as anode current by a Keithley 485 picoammeter. Another tungsten probe was connected to the gate layer and used to change the gate voltage controlled by an Agilent 4156C semiconductor parameter analyzer. I began examining the field emission with the gate

voltage set to zero. I subsequently introduced positive and negative gate voltages and studied the impact of a triode structure on field emission.

Please note all the field emission tests were repeated on a number of individual emitters and samples in order to ensure the reproducibility of the triode-type CNT FEAs properties. Each measurement was taken using a 25 μm diameter anode probe that stimulated multiple devices simultaneously. The collective field emission from each subset, the 25 μm diameter area defined by the anode probe, is the sum of the emission from the devices within that substrate. Although individual devices may exhibit slight variations in morphology, field emission measurements taken from subsets across the array were highly uniform.

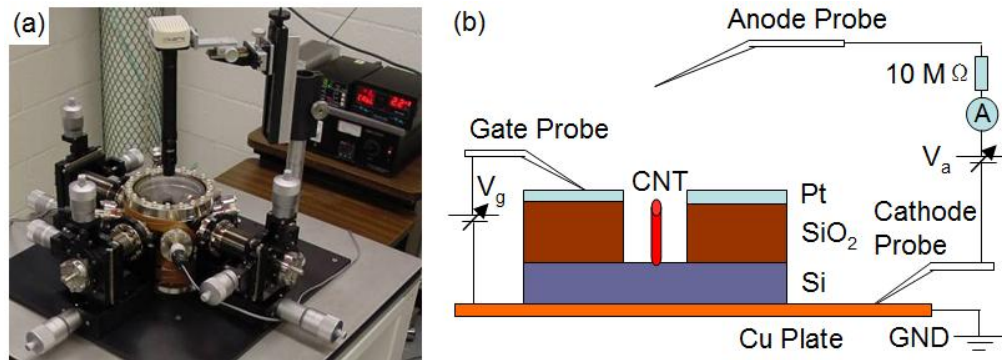


Fig. 5.1 UHV field emission measurement system.

(a) A photo of the field emission probe station. (b) Schematic illustration of the field emission measurement setup.

5.2 Impact of Initial Catalyst Thickness on Field Emission Properties of CNT Film

Before I tested the field emission properties of triode-type CNT FEAs, I tested the field emission properties of a series of CNT film samples synthesized under different parameters, for example, different initial catalyst layer thicknesses, or different gas concentrations. Through this study, I explored the relationship between the field emission properties and the morphology of a CNT film.

Here I present a detailed description of the impact of initial catalyst thickness on the field emission properties of CNT film. As discussed in chapter 2, due to surface tension considerations, the catalyst film will break into particles during the annealing process. The CNTs deposit around these catalyst particles. So, the thickness of the initial catalyst layer affects the CNT diameter, length and density of growth. In my experiment, thicker initial catalyst layers annealed into catalyst particles with a larger radius. The CNTs synthesized from these particles were longer and thicker than CNTs grown from thinner initial catalyst films (Fig. 5.2).

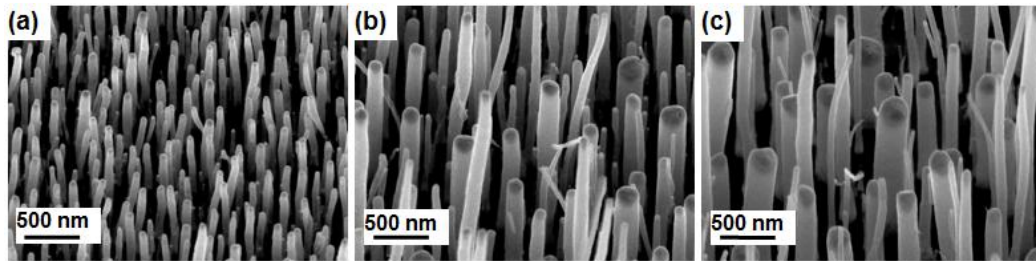


Fig. 5.2 Effect of initial catalyst layer thickness.

(a) 1nm Ni film catalyst. (b) 3nm Ni film catalyst. (c) 6nm Ni film catalyst.

The most uniform and aligned CNTs, those grown on 1 nm of Ni, showed the poorest emission characteristics (a turn-on field of 30.6 V/ μm , the highest tested here). This is attributed to the lack of field enhancement due to the close proximity and uniform height of the nanotubes, leading to the screening of the electric field. The longer CNTs, grown on 3 nm Ni film, showed slightly better emission results with a turn-on field of 16.8 V/ μm . These CNTs are not as well ordered as those grown on 1 nm of Ni, with some CNTs protruding high above the rest. If we consider height relative the surrounding CNTs instead of absolute height, we see that the CNTs grown from the 1 nm film all have roughly zero height, while scattered CNTs grown from the 3 nm film have significant positive heights. These large relative heights likely correspond to increased field enhancement factors. Finally, in Fig. 5.3 it can be seen that CNTs grown on 6 nm of Ni film exhibit the best emission characteristics with a turn on field of 13.9 V/ μm . The better emission from these CNTs is likely to be a consequence both of morphological irregularity in Fig 5.2 and a decrease in the CNT density. The corresponding Fowler–Nordheim (F-N) plots are shown in the Fig. 5.3b. The results are summarized in Table 5.1. The field screening associated with relative height will continue to be a significant factor in our theoretical consideration of field emission from CNT FEAs (section 5.5.4).

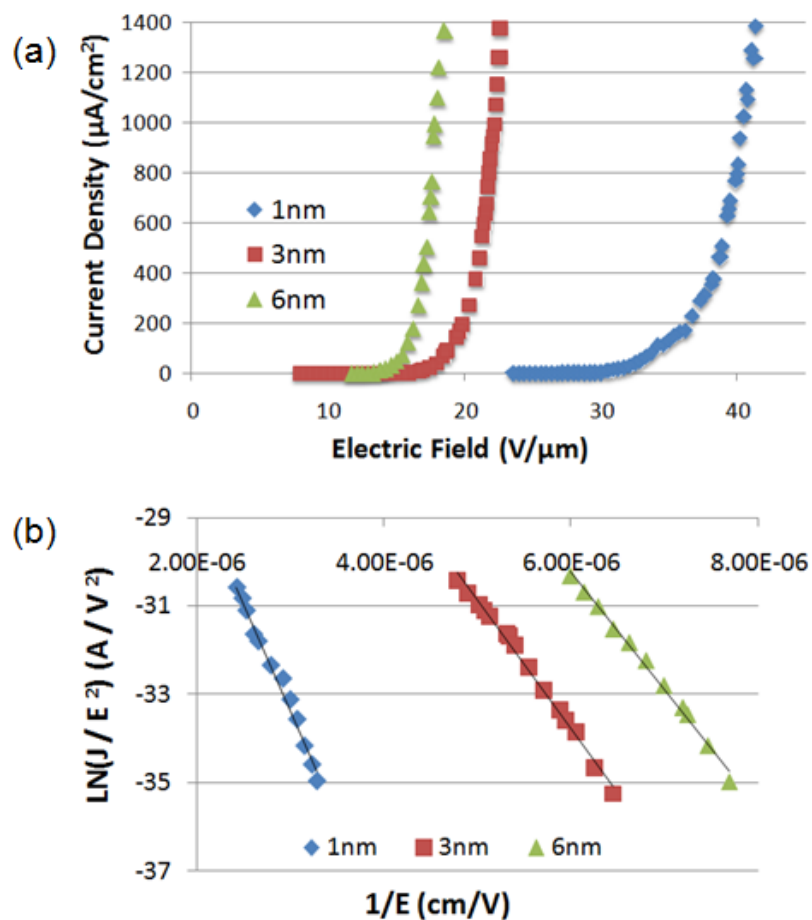


Fig. 5.3 Impact of initial catalyst thickness on CNTs film field emission properties. (a) Current density vs. electric field plot. (b) F-N plot. Field enhancement factor is calculated from the slope of the linear best fit.

Table 5.1 Turn-on field, threshold field and field enhancement factor for CNTs made by different initial catalyst layer thickness.

<i>Initial catalyst thickness</i>	<i>Turn-on electric field ($\text{V}/\mu\text{m}$)</i>	<i>Threshold electric field ($\text{V}/\mu\text{m}$)</i>	<i>Field enhancement factor β</i>
1 nm	30.6	46.4	155
3 nm	16.8	26.2	258
6 nm	13.9	21.0	283

5.3 Field Emission Properties of Triode-type CNT FEAs

Field emission tests were conducted in large area CNT FEAs (Fig. 3.11) with various applied gate voltages. The field emission tests were structured such that the anode to cathode distance (50 μm) was much larger than the gate to the CNT emitter distance (~ 0.1 μm). Therefore, small changes in gate voltage (in the range of -1V to 1V) were able to generate large changes in the local electric field. Fig. 5.4a shows three plots of typical emission current densities versus electric fields. This data was obtained with the Pt gate layer biased at -0.2 (negative gate voltage), 0, and +0.1 V (positive gate voltage). These voltages were selected to investigate the impact of negatively and positively biased gate layers on emitter current density. Also, since the energy stored in emitter arrays ($E = CV_g^2/2$) is proportional to the voltage squared, it is desirable to have the lowest possible gate voltage (V_g) because larger gate voltages could cause damage to the SiO_2 isolating layer. The plots in Fig. 5.4a clearly indicate that emission current densities can be effectively altered by gate bias. The turn on electric field, defined as the field at which current density reaches 10 $\mu\text{A}/\text{cm}^2$, decreased from 20.0 to 16.4 $\text{V}/\mu\text{m}$ as a result of the increase in gate voltage (V_g) from -0.2 to 0.1 V. Similarly, the threshold field, defined as the field at which current density is equal to 1 mA/cm^2 (indicated with an arrow in Fig. 5.4a), decreased from 23.8 to 20.8 $\text{V}/\mu\text{m}$ as a result of the increase in V_g from -0.2 to 0.1 V.

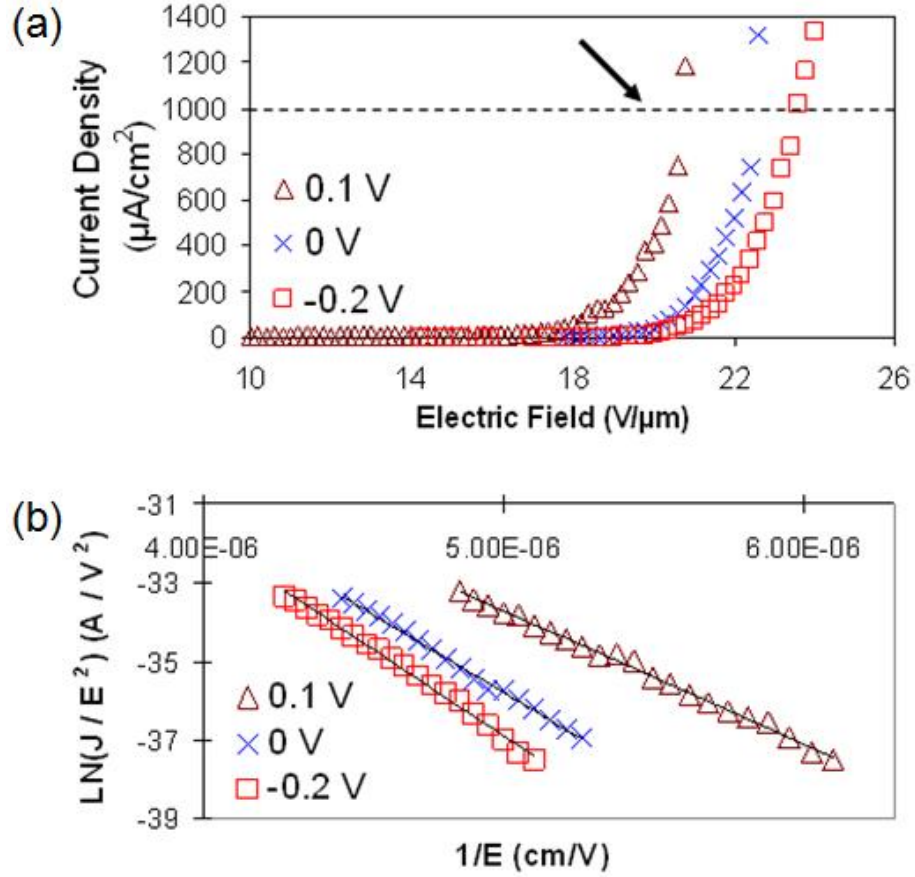


Fig. 5.4 Field emission properties of triode-type CNT FEAs.

(a) Current density vs. electric field plot. The arrows indicate the threshold field, defined as the fields at which current density is equal to $1 \text{ mA}/\text{cm}^2$. (b) F-N plot. Field enhancement factor is calculated from the slope of the linear best fit.

I used the Fowler-Nordheim (F-N) field emission model in interpreting my results. According to the F-N theory [119, 120], the current density J (Ampere/ cm^2) can be expressed as:

$$J = \frac{I}{A} = \frac{k_1 \beta^2 E^2}{\phi} \exp\left(-k_2 \frac{\phi^{3/2}}{\beta E}\right),$$

where $k_1 = 1.54 \times 10^{-6} \text{ A eV V}^{-2}$ and $k_2 = 6.83 \times 10^7 \text{ eV}^{-3/2} \text{ V cm}^{-1}$. I is the emission current (Ampere), A is the emission area (cm^2), β is the enhancement factor, E is the applied electric field in V cm^{-1} , and ϕ is the work function in eV. The equation can be further expressed as:

$$\frac{J}{E^2} = \frac{k_1 \beta^2}{\phi} \exp\left(-k_2 \frac{\phi^{3/2}}{\beta E}\right), \text{ and thus}$$

$$\ln\left(\frac{J}{E^2}\right) = \ln\left(\frac{k_1 \beta^2}{\phi}\right) - k_2 \frac{\phi^{3/2}}{\beta} \left(\frac{1}{E}\right).$$

Hence, the field enhancement factor, β , can be calculated from the slope (S) of the F-N curve $\left[\ln\left(\frac{J}{E^2}\right) \text{ versus } \frac{1}{E}\right]$ using the equation:

$$S = -k_2 \frac{\phi^{3/2}}{\beta}.$$

The multi-walled CNT has a work function of $\phi = 4.95 \text{ eV}$ [121]. The F-N plot shown in Fig. 5.4b depicts the effect of gate voltages (V_g) on the triode-type CNT FEAs device. The linearity of the F-N plots confirms that the field emission results from a quantum mechanical tunneling process. This plot also demonstrates that gate potential plays an important role in field emission control. Theoretically, increasing V_g should introduce an additional electric field which can help excite more electrons from the CNT emitters, leading to an increase in β and a decrease in turn on and threshold field. The slope (S) of the F-N plot decreased with increasing V_g , indicating the field enhancement factors (β) increased as expected (results summarized in Table 5.2).

Table 5.2 Relationships between gate voltage (V_g) and the turn on electric field, threshold electric field, and field enhancement factor of the triode-type CNT FEAs.

<i>Gate voltage</i> V_g (V)	<i>Turn on electric</i> <i>field</i> (V/ μm)	<i>Threshold electric</i> <i>field</i> (V/ μm)	<i>Field</i> <i>enhancement</i> <i>factor</i> β
-0.2	20.0	23.8	149
0	19.2	22.4	165
0.1	16.4	20.8	222

5.4 Field Emission Theoretical Simulation Method and Model Details

In the above discussion, field emission tests indicated that the emission current densities can be effectively altered by gate bias. However, there are numerous parameters influencing the field emission properties of a given triode-type CNT FEA. Theoretical calculations are essential to identifying critical parameters and establishing the correlations among them.

Here, I report the investigation of the relationship between various geometric parameters of the triode-type CNT FEAs and the resultant field emission through the study of local electric field (LEF), surface potential barrier thickness and field enhancement factor. The simulation results will assist me in further optimization of the devices. Using the simulation, I am able to predict (given the geometric structure of the device) the functional relationship between the applied anode and gate potentials and the LEF. Once a target structure is identified, it is relatively easy to construct a field emitter with the desired morphology by returning to the fabrication methods and growth parameters discussed above. For example, if a shorter CNT is desired for

optimal field emission, a device developer would simply need to reduce the plasma exposure time during PECVD growth.

5.4.1 Finite element method for theoretical simulation

For triode-type CNT FEAs simulation, it will be too complicated to simulate the entire continuous domain of interest. In order to simplify the simulation process, I used Finite Element Methods (FEM) to obtain approximated solutions to boundary value or initial-value problems. FEM replace an entire continuous domain of interest by a number of subdomains in which the unknown function is represented by simple interpolation functions with unknown coefficients. Thus, the original boundary-value problem with an infinite number of degrees of freedom is converted into a problem with a finite number of degrees of freedom [122].

In simulation process, FEM use a complex system of points called nodes, which make up a grid called a mesh. This mesh is programmed to contain the properties that define how the structure will react to certain loading conditions. Nodes are assigned at a certain density depending on the anticipated stress levels of a particular area. Regions that have large amounts of stress usually have a higher node density than those that experience little stress.

The FEM procedure can be summarized as follows:

1. Discretize the targeted domain into basic element models.
2. Construct a balancing (equilibrium) equation (local matrix) at each basic element model.

3. Combine all local matrices, add boundary conditions, and solve the global matrix.

The triode-type CNT FEAs simulation was calculated using the FlexPDE software package [123], which employs the FEM to obtain numerical solutions of partial differential equations. FlexPDE uses an adaptive mesh to allow for a wide range of geometric scales within a single simulation. For example in this case, it enabled high-resolution calculations around the CNT emitters and gate structures while keeping the resolution over the large areas between the anode and the cathode relatively low. The finite element method is now the preferred method for analyzing field emission devices [124]. Fig. 5.5 shows the nodes and meshes for a triode-type CNT FEAs simulation. Fig. 5.5b shows the emitter region labeled in Fig. 5.5a.

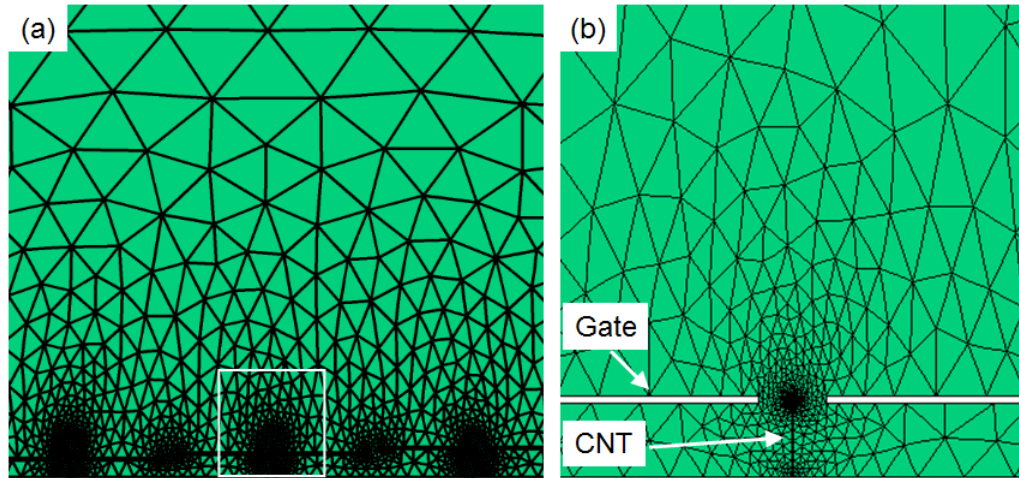


Fig. 5.5 Finite element method simulation triode-type CNT FEAs.

(a) Simulation area includes triode-type CNT FEAs. Nodes were assigned at a certain density depending on the stress levels. (b) Detail of nodes and meshes in the emitter region labeled in Fig. 5.5a.

5.4.2 Simulation model details

I used simplified, idealized conditions because the experimentally fabricated triode-type CNT FEAs were too complicated to simulate. The basic geometrical parameters of the simulation include a CNT emitter height of 2 μm and diameter of 40nm, an anode-to-emitter distance of 50 μm , a gate hole diameter of 2 μm , a gate thickness of 200 nm and a device emitter-to-emitter distance of 3 μm . I only considered the case of a single CNT emitter, rather than the type of circle growth synthesized in the actual experiment, and modeled the CNT emitter as a metallic cylinder capped with a hemisphere.

The local electric potential distribution around a triode-type CNT FEA satisfies the Poisson equation,

$$\nabla^2 \phi = \frac{\delta}{\epsilon},$$

where δ , ϵ , and ϕ are the charges density, permittivity of the insulation medium constant and the potential of electric distribution, respectively. The boundary conditions of the potential distributions are as follows: $\phi|_{cathod} = 0$, $\phi|_{anode} = V_a$, $\phi|_{gate} = V_g$. According to Xie et al. [125], a LEF less than 1 V/nm will not allow field emission to occur. Based on this requirement, I fixed anode potential (V_a) at 1000V throughout the simulation, resulting in a sufficient applied external field (20 V/ μm) to generate the LEF necessary for field emission. I set the gate potential (V_g) at 10V.

Space charge is the presence of electron charges between the cathode and anode. In thermionic emission, when the metal emitter is heated to incandescence, the electrons are surrounding the metal emitter in a cloud of free electrons. Due to the negative charge of the resulting cloud, most of the electrons emitted by the cathode are driven back to the emitter by the repulsion of the electron cloud. This is called the space charge effect, which reduces the thermionic emission when the emission current increases [126]. However, for field emitter cathodes, the space charge can be neglected because the very large electric field at the emitter tip negates the formation of space charge [127]. Thus I neglect the space charge effects in the current simulation, and the Poisson equation becomes the Laplace equation:

$$\nabla^2 \varphi = \frac{\partial^2 \varphi}{\partial r^2} + \frac{\partial^2 \varphi}{\partial z^2}.$$

To satisfy the Laplace equation I must restrict the potential distribution to $\nabla^2 \varphi = 0$. Thus the electric field intensity on the top of the nanotube is obtained from the formula: $-\nabla \varphi = E$, the electric potential gradient where $E_r = \frac{\partial \varphi}{\partial r}$, $E_z = \frac{\partial \varphi}{\partial z}$ and E_r and E_z are the electric field intensities in the radial direction and axial direction, respectively.

In Section 5.5, I discuss the simulation results showing the effects of gate types, gate potentials, field screening, and various geometric parameters, and demonstrate how one can control field emission through the gate electrode.

5.5 Field Emission Theoretical Simulation Results

5.5.1 Effect of gate types

I modeled field emission from three different gate types: top gate (the gate layer is positioned 0.5 μm above the tip of CNT emitter), standard gate (the gate is placed on the same level as the CNT emitter tip) and side gate (the CNT emitter protrudes 0.5 μm through the gate layer), as shown in Fig. 5.6. The equipotential lines are also plotted for each gate type.

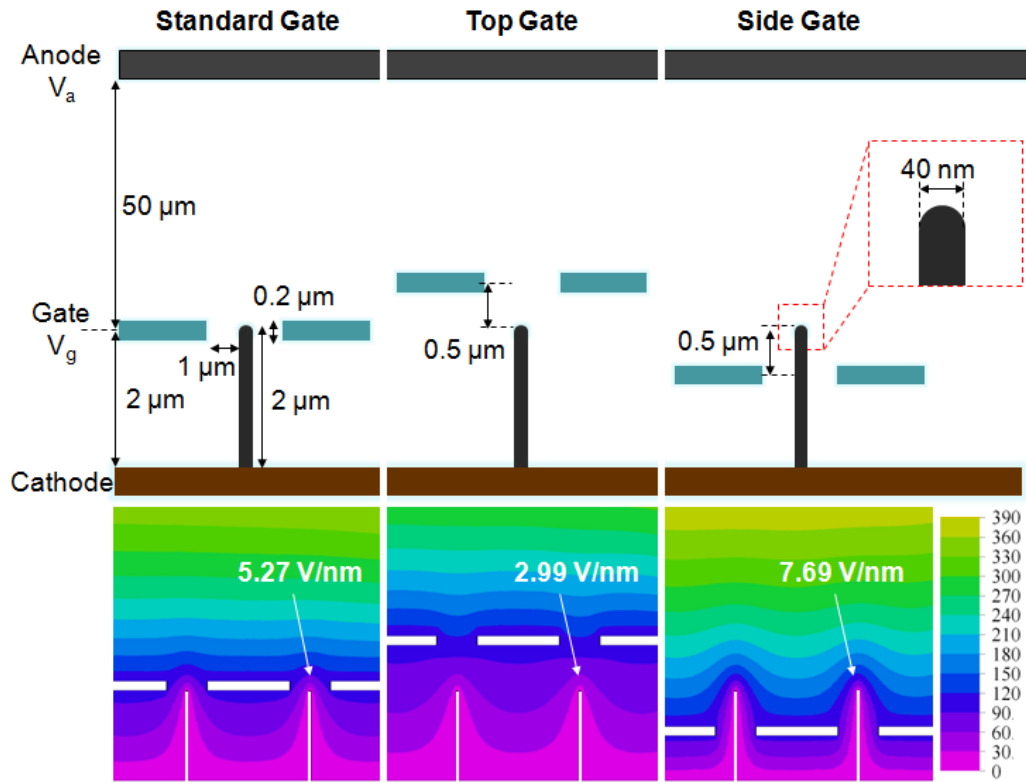


Fig. 5.6 Standard gate, top gate and side gate.

Surface potential barrier thickness is investigated here to study the relationship between LEF and the field emission process. When no electric field is present, the surface potential barrier is like a step potential barrier. When a potential is applied, the surface potential barrier becomes triangular. The slope of the surface potential barrier is decided by the LEF on the tip of the CNT. The larger the LEF, the steeper the slope of the surface potential barrier will be and the thinner the surface potential barrier thickness. Fig. 5.7 shows a schematic of the simulated surface potential barriers along the central axis of the CNT's tip under top, standard and side gate settings (listed in Table 5.3). In the field emission process, electrons escape by F-N tunneling through the triangular barrier at the Fermi level, which is influenced by the work function: ϕ . The CNT has a work function of $\phi = 4.95$ eV. It is known that for CNT emitters, if the potential barrier thickness is comparable to the electron wavelength (around 40 nm), there is a significant chance that the electrons will pass through the barrier and escape into the vacuum, a process called quantum tunneling [128]. In the simulations, changing the gate type from top gate to standard gate to side gate, increased the LEF from 2.99 to 5.27 to 7.69 V/nm, decreasing the potential barrier thickness from 43.4 to 21.0 to 12.2 nm respectively. In general, the larger the LEF, the smaller the surface potential barrier thickness, and the easier it is to start field emission. The reduced electric fields over the top and standard gates can be attributed to the field screening effect, as the gate layer interacted with the emitters (section 5.5.4).

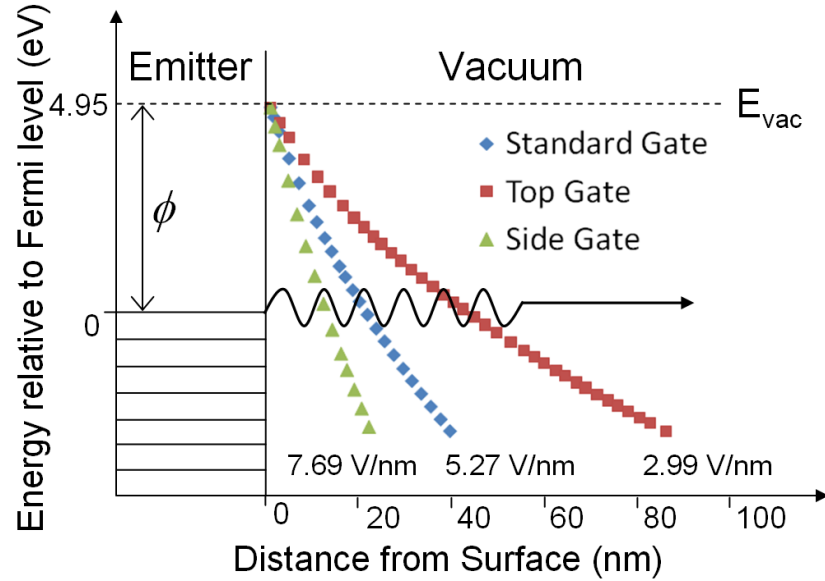


Fig. 5.7 Effect of gate types.

Table 5.3 Relationships between LEF and surface potential barrier thickness given top gate, standard gate and side gate settings.

Gate Settings	LEF (V/nm)	Surface Potential Barrier Thickness (nm)
Top Gate	2.99	43.4
Standard Gate	5.27	21.0
Side Gate	7.69	12.2

5.5.2 Effect of gate potentials

In order to better understand the trends associated with gate potential, I simulated one triode-type CNT field emitter and plotted the potential energy contours around the cap under an external field of 20 V/ μm . Using the selected anode and gate voltages, I was able to establish the correlation between gate voltage, anode voltage, and field emission. In this simulation, I solved Laplace's equation to determine the variation in electrostatic potential energy, represented in Fig. 5.8a as a color spectrum

from blue (low potential) to red (high potential). The dotted line marks the energy contour for Fermi energy (-4.95 eV) of the multiwalled CNT. Note that the equipotential surfaces are closest together directly above the CNT tip, indicating that the strongest electric field points along the central axis and that this is the direction the electrons are most likely to tunnel.

Fig. 5.8b shows a schematic of the simulated surface potential barrier along the central axis of the CNT's tip under five different field emission conditions (listed in Table 5.4). As anode voltage increases from 600 to 1000 to 1400 V, the surface potential barrier thickness decreases from 35.9 to 17.9 to 11.8 nm respectively. If the surface potential barrier is thin, there is a significant chance that the electrons will pass through the barrier and escape into the vacuum, a process called quantum mechanical tunneling [129]. The probability of tunneling vanishes with the increased thickness of the barrier, which can be adjusted by changing the gate voltage. To determine the impact of positive and negative gate voltages on surface potential barrier thickness, I simulated a gated CNT emitter with constant anode voltage of 1000 V and gate voltages of -10, 0, 10 V. The negative gate voltage increased the tunneling surface potential barrier thickness from 17.9 to 20.7 nm, decreasing field emission, while the positive gate decreased surface potential barrier thickness from 17.9 to 15.8 nm, increasing field emission (Fig. 5.8b). This trend is consistent with the experimental data (Table 5.2). This suggests that changing the gate voltage will effectively modify the emission current generated by the anode and cathode voltage.

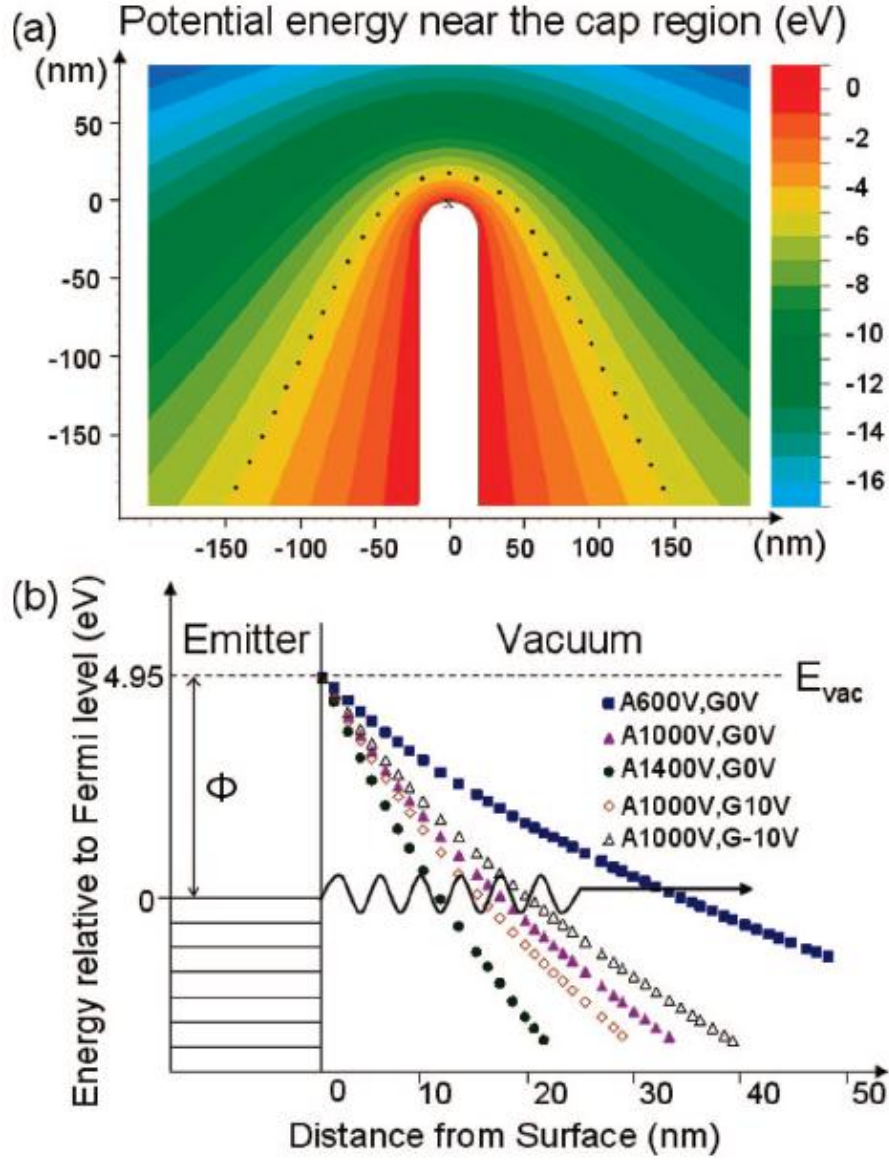


Fig. 5.8 Effect of gate potentials.

(a) Potential energy contour plot in the CNT emitter cap under constant anode voltage 20 V/ μm . The dotted line is the equipotential line for the Fermi energy (-4.95 eV). (b) Schematic diagram of the energy barriers along the central axis of one of triode-type CNT FEAs under different anode and gate voltages.

Table 5.4 Simulation data of surface potential barrier thickness under different anode and gate voltages.

<i>Anode voltage (V)</i>	<i>Gate voltage (V)</i>	<i>Barrier thickness (nm)</i>
600	0	35.9
1000	0	17.9
1400	0	11.8
1000	-10	20.7
1000	10	15.8

5.5.3 Effect of field screening for diode-type device

The field screening effect will decrease the LEF at the peak of an object when there are other objects sufficiently close by. For a diode-type device like the CNT film discussed in section 5.2, the field screening effect is related to the CNT-CNT distance.

The basic geometrical parameters of the simulation remained as above (CNT emitter height of 2 μm , CNT diameter of 40 nm, anode-emitter distance of 50 μm). The CNT-CNT distance was varied from 1 to 6 μm .

Fig. 5.9a shows a simulated potential distribution of an un-gated vertically aligned CNT under a uniform electric field. The nearest neighboring CNT is 6 μm from this one. When CNTs are brought closer (Fig. 5.9b-d), the neighboring CNTs start to screen, limiting the penetration of the equipotential lines between these CNTs. This reduces the local electric field and decreases the field emission. Please note that increasing the spacing between CNTs to more than 6 μm will not further increase the local electric field, since it is well established that once the distance between CNTs is

more than twice the emitter height, the field screening effect no longer impacts the LEF at the CNT tip [130].

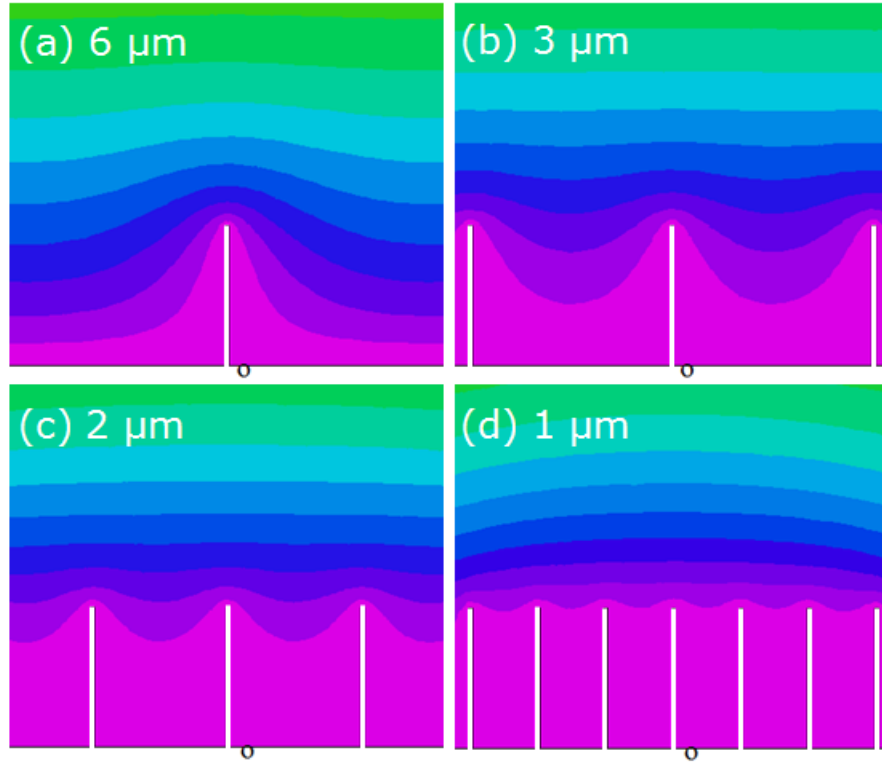


Fig. 5.9 Simulated potential distribution for CNTs of different spacing (1, 2, 3, 6 μm) under a uniform electric field.

5.5.4 Effect of field screening for triode-type devices

For triode-type devices, there are two kind of screening effects: emitter-emitter screening and gate-emitter screening.

5.5.4.1 Emitter-emitter screening effect

Here I examined the possibility of a field screening effect between neighboring CNT emitters in triode-type emitter arrays. I considered top, standard and side gated

arrays with device distances of 3, 6 and 12 μm . The simulated LEF across these arrays are shown in Fig. 5.10 and indicate that, for all three kinds of gate settings, the LEF is virtually unaffected as the emitter spacing distance is increased from 3 μm to 12 μm . First let us consider the side gated emitters. Although the CNT is actually 2 μm high, due to gate screening the relative CNT emitter height is only 0.5 μm (since the side gate is 0.5 μm lower than the actual height of the CNT). Thus the emitter spacing (3 to 12 μm) is at least 6 times larger than the relative CNT emitter height. When the distance between CNT is more than twice the emitter height, the field screening effect no longer impacts the LEF at the CNT tip [133]. The simulation results agree well with this explanation. This reasoning holds in the cases of top and standard gated emitters since the gate itself overshadows the emitter, reducing their relative heights to zero or below.

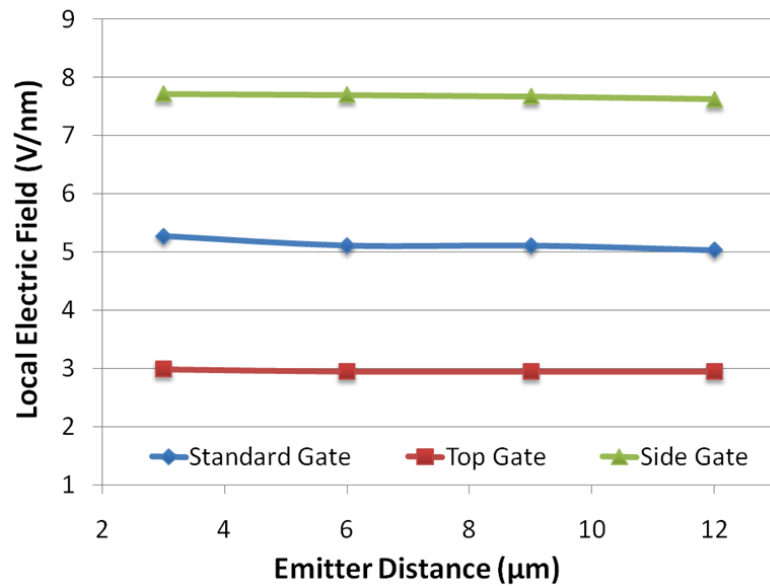


Fig. 5.10 The emitter-emitter field screening effect for top, standard and side gated emitters.

5.5.4.2 Gate-emitter screening effect

Although the emitter-emitter screening effect does not impact triode-type configurations, the gate-emitter screening effect certainly does. In diode-type emitter arrays, the high LEF is mainly concentrated in the emitter tip areas. However, in a triode structure a strong gate-emitter interaction ensues. Fig. 5.11a compares the LEF of emitters in each gate type with different gate radii (1, 2, 3 μm). Note that no voltage is applied to the gate layer; its impact on LEF here arises purely from its relative height and placement. In all the simulations presented in Fig. 5.11 and Table 5.5 the emitter-to-emitter distance is fixed at 10 μm . The positive slopes of each of the plots indicate that the gate-emitter field screening effect inhibits LEF more significantly when the gate is closer to the emitter (when the gate radius is small). The results also show that side gated arrays have the highest LEF (7.36 ~ 10.77 V/nm), followed by standard gate (4.27 ~ 9.04 V/nm), then the top gate (2.34 ~ 7.46 V/nm). This conforms with my qualitative understanding that the LEF tends to be highest around the tallest object in a system: in the side gate structure this object is the emitter, and in the top gate it is the gate. One should also note that increasing the gate radius from 1 to 3 μm increased the LEF more greatly in top gated CNT FEAs (a 5.12 V/nm increase) compared to standard gated (4.77 V/nm) and side gated (3.41 V/nm) CNT FEAs.

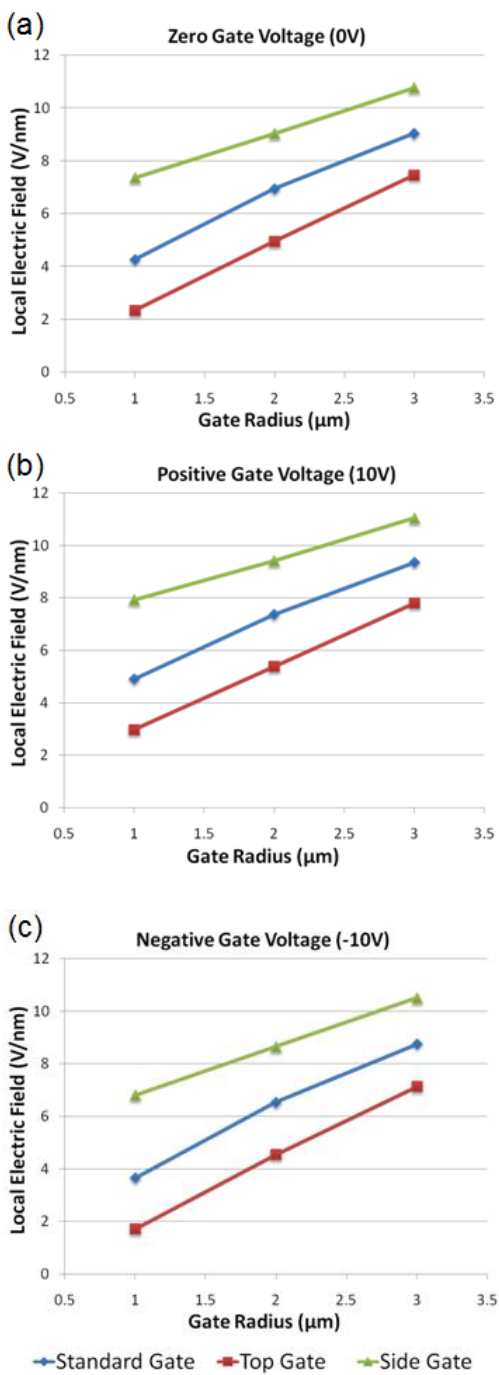


Fig. 5.11 The relationship between gate radius and LEF on standard gate, top gate and side gate settings under (a) zero, (b) positive (10 V) and (c) negative (-10 V) gate voltages.

Thus far, I have discussed the effects resulting from the geometric construction of a triode-type CNT FEA device. Now I turn to the effects of the gate potential itself. Fig. 5.11b and 5.11c display the LEF around the same devices discussed above when a small positive or negative potential was applied respectively.

With a 10 V gate voltage (Fig. 5.9b), the LEF (and thus the field emission) increased under all the gate settings compared with the same geometric conditions at zero gate voltage. The LEF of side gated emitters was still highest (7.92 ~ 11.04 V/nm), followed by standard gate (4.90 ~ 9.35 V/nm) and top gate (2.97 ~ 7.79 V/nm). As the gate radius increased from 1 μm to 3 μm , the LEF of top gated emitters increased 4.82 V/nm, standard gated emitters increased 4.45 V/nm, and side gated emitters increased 3.12 V/nm.

Similarly, with -10 V applied gate voltage (Fig. 5.11c), the LEF decreases under all the gate settings, depressing the field emission. The smaller gate openings gave rise to a smaller LEF, with field screening effect and the negative voltage both dampening the LEF. The LEF of side gated emitters was still highest (6.80 ~ 10.50 V/nm, 3.70 V/nm increase), followed by standard gate (3.65 ~ 8.74 V/nm, 5.09 V/nm increase), then top gate (1.71 ~ 7.13 V/nm, 5.42 V/nm increase).

With both applied voltages, the impact of gate voltage on LEF was greater when the gate radius was small. From Table 5.5a I can see that with a fixed setting (standard gate, 1 μm gate radius), the LEF increased from 3.65 to 4.27 to 4.90 V/nm (a 1.25 V/nm increase) when the gate voltage changed from -10 to 0 to 10 V. With a 3 μm gate radius, the LEF increased from 8.74 to 9.04 to 9.35 V/nm (a mere 0.61

V/nm increase) when the gate voltage changed from -10 to 0 to 10 V. In other words, the smaller the gate radius, the larger the influence of gate voltage on the LEF. This trend holds for top and side gated devices as well.

Table 5.5 Relationships among gate radius, geometric correlation factor, LEF and field enhancement factor for (a) standard gate, (b) top gate; and (c) side gate settings under zero, 10 V and -10 V gate voltages.

(a) Standard gate:

Gate radius (μm)	k_a ($1/\mu\text{m}$)	k_g ($1/\mu\text{m}$)	-10 V gate voltage		0 V gate voltage		10 V gate voltage	
			LEF (V/nm)	β	LEF (V/nm)	β	LEF (V/nm)	β
1	4.27	62	3.65	182.5	4.27	213.5	4.90	244.5
2	6.94	41	6.53	326.5	6.94	347.0	7.36	367.5
3	9.04	30	8.74	437.0	9.04	452.0	9.35	467.0

(b) Top gate:

Gate radius (μm)	k_a ($1/\mu\text{m}$)	k_g ($1/\mu\text{m}$)	-10 V gate voltage		0 V gate voltage		10 V gate voltage	
			LEF (V/nm)	β	LEF (V/nm)	β	LEF (V/nm)	β
1	2.34	63	1.71	85.5	2.34	117.0	2.97	148.5
2	4.95	42	4.53	226.5	4.95	247.5	5.37	268.5
3	7.46	33	7.13	356.5	7.46	373.0	7.79	389.5

(c) Side gate:

Gate radius (μm)	k_a ($1/\mu\text{m}$)	k_g ($1/\mu\text{m}$)	-10 V gate voltage		0 V gate voltage		10 V gate voltage	
			LEF (V/nm)	β	LEF (V/nm)	β	LEF (V/nm)	β
1	7.36	56	6.80	340.0	7.36	368.0	7.92	396.0
2	9.03	38	8.65	432.5	9.03	451.5	9.41	470.5
3	10.77	27	10.50	525.0	10.77	538.5	11.04	552.0

5.5.5 Effect of geometric parameter k_g and k_a

In a triode structure, the LEF at the tip of the CNT emitters should be a function of applied potentials (gate potential V_g and anode potential V_a) and the geometric parameters of the triode-type device. According to Nicolaescu et al. [131], the LEF at the tip of triode-type CNT emitters can be written as a linear combination of two terms associated with the gate potential V_g and anode potential V_a as:

$$E = k_g V_g + k_a V_a ,$$

where k_g and k_a are correlation factors related to gate voltage and anode voltage, respectively. The first term, $k_g V_g$ is the field contribution of the gate electrode, while $k_a V_a$ is the field contribution from the anode electrode. Correlation factors k_g and k_a are decided by the geometric parameters of the triode-type device. Having derived the k_g and k_a factors for a given geometry, I can compute the LEF for any anode and gate potentials. The field enhancement factor β can also be calculated by:

$$\beta = \frac{E}{E_0} = \frac{k_g V_g + k_a V_a}{\frac{V_a}{d}} = dk_g \frac{V_g}{V_a} + dk_a ,$$

where d is the distance between the anode and the CNT emitter tip.

According to the theory above, I derived the correlation factors from the simulated LEF values and included them in Table 5.5. Small gate radii increase the electric field screening effect, decreasing the influence of the anode and thus the k_a , while simultaneously increasing the influence of the gate layer and thus the magnitude of k_g . I can also use the correlation factors to compare the relative influences of gate and anode voltage in each of the three gate types. With a fixed 1 μm gate radius, k_a

changes from 2.34 to 4.27 to 7.36 and k_g changes from 63 to 62 to 56 when the gate type is changed from top gate to standard gate to side gate, respectively. Thus the anode has less influence with the top gate setting than standard or side gate settings. The field enhancement factors β for different geometry and electric parameters were also calculated and listed in Table 5.5.

5.5.6 Function of the gate: control over field emission

From the above results, it is clear that side gate has some significant advantages over top and standard gate structures, offering less gate-emitter field screening effect, a larger LEF, and a larger field enhancement factor. Thus it will likely prove useful in low anode voltage field emission applications. However, I have so far not discussed another very important function of the gate yet -- the control over field emission. Many applications require the gate to function as a switch, easily turning on and turning off the field emission. In order to gauge the degree of control of a given gate over field emission, I examined the turn-off voltage (the gate voltage necessary to entirely cut off field emission). In this simulation, the anode is still held constant at 1000 V, and I consider top, standard and side gates with a range of radii (1, 2 and 3 μm). The simulated turn off voltages for each gate type are listed in Table 5.6. Note that for a top gate with 1 μm radius, a gate voltage of a mere -21.5 V is sufficient to turn off the field emission. The 1 μm standard gate needs -52.6 V, while the side gate requires -113.0 V to turn off the field emission. It is clear that top gated and, to a lesser degree, standard gated emitters have significantly better control over field emission. This trend is maintained for all the gate radii examined here. I also see that

for all of the gate types, as the gate radius increases, the voltage needed to turn off the device increases rapidly. It appears that gates with a larger radius cannot be used to easily control field emission regardless of gate type.

Table 5.6 Turn-off voltages for top, standard and side gates CNT FEAs of varying radius.

Gate radius (μm)	Voltage to turn off top gate device (V)	Voltage to turn off standard gate device (V)	Voltage to turn off side gate device (V)
1	-21.5	-52.6	-113.0
2	-94.4	-143.2	-214.1
3	-198.1	-265.6	-360.7

5.6 Recommend Configurations and Parameters for Specific Applications

Based on the simulation results presented in Section 5.5, I can design and optimize triode-type field emission devices for specific applications. In this section, I list three triode-type field emission applications. After determining their requirements and specifications, I list some recommend geometric and electric parameters based on these simulation results.

5.6.1 Parallel electron beam lithography

A sub-100 nm semiconductor lithography technique needs to be developed in order to develop a current microprocessor. Electron-beam direct write is a potential candidate for this technique. However, current electron-beam direct write utilizes only a single electron beam to write, which is a relatively slow process. A possible solution is to use an array of parallel electron beams. This application requires the beam to be

quickly and easily turned on and off. For this reason, a triode structure with an integrated gate electrode is preferred.

Furthermore, for the best capability to control the field emission process, I choose top gate setting instead of standard or side gate settings. In addition, in order to lower the field emission turn-off voltage, I choose a small gate radius (1 μm). Based on these parameters, I can calculate the related geometry correlation factors k_a and k_g , and recommend gate and anode voltages in order to fit the minimum LEF requirement (1 V/nm) to start the field emission. The recommended configuration and parameters are listed in Table 5.7. Through this simulation, I can reduce the power, complexity and cost to drive the device.

Table 5.7 Recommended configuration and parameters for an electron-beam direct write application.

Gate types	Gate radius (μm)	Device distance (μm)	k_a (1/ μm)	k_g (1/ μm)	Anode Voltage (V)	Gate Voltage (V)
Top gate	1	10	2.34	63	400 ~ 600	-5 ~ 5

5.6.2 Field emission display

A field emission display typically consists of a substrate containing an array of addressable gated emitters whose electrons are emitted towards a phosphor anode.

At present, most field emission displays use a Spindt-type triode structure. By applying a positive gate voltage to the gate columns with respect to the emitter rows, pixels can be active for field emission. Each pixel is addressed by one field emitter.

The emission electrons cause the phosphor pixels to work via the electroluminescent process.

Based on these requirements, I optimized some parameters for the field emission display application. For the best capability to start the field emission process, I choose a standard gate setting instead of top or side gate settings. In addition, small gate radius (1 μm) is preferred due to the large gate impact on active pixel emission. Also, if I ignore the redundancy requirement, the device (emitter-emitter) distance can be set to $\sim 100 \mu\text{m}$, which means the pixel distance is 0.1 mm, good enough for field emission display requirements. Based on these parameters, I calculate the related geometry correlation factors k_a and k_g . Then I can get the recommended gate and anode voltages in order to fit the field emission requirement. The recommended parameters are listed in Table 5.8.

Table 5.8 Recommended configuration and parameters for field emission display application.

Gate types	Gate radius (μm)	Device distance (μm)	k_a (1/ μm)	k_g (1/ μm)	Anode Voltage (V)	Gate Voltage (V)
Standard gate	1	100	4.27	62	200 ~ 400	-4 ~ 4

5.6.3 Microwave power amplifier tube

Most long range telecommunication systems are based on microwave links including transmitters on ground stations and on satellites. Traditional thermionic cathodes need to be heated $> 800^\circ\text{C}$ for electron emission [132]. In addition, for high

frequency application, the cathode and gate distance cannot be close enough to achieve short electron transit time.

However, the incorporation of cold cathodes in vacuum tubes can result in high power and long lifetime [133]. Cold cathode tubes can be turned on instantaneously, without the warm-up process inherent thermionic cathodes. At the same time, the gate can be put closer to the cathode to enable lower gate voltage and higher frequency.

Based on these requirements, I optimized some parameters for the microwave power amplifier tube. For the best capability to induce and control field emission, I choose top gate setting triode structure. In addition, microwave amplifiers need extremely high current density and can be operated at high pulse repetition rates. Due to this reason, middle gate radius (2 μm) and higher device density (device distance 8 μm) is preferred to balance the large LEF (larger emission current) and good controllability of the gate. Based on these parameters, I calculate the related geometry correlation factors k_a and k_g . Then I can get the recommended gate and anode voltages in order to start the field emission. The recommend parameters are listed in Table 5.9.

Table 5.9 Recommended configuration and parameters for microwave power amplifier tube application.

Gate types	Gate radius (μm)	Device distance (μm)	k_a (1/ μm)	k_g (1/ μm)	Anode Voltage (V)	Gate Voltage (V)
Top gate	2	8	4.95	42	200 ~ 300	0 ~ 10

Chapter 6 CONCLUSIONS

This work has presented an effective and controllable method of synthesizing CNT FEAs and demonstrated the significance of gate layer bias in field emission from such triode-type emitters. These experimental results were complemented with a theoretical simulation of the relationships between geometrical parameters, gate bias and local electric field. The experimental and theoretical approaches will prove advantageous in designing CNT FEAs tailored to specific applications. For example, it will be possible to devise a set of morphological guidelines based on simulation results and then harness the controllability of the FIB- and PECVD-based synthesis methods presented here to build devices to these geometrical specifications.

One of the main focuses of this work was devising a methodology for creating effective CNT FEAs. CNTs grown by PECVD are determined to be more desirable for field emission applications than those grown by CVD. The morphology of these CNTs are affected by a number of growth parameters, such as catalyst type, initial catalyst thickness, growth temperature, temperature ramping rate, the ratio of C_2H_2 to NH_3 , chamber pressure, and plasma voltage. The size of the Ni catalyst nanoparticles directly affects the CNT diameter and can be controlled by changing the initial Ni film thickness, growth temperature and/or temperature ramping rate. The structures observed on the SEM and TEM indicate a tip growth model, and Ni particles found in the body of the CNTs were caused by the Ni catalyst moving upwards toward the anode during growth. The internal structures of the CNT emitter display bamboo-like

fringes characterized by periodic curving graphitic bands normal to the tube axis. Two in-situ CNT property test methods aided in performing basic research on the internal structures of CNT and CNT/substrate interface properties.

I investigated two approaches to synthesizing triode-type CNT FEAs: the “top-down”, etch-deposit-synthesize method and a novel “bottom-up” method to fabricate large-scale, reproducible triode-type CNT FEAs. The “bottom-up” method employs dual-beam FIB to carve gated holes from a multilayer embedded-catalyst substrate, and PECVD to synthesize CNT emitters in these micro-gated holes. PECVD growth parameters were selected to produce CNT morphologies well suited to emitter applications. Modified hole and gate structures were designed to prevent short-circuiting between the cathode and gate layers, to mill to optimal depth, to reduce cathode-gate capacitance, and to ensure an optimal CNT emitter yield.

I found that gate voltage plays a significant role in field emission: increasing gate voltage from -0.2 to 0.1 V lowered the turn-on field from 20.0 to 16.4 V/ μm and the threshold fields from 23.8 to 20.8 V/ μm , while increasing the field enhancement factor from 149 to 222. A theoretical simulation of the relationships among anode voltage, gate voltage, and tunneling barrier thickness was conducted. The results confirm that negative gate voltages increased tunneling barrier thickness, while positive gate voltages decreased thickness, making electron tunneling significantly easier and thus generating a higher emission current density.

I developed an effective method for analytically calculating the effect of various other gate parameters on field emission from triode-type CNT FEAs. This

simulation method allows me to predict, given the geometric structure of the device, how the local electric field (LEF) will react to applied anode and gate potentials. The simulations revealed the importance of gate radius: voltage applied to gate with a 1 μm cavity radius impacts LEF roughly twice as much as voltage applied to a gate with 3 μm radius. It also displayed the relative advantages of different gate heights: given a 1 μm gate radius, side-gated arrays produced 5.02 V/nm higher LEF than top-gated arrays, while top-gated arrays displayed significantly greater controllability, turning off the field emission with as little as -21.5 V compared to -113 V in side-gated arrays. Understanding the effects of gate geometry is the key to taking full advantage of the benefits of a gate layer. The fabrication methods presented here facilitate the creation of controlled, reproducible CNT FEAs and the theoretical results provide information that will prove useful in designing and optimizing triode-type CNT devices targeted at specific applications.

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Appendix: List of Publications and Awards

2010

1. J. Wu and J. Jiao, "Fabrication and Model Simulation of the Ring-shaped Gate Carbon Nanotube Emitter Arrays", submitted to Microscopy and Microanalysis, (2010).

2009

1. Best Research Poster Awards, Fifth annual Student Research Symposium, Columbia-Willamette Chapter of SIGMA XI, April 2009.
2. J. Wu, M. Wyse, D. McClain, N. Thomas and J. Jiao, "Fabrication and Field Emission Properties of Triode-Type Carbon Nanotube Emitter Arrays", Nano Letters, 9(2), pp 595–600 (2009).
3. J. Wu, M. Wyse and J. Jiao, "Fabrication and Model Simulation of the Triode-Type Carbon Nanotube Emitter Arrays", Microscopy and Microanalysis, Vol. 15, Supplement 2, 1274-1275 (2009).

2008

1. MSA First Prize Poster Awards, Microscopy & Microanalysis 2008 Meeting, Albuquerque, New Mexico, USA, August 2008.
2. Best Research Poster Awards, Fourth annual Student Research Symposium, Columbia-Willamette Chapter of SIGMA XI, April 2008.
3. President's Service Awards, Portland State University, Oregon, USA, June 2008.
4. J. Wu, J. Walenza-Slabe, T. Gutu and J. Jiao, "Direct Growth of Single Walled Carbon Nanotubes for the Characterization of Structural and Electronic

Properties", Materials Research Society, Symposium Proceeding, Vol.1081, Paper # 1081-P04-02 (2008).

5. J. Wu, J. Walenza-Slabe, M. Mann, K.B.K. Teo, W.I. Milne and J. Jiao, "Novel Fabrication of Carbon Nanotube Vias for VLSI Interconnects", Microscopy and Microanalysis, Vol. 14, Supplement 2, 298-299 (2008).

2007

1. MSA Second Price Poster Awards, Microscopy & Microanalysis 2007 Meeting, Ft. Lauderdale, Florida, USA, August 2007.
2. J. Wu, M. Eastman, T. Gutu, M. Wyse and J. Jiao, S.-M. Kim, M. Mann, Y. Zhang and K.B.K. Teo, "Fabrication of Carbon Nanotube-Based Nanodevices Using a Combination Technique of Focused Ion Beam and Plasma-enhanced Chemical Vapor Deposition", Applied Physics Letters, 91, 173122 (2007).
3. C. Xu, S. Youkey, J. Wu, J. Jiao, "Electrical Behavior of Ferromagnetic BiMn-Codoped ZnO Bicrystal Nanobelts to Pt Contacts", Journal of Physical Chemistry C, 111(33), 12490-12494 (2007).
4. J. Wu, T. Gutu, M. Eastman, M. Wyse, S.-M. Kim, Y. Zhang, K.B.K. Teo, W.I. Milne and J. Jiao, "Electron Microscopy and Spectroscopy Characterization of As-Made CNTs", Microscopy and Microanalysis, Vol. 13, Supplement 2, 742-743 (2007).
5. T. Gutu, J. Wu, C. Jeffryes, C. Chang, G.L. Rorrer, and J. Jiao, "Dual Beam Focused Ion Beam and Transmission Electron Microscopies of Nanoscale Sectioned Diatom Frustules", Microscopy and Microanalysis, Vol. 13, Supplement 2, 678-679 (2007).

6. S-M Kim, Y. Zhang, K. B. K. Teo, M. S. Bell, L. Gangloff, X. Wang, W. I. Milne, J. Wu, J. Jiao and S-B Lee, "SWCNT growth on Al/Fe/Mo investigated by in-situ Mass spectroscopy", *Nanotechnology*, 18, 185709 (2007).
7. D. McClain, J. Wu, N. Tavan, J. Jiao, C. M. McCarter, R. F. Richards, S. Mesarovic, C. D. Richards, D. F. Bahr, "Electrostatic Shielding in Patterned Carbon Nanotube Field Emission Arrays", *Journal of Physical Chemistry C*, 111(20), 7514 -7520 (2007).

2006

1. MSA First Prize Poster Awards, Microscopy & Microanalysis 2006 Meeting, Festival Hall at Navy Pier, Chicago, Illinois, USA, July 30-August 3, 2006.
2. 2nd Place, Graduate student poster Competition, the 17th Annual Symposium of the Pacific Northwest Chapter of the American Vacuum Society Science and Technology Society (PNWAVS), Forest Grove, Oregon, USA, September 21 - 22, 2006.
3. J. Wu, L. Dong, T. Gutu, J. Jones and J. Jiao, "Electron Microscopy Study of Carbon Nanotubes Synthesized by Plasma-Enhanced Chemical Vapor Deposition" *Microscopy and Microanalysis 2006*, Vol. 12, Supplement 2, 652-653 (2006).
4. J. Wu, L. Dong, C.C. Pan and J. Jiao, "Fabrication and Electron Microscopy Characterization of Metal-Gated Carbon Nanotube Emitter Arrays," *International Journal of Nanoscience*, Vol. 5, Nos. 4 & 5, 579-583, 2006.

2005

1. 3rd Place, Graduate student poster award, the 16th Annual Symposium of the Pacific Northwest Chapter of the American Vacuum Society Science and Technology Society (PNWAVS), McMinn Edgefield in Troutdale, Oregon, USA, September 15 - 16, 2005.
2. J. Wu, L. Dong, J. Petty, C.C. Pan and J. Jiao, "Fabrication of Metal-Gated Carbon Nanotube Emitter Arrays Assisted by Focused Ion Beam and Chemical Vapor Deposition." *Microscopy and Microanalysis* 2005, Vol. 11, Supplement 2, 1956-1957 (2005).