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Vertical nanowire transistor in flexible polymer foil

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Fabrication and operation of a vertical nanowire field-effect transistor is reported. The device is prepared by growing vertical wires in the cylindrical pores of a polymer foil stack. The nanowire diameter is approximately 100 nm, the packing density up to 10^8 cm^{-2} . The polymer foil stack consists of two polymer layers and an intermediate metal layer. Cylindrical holes are prepared in this stack by using fast ion irradiation and subsequent etching. Well-defined cylindrical openings with diameters between 50 and 150 nm are obtained. The semiconductor growth involves electrodeposition of the *p*-type quaternary compound CuSCN. Electrical measurements on first devices show transistor action with some gate leakage, which may be improved in future designs. The arrangement of inorganic device material embedded in soft polymer matrix is structurally robust, and the devices show low sensitivity to mechanical strain of the foil. Single electron effects may be expected in these devices, when the dimensions are further reduced. © 2003 American Institute of Physics. [DOI: 10.1063/1.1587258]

Nanoscale sized definition and flexible device structures are presently among the most ambitious development goals in the semiconductor field. One approach to attain these goals is based on the use of hybrid structures combining the flexibility of organic materials as substrates with the device functions of inorganic semiconductors.^{1,2} However, the lack of thermal robustness of many flexible materials and mechanical compatibility problems at the organic/inorganic interface severely limit progress in this research area. Here, we show that vertical field-effect transistors (VFETs) with dimensions below $\sim 100 \text{ nm}$ can be prepared inside the cylindrical pores of thin polymer films at packing densities of 10^8 cm^{-2} . Many of the basic problems encountered with layered hybrid structures are alleviated in this approach. Since the devices are entirely embedded in the flexible matrix, the resulting structures are very robust and exhibit stable electrical characteristics. We report preparation and characterization of vertical transistors and discuss the possibility of further reducing their dimensions.

Figure 1 illustrates the basic design of a VFET, embedded in a flexible matrix, which consists of two polymer films and an intermediate metal layer. The vertical columns of semiconductor material are contacted at the top and the bottom face, and in a ring-like manner at intermediate height. Top and bottom contacts are in electrical conduct with the nanowire and act as source and drain electrodes, respectively. The ring-like contact at intermediate height is isolated by a thin insulator layer, and acts as a gate contact. The semiconductor volume enclosed by the intermediate metal layer acts as the channel for the vertical transistor. When the column diameter is small enough, the potential induced by the gate contact reaches radially through the whole column, a large conductance variation between source and drain contacts can be achieved, and switching and amplification become

possible.³ There are several advantages to this device arrangement: a high packing density that can be obtained without the use of lithography, a high structural robustness, and a small gate width, defined here by the thickness of the intermediate metal layer, and permitting high currents and fast switching. The fabrication is as follows. As a first step, a stacked arrangement of polyethyleneterephthalate (PET) foils with a metallic layer sandwiched between the two foils is prepared. Secondly, this stack is exposed to a heavy ion beam, using highly ionized Xe or Au ions with a kinetic energy of $\sim 500 \text{ MeV}$. The passage of these ions leaves an amorphized track in the polymer,⁴ which can be etched in a third step to a diameter of 30–3000 nm,⁵ leaving cylindrical openings in the two foils. Another etching step is then applied to remove the remains of the intermediate metal film in the cylinders. Semiconductor and insulator deposition in this template structure follows a path explored by others^{6,7} and ourselves,^{8,9} using chemical and electrochemical techniques. On one side of the stacked foils, a metal contact layer is then provided. This layer serves as an electrode in an electrochemical cell to grow a compound semiconductor into the cylindrical openings of the foil stack. The arrangement is

FIG. 1. Schematic diagram of vertical nanowire transistor embedded in a polymer/metal/polymer stack.

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FIG. 2. Micrographs of polymer template and semiconductor nanowires. (a) Cross-sectional micrograph of stacked polymer films with center metal layer of 200-nm thickness. (b) Top view of conically etched pores with 200-nm diameter at the top exposed side and 40-nm pores at the bottom of the pores. (c) Free-standing polycrystalline CuSCN columns obtained after template growth in polymer pores and subsequent dissolution of the polymer template. The column diameter is 110 nm.

then provided with a metallic top contact. The top and bottom electrodes serve as source and drain contacts, respectively, the center metal layer serves as a gate contact, and the grown semiconductor wires provide the channel. Electrical insulation between gate and channel is a critical element in this design, and several possibilities have been considered, among them (a) oxidation of the metal layer edge inside the cylinder, (b) insulator deposition on the cylinder walls prior to semiconductor deposition, and (c) under-etching of the center metal layer to provide an air pocket for insulation.

It is noted from this design that most relevant elements of the transistor are robustly embedded in the polymer stack. Previous experiments indeed showed that strong flexing and stress action on the foils give rise to extremely small conductance changes in the embedded semiconductor column.⁹ This finding was attributed to the fact that the soft polymer matrix takes up most of the mechanical energy. It is also noted that lithography on the scale of single transistors is not necessary in the present design. It may, however, be incorporated on a larger length scale to address arrays of transistors by the source, drain, or gate contacts. When an ion track density of $10^8/\text{cm}^2$ is assumed, a pixel of $30\text{-}\mu\text{m}$ side length will contain 900 transistors, and operation of this pixel can then be performed with an accuracy of $\sim 3\%$ despite of the statistical distribution of the transistors. While many applications appear possible in such a scheme, further improvement of the lateral uniformity and of the packing density would be feasible with the use of guided ion beams.

For the fabrication of the first devices, we used PET foils of $8\text{-}\mu\text{m}$ thickness. These were cleaned in ethanol and a 60–200-nm-thick center gate contact layer was provided by vacuum evaporation of Cu. The second foil was attached to the freshly deposited Cu layer at a pressure of 100 kPa and a temperature of 90°C by using N-(2-aminoethyl)-3-aminopropyltrimethoxysilane as a monomolecular coupling agent. A gold back contact was then provided on one side of the stack. Since this contact serves as an electrode in an electrochemical deposition, this layer should be thick enough to completely cover the etched pores. Figure 2(a) shows a scanning electron micrograph of the foil stack. 400-MeV Xe^{20+} ions were obtained from the Ion Beam Lab Berlin at the Hahn-Meitner Institut (HMI). At minimum current density, typical exposure times were 5–10 s, resulting in

FIG. 3. Device characteristics of an array of ~ 1500 VFETs in polymer foil. (a) Transfer characteristic on a logarithmic scale; the source–drain voltage is 1 V. (b) Source–drain characteristic at different gate potentials.

track densities of $\sim 5 \times 10^7/\text{cm}^2$. We used 7 M NaOH/ H_2O and 1 M $\text{HNO}_3/\text{H}_2\text{O}$ for the etching of the polymer and metal layer, respectively. The polymer etching was carried out in such a way that a conical hole with top diameter of $\sim 200\text{ nm}$ and a bottom diameter of $\sim 40\text{--}70\text{ nm}$ is obtained in the top foil. For the same etching conditions the bottom foil typically showed somewhat ($\sim 15\%$) smaller diameters. The reason for these differences is not completely clear, but may lie in the gluing and metalization processes, which necessitate an unequal treatment of the two foils. Figure 2(b) shows scanning electron micrographs of the etch cylinders in the top foil. In the vertical perspective the narrower bottom diameter is clearly visible. We believe that the bottom diameter can be made as small as $10\text{--}30\text{ nm}$ by using refined etch techniques or the deposition of ultrathin layers after etching. CuSCN, a quaternary *p*-type semiconductor, was then grown as channel material under conditions, as reported in detail previously. Figure 2(c) shows the free-standing vertically oriented columns as the polymer foil has been completely removed. A previous study showed that the CuSCN columns consist of stacked polycrystalline grains.⁹ The predominant orientation of these grains can be affected somewhat by the growth conditions.

The critical issue in this fabrication technique is the gate insulation. We have tried several ways for insulation. When the metallic center layer is very thin and is under-etched sufficiently, the under-etched volume will not be filled up in the CuSCN deposition process. In this case, the air pocket between the gate electrode and the CuSCN may be used for gate insulation. Exploring this simplest approach experimentally has, however, not led to very satisfactory electrical results. The resulting under-etched volume was apparently not small enough to be excluded from deposition, and high gate leakage currents were observed. We therefore deposited a thin insulation layer on the inner walls of the pores and over the metallic face of the gate layer using the same process as in the gluing process of the foils. Although this process has not yet been brought to perfection, it appears that first devices with reasonably low leakage currents can be made in this way.

Figure 3 shows typical device characteristics of approximately 1500 devices. The transfer current can be changed over approximately two orders of magnitude by changing the gate potential between -1.5 and 0 V . At high negative gate voltages, leakage is still appreciable, indicated by a finite transfer current at zero source–drain voltage. Several ap-

proaches for reducing the leakage currents are now under way. The electrical results indicate that more positive gate voltage puts the *p*-type channel material into hole depletion, and this interpretation is consistent with a more extensive characterization of the material carried out previously.¹⁰ In conductive-tip atomic force microscopy measurements, we measure a typical current of 10 pA for source-drain voltages of 1 V across a single CuSCN wire of 150-nm diameter and 16- μ m height. Assuming a carrier density of 10^{16} cm⁻³ as obtained from Hall experiments on CuSCN thin films in our lab, this current corresponds to the passage of 2500 holes through the column. This in turn means that there are about 40 holes in the gated channel region. Thus, by reducing the side length of the channel volume to $\sim 30\%$ in each direction, single-electron effects should clearly be expected. Besides the possibility to fabricate single-electron devices on this scheme, there is the interesting perspective of obtaining very small channel widths by reducing the intermediate metal layer thickness.

To conclude, we have reported experimental results on a nanowire transistor which is vertically embedded in a flexible soft substrate. In this arrangement, most of the mechanical stress and the resulting structural distortions are taken up by the plastic environment, and the semiconductor device remains comparatively insensitive to flexing, bending, and stretching motion of the foil. The lateral extension of the transistors is ~ 100 nm. Packing densities of 10^8 cm⁻² are

achievable without lithographic processing. Gate widths in the range of 100 to 200 nm have been explored. These can easily be further reduced by using thinner metallic intermediate layers, allowing large source-drain currents, fast switching, and single-electron operation in this device arrangement.

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