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Citation Details

Perkowski, Marek and Khan, Mozammel H.A., "Synthesis of Reversible Synchronous Counters" (2011).
Electrical and Computer Engineering Faculty Publications and Presentations. 203.
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Synthesis of Reversible Synchronous Counters

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ISMVL 2011, 23-25 May 2011, Tuusula, Finland

Agenda

- Motivation
- Background
- Previous Works on Reversible Sequential Logic
- Reversible Logic Synthesis using PPRM Expressions
- Synthesis of Synchronous Counters
- Conclusion

Motivation

- Reversible circuits dissipate less power than irreversible circuits
- Reversible circuits can be used as a part of irreversible computing devices to allow **low-power** design using current technologies like CMOS
- Reversible circuits can be realized using **quantum** technologies

Motivation (contd.)

- Reversible circuits have been implemented in ultra-low-power CMOS technology, optical technology, quantum technology, nanotechnology, quantum dot, and DNA technology
- Most of the reversible logic synthesis attempts are concentrated on reversible **combinational logic synthesis**

Motivation (contd.)

- Only limited attempts have been made in the field of reversible **sequential** circuits
- Most papers present reversible design of latches and flip-flops and suggest that sequential circuits be constructed by **replacing the latches and flip-flops** of traditional designs by the reversible latches and flip-flops

Motivation (contd.)

- In this paper, we concentrate on design of synchronous counters **directly from reversible gates**

Background

- A gate (or a circuit) is *reversible* if the mapping from the input set to the output set is *bijective*
- The bijective mapping from the input set to the output set implies that a reversible circuit has *the same number* of inputs and outputs

Background (contd.)

A	A'
0	1
1	0

(a) NOT gate

AB	AP
00	00
01	01
10	11
11	10

(b) Feynman gate

ABC	ABP
000	000
001	001
010	010
011	011
100	100
101	101
110	111
111	110

(c) Toffoli gate

ABC	APQ
000	000
001	001
010	010
011	011
100	100
101	110
110	101
111	111

(d) Fredkin gate

Figure 1. Commonly used reversible gates – symbols and truth tables

Background (contd.)

- Toffoli gate may have more than three inputs/outputs.
- In an $n \times n$ Toffoli gate, the first $(n - 1)$ inputs (say $A_1, A_2, \dots, A_{n-1}$) are control inputs and the last input (say A_n) is the target input.
- The value of the target output is
$$P = A_1 A_2 \dots A_{n-1} \oplus A_n$$

Background (contd.)

- The 1×1 and 2×2 gates are technology realizable primitive gates and their **realization costs** (**quantum costs**) are assumed to be one
- The 3×3 **Toffoli** gate can be realized using **five** 2×2 primitive gates
- The 3×3 **Fredkin** gate can be realized using **five** 2×2 primitive gates

Background (contd.)

Figure 2. Realizations of (a) 4×4 (cost = 10, garbage = 1) and (b) 5×5 Toffoli gates (cost = 15, garbage = 2)

Previous Works on Reversible Sequential Logic

- 24) J.E. Rice, *Technical Report: The State of Reversible Sequential Logic Synthesis*, Technical Report TR-CSJR2-2005, University of Lethbridge, Canada, 2005.
- 25) S.K.S. Hari, S. Shroff, S.N. Mohammad, and V. Kamakoti, "Efficient building blocks for reversible sequential circuit design," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2006.
- 26) H. Thapliyal and A.P. Vinod, "Design of reversible sequential elements with feasibility of transistor implementation," *International Symposium on Circuits and Systems (ISCAS 2007)*, 2007, pp. 625-628.
- 27) M.-L. Chuang and C.-Y. Wang, "Synthesis of reversible sequential elements," *ACM journal of Engineering Technologies in Computing Systems (JETC)*, vol. 3, no. 4, 2008.
- 28) A. Banerjee and A. Pathak, "New designs of Reversible sequential devices," *arXiv:0908.1620v1 [quant-ph]* 12 Aug 2009.

Previous Works on Reversible Sequential Logic (contd.)

- All the above works present reversible design of latches and flip-flops
- They suggest that reversible sequential circuit can be constructed by replacing flip-flops and gates of traditional design by their reversible counterparts
- The (non-clocked) latches have limited usefulness in practical sequential logic design

Previous Works on Reversible Sequential Logic (contd.)

- Level-triggered flip-flops and edge-triggered/master-slave flip-flops have usefulness in sequential logic design

Previous Works on Reversible Sequential Logic (contd.)

TABLE I. Comparison of realization costs and number of garbage outputs (separated by comma) of level-triggered flip-flop and edge-triggered/master-slave flip-flop designs

Ref	Level-triggered flip-flop				Edge-triggered/master-slave flip-flop			
	RS	JK	D	T	RS	JK	D	T
[24]					50,16	62,18	51,16	63,18
[25]		12,4	10,2	7,2		22,6	12,3	13,3
[26]			6,2	6,2			13,4	17,4
[27]		26,5	6,2	6,2		43,4	13,3	13,3
[28]	18,3	12,3	7,2	6,2	24,3	18,3	13,2	12,2

Reversible Logic Synthesis using PPRM Expression

- Positive Davio expansion on all variables results into PPRM expression

$$f(x_1, x_2, \dots, x_n) = f_0 \oplus x_i f_2$$

$$f_0 = f(x_1, \dots, x_{i-1}, 0, x_{i+1}, \dots, x_n)$$

$$f_1 = f(x_1, \dots, x_{i-1}, 1, x_{i+1}, \dots, x_n)$$

$$f_2 = f_0 \oplus f_1$$

Reversible Logic Synthesis using PPRM Expression (contd.)

- An n -variable PPRM expression can be represented as

$$f(x_1, x_2, \dots, x_n) = f_{00\dots 00} \oplus f_{00\dots 01}x_n \oplus f_{00\dots 10}x_{n-1} \oplus \\ f_{00\dots 11}x_{n-1}x_n \oplus \dots \oplus f_{11\dots 11}x_1x_2 \dots x_{n-1}x_n \\ (\forall i \in \{0,1\}^n) f_i \in \{0,1\}$$

Rversible Logic Synthesis using PPRM Expression (contd.)

Figure 3. Computation of PPRM coefficients
from output vector

$$F(A, B, C) = BC \oplus A \oplus AC$$

Figure 3. Computation of PPRM coefficients
from output vector

Reversible Logic Synthesis using PPRM Expression (contd.)

- The PPRM expression is written from the final coefficient vector $[00011100]^T$
- The resulting PPRM expression for the given function in Figure 3 is

$$F(A, B, C) = BC \oplus A \oplus AC$$

Rversible Logic Synthesis using PPRM Expression (contd.)

- The PPRM expression can be realized as a cascade of Feynman and Toffoli gates

Figure 4. Realization of PPRM expression as cascade of Feynman and Toffoli gates

Synthesis of Synchronous Counter

- We construct truth table considering the **clock** input and the **present states** as the inputs and considering the next states as the outputs
- Then we calculate **PPRM expression** of all the outputs and realize them as cascade of **Feynman and Toffoli gates**
- The **feedback** from the next state output to the present state input is done by making a copy of the next state output using **Feynman gate**

Synthesis of Synchronous Counter (contd.)

- The synthesized counter is a **level-triggered** sequential circuit and clock pulse width has to be determined based on the total delay of the circuit
- SHOULD WE DO THIS FOR REVERSIBLE SIMULATE?
- Quantum?
- Quantum is different

Synthesis of Synchronous Counter (contd.)

Input	Output	PPRM Coefficients
$CQ_2Q_1Q_0$	$Q_2Q_1Q_0$	$Q_2Q_1Q_0$
0000	000	000
0001	001	001
0010	010	010
0011	011	000
0100	100	100
0101	101	000
0110	110	000
0111	111	000
1000	001	001
1001	010	010
1010	011	000
1011	100	100
1100	101	000
1101	110	000
1110	111	000
1111	000	000

TABLE II. Truth table and PPRM coefficients of the next state outputs for mod 8 up counter

Synthesis of Synchronous Counter (contd.)

The PPRM expressions for the next state outputs are

$$Q2_{t+1} = Q2_t \oplus CQ1_t Q0_t$$

$$Q1_{t+1} = Q1_t \oplus CQ0_t$$

$$Q0_{t+1} = Q0_t \oplus C$$

Synthesis of Synchronous Counter by direct method

Figure 5. Reversible circuit for mod 8 up counter

Modulo 8 counter

initialization

External feedback wires

$$Q2_{t+1} = Q1_t Q0_t C \oplus Q2_t$$

$$Q1_{t+1} = Q0_t C \oplus Q1_t$$

$$Q0_{t+1} = C \oplus Q0_t$$

- Figure 5. Reversible circuit for mod 8 up counter.

Synthesis of Synchronous Counter (contd.)

Figure 6. Traditional circuit for mod 8 up counter

mod 8 up counter by replacement method:

- Figure 7. Reversible circuit for mod 8 up counter after replacement of the T flip-flops and AND gates of Figure 6 by their reversible counter parts.

Direct Synthesis of Mod 16 Synchronous Counter

- We can determine the PPRM expressions for the next state outputs of mod 16 up counter as follows

$$Q3_{t+1} = Q3_t \oplus CQ2_t Q1_t Q0_t$$

$$Q2_{t+1} = Q2_t \oplus CQ1_t Q0_t$$

$$Q1_{t+1} = Q1_t \oplus CQ0_t$$

$$Q0_{t+1} = Q0_t \oplus C$$

Direct Synthesis of Mod 16 Synchronous Counter

Cost = 35

Garbage = 4

$$Q3_{t+1} = Q3_t \oplus CQ2_tQ1_tQ0_t$$

$$Q2_{t+1} = Q2_t \oplus CQ1_tQ0_t$$

$$Q1_{t+1} = Q1_t \oplus CQ0_t$$

$$Q0_{t+1} = Q0_t \oplus C$$

Figure 8. Reversible circuit for mod 16 up counter

Synthesis of classical Mod 16 Synchronous Counter

Figure 9. Traditional circuit for mod 16 up counter

Direct Synthesis of Reversible circuit for mod 16 up counter.

Flip-flop replacement method for Reversible circuit for mod 16 up counter.

Figure 10. Reversible circuit for mod 16 up counter **after replacement** of the T flip-flops and AND gates of Figure 9 by their reversible counter parts.

Synthesis of Synchronous Counter (contd.)

TABLE III. Comparison of our direct design and replacement technique for mod 8 and mod 16 up counters

	Our direct technique		Replacement technique	
Counter	Cost	Garbage	Cost	Garbage
mod 8	19	2	24	4
mod 16	35	4	40	6

CONCLUSION: Our method creates counters of smaller quantum cost and number of garbages than the previous methods

Synthesis of Synchronous Counter (contd.)

- PPRM expressions of the next state outputs can be written in general terms as follows

$$Qi_{t+1} = Qi_t \oplus CQ(i-1)_t Q(i-2)_t \cdots Q0_t \quad \text{for } i > 0$$

$$Q0_{t+1} = Q0_t \oplus C \quad \text{for } i = 0$$

- These generalized PPRM expressions allow us to **implement any up counter** directly from reversible gates very efficiently

Conclusions

1. Reversible logic is very important for low power and quantum circuit design.
2. Most of the attempts on reversible logic design concentrate on reversible combinational logic design [9-22].
3. Only a few attempts were made on reversible sequential circuit design [23-28, 32-35].
4. The major works on reversible sequential circuit design [23-27] propose implementations of flip-flops and suggest that sequential circuit be constructed by replacing the flip-flops and gates of the traditional designs by their reversible counter parts.

Conclusions 2

- These methods produce circuits with high realization costs and many garbages
- We present a method of synchronous counter design directly from reversible gates
- This method produces circuit with lesser realization cost and lesser garbage outputs
- The proposed method generates expressions for the next state outputs, which can be expressed in general terms for all up counters

Conclusions 3

- This generalization of the expressions for the next state outputs makes synchronous up counter design very **easy and efficient**.
- Traditionally, **state minimization and state assignment** are parts of the entire synthesis procedure of finite state machines.
- The role of these two processes in the realization of reversible sequential circuits [32,34] has been investigated by us
- It should be further investigated.

Conclusions 4

- We showed a method that is specialized to **certain type of counters**.
- We created a similar method for quantum circuits which is specialized to **other types of counters**
- T flip-flops are good for counters
- T flip-flops are good for arbitrary state machines realized in reversible circuits.
- Excitation functions of T ffs are realized as products of **EXORs of literals** and **Inclusive Sums of literals**
- **Don't' cares** **should be used** to realize functions of the form:

$$Qi_{t+1} = Qi_t \oplus a \bullet b \bullet c \bullet d \bullet e$$

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