1994

Programmable Analog Array Circuit

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US005959871A

United States Patent [19]

Pierzchala et al.

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[54] **PROGRAMMABLE ANALOG ARRAY CIRCUIT**

[75] Inventors: **Edmund Pierzchala**, Milwaukie; **Marek A. Perkowski**, Beaverton, both of Oreg.

[73] Assignee: **Analogix/Portland State University**, Portland, Oreg.

[21] Appl. No.: **08/362,838**

[22] Filed: **Dec. 22, 1994**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/173,414, Dec. 23, 1993, abandoned.

[51] **Int. Cl.**[6] **H03K 17/693**

[52] **U.S. Cl.** **364/489**; 327/565; 326/39

[58] **Field of Search** 364/488, 489, 364/490; 326/39, 41; 327/341, 526, 566, 565

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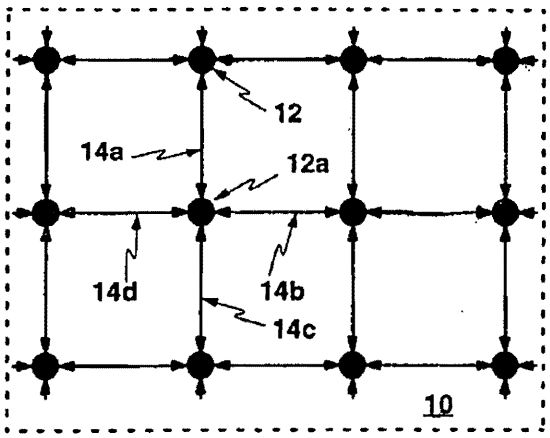
Primary Examiner—Vincent N. Trans

Attorney, Agent, or Firm—Jeffrey B. Oster

[57] **ABSTRACT**

There is disclosed a programmable analog or mixed analog/digital circuit. More particularly, this invention provides a circuit architecture that is flexible for a programmable electronic hardware device or for an analog circuit whose input and output signals are analog or multi-valued in nature, and primarily continuous in time. There is further disclosed a design for a current-mode integrator and sample-and-hold circuit, based upon Miller effect.

6 Claims, 16 Drawing Sheets



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PMI, GAP–01, Analog Signal Processing Subsystem.

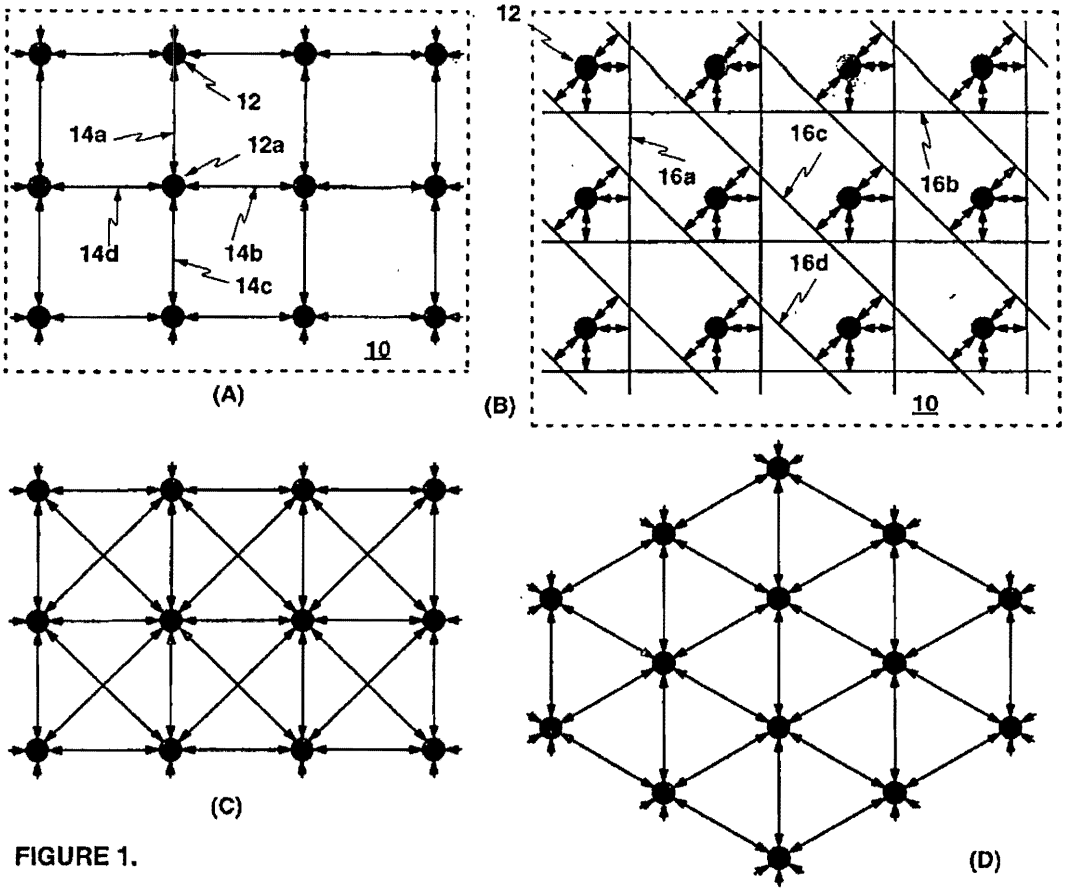


FIGURE 1.

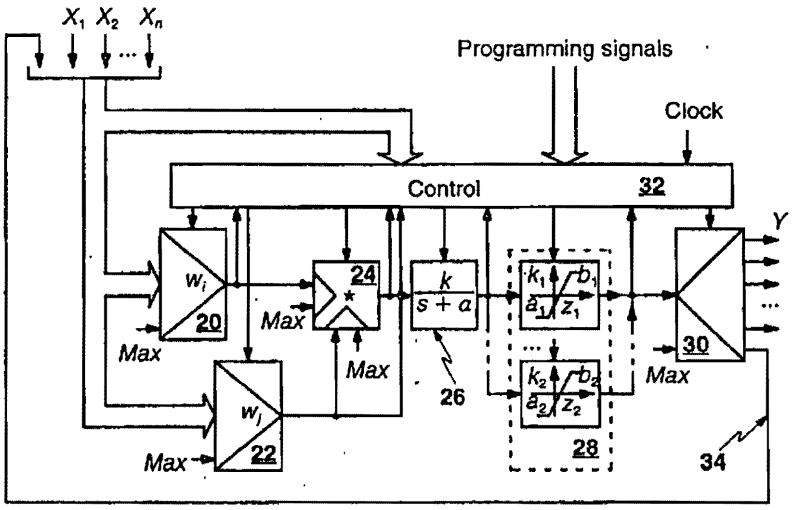


FIGURE 2.

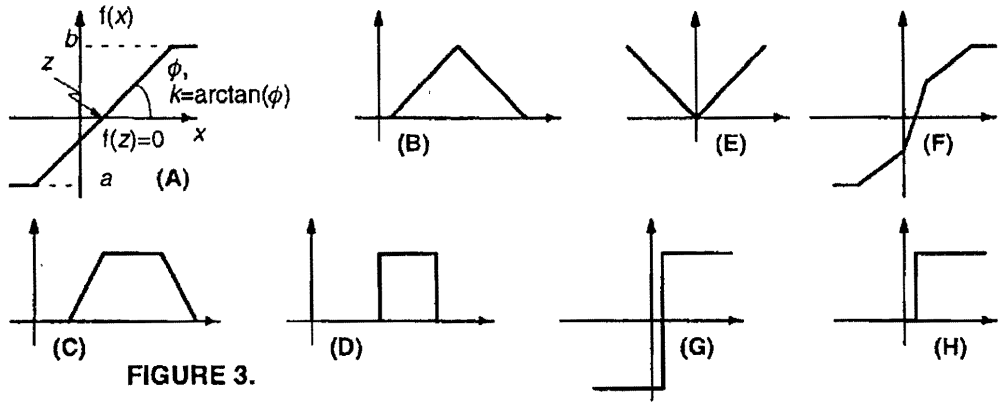


FIGURE 3.

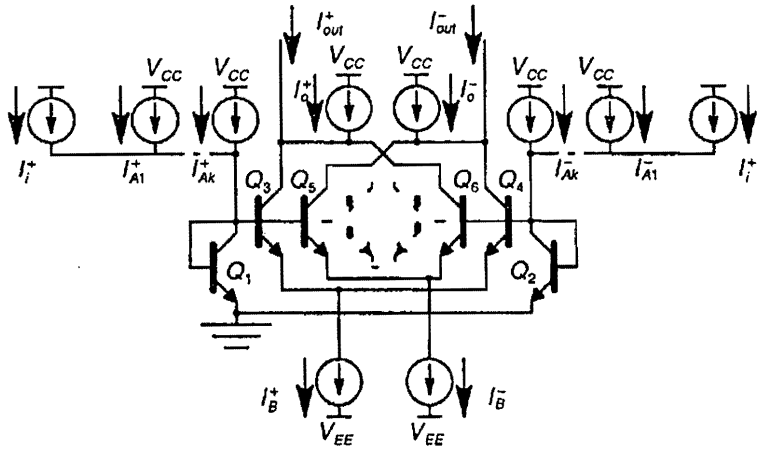


FIGURE 4.

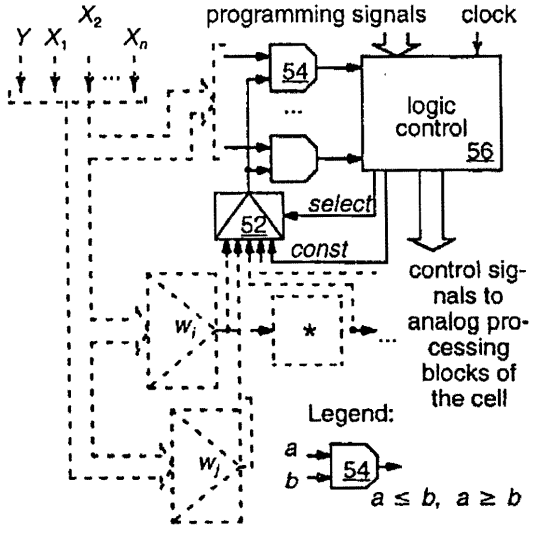


FIGURE 5A.

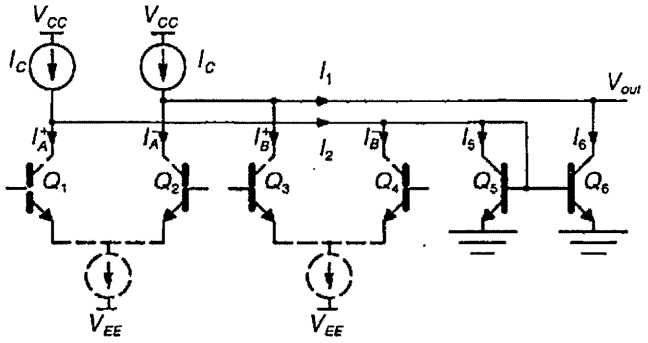


FIGURE 5B.

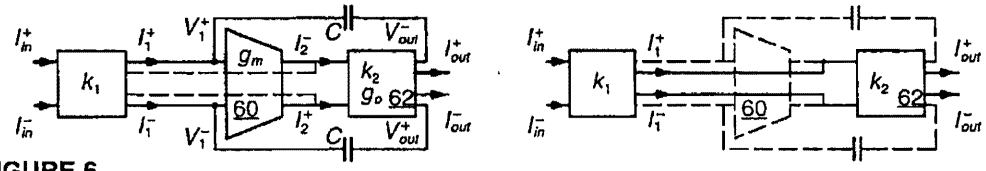


FIGURE 6.

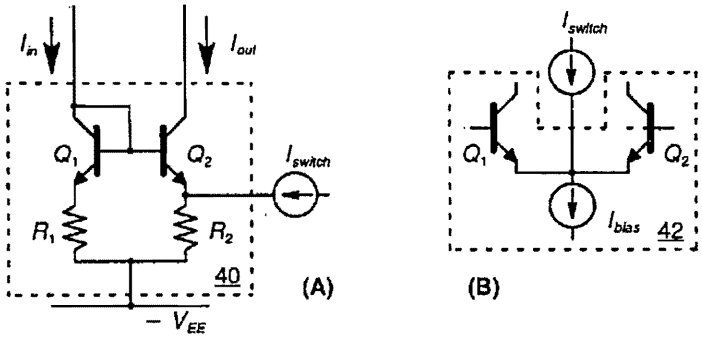
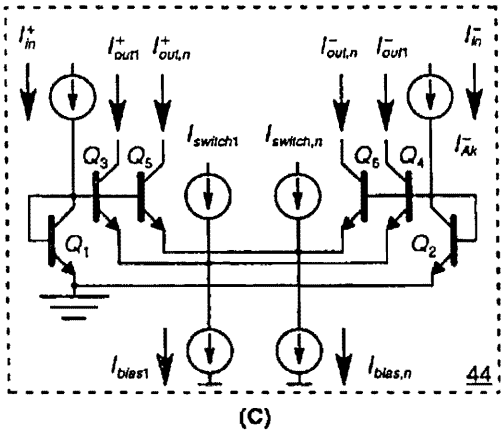


FIGURE 7.



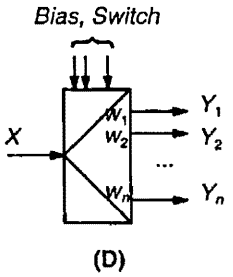
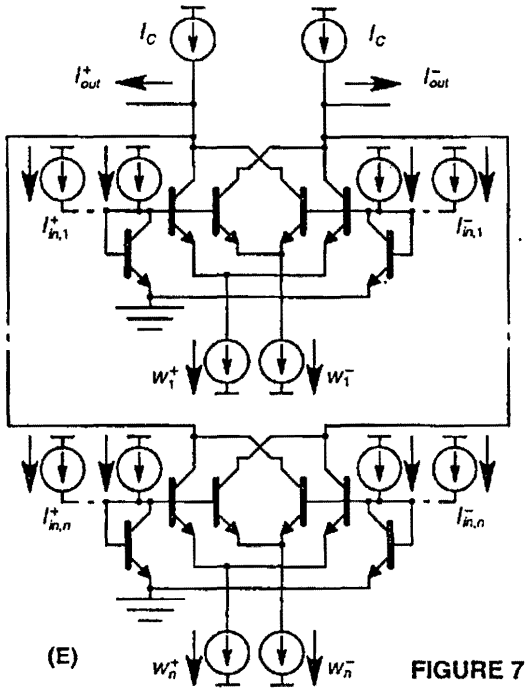
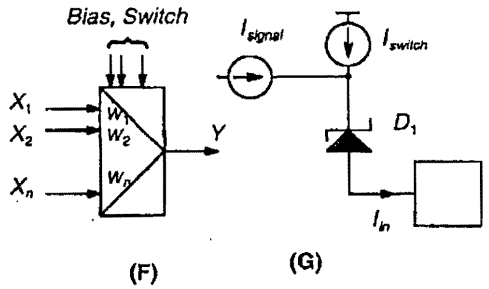


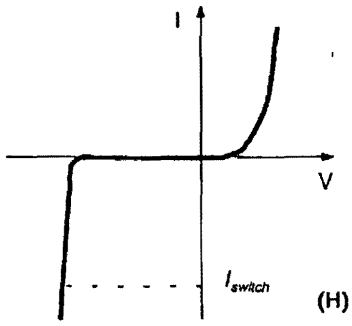
FIGURE 7 (continued).



(E)

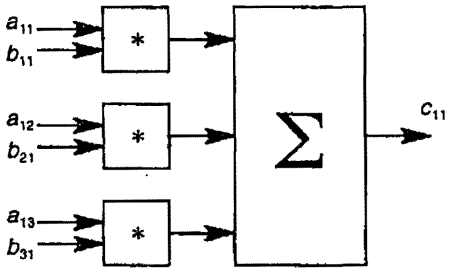


(F) (G)

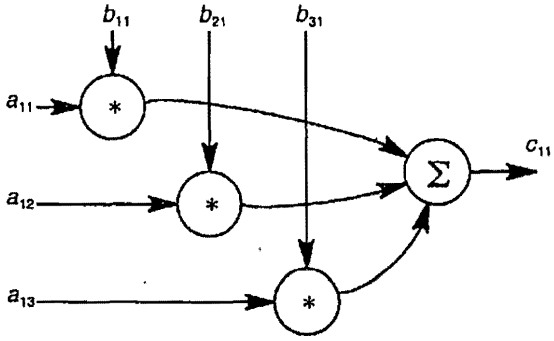


(H)

FIGURE 7 (continued).

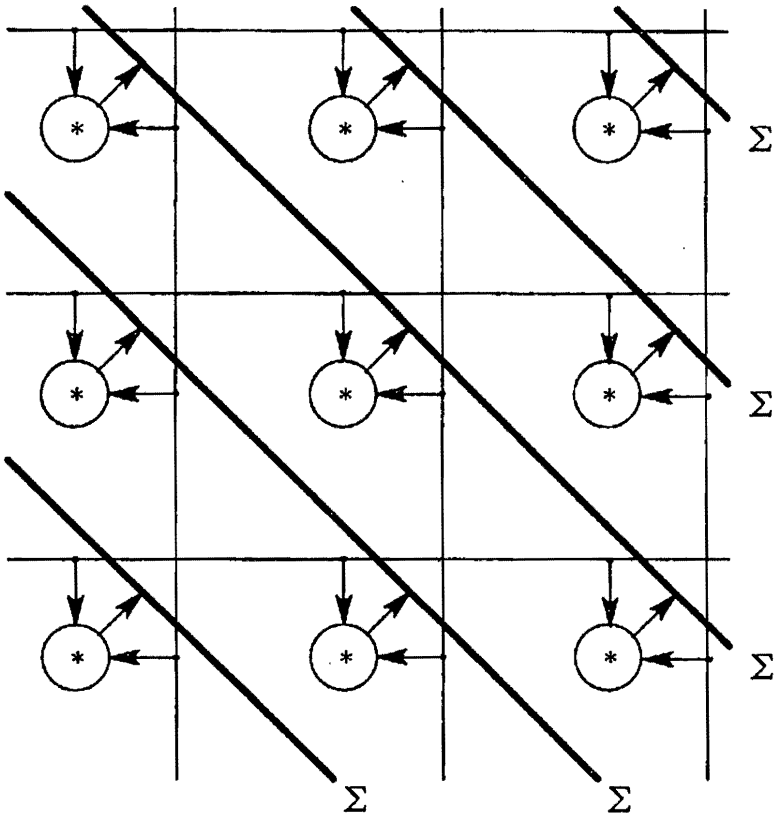


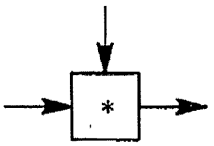
(A)



(B)

FIGURE 8.





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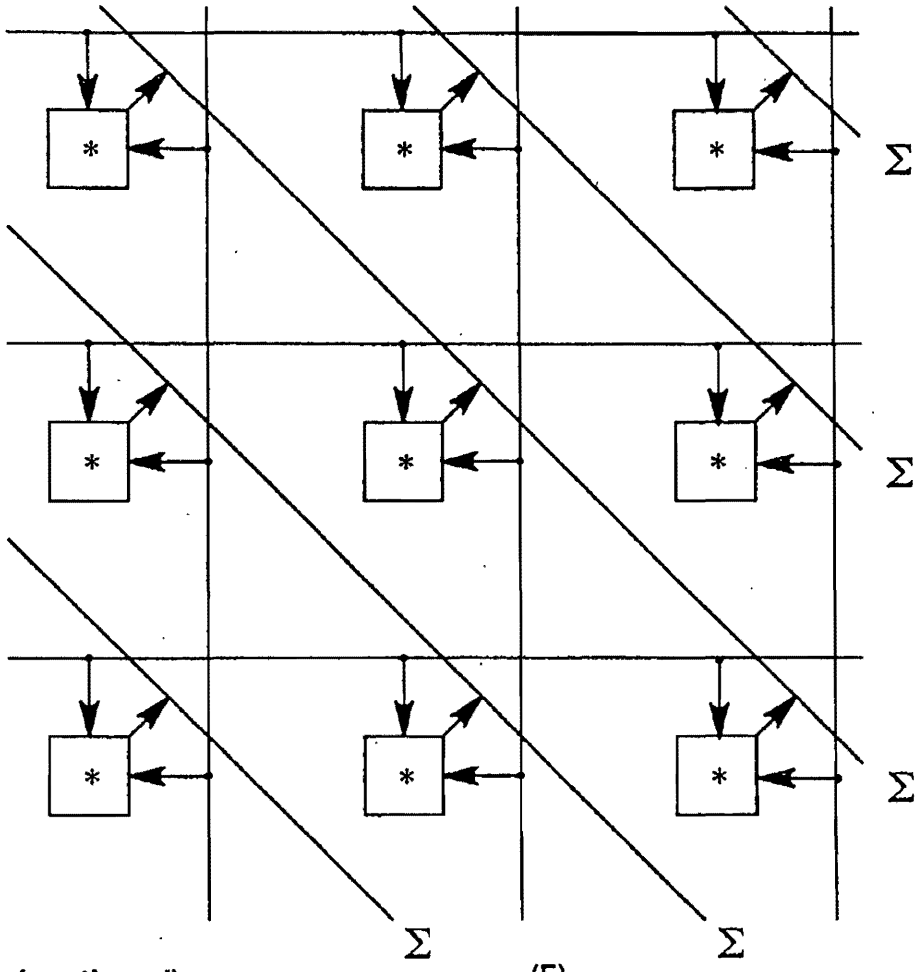


FIGURE 8. (continued).

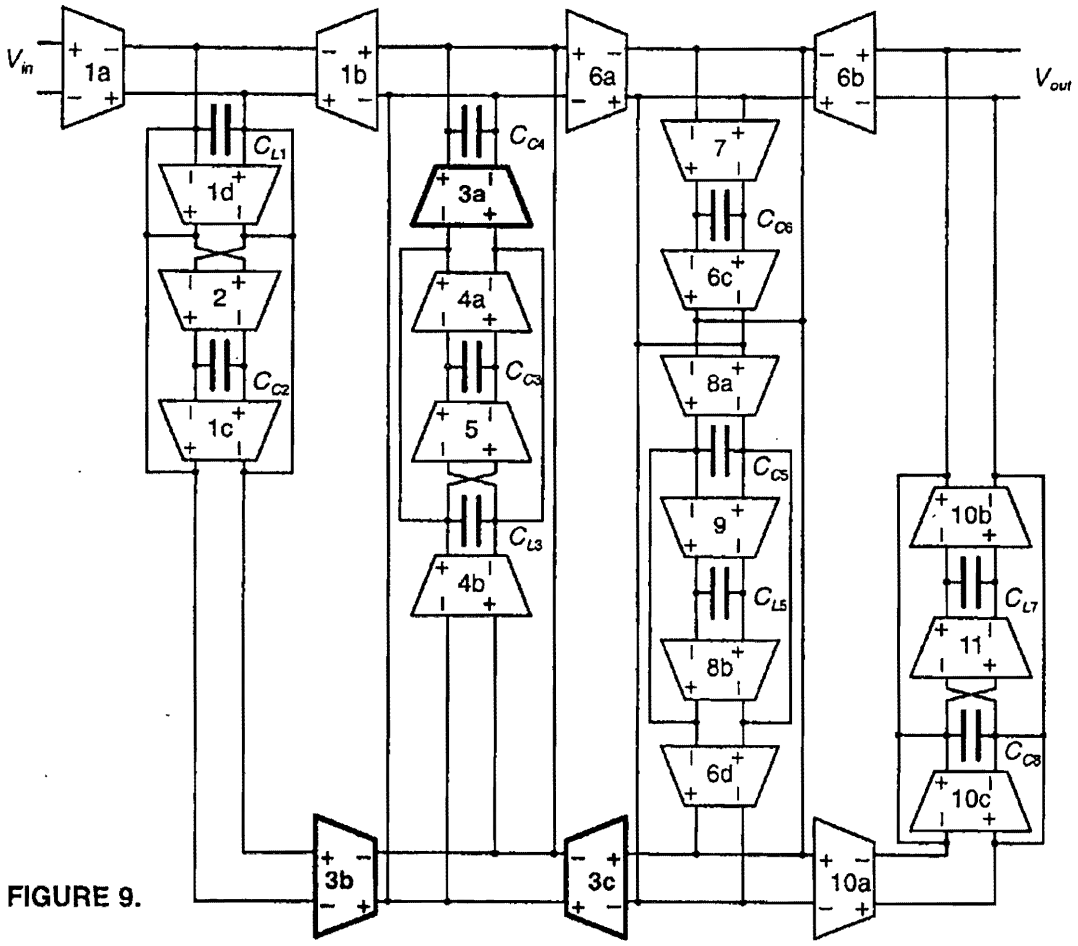


FIGURE 9.

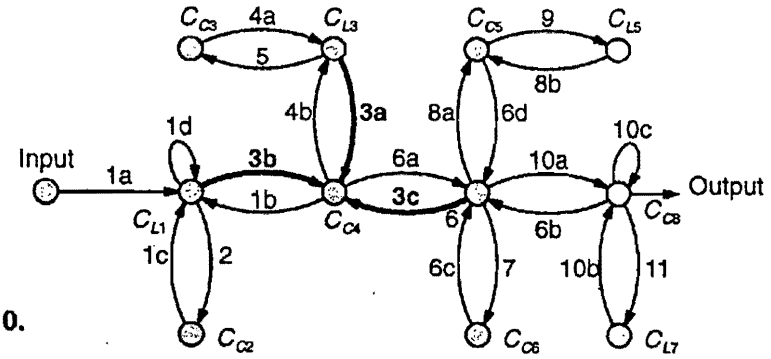


FIGURE 10.

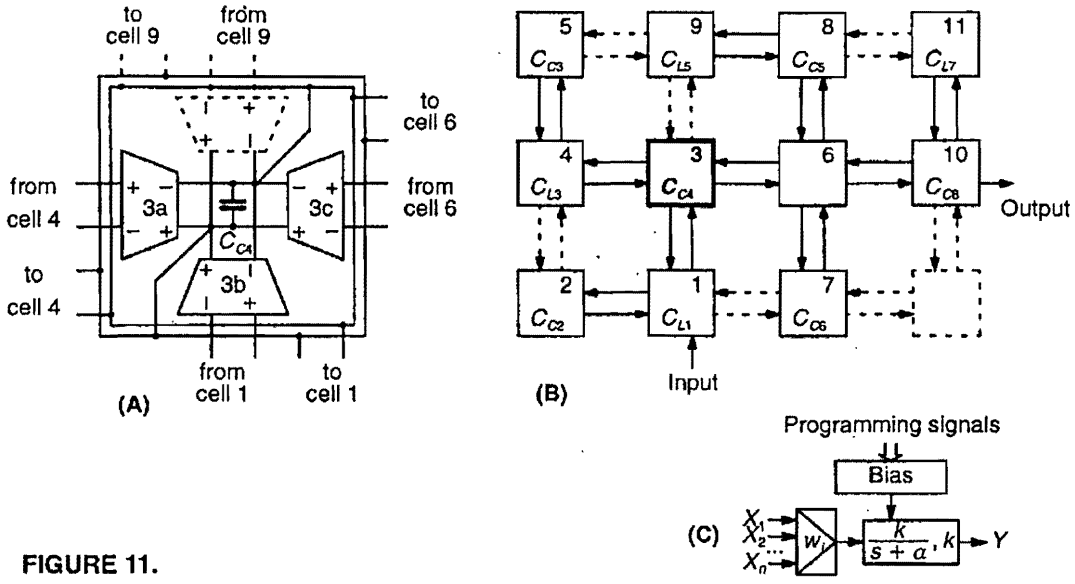


FIGURE 11.

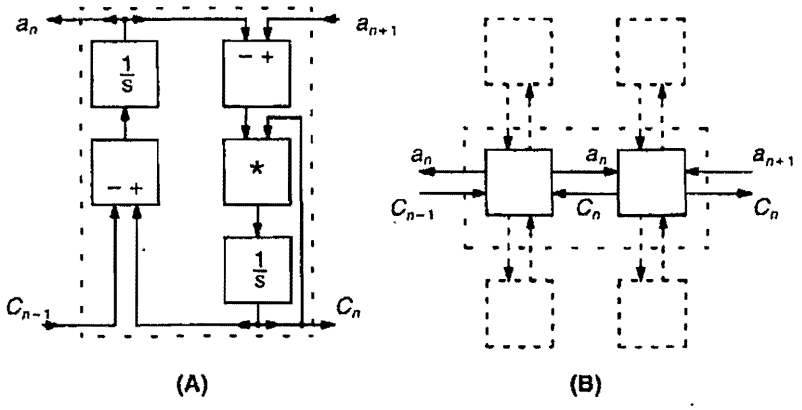


FIGURE 12.

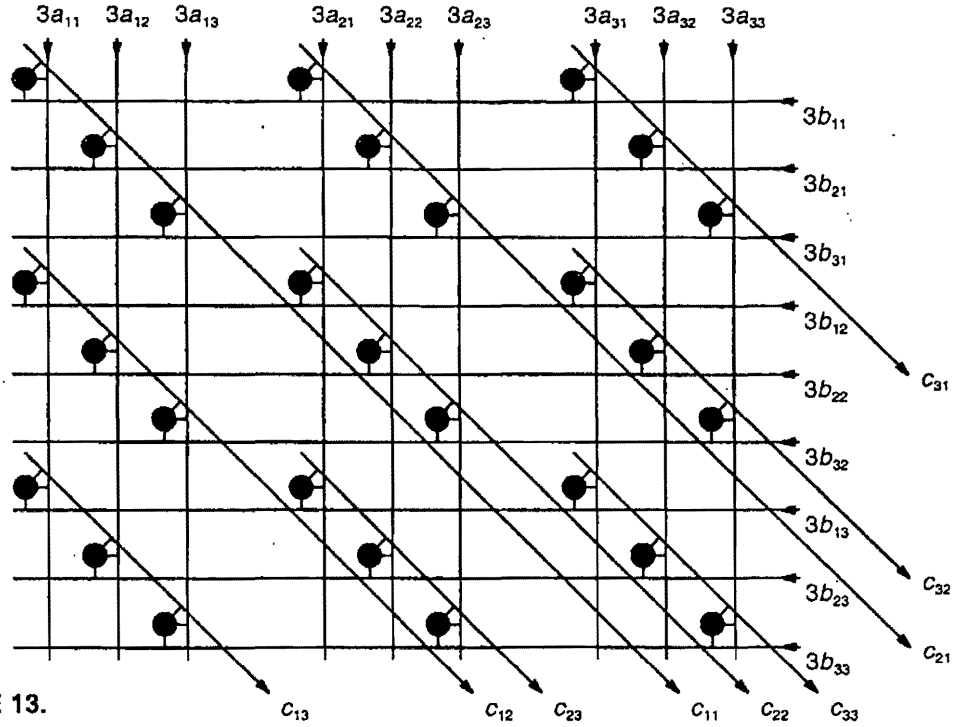


FIGURE 13.

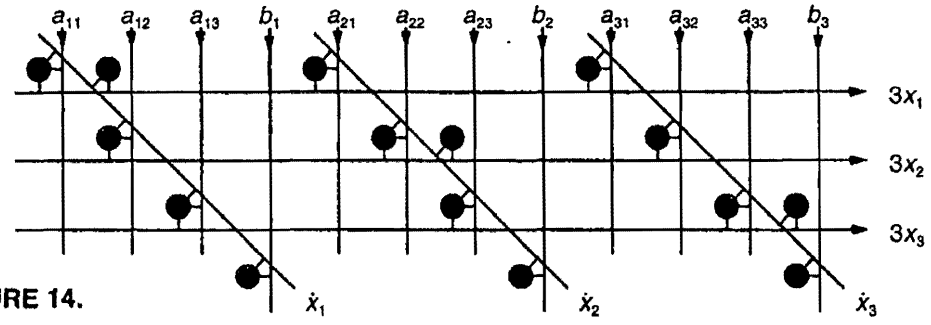
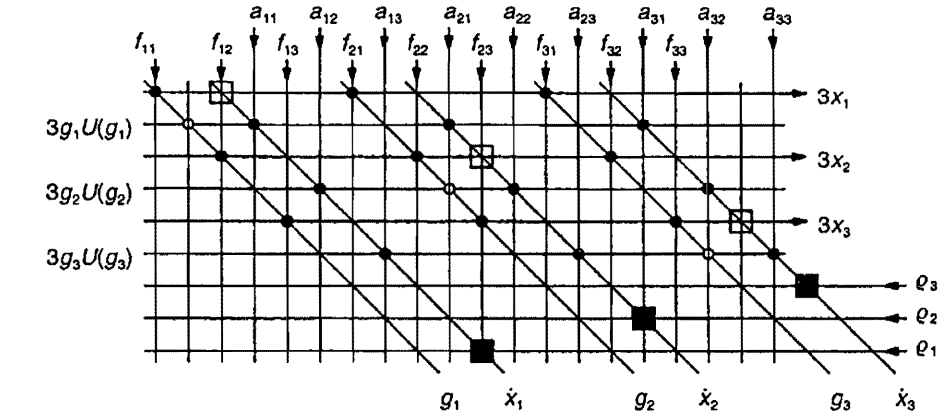


FIGURE 14.



Legend:

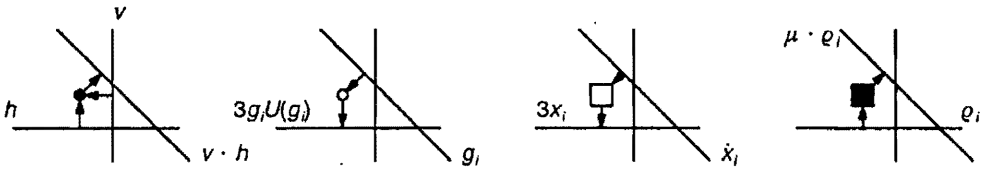


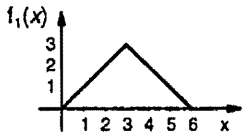
FIGURE 15.

$a \oplus b$	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

(A)

$a \otimes b$	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

(B)



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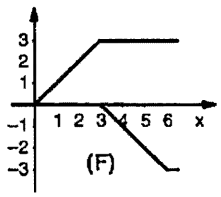
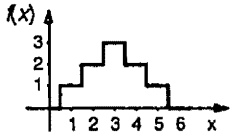


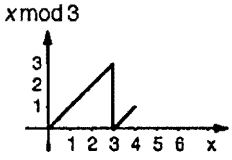
(F)

$f(a+b)$	0	1	2	3
0	0	1	2	3
1	1	2	3	2
2	2	3	2	1
3	3	2	1	0

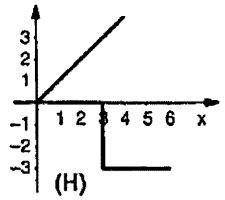
(C)



(D)

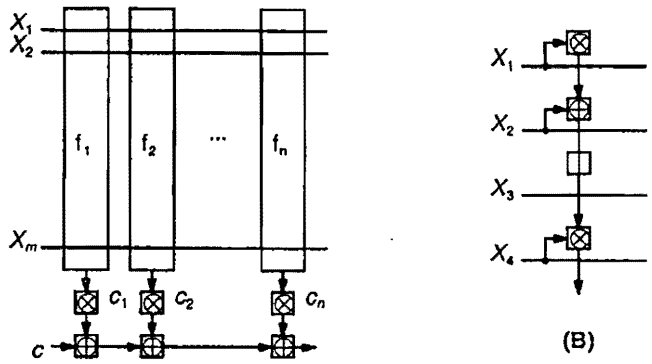


(G)



(H)

FIGURE 16.



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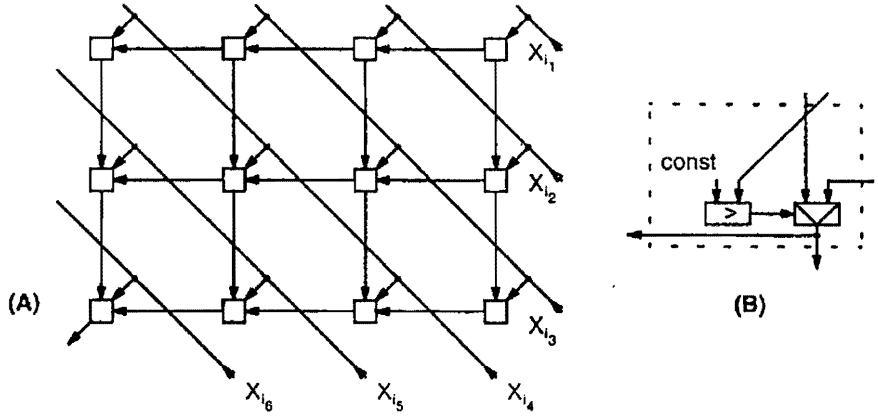

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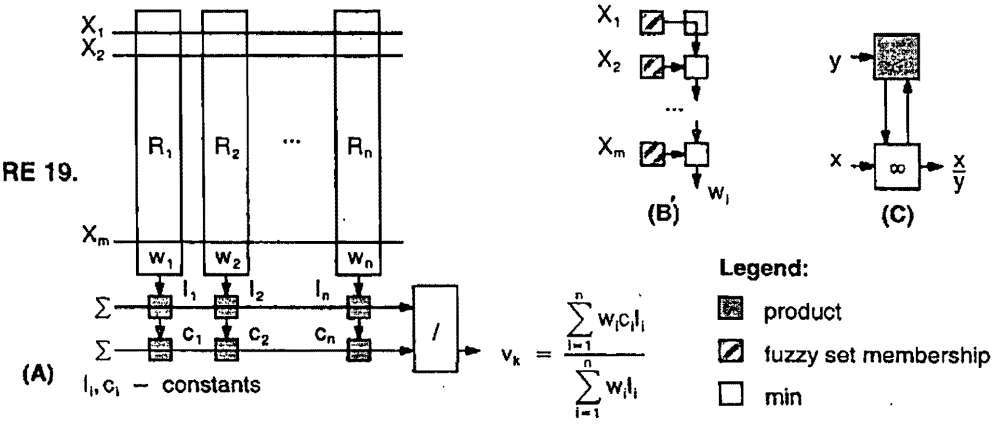
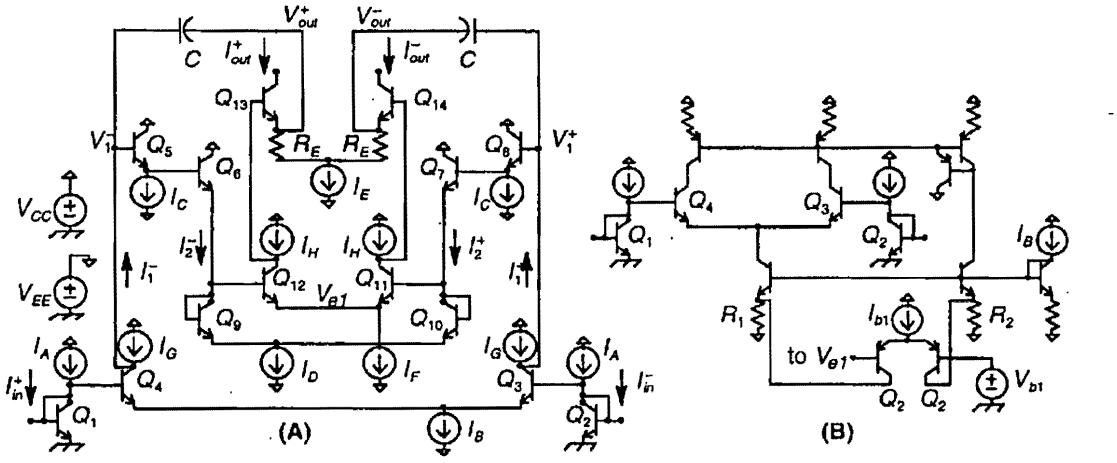


$$v_k = \frac{\sum_{i=1}^{n} w_i c_i l_i}{\sum_{i=1}^{n} w_i l_i}$$

FIGURE 19.



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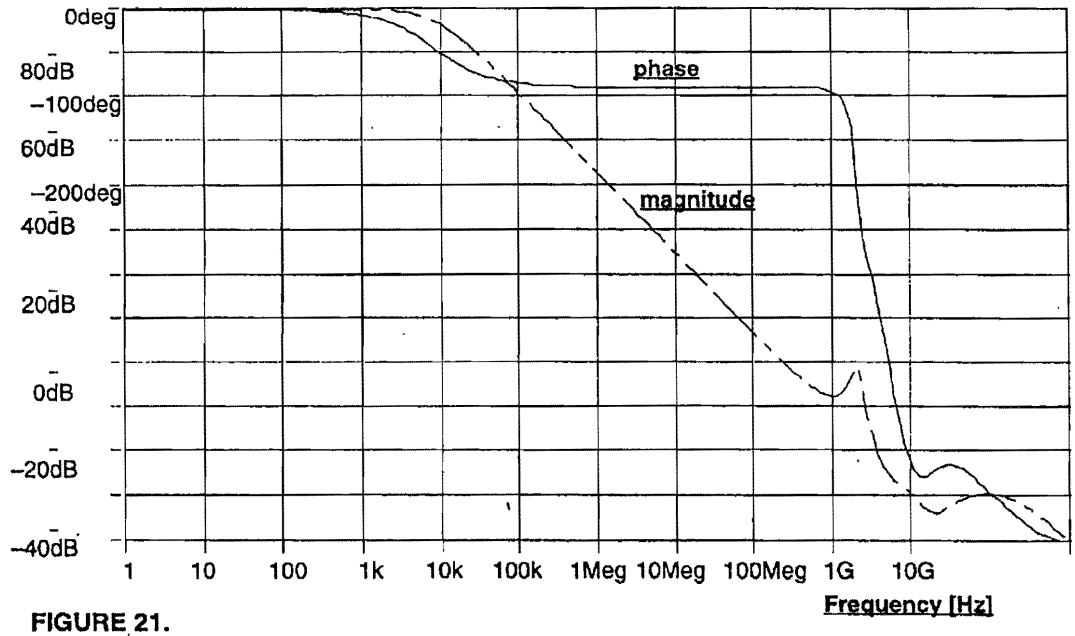

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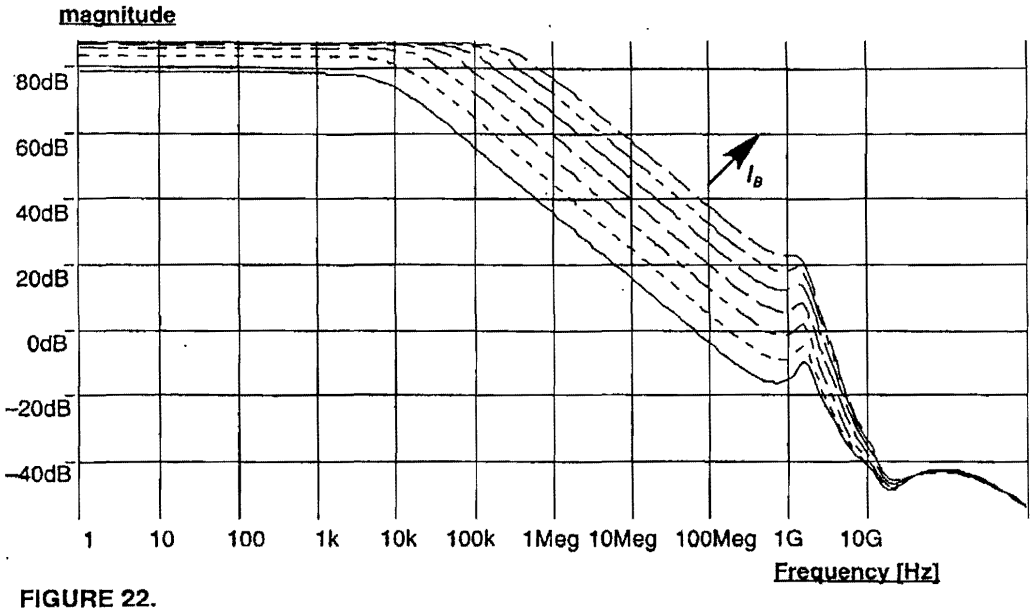

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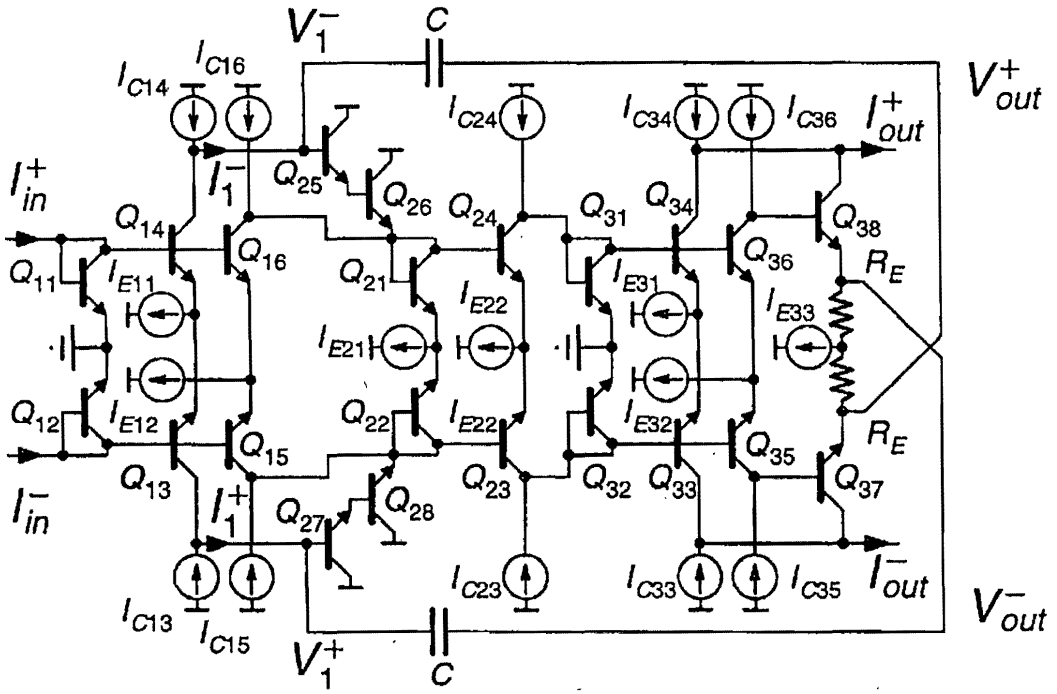

FIGURE 23.

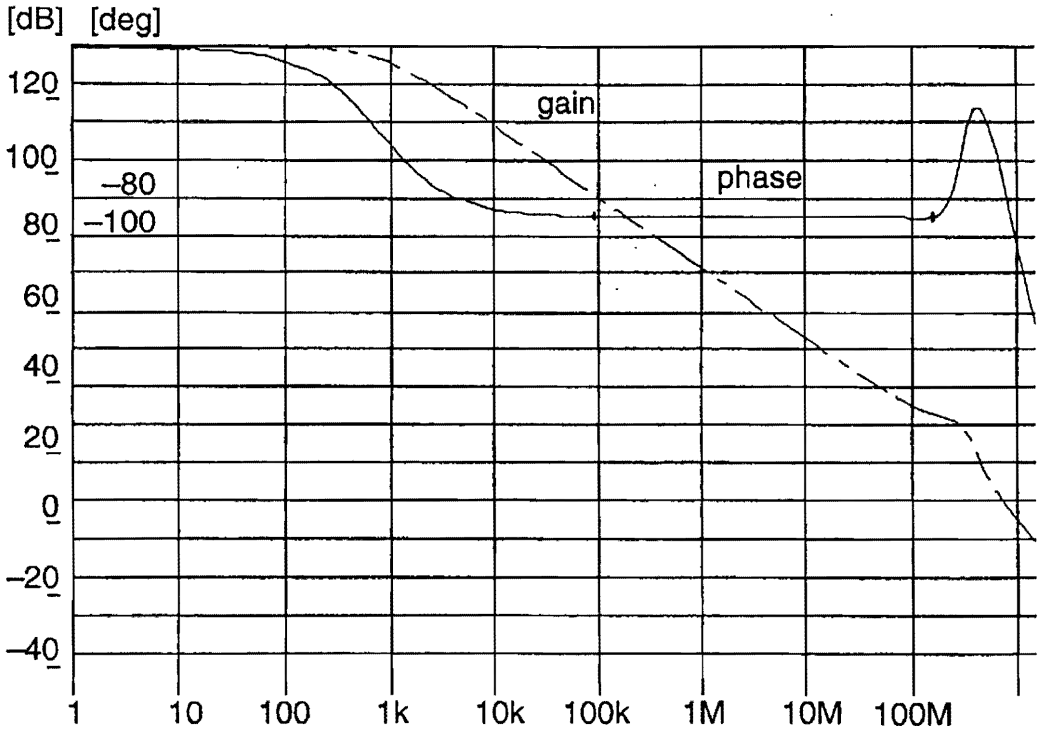
[dB]
[deg]
120
100
80
60
40
20
0
-20
-40
-80
-100
gain
phase
1
10
100
1k
10k
100k
1M
10M
100M
Frequency [Hz]

FIGURE 24.

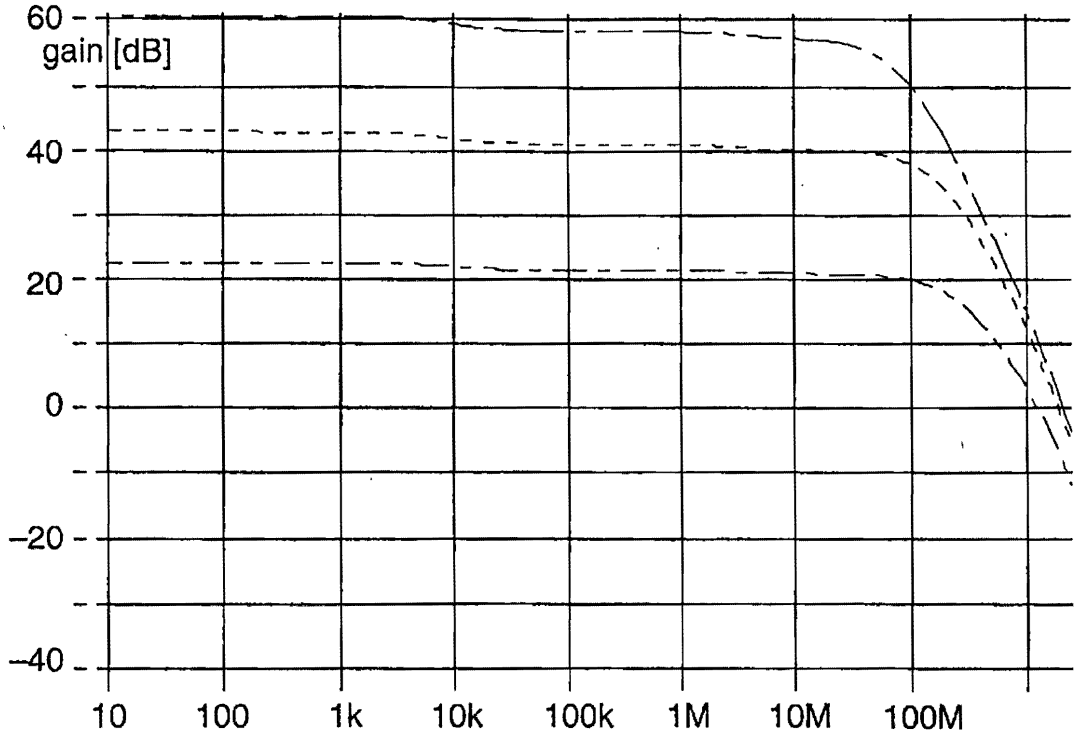
60
gain [dB]
40
20
0
–20
–40
10
100
1k
10k
100k
1M
10M
100M
Frequency [Hz]

FIGURE 25.

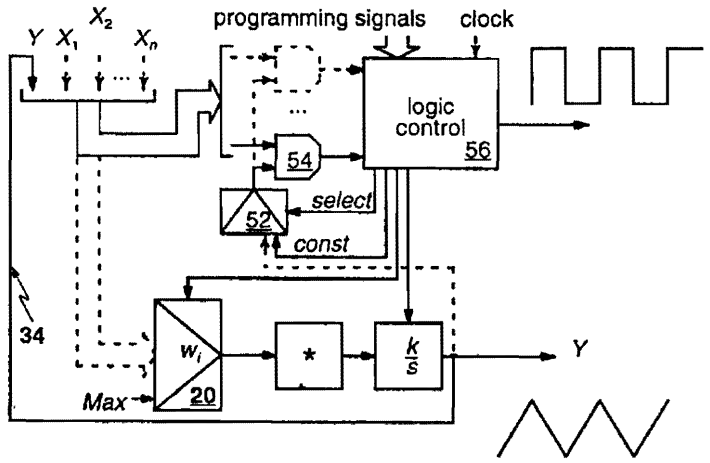

FIGURE 26.

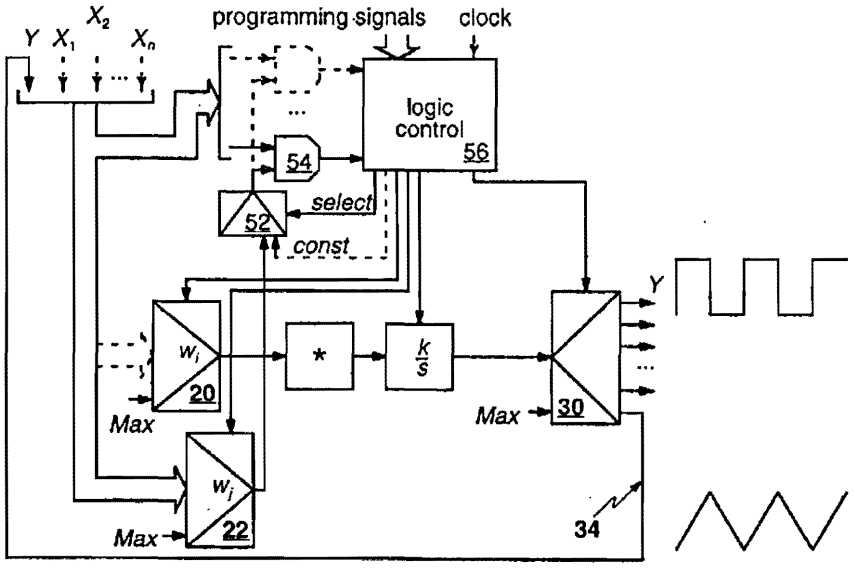

FIGURE 27.

PROGRAMMABLE ANALOG ARRAY CIRCUIT

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a continuation-in-part of U.S. patent application Ser. No. 08/173,414 filed Dec. 23, 1993 now abandoned.

TECHNICAL FIELD OF THE INVENTION

This invention provides a programmable analog or mixed analog/digital circuit. More particularly, this invention provides a circuit architecture that is flexible for a programmable electronic hardware device or for an analog circuit whose input and output signals are analog or multi-valued in nature, and primarily continuous in time. This invention further provides a design for a current-mode integrator and sample-and-hold circuit, based upon Miller effect.

BACKGROUND OF THE INVENTION

Analog circuits are a necessary component of many modern signal and information processing systems. The "real world" is primarily analog in nature and almost every digital system that interacts with the "real world" must have analog-to-digital and digital-to-analog interfaces. Analog circuits are continuous in time with a continuous signal, whereas circuits such as CNN's (cellular neural networks) operate in a discrete time (d-t) mode. In several applications (e.g., anti-aliasing and smoothing (reconstruction) filters, or pulse-slimming circuits in computer disk memories), analog circuits cannot be replaced by digital circuits either for reasons of speed or for analog's unique ability to work in a continuous-time (c-t) mode. Digital information can be processed in analog form to gain speed (e.g., image processing requiring many multiplications). Moreover, even if a digital solution exists, an analog solution may be smaller, require less power, generate less noise and be more reliable (e.g., a smaller number of elements to go wrong). Analog circuits have been avoided in the art since analog designs are often more difficult than digital and have often had to consider low-level circuit interactions, and since analog system have suffered dependencies, such as on temperature, fabrication run and time. Therefore, there is a need in the art for a novel analog architecture that is flexible and can even accommodate mixed signal (digital and analog) system designs.

In some signal processing applications, analog circuits are preferred over digital circuits for their relative simplicity. In the field of analog c-t circuit design and architecture, full programmability (i.e., one of parameters and structure) has not been achieved commercially. Previous analog programmable circuit designs have favored flexibility (universality) of the architecture (i.e., pattern of connections in a programmable device) rather than performance. There is a wide spectrum of architectures of analog circuits which do not comprise any particular "pattern" or architecture of interconnection schemes. Therefore, programmable devices for analog circuits in the art feature long global signal interconnection schemes. The common characteristic of long global interconnection schemes of current programmable analog circuits is that they achieve greater flexibility of interconnection patterns, sometimes allowing every cell in a programmable device to be connected with every other cell. Such an approach favors flexibility of a programmable device, but jeopardizes high frequency performance. This also causes parasitic problems associated with long signal lines and crosstalk between long analog lines and digital lines on the same chip increasing noise and stability problems in analog and mixed signal (analog and digital) designs. Such problems are most acute in a high-frequency (HF) domain where analog circuits have their most desired applications.

There are many published circuits for multiple-valued logic and continuous or fuzzy logic circuits, there are no programmable devices for multiple-valued, continuous or fuzzy logic circuits. Therefore, there is a need in the art for a field-programmable analog array (FPAA) that can be used for implementation of a wide class of multi-valued logic, fuzzy logic and other continuous logic circuits.

Programmable hardware devices for digital circuits include such devices as programmable logic arrays (PLAs), programmable logic devices (PLDs), and field-programmable gate arrays (FPGAs). "Programmability" in this context means the ability of a hardware device to change its configuration and function in response to some kind of programming information, in order to perform a required task. This programmability is distinct from "software" programmability (such as the programmability of a microprocessor), which directs a sequence of steps to be performed but does not necessarily produce changes in the hardware characteristics of the device. Programmable hardware devices for discrete-time signal processing are limited to relatively low frequencies when used to process analog signals. Such circuits also cannot substitute for continuous-time circuits in applications such as anti-aliasing. Programmable hardware devices for analog, continuous-time signal processing, however, are not commercially available.

Programmability opens up new ways of designing and building circuits for a given domain. For example, as soon as a technical means for realizing digital programmable circuits became available, new techniques of implementing digital circuits emerged. However, techniques for attaining programmability of digital circuits are inappropriate for analog circuits, for at least two reasons. First, to attain flexibility for creating various topologies of digital circuits realized by means of programmable devices, long global signal interconnections are often employed. These long interconnections introduce signal delays and phase errors that are tolerable, although undesired, in digital circuits. Such delays and errors would be fatal to analog circuits. Secondly, digital programmability techniques usually employ some kind of electronic switches. All realizations of such switches of practical interest for integrated circuits (ICs) suffer from considerable parasitics, namely substantial resistance in the "on" state, and parasitic capacitances. The net result of these parasitics is the introduction of phase errors in transmitted signals, an effect similar to that caused by long signal interconnections. Again, whereas these errors are tolerable in digital circuits, they are fatal for analog circuits. The foregoing problems are most severe for the fastest (i.e., HF analog circuits) which are the most desirable ones.

The development of various analog integrated circuits (ICs) has led analog IC design to the point where it is desirable and advantageous to have universal analog and mixed-signal programmable circuits. Multi-valued and fuzzy-logic circuits are often based on the same or similar circuit techniques as analog circuits and analog programmable circuits could be used for their implementation.

Circuits can generally operate in current-mode or in voltage mode. The majority of circuit designs operate in a voltage mode. Advantages of current-mode operations of circuits are speed and immunity or resistance to noise.

Low frequency (e.g., acoustic range) analog programmable circuits can be built easily in MOS subthreshold technology. In this technology processing elements (i.e., cells of the programmable device) can work in subthreshold mode, whereas the switches (for programming the programmable device) can be realized as MOS transistors working in inversion mode. This approach would be suitable for low-frequency applications only. Consequently, even though a field-programmable analog array is theoretically possible, the realization of such a programmable device would have a most limited scope of applications, limited to artificial neural networks (ANN's) and low-frequency signal processing. One advantage of analog c-t processing is speed. Slower applications can be adequately served by digital or switched-capacitor (SC) circuits, where programmability is easier to achieve. Fully programmable SC circuits are commercially available.

The nature of cellular neural networks (CNNs) is different than that of fully programmable circuits. CNNs are massively parallel collections of information processing units called cells, having memory (state information). CNNs are capable of attaining one of many equilibrium states due to a complex pattern of cell interactions through exclusively local interconnections. A CNN is either in one equilibrium state, when state and output information in cells is constant over time, and represents a solution of a certain problem, or is in the process of changing state and output information of its cells in order to attain one of its equilibria. Such a process of changing state and output information of its cells is actually the computation performed by a CNN. It is initiated by providing initial state information and input information.

CNNs are not programmable devices in any sense. CNNs are, instead, special processors dedicated to solving certain information processing problems. Although the computation of a CNN can be performed continuously in time and in signal domain, the state and output information of CNN cells is not meaningful until the CNN reaches an equilibrium. Thus, a CNN is, de facto, a d-t processor, since meaningful output information is available only at time intervals when it remains in an equilibrium. Moreover, since the set of equilibria in a CNN is discrete, the output information of a CNN is also in discrete form.

Field-programmable gate arrays for digital circuits are available from a few sources. However, field-programmable gate arrays for analog circuits are not available. Field-programmable gate arrays for analog circuits have to overcome several problems such as bandwidth, linearity, signal-to-noise ratio, frequency response and the like. One approach has been attempted by Lee and Gulak ("Field-Programmable Analogue Array Based on Mosfet Transconductors" *Electronics Lett.* 28:28–29, 1992). Lee and Gulak attempted to achieve full programmability by having connections between configurable analog blocks realized using MOSFET transconductors and controlling conductance by varying the gate voltage defined by a multivalued memory system.

In another attempt using a digital system, Furtek (U.S. Pat. No. 4,918,440) describes exclusively digital programmable logic cells and arrays of such cells having an integrated logic and communications structure which emphasizes local communication.

Therefore, there is a need in the art for a programmable analog device suitable for high frequency analog operation, a family of general-purpose mixed (analog and digital) signal-processing cells, and a method of creating architectures, i.e., patterns of interconnections of collections of such cells, suitable for a wide class of analog, multi-valued and fuzzy logic, circuit applications.

An integrator is a basic building block for many analog signal processing systems, such as filters (Schaumann et al., "Design of Analog Filters" Prentice Hall, Englewood Cliffs, N.Y., 1990). The main requirement for an integrator design are low excess phase, high linearity (frequency range and slew rate), high DC gain, and availability of electronic tuning. In one OTA-C (operational transconductance amplifier and capacitor) technique of filter implementation, integrators are realized by loading a transconductor (OTA) with a capacitor. The output signal is taken directly from the capacitor and the circuit has high output impedance, inherited from the OTA. To alleviate the loading effect of other OTAs typically connected to the integrator's output, techniques, such as parasitic absorption (Schaumann et al. infra.) have been developed. Another solution is a voltage-to-voltage, or current-to-voltage integrator, based on the Miller effect. A voltage-output Miller integrator was followed by an OTA ((Haigh, "Continuous-time and Switched Capacitor Monolithic Filters Based on LCR Filter Stimulation using Current and Charge Variables" in Analogue IC Design, the current-mode approach, ed. Toumazou et al., Peter Peregrinus Ltd. 1990) to realize a current-to-current integrator. In this arrangement, the linearity of the integrator depends on the linearity of the OTA. However, there is a need in the art for an integrator with current input and current output, and good linearity and high speed. This invention was also made to address this need.

The full speed potential of analog circuits can be utilized by c-t Field-Programmable Analog Arrays (FPAAs). However, there are two problems that first need to be overcome. The first is to provide an architecture (interconnection scheme) complex enough to be programmable, yet contributing little interference, crosstalk and noise problems that are major problems in analog designs. The present invention overcomes this first problem. The second problem is designing a flexible, universal unit of a FPAA without explicit use of electronic switches in the signal path to attain programmed functionality. Switch parasitics, such as finite on resistance and stray capacitances, lead to frequency performance degradation. The present invention overcomes this second problem as well.

SUMMARY OF THE INVENTION

This invention provides a programmable analog or mixed (i.e., analog/digital) circuit, called a FPAA. More particularly, this invention provides a circuit architecture that is flexible for a programmable electronic hardware device or for a predominantly analog circuit whose input and output signals are analog or multi-valued in nature, and primarily continuous in time.

The invention provides a circuit architecture scheme for designing an analog circuit or a mixed analog/digital circuit device comprising an array of analog signal processing cells wherein each cell comprises an analog signal processing portion and a control circuit, wherein the array of cells are connected by a plurality of local signal interconnects. Preferably, the signals carried by the local signal interconnects are in a current-mode.

The invention further provides a programmable analog device comprising an array of programmable analog signal processing cells, wherein each analog signal processing cell comprises an analog signal processing portion and a control circuit, wherein the control circuit controls the operation of the analog signal processing portion and may also take part

in auxiliary information processing, wherein the cells in the array are interconnected by one or a plurality of local signal interconnections to form the programmable analog device. A signal interconnection is considered local in that the number of cells connected to the signal interconnection does not change as the number of cells in the programmable analog device varies. For example, if the number of programmable analog signal processing cells is doubled to provide for a larger programmable device, the number of cells connected to then-existing local signal interconnections does not change. Preferably, the programmable analog device further comprises one or a plurality of global signal interconnections for connecting various cells of the array together. A signal interconnection is considered global in that the number of programmable analog signal processing cells connected by a global signal interconnection changes as the number of cells in the array varies.

The invention further provides a method for making the inventive programmable device comprising, (a) deriving a circuit interconnection labeled multi-graph from a schematic diagram of a representative circuit within a class of circuits, (b) adding nodes and edges to the circuit interconnection labeled multi-graph according to a predetermined strategy to create a superset of the circuit interconnection labeled multi-graph, (c) grouping together one or more selected edges and nodes from the graph to form an interconnection labeled multi-graph to impart functionality to the cells within the programmable device, and (d) deriving a floor plan of the programmable device, whereby the total length of signal interconnections in the floor plan is minimized.

The invention further provides a method for mapping a particular circuit onto a programmable device to form a programmed device, comprising (a) providing a programmable device comprising an array of signal processing cells connected by local and global signal interconnections, wherein the array of signal processing cells is described by an interconnection labeled multi-graph defined by a particular number and arrangement of signal interconnections to each cell, (b) deriving a circuit labeled multi-graph of electrical connections from a schematic diagram of the particular circuit, and (c) embedding the circuit labeled multi-graph into the interconnection labeled multi-graph by selectively programming cells or signal interconnections in the device. Preferably, the embedding step may comprise selecting signal interconnections in the programmable device, according to a predetermined strategy to minimize overall length of interconnections within the programmed device (as defined by its floor plan), wherein the predetermined strategy comprises a one-to-one mapping of the circuit labeled multi-graph into the interconnection labeled multi-graph, whereby the total length of interconnections is minimized.

The invention further provides a method for programming an electronic subcircuit, comprising (a) providing a programmable electronic subcircuit comprising a signal path and one or more transistors controlling signal flow through the signal path, wherein each transistor comprises multiple operating points that determine the signal propagation characteristics of the transistor, (b) providing a source of control current or voltage to part of the transistor, with the source being removed from the signal path, and (c) changing the operating point of the transistor by changing the control current or voltage sufficiently to switch the transistor on and off and thereby turn on and off the signal flow through the signal path of the circuit. Preferably, the electronic subcircuit comprises a two-transistor current mirror using bipolar or field-effect transistors. Preferably, the electronic subcircuit further comprises a differential pair of transistors. The analog subcircuit comprises a part of the analog signal processing portion of the cell. The analog subcircuit adds switching capability without introducing additional switching devices into the signal path of the circuit.

There is further provided a programmable current-mode integrator/amplifier having a circuit based on the Miller effect, wherein the current-mode integrator/amplifier is capable of integrating or amplifying a current-mode signal input into a current-mode signal output. The current-mode integrator comprises a current buffer, having an input signal and an output signal, an operational transconductance amplifier (OTA) input stage, having an input signal connected to the output of the current buffer and an output signal, connected to a current amplifier, wherein the current amplifier comprises an additional voltage mode output, and a capacitor or a plurality of capacitors connected to the voltage mode output of the current amplifier and to the input of the OTA, whereby a feedback connection typical of the Miller integrator is created. The current-mode output of the amplifier is proportional to its voltage-mode output signal, which represents the integral of the input current-mode signal. In this feedback arrangement, the OTA works with a very small input voltage swing (provided that the gain in the loop is high) which provides for high linearity of the circuit. The circuit also has a high DC gain (up to 90 dB or more). In one implementation, the current-mode integrator comprises a highly linear, no feedback, current path having a Gilbert amplifier cell and a voltage feedback path with capacitors, realizing integration.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A–C illustrate exemplary block diagrams of cells and local and global signal interconnections in field-programmable analog and mixed signal array devices. This illustrates a FPAA based upon a regular, square array of current-mode processing cells, interconnected on two levels, local and global. Each cell is connected to its four nearest neighbors by a two-way current-mode signal interconnection and is able to receive four different signals produced by those neighbors, whether all of them or just selected ones. FIG. 1A shows the local signal interconnections of the FPAA, FIG. 1B shows the global signal interconnections of the FPAA, FIG. 1C shows non-planar signal interconnections of the FPAA, and FIG. 1D shows hexagonal signal interconnections of the FPAA. The cell's own output signals are programmably distributed to the same four neighbors (FIG. 1A). The global interconnection pattern is superimposed on the local one, but it is shown separately to avoid clutter (FIG. 1B). Each cell can broadcast its output signals to any of the four global lines to which the cell is connected (possibly to more than one line at a time). The presented schemes of interconnections are planar. To allow realization of non-planar circuits in the FPAA, a non-planar structure of signal interconnections can be used. Such a structure can be easily obtained from any planar structure (such as that shown in FIGS. 1A and 1B) by adding non-planar connections (such as two diagonal connections shown in FIG. 1C).

FIG. 2 illustrates an exemplary functional block diagram of a cell within the array, showing an analog signal processing portion and a control circuit. The design of the cell is a result of a compromise between the circuit's power and its simplicity. The illustrated cell processes current-mode differential signals. The analog processing portion provides required operations on signals processed by the cell. The control circuitry determines the operation of analog processing portion: the operations performed by the analog blocks

and the parameters of analog blocks based on the feedback received from the analog processing portion and the programming signals.

FIGS. 3A–H show exemplary DC transfer characteristics of the cell which are achieved by combining (summing) the characteristics of two clipping (saturation) blocks. Some of those characteristics are necessary for multi-valued logic (MVL) and fuzzy logic applications such as triangle or trapezoidal ones shown in FIGS. 3B, C.

FIG. 4 shows an elementary building block of the cell based on the Gilbert current amplifier cell. In its simplest form the circuit comprises only transistors Q_1–Q_4 and current source I_B^+. Current sources I_A represent the circuits input signals.

FIG. 5 is an exemplary functional block diagram of the control circuit of the cell shown in FIG. 2. The control block directs the operation of the analog processing circuits of the cell and enhances functionality of the cell, enabling nonlinear operations such as a min/max follower, signal-controlled generation of programmed waveforms, signal-to-frequency conversion (VCO), and MVL operations. FIG. 5B shows a current-mode comparator as a part of a current-mode cell of the FPAA. It comprises two differential current-mode inputs $I_A=I_A^+-I_A^-$ and $I_B=I_B^+-I_B^-$, two constant current sources I_C, and a current mirror Q_5, Q_6. It produces a single-ended voltage signal V_{out}, representing logical value of the condition $I_A>I_B$.

FIGS. 6A and B shows a current-mode integrator and sample-and-hold circuit.

FIGS. 7A, B show a programmable current mirror and a programmable differential pair. FIG. 7C shows a differential, current-mode analog demultiplexer with independent tuning of output weights, which contains a multi-output version of the circuit shown in FIG. 7B. FIG. 7D shows its block diagram symbol of the demultiplexer shown in FIG. 7C. The signals are depicted by single lines, even though they are preferably differential. FIG. 7E shows a schematic of a differential, current-mode analog signal multiplexer/summer with independent tuning of input weights. Additional summation (without independent tuning) is realized by connecting a number of signals to each input. FIG. 7F shows the block diagram symbol of the multiplexer/summer shown in FIG. 7E. The signals are depicted by single lines, even though they are differential. FIG. 7G shows a schematic and FIG. 7H explains the operation of a Zener diode D1 (FIG. 7G). The Zener diode is connected in the path of current signal in reverse direction, i.e., when the current I switch is off, the diode does not pass the signal. When the I switch is turned on, the diode enters the breakdown region (FIG. 7H), provided that the reverse voltage forced across the diode by the current source is sufficiently high, and the signal can now pass through the diode. Due to very small incremental resistance of the diode in the breakdown region this makes an almost ideal switch.

FIGS. 8A–E illustrate an example of constructing an FPAA for a matrix product tracking circuit. A circuit representing a class of circuits of interest is selected and its schematic diagram obtained. FIG. 8A shows the result of these steps. Next, a circuit labeled multi-graph for the matrix product tracking circuit is derived, as shown in FIG. 8B. The multi-graph is then generalized to a superset, as shown in FIG. 8C. In the current-mode, summing is performed on signal lines. Global signal interconnections are selected because if the matrices are scaled up, the number of nodes connected to the summing interconnections grows, so does the number of nodes connected to the input signal interconnections. The contents of the individual cells are then determined, as shown in FIG. 8D. Connections between the cells are made according to the graph of FIG. 8C, yielding a floor plan shown in FIG. 8E.

FIG. 9 illustrates an electrical schematic of an eight-order, elliptic band-pass filter realized as an OTA-C (operational transconductance amplifier and capacitor) ladder. This is a voltage-mode circuit, since each OTA takes a voltage signal as input, and although it produces a current signal, this current is always turned into voltage, either by the integrating operation of a capacitor. Each signal created in this circuit is going to be fed to some OTA (which can accept only voltage-mode signals as input) or connected to the output terminals of the circuit, which also require a voltage-mode signal. This circuit, and other voltage-mode circuits, can be realized in an equivalent current-mode form in the structure of the inventive device, if current-mode implementation of the device is preferred. The circuit preferably employs current sources I_{switch} in the fashion shown in FIGS. 7B, C, which are not shown to avoid clutter.

FIG. 10 shows a labeled multi-graph of the ladder filter of FIG. 9. It demonstrates that the filter has a topology comprising only local interconnections.

FIG. 11A shows how the elements of the filter of FIG. 9 can be grouped into "cells".

FIG. 11B shows how 11 "cells" of FIG. 11A, interconnected only locally, comprise the entire filter. This figure also demonstrates the topology of the realization of the filter in the inventive FPAA structure. Dashed lines represent inactive cells and signal interconnections. FIG. 11C shows the functionality of the FPAA cell in example 7.

FIG. 12A shows a block diagram of a single cell of an analog rank filter and FIG. 12B shows how it can be mapped into the structure of the inventive FPAA. Two cells of the FPAA are necessary to implement one cell of the rank filter. The left cell in FIG. 12B implements the left-hand part of the rank filter cell, and the right cell the right-hand part. One of ordinary skill in the art can identify functions performed by each cell in FIG. 12B. A required number of such cells can be placed next to each other to realize a rank filter circuit of arbitrary size.

FIG. 13 shows the structure of a matrix product tracking circuit implemented in the structure of the inventive device realized in current-mode. It takes two time-varying matrices $A(t)=[a_{ij}]$ and $B(t)=[b_{ij}]$, both 3×3, and creates their product $C(t)=A(t)\cdot B(t)$ (a factor of 3 is required to account for the distribution of each input signal to 3 cells; alternatively the gain k (FIG. 2) of each cell could be increased by the same factor). The circuit can be generalized for any rectangular conformable matrices. Each element $c_{ij}(t)$ of the product matrix is produced by a "local" group of cells along a diagonal global signal line. However, to distribute the input signals and to collect the results signals, global connections are necessary. Each diagonal output line is used to sum elementary products $a_{ij}\cdot b_{jk}$, $j=1, \ldots, n$, comprising the product element c_{ik}.

FIG. 14 illustrates a circuit solving a system of 3 algebraic equations with 3 unknowns $x_1(t), \ldots, x_3(t)$. The global connections in this circuit carry internal feedback signals, although the distance traveled by these signals is small.

FIG. 15 is a continuous-time circuit for solving a linear programming problem: given a set of constraints $g(t)=F(t)\cdot x(t)=[g_1(t), \ldots, g_m(t)]'\leqq 0$ (the inequality is supposed to hold for every element of the vector; F is a rectangular matrix of constraints coefficients, g is a vector representing individual constraints), minimize the objective function

$\epsilon(x_1, \ldots, x_n)=\epsilon \cdot x=\epsilon_1 x_1+ \ldots +\epsilon_n x_n$, where $\epsilon=[\epsilon_1, \ldots, \epsilon_n]$. Application of the method of steepest descent leads to a system of equations $\dot{x}=-\mu \cdot \epsilon'-2a \cdot A \cdot diag(g) \cdot U(g)$, where U(g) denotes the step function, diag(g) denotes a diagonal matrix with elements of vector g on the main diagonal, and μ and a are constants ($\mu \rightarrow 0$, $a \rightarrow \infty$). This system can be solved by the circuit shown in FIG. **18**.

FIGS. **16**A and B show the tables for addition and multiplication in Galois field of four elements ($GF(2^2)$), respectively. Each of these operations can be realized by the FPAA cells; only two of the cell's inputs are used at a time. Addition can be realized as $a \oplus b=f(a+b)$ for $a \neq b$ (FIGS. **16**C and D), and $a \oplus b=0$ otherwise. The condition $a=b$ can be detected by the control block of a cell. Instead of function $f(x)$ (FIG. **16**D) a smooth function $f_1(x)$ (FIG. **16**E) can be used. This function can be realized by adding two characteristics of the clipping blocks shown in FIG. **16**F. If the function of the form shown in FIG. **16**D is required, it can be realized by providing more clipping blocks in the cell. Multiplication $a \otimes b$ in ($GF(2^2)$) (FIG. **16**B) can be realized as $a \otimes b=((a+b-2) \bmod 3)+1$ for $a \neq 0$ and $b \neq 0$, and $a \otimes b=0$ otherwise. Mod 3 operation can be realized, as shown in FIGS. **16**G, by adding two characteristics of the clipping blocks shown in FIG. **16**H.

FIG. **17**A shows a block diagram of a structure realizing an orthogonal expansion of a 4-valued function of input variables $X_1, X_2, \ldots, X_m$, over $GF(2^2)$. Each column realizes one orthogonal function over $GF(2^2)$. Multiplied by a constant from $GF(2^2)$, this function is added to the other orthogonal functions. All operations are in $GF(2^2)$. FIG. **17**B shows an example of realization of one of the functions f_i.

FIG. **18**A shows a structure for implementations based upon generalized Shannon expansion of MVL functions. Some input variables need to be connected to more than one diagonal line. More general forms of the same kind are possible, based upon other operators than > used for separation, for instance even vs. odd parity, based on matrix orthogonality, which is a generalization of an approach for two-valued functions. FIG. **18**B shows functions performed by each cell.

FIG. **19** shows an example of a fuzzy controller. FIG. **19**A shows the implementation of a controller with m input variables and n fuzzy inference rules. FIG. **19**B shows details of each rule implementation. Fuzzy membership function is implemented as a trapezoidal transfer function of the kind shown in FIG. **3**C. Activation values w_i are multiplied by centroid values of the fuzzy rules consequents c_i, and their areas I_i, yielding two sums computed on two horizontal global lines. The final expression for the defuzzified output variable v_k is produced by a two-quadrant divider shown in FIG. **19**C.

FIG. **20** shows an electrical schematic of an integrator. Transistors Q_1+Q_4 form a Gilbert "type A cell", working as the input buffer with current sources I_A biasing the input pair Q_1, Q_2. This circuit is characterized by excellent linearity and high bandwidth (simulated −3 dB bandwidth for unity gain is better than 6 GHz). Transistors Q_5+Q_8 realize the OTA input stage. The current-mode amplifier, again based on the Gilbert "type A cell" is realized by Q_9+Q_{12}. Loaded by current sources I_H, it provides high voltage gain. Its output voltage signal is connected to the emitter follower Q_{13}, Q_{14}, providing an output current, I_{out}, and output voltage connected to the capacitors.

FIG. **21** shows the frequency response of the integrator of FIG. **20**.

FIG. **22** shows tuning the gain of the integrator of FIG. **20**.

FIG. **23** shows an implementation of a programmable current-mode amplifier/integrator, based on the inventive current-mode Miller integrator design (the block diagram of the amplifier/integrator is shown in FIGS. **6**A, B).

FIG. **24** shows the frequency response of the circuit of FIG. **23** in integrating mode and FIG. **25** shows its frequency response in amplifying mode. It is important that programming of the function of the circuit is attained without any switches in the signal path.

FIG. **26** demonstrates an application of a single cell of the inventive device as a digitally-controlled oscillator. The const value is downloaded to the logic control block via the programming signals connection.

FIG. **27** illustrates another variation as a signal-controlled oscillator. It is based on using one of the input signals X_1, n . . . , X_n (or a mathematical function thereof, see Table 2) instead of const to be compared against the output of the integrator. In this case, one of the input multiplexer/summers (e.g., 22) is used to derive the desired signal to be used for comparison in place of const.

DETAILED DESCRIPTION OF THE INVENTION

As used herein, the following terms have the following meanings:

Analog signal (continuous signal) is a signal that can assume any value in a certain interval. Each value of the signal in such interval conveys useful information. All other types of signals are special cases of an analog signal.

Bipolar device is a bipolar transistor or diode.

Bipolar signal is a signal that can assume positive, as well as negative values; two-directional signal.

Continuous-time (c-t) signal is a signal which conveys useful information in every instance of time.

Current mode signal is an electric signal which is represented by a current in a circuit branch, or a mathematical function of a number of currents (such as a difference of two currents).

Digital signal is a binary (two-valued) signal.

Discrete-time (d-t) signal is a signal that conveys useful information (is defined) only at certain predetermined periods of time or points in time. At all other times the signal values do not necessarily convey useful information (the signal is undefined). Discrete-time signal may be associated with some kind of a clock signal, or a system of clock signals, and the time periods (points in time) when the signal is defined are sometimes referred to as clock ticks in which case it is a synchronous signal. If there is no clock signal, and the time periods when the signal is defined are determined in another way (e.g., as a sequence of events), the signal is called asynchronous.

Discrete signal (multi-valued signal) is a signal which can possibly assume any value from a certain interval, but only a finite number of such values (called levels) convey meaningful information. Depending on the particular purpose of the signal, values of the signal other than the levels are assumed to convey information of one of the neighboring levels, or to convey undefined (illegal) information. Multi-valued signal can have two levels in particular, in which case it is called a binary signal.

Embedding of a labeled multi-graph into another labeled multi-graph

1. a process of assigning groups of nodes and edges of a first graph to the groups of nodes and edges of a second

graph, such that a number of nodes and edges of the first graph is assigned to a number of nodes and edges of the second graph.

2. a result of such process.

Floor plan is a general diagram showing location of circuit blocks or elements in space (or on a plane).

Global connections. A cells is considered globally connected in that the number of cells connected to a given cell by programmable analog signal connections connected to the cell changes when the number of cells in the structure varies.

Local connections. A cell is considered locally connected in that the number of cells connected to a given cell by programmable analog signal connections connected to the cell does not change as the number of cells in the structure varies.

Labeled multi-graph is a generalization of a graph, having edges incident with two or more nodes, and both edges and nodes having symbols assigned to them (those symbols are called labels).

Line (signal line) is the same as signal interconnection.

Mapping of a labeled multi-graph into another labeled multi-graph: an embedding where for each node and each edge of the first graph there is assigned exactly one edge and node, respectively, in the second graph, and the nodes and edges assigned to each other in the two graphs have matching labels.

Minimum embedding is an embedding of a circuit labeled multi-graph into an interconnection graph which does not lead to using cells as "wires" or "repeaters" i.e., cells programmed to merely transmit information (cells realizing only identity operation).

One-time programmability is one that can be applied only once.

Other Electron Devices mean electron devices having two, three, or more terminals, and displaying (a) linear or (b) nonlinear relationship(s) between electrical quantities such as voltage, current and charge, on those terminals, whereby the linear or nonlinear relationship is required to achieve amplifying, rectifying or similar operation, such as the operation of a transistor or a diode.

Port means a single entry point for the signal (input port), or an output point for the signal (output port). Since signals can be transmitted on a plurality of wires (e.g. pairs of wires), it is more convenient to talk about ports than about wires.

Programmability means an ability of a hardware device to perform a function or a composition of functions according to programming information, originating in the outside of the device. Programmability can be of software kind or of hardware kind. Software programmability does not necessarily involve changes in device's hardware characteristic. Hardware programmability involves such changes. Hardware programmability can be of two kinds: (i) tunability, which normally does not involve changes in the structure (configuration) of the device (structure of the signal path for signals processed by the device), also called parameter programmability, and (ii) structure programmability, involving changes in the structure (configuration) of the device (signal path for signals processed by the device). Finally, full programmability is programmability combining tunability and structure programmability. The term "reconfigurability" is used in literature to denote structure programmability.

Programmable circuit (device) is (1) a circuit (hardware device) exhibiting any kind of hardware programmability, or (2) a circuit (hardware device) exhibiting full programmability.

Repeated programmability is one that can be applied many times.

Voltage mode signal is an electric signal which is represented by a voltage between circuit nodes, or a mathematical function of a number of voltages (such as a difference of two voltages).

The present invention was made as part of an effort in designing analog programmable circuit architecture suitable for high-speed, high performance fully programmable analog operation. The highest performance can be achieved by reducing the length of signal interconnect lines, if possible, using only local signal interconnects. There is a tradeoff between the complexity of connections of a programmable device (and hence its functionality) and performance. Use of only local signal interconnects limits the class of such programmable analog devices to applications such as ladder continuous-time filters and other circuits. The present invention provides an architecture of a fully field-programmable analog array using primarily local signal interconnect architecture to create complex analog designs without compromising high-performance for the sake of functionality. Global interconnections can be incorporated into the inventive architecture and used only when absolutely necessary.

The control circuit, as used herein, includes, for example, a means for exchanging information to and from the control circuit, a means for storing information, a means for processing information, or a means for communicating with an associated analog processing portion of a cell. With such means, the control circuit is programmed to determine the operation of the analog processing portion of the cell. The analog processing portion of a cell, includes, for example, a means for performing one or more mathematical and other functions, including, but not limited to, weighted summing, multiplication, integration, exponentiation, logarithms, trigonometric functions, and the like.

The essential feature of the inventive device is that the length of the local signal interconnections in the array is minimized. Preferably, the cells of the array are arranged to minimize the length of local signal interconnections required to form the programmed device. Additionally, the total length of unprogrammed local and global signal interconnections is preferably minimized (for a given graph of connections between the cells). This architecture will minimize undesired noise effects and other signal distortions such as phase errors in the device.

The present architecture, described and exemplified herein, is suitable for the realization of a wide class of analog circuits. This specific architecture results from the general premise to use local signal interconnections whenever possible, and global signal interconnections only when absolutely necessary. The design of individual cells, and specific details of the architecture, were determined upon consideration of the perceived applications of the device, i.e., fast dynamic systems and fuzzy and multi-valued logic circuits. Although only continuous time examples are provided herein, the inventive device is capable of discrete-time operation as well.

The inventive device, and particularly, the inventive general purpose field-programmable analog array can be used for the implementation of various analog and logic circuits. We have shown that the realizations of MVL functions based upon orthogonal expansions as well as more general ones based on sets of not necessarily orthogonal functions, lead to regular circuit structures which can easily be mapped to the inventive FPAA. Other circuits, such as ladder filters, have the same property. Therefore, the inventive FPAA is an