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FEA Simulations for Thermal Distributions of Large Scale 3DIC Packages

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ABSTRACT As the market increases for Artificial Intelligence and High-Performance Computing applications, the geometry of 3-Dimensional Integrated Circuit packages becomes more complicated; therefore, predicting the thermal distributions of the structures becomes not only more important but also more challenging. The physics governing the thermal distribution is a 3-dimensional partial differential equation. In order to predict the thermal distributions, various approaches such as the layer modeling method have been invented. While practical, these approaches solve a simplified version of the differential equation placing an inherent limitation on their capabilities which may be improved upon. In this research we solve the actual differential equation using Finite Element Analysis. Finite Element Analysis is known to produce accurate solutions, albeit being computationally intensive, and may take days to run even with a powerful computer, making it impractical for some applications. In this paper, we present case studies of computing the thermal distributions of large scale 3-dimensional integrated circuit models using XSim. We find that XSim's solving capabilities are capable of computing accurate thermal distributions of large-scale models in minutes instead of days. This suggests a new way to compute the thermal distributions rapidly and accurately for large 3-Dimensional Integrated Circuit packages, which may bring potential benefits in research, design and development of 3-Dimensional Integrated Circuit packages.

INDEX TERMS thermal distribution**,** 3DIC, BBCube, FEA simulation

I. INTRODUCTION

Since the advent of computers, the demand for more computational power has endlessly increased. This demand makes the design of Integrated Circuits **(**IC) become progressively more complex. Currently, we are seeing the market adoption of 3-Dimensional Integrated Circuit (3DIC) technologies to develop high-density, high-bandwidth, high-power, and high-performance computation chips. At present, two of the most popular 3DIC technologies in use are Chip-on-Wafer-on-Substrate (CoWoS) and Wafer-on-Wafer (WoW). CoWoS has been used for High Bandwidth Memory (HBM) and chiplets in High Performance Computing (HPC). WoW, on the other hand, is employed for heterogeneous 3D stacking ICs. In the design process of a 3DIC, one of the most important considerations is the thermal analysis or chip temperature versus chip power consumption and heat distribution.

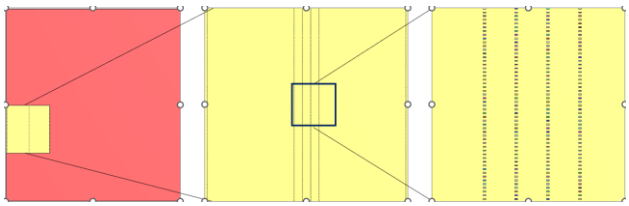
3DIC structures have many variations. The current 3DICs typically possess a few to approximately 16 layers. One common 3DIC structure involves stacking memory wafers on logic wafers. This structure has four advantages: it (1) greatly reduces the signal path length between computation and memory units, (2) dramatically increases the data transmission rate, (3) reduces the transmission power, and (4) provides a natural structure for near-memory computing as presented in [3]-[4]. One such kind of technology is the Bumpless Build Cube (BBCube) [9], [13]. BBCube introduced bumpless Wafer-on-Wafer stacking by applying a method similar to multilevel metallization in the Back-End of Line (BEOL). BBCube can reduce parasitic capacitance of Through-Silicon Vias (TSVs) to 1/20th compared to conventional 3DI using micro-bumps. Compared to High Bandwidth Memory (HBM) based on conventional 3DI using micro-bumps, BBCube's TSVs offer four-times higher bandwidth with only 13 % of the data transmission power compared to conventional 3DI using micro-bumps. But on the other hand, the heat trapped in the BBCube's Dynamic Random Access Memory (DRAM) regions may cause failures, which prevents the BBCube technology from being widely used in production. To solve this problem and understand the heat distribution in the DRAM regions, computer experts have developed approximate thermal layer modeling methods [12], [13]. This thermal layer modeling method can be used to analyze heat distributions for large scale 3DIC packages. However, achieving accurate thermal distributions is

challenging as it only solves a simplified version of the original problem. In this paper we propose to compute the thermal distributions of the BBCube architecture and other large scale 3DIC architectures using the FEA method, known for its precision but deemed too slow for large models. To mitigate the computational intensity of the FEA method for large models, we propose to use XSim, a software tool by DGClaim, Inc. XSim is designed to speed-up FEA computation with some unique technologies for large and complex models. In section II, we simulate the thermal distribution of a full BBCube with 10 nm TSV pitch and 10 layers of DRAM. In section III, we validate the result obtained in section II by hand calculations. In section IV, we validate XSim results with Ansys using four different models. In section V, we study the temperature influence of the Application-Specific Integrated Circuits (ASICs) on the BBCubes. All of these Finite Element Analysis (FEA) simulations took approximately 15 minutes on a consumer laptop computer.

II. THERMAL SIMULATION OF A FULL BBCUBE

In this section we will compute the temperature distribution of a full BBCube model using the FEA method through XSim. The construction of the BBCube model will follow the description provided in [13]. We will simulate the temperature distribution in this section and validate it in the next section.

The dimension of the BBCube is 10 mm by 11 mm. The BBCube model consists of a total of 21 layers. The interposer layer is located at the bottom of the BBCube, while the xPU layer is situated on the top. We model these two layers using silicon (SI) material. The middle nineteen layers correspond to 9 DRAM layers, each of which are modeled using a layer of SI and a layer of SIO2. The thickness of the interposer layer and the xPU layer is 0.03 mm, while the thickness of the SIO2 layers is 0.004 mm and the thickness of the SI layers is 0.006 mm. Our focus lies on a 2.5 mm by 2.75 mm area, within which TSVs with a pitch of 10 nm are created, as discussed in [13]. TSVs are not created outside this area of interest, as they would have a minor influence on the thermal distribution within it. Please refer to Figure 1 below. Figure 1 (a) is the top view of the BBCube with the small yellow rectangle being the area of interest; Figure 1 (b) is the zoom-in view of the area of interest, where we can see the small TSVs as tiny dots. Figure 1 (c) is a further zoom-in view of the area of interest. We model the TSVs using copper as the material.



(a) The whole Model (b) The Area of Interest (c) Closer Look

Figure. 1. Top View of the BBCube Model

The parameters for the materials SI, SIO2 and COPPER are listed in the table below:

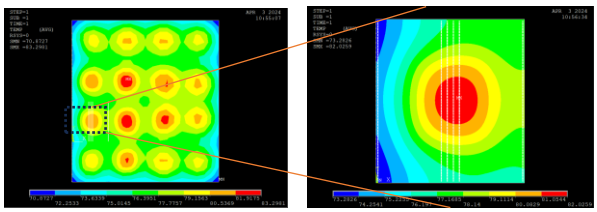
	Density G/CC	Conductivity W/M-K	Specific Heat J/g-°C
COPPER	8.93	401	0.385
SI	2.329	105	0.713
SIO2	2.65	138	0.74

Table 1. Materials Parameters

For heat sources, we divide the interposer layer into 16 equal 2.5 mm by 2.75 mm tiles. We place a heat source of 0.8 W in the middle of each tile, resulting in a total heat source of 12.8 W in the interposer layer. In the xPU layer we distribute a heat source of 45 W uniformly across the entire layer, matching the total heat source in xPU as mentioned in [13]. Similarly, for the DRAM layers, we apply a uniform heat source of 0.4 W.

Now let's define how the BBCube exchanges temperature with its environment. We assume water cooling on the top and 4 side faces with a film coefficient of 13,000 W / m^2-K. Additionally, we assume the bottom of the BBCube is almost insulated with a film coefficient 4 W / m^2-K. Furthermore, we assume the environment temperature to be 40 °C, with the initial temperature of the BBCube set at 26 °C.

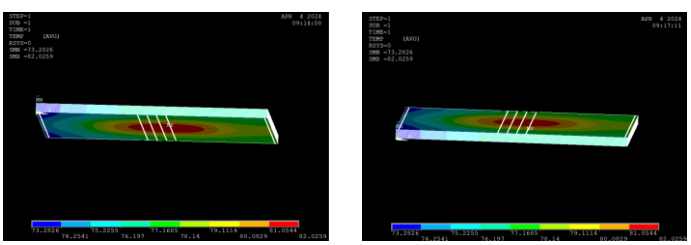
For the BBCube model as described above, we run XSim. The total run-time is about 15 minutes on a consumer laptop computer. The temperature range for the entire BBCube is 70.87 °C to 83.30 °C. The temperature range over the DRAM region of the BBCube is 73.28 °C to 82.03 °C. Figure 2(a) depicts the top view of the memory region of the BBCube, while Figure 2(b) provides a zoom-in view of the region enclosed by the dotted rectangle in Figure 2(a).



(a) Over whole model (b) Over the Area of interest

Figure 2. Heat Distribution

Figure 3 below depicts the temperature distribution of the DRAM layers. Figure 3 (a) shows the bottom of the DRAM layers while Figure 3 (b) shows the top view. The 6 white lines (4 lines near the center and 2 lines near the border) on the top/bottom faces are the TSVs. It can be seen that these TSVs do not affect the temperature distribution much since the convection on the top/side faces is strong and the high conductivity of the copper TSVs is insignificant. Even though the XPU has a strong heat source of 45 W, the temperature generated is dissipated directly through the top face. The temperature generated by the interposer is dissipated through the top face too, because the bottom face is nearly insulated (convection coefficient is 4 comparing with the 13000 of the top face). Since the thickness of the DRAM block is relatively small compared to the BBCube's dimension (0.1 / 10 ratio), the temperature profile (the red oval shape) is carried over from the bottom to top of the DRAM block.



(a) DRAM bottom view (b) DRAM top view

Figure 3. DRAM layers Heat Distribution 3D views

III. VERIFICATION BY HAND CALCULATIONS

In this section we validate the temperature distribution obtained in section II. Through hand calculations, we have obtained the average temperature of 78.635 (°C). This average temperature falls within the temperature range obtained in section II, with a minimum of 70.87 °C and a maximum of 83.298 °C, which is in line with our expectations.

Let the BBCube temperature be 26 °C initially, and the environment temperature be 40 °C. Let A be the average of the thermal distribution of the BBCube at time T. Let D be the temperature difference:

$$D = A - 40 \quad (1)$$

Since the TSVs are small compared with the BBCube, and the parameters for SI and SIO2 are close, we assume the whole BBCube model is SI.

The mass of the BBCube is:

density × volume
= 2.329 g/cc × 15.4 E-9 m^3
= 2.329×15.4 (kg / m^3)
= 3.58667 E-5 (kg)

Energy needed to keep the BBCube 1 °C higher:

1 (°C) × mass × specific heat
= 1 (°C) ×3.58667 × E-5 (kg) × 713 (J/ kg-°C)
= 2.557 E-2 (J) (2)

The total heat source is 58.2 (J/s). If the simulation runs for T seconds, then the total heat generated is:

Total heat generated = 58.2 × T (J) (3)

We compute the heat dissipated through the 6 faces of the BBCube next.

Energy flux q:

q = Film coefficient × D = 13000 × D (W/m^2)

Power Q:

Area × Energy flux
= 115.88 E-6 (m^2) × 1.3 E+4 × D (W /m^2)
= 1.506×D (W)

Energy dissipated in T seconds through the top and 4 side faces:

1.506× D × T (W s) = 1.506× D × T (J) (4)

For the bottom face energy flux q:

Film coefficient × D = 4 (W/m^2-K) × D
= 4 × D (W / m^2)

Area of the bottom face:

Bottom face area: 110 (mm^2)
= 1.10 E-4 (m^2)

Power Q of bottom face:

Area × Energy flux
= 1.1 E-4 (m^2) × 4 × D (W / m^2)
= 4.4 × D E-4 (W)

Energy dissipated in T seconds through the bottom face:

4.4×D E-4 × T (W s)
= 4.4 × D × T E-4 (J). (5)

Combining (4) and (5), we get the total energy dissipated in T seconds through all 6 faces of the BBCube:

1.5064×D×T (J) (6)

By (3) and (6), the total net heat energy gained in the end of T seconds:

$$58.2 \times T - 1.5064 \times D \times T \text{ (J)} \quad (7)$$

This energy gained equals the energy needed to raise the BBCube temperature from 26 °C to the average temperature A, so we have the equation by using (2):

$$58.2 \times T - 1.5064 \times D \times T = (A - 26) \times * 2.557 \text{ e-2 (J)}. \quad (8)$$

When T is large, the thermal distribution will approach the steady state thermal distribution, and therefore the average temperature A will approach a finite number. In equation (8), we divide by T and let T approach infinity to take the limit; the right side of the equation will be 0. Solving for D, we have:

$$D = 58.2/1.5064 \text{ (°C)} = = 38.6352 \text{ (°C)} \quad (9)$$

Combining (1) and (9) we have

$$A = 78.6352 \text{ (°C)} \quad (10)$$

This is the average temperature within the BBCube.

Equation (10) can be rewritten by using named variables as:

$$A = \text{EnvTemp} + \sum \text{CA}*\text{CC (°C)}, \quad (11)$$

where EnvTemp is the environment temperature, which is 40 °C for our case, the summation is over all convection areas and CA is the area of a convection face and CC is the convection coefficient. Formula (11) can be used to compute average temperature, skipping all intermediate steps of calculations.

IV. VERIFICATION WITH ANSYS

In this section, we will validate XSim simulation results with Ansys using four models based on the BBCube architecture. Since Ansys does not perform well with large or complicated models, TSVs will not be included in these models. We will only focus on a quarter of the xy-extent of a whole BBCube and a much smaller number of layers. The first model (Model 1) consists solely of an interposer layer. The second model (Model 2) comprises an interposer layer with an XPU layer on top. The third model (Model 3) integrates one memory layer between the interposer and the XPU layers. Finally, the fourth model (Model 4) features two memory layers between the interposer and the XPU layers.

The xy-extent of the interposer, XPU, and memory layers is 5 mm by 5.5 mm. The thicknesses of the interposer layer, XPU layer, and memory layer are 0.04 mm, 0.026 mm, and 0.02 mm, respectively. The simulation environment remains consistent with the description provided in the previous sections.

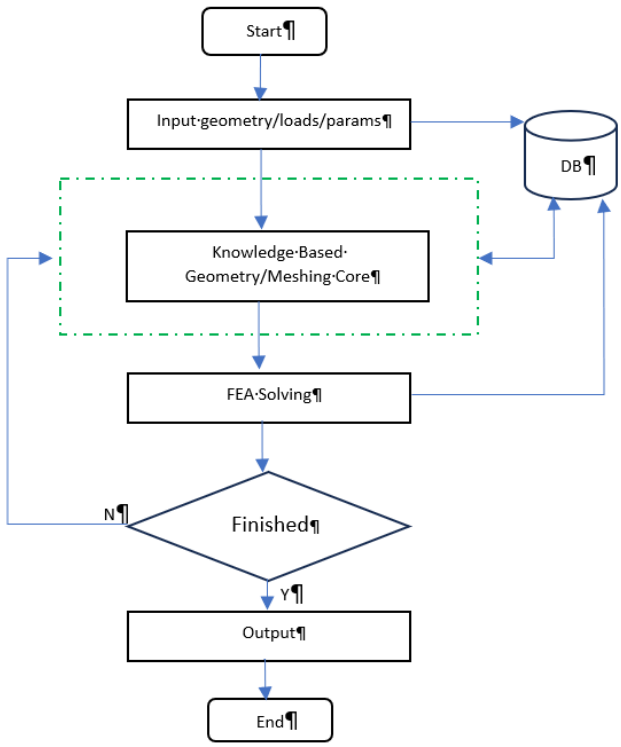
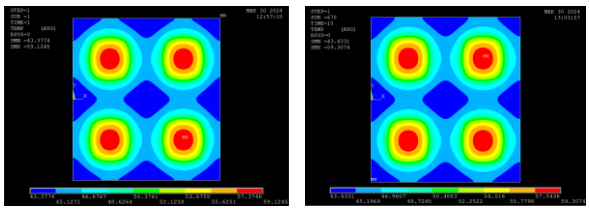


Figure 4. XSim Flow Diagram

XSim is a software tool specially designed for large-scale 3DIC package thermal/mechanical simulations using FEA methods. Its database, geometry, and meshing capabilities are all specialized for 3DIC structures. Figure 5 above shows the top-level flow of XSim. The input to XSim, in scripting form, contains geometry details at several levels, along with simulation environment parameters and loads. The Geometry/Meshing Core generates an initial heat distribution that is as close as possible to the final heat distribution, enabling the solver to converge in fewer iterations. Additionally, the Geometry/Meshing Core endeavors to generate good meshes for the current geometry model based on its knowledge. The FEA Solver can be internal or external. The four models are simulated using the above flow to generate four XSim temperature maps.

For each of the four models, we use Ansys to generate the geometry, mesh them, apply boundary and initial conditions, and generate four Ansys temperature maps. We utilize 10-node tetrahedral elements with a default smart mesh size of 6 for meshing.

Figures 5, 6, 7, and 8 below display the temperature maps for the four models. In each figure, the picture on the left side shows the XSim result, and on the right side is the Ansys result. In these figures, “MT” stands for maximum temperature.



(a) XSim: MT=59.1245 C (b) Ansys: MT=59.3074
Figure 5. Model 1 Heat Distribution

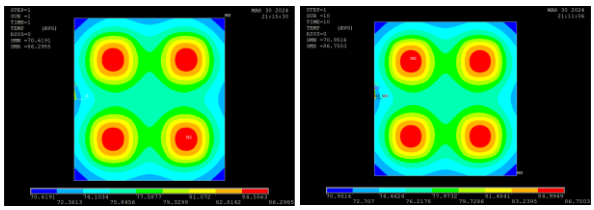


Figure 6. Model 2 Heat Distribution

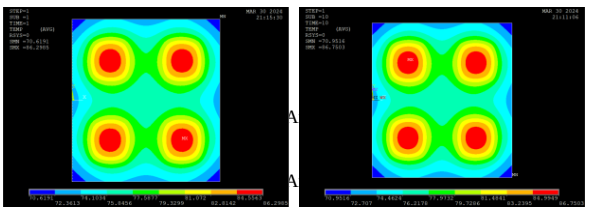


Figure 7. Model 3 Heat Distribution

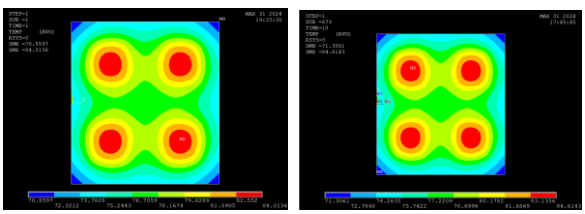


Figure 8. Model 4 Heat Distribution

Table 2 below compares the temperature differences between XSim and Ansys. It shows that the maximum difference is 3.1%, which falls within an acceptable range.

	Model 1 Max Temp	Model 2 Max Temp	Model 3 Max Temp	Model 4 Max Temp
XSim	59.1245	86.2985	85.5528	84.0136
Ansys	59.3074	86.7503	86.977	84.6143
Difference	0.3%	0.5%	1.7%	3.1%

Table 2. Four Models Max Temperature comparison

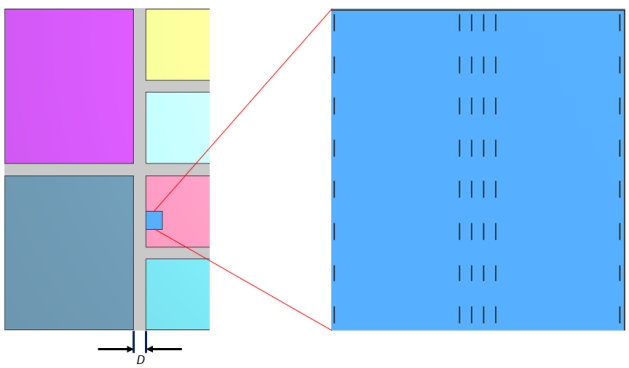
Table 3 shows the difference in run-time between XSim and Ansys (run-time is defined as the FEA solving time, excluding the interactive GUI operation time required to build the model, generate the mesh, and apply the loads). It can be observed that XSim can be several thousand times faster, especially for large models.

	Model 1 run time	Model 2 run time	Model 3 run time	Model 4 run time
XSim	1 s	2 s	3 s	5 s
Ansys	290 s	600 s	4260 s	8460 s
Difference	290 x	300 x	1420 x	1692 x

Table 3. Four Models Simulation Run Time Comparison

V. STUDY OF THE DRAM REGION THERMAL DISTRIBUTION AFFECTED BY NEIGHBOR ASIC DIES

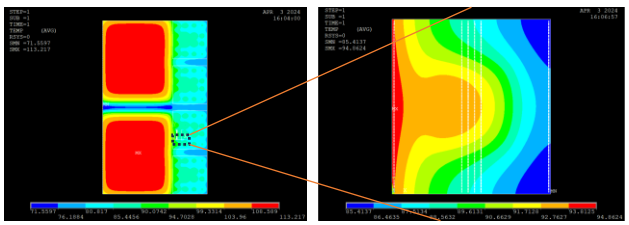
The maximum temperature in the DRAM region cannot be too high to avoid package failure, so understanding thermal distribution over the DRAM region is critical in package designs. In real applications, the thermal distribution in the DRAM region of a BBCube may depend on many parameters. Similar to [12], we will use our proposed approach to study the temperature distribution of a package with 2 ASIC units and 4 BBCubes on one side of the ASIC units (Figure 9). In this section, we will experiment with how the thermal distribution of the DRAM region of a BBCube depends on the parameter *D*, which is the horizontal distance from the logic unit ASIC to the BBCubes (Figure 9). There are 2 ASIC dies with dimensions 20 mm by 24 mm and 4 BBCubes in this package. The heat source for each ASIC unit is 360 W. The BBCubes are as defined in section II.



(a). layout of the package (b). The area of interest

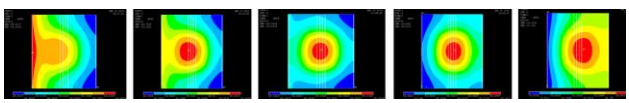
Figure 9.

For the same simulation settings as described in section II, we run XSim for 5 different scenarios with the parameter values *D* =0.2 mm, *D* =0.4 mm, *D* =0.6 mm, *D* =0.8 mm, and *D* =1.0 mm. The running time for each scenario is ~15 minutes on a normal consumer laptop computer. Figure 10 (a) shows the temperature map for the entire package when D=0.2 mm. Figure 10 (b) shows the temperature map for the area of interest, which is a zoom-in view of the small dotted rectangle in Figure 10 (a). Figure 11 shows the max temperature of the interest DRAM region for the 5 parameter *D* values, where *MT* stands for the maximum temperature over the interest region of the DRAM. The parameter *D* values for the 5 images in Figure 11 from left to right are 0.2 mm, 0.4 mm, 0.6 mm, 0.8 mm, and 1. mm. As shown in the Figure, when the ASICs are getting farther away from the BBCubes, the maximum temperature in the DRAM region becomes less affected. The deviation of the maximum temperature is ~8 °C. From Figure 10 (a) we can see that the 2 ASIC units have much higher temperature, therefore the closer the BBCubes are to the ASICs, the higher temperature they will be.



(a). Map of the package (b). Map of interest area

Figure 10.



MT=94.9 °C *MT*=92.0 °C *MT*=90.5 °C *MT*=89.2 °C *MT*=87.2 °C

Figure 11.

We plot the thermal distribution as a function of the distance *D* in Figure 5:

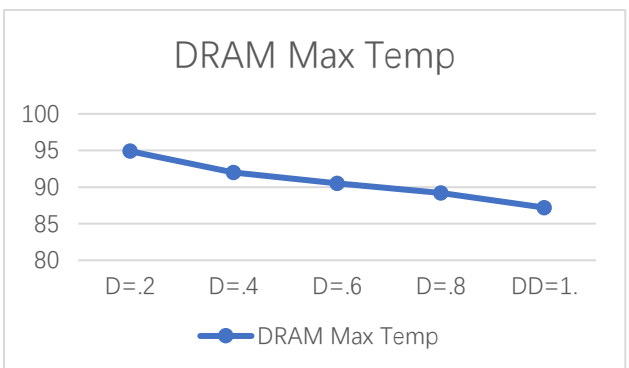


Figure 12. Max DRAM temperature as a function of the distance *D*

VI. CONCLUSION

In this paper, we propose an approach to studying the temperature characteristics of large 3DIC packages. Using XSim, we can apply the FEA approach to quickly and precisely compute the temperature distributions of large 3DIC structures from advanced WoW and CoWoS packaging technologies. The approach was successfully applied to two example models: a BBCube which stacks memory layers and an xPU layer over an interposer layer, and a chiplet package of 2 ASICs and 4 BBCubes. Additionally, a hand-calculated verification was performed to demonstrate the validity of the simulation

results. Ansys simulations were also carried out to validate the XSim results using four models. The proposed approach can be used to study generalized large 3DIC models for their thermal characteristics. An immediate benefit of this research work is that researchers and developers can use this approach to identify and address potential thermal issues early in the design phase. By studying the thermal characteristics of different parameter settings of the relevant models quickly and accurately, researchers and developers can optimize their design to enhance heat dissipation, prevent overheating, reduce defects and improve product reliability in quick iteration cycles. Based on our observation, the simulation can be completed in minutes except for models that are too large to fit into computer memory.

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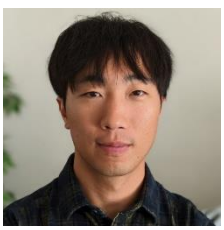

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