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A 40 GHz Power Amplifier Using a Low Cost High Volume 0.15 um Optical Lithography pHEMT Process

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A 40 GHz Power Amplifier Using a Low Cost High Volume
0.15 um Optical Lithography pHEMT Process

by

Kenneth W. Mays

A thesis submitted in partial fulfilment of the
requirements for the degree of

Master of Science
in
Electrical and Computer Engineering

Thesis Committee:
Branimir Pejcinovic, Chair
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2012

Abstract

The demand for higher frequency applications is largely driven by bandwidth. The evolution of circuits in the microwave and millimeter frequency ranges always demands higher performance and lower cost as the technology and specification requirements evolve. Thus the development of new processes addressing higher frequencies and bandwidth requirements is essential to the growth of any semiconductor company participating in these markets.

There exist processes which can perform in the higher frequency design space from a technical perspective. However, a cost effective solution must complement the technical merits for deployment. Thus a new 0.15 μm optical lithography pHEMT process was developed at TriQuint Semiconductor to address this market segment. A 40 GHz power amplifier has been designed to quantify and showcase the capabilities of this new process by leveraging the existing processing knowledge and the implementation of high frequency scalable models.

The three stage power amplifier was designed using the TOM4 scalable depletion mode FET model. The TriQuint TQP15 Design Kit also implements microstrip transmission line models that can be used for evaluating the interconnect lines and matching networks. The process also features substrate vias and the thin film resistor and MIM capacitor models which utilize the capabilities of the BCB process flow. During the design stage we extensively used Agilent ADS program for circuit and EM simulation in order to optimize the

final design. Special attention was paid to proper sizing of devices, developing matching circuits, optimizing transmission lines and power combining.

The final design exhibits good performance in the 40 GHz range using the new TQP15 process. The measured results show a gain of greater than 13 dB under 3 volt drain voltage and a linear output power of greater than 28 dBm at 40 GHz. The 40 GHz power amplifier demonstrates that the new process has successfully leveraged an existing manufacturing infrastructure and has achieved repeatability, high volume manufacturing, and low cost in the millimeter frequency range.

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Chapter 1

Introduction

1.1 Overview

A new 0.15 um optical lithography pseudomorphic high electron mobility transistor (pHEMT) process has been used to fabricate a power amplifier for 40 GHz operation. This high volume 150 nm process known as TQP15 has been developed by TriQuint Semiconductor to meet the increase in demand for applications requiring good power performance at higher frequencies while maintaining a minimum 12 volt breakdown voltage. We set out to design a 40 GHz amplifier for a nominal gain of over 13 dB and greater than 28 dBm nominal output power under typical 3 volt operations. This type of design can then be optimized to address markets including Automotive Radar, Point-to-Point Radio, Very Small Aperture Terminal (VSAT), and other Ka to V band applications. There have been several papers reporting amplifier performances in the Ka and Q band [1] – [8]. However, these designs use either air bridge metallization and/or are not an optical lithography gate process manufactured on a commercial high volume process.

This thesis will demonstrate the capabilities of the process through the design flow from simulation through fabrication and measurement. The process parameters will be summarized for the device technology and both DC and RF measurements will be presented. Additionally, load pull data tuned for power

that demonstrates the gain and Power Added Efficiency (PAE) will be presented as well as standard small signal Scattering Parameter (S-parameter) data.

In addition to active devices in TQP15 process, the technology allows for the integration of resistors, capacitors, and inductors as well as low loss substrate vias. For designs requiring lower loss ground connections and improved thermal dissipation, flip chip technology can also be used instead of substrate vias.

A description of the design and performance of the 3-stage power amplifier (PA) will be covered. This will include the typical DC and RF characteristics of the transistor cells and how they are integrated into the amplifier design. Also addressed will be the impedance transformations and matching networks necessary for the interstage matching as well as the input and output networks. Information regarding the device periphery and stage ratios to achieve sufficient power gain, and related output power will also be discussed. In summary, this work demonstrates the performance capabilities of an advanced low-cost, reliable high volume millimeter wave (mmWave) Gallium Arsenide (GaAs) process.

Chapter 2

Amplifier Characteristics Overview

2.1 Classes of Operation

Numerous references have been published dedicated to amplifier characteristics [9] - [12], thus only an overview will be presented in this chapter. Amplifiers are typically distinguished from one another by their class of operation. The class of operation is represented by the current and voltage waveforms as will be illustrated later. There are several classes that power amplifier can be designed to operate in. These classes are generally defined by four criteria: efficiency, power, linearity, and conduction angle.

Efficiency is defined as the ratio of the Radio Frequency (RF) power to the Direct Current (DC) power. Power is the capability of delivering a voltage or current to the amplifier's load at the frequency of interest. The linearity performance of the amplifier is defined by other Figures Of Merit (FOM). These include the one decibel (1dB) compression point and the Third Order Intercept (TOI) point. Conduction angle is considered 100% when the device is always on and the waveforms are not distorted. All of these will be discussed later in more detail. To a lesser degree the biasing and matching networks provided to the amplifier also help to define what class of operation the amplifier performs in. Table 1 summarizes the qualities of amplifiers operating in different classes of operation.

Table 1: Summary of Amplifier Class of Operations

Class	Efficiency	Power	Linearity	Conduction Angle
A	25% Max.	High	Best	100%
AB	< 78.5%	High	Some Distortion	< 100%
B	78.5% Max.	High	More Distortion	50%
C	> 78.5%	Low	Poor	< 50%
D	< 100%	Medium	Moderate	50%
E/F	100%	Low	Poor	50%

2.1.1 CLASS A

The classic defining behavior of a Class A amplifier is linearity. As can be seen in Figure 1 a signal is amplified while maintaining its linear transfer characteristic with no distortion.

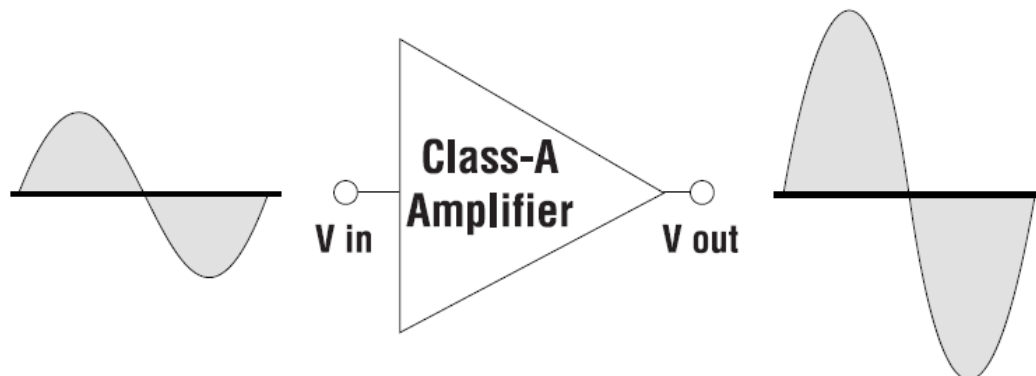


Figure 1: Linear Operation of Class A Amplifier

The typical single stage amplifier employing a common emitter/source configuration inverts the phase of the signal but maintains a constant gain associated with the power entering the device. The power level applied to a class A amplifier can be described by injecting a relatively low level of power where the device is not pushed into the saturation region and thus maintains its

linear response. A typical design would use a load line technique as shown in Figure 2 [13] to ensure that the device is biased appropriately.

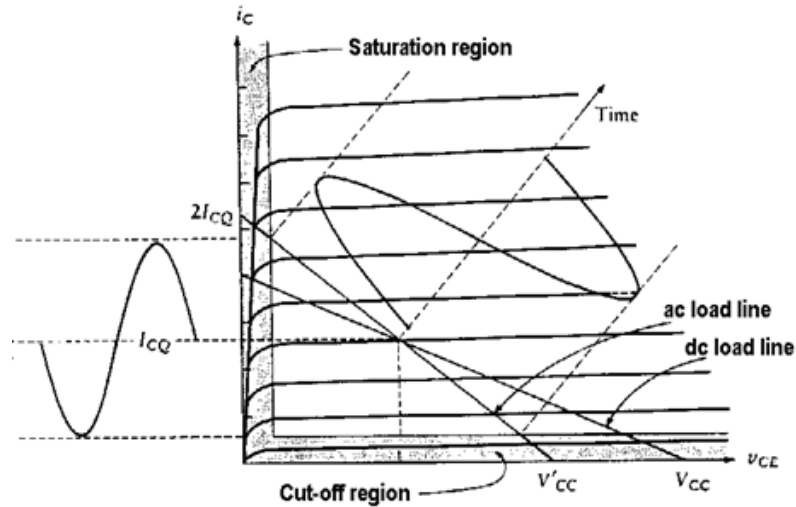


Figure 2: Graphical Depiction of Load Line Technique for Biasing Device

The waveform of the collector or drain current is biased at a level greater than the amplitude of the input signal current in order to maintain its undistorted characteristics. Because current flows during the whole waveform period the conduction angle is referred to as being 100%. It can also be described as an unclipped waveform as seen in Figure 3.

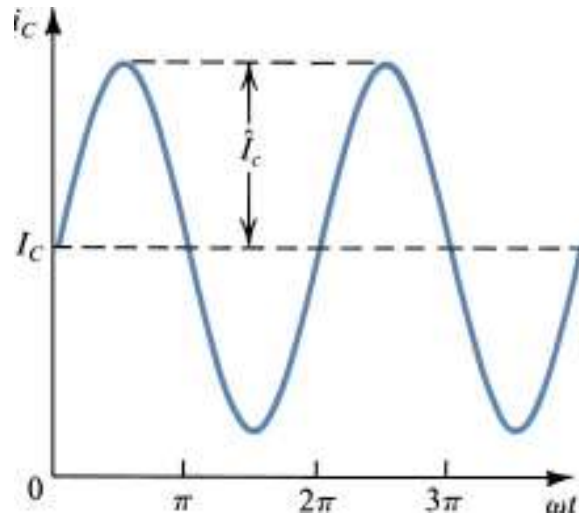


Figure 3: Collector/Drain Current Waveform for Class A

2.1.2 CLASS B

When a device operates as a Class B amplifier then the most obvious contrast is evident in the collector/drain or emitter/source current waveforms where the conduction angle is now 50%. This is seen in Figure 4 where the device will conduct current only half the time while being in an off condition the other half. The device is biased in such a way that the signal current is the only source to turn on the device and the DC bias current is zero. It is also evident that the signal being amplified will have more distortion compared to the Class A amplifier.

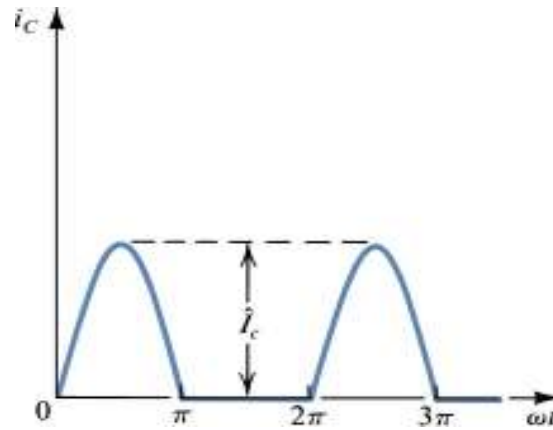


Figure 4: Collector/Drain Current Waveform for Class B Operation

2.1.3 CLASS AB

A compromise between Class A and Class B operation is appropriately named class AB. The device is biased at a non-zero DC current where the magnitude of the current is dictated by the trade-off between linearity, efficiency, and power. The bias point selected determines the voltage swing and the conduction angle which is seen in Figure 5.

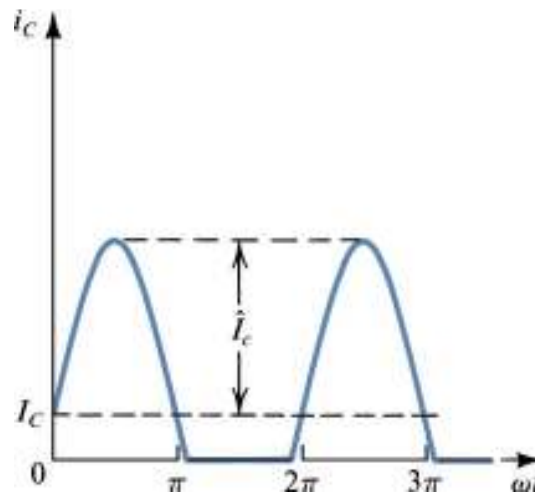


Figure 5: Collector/Drain Current Waveform for Class AB Operation

2.1.4 CLASS C

Operations under Class C conditions occur when the output tuning network conditions the signal, typically through a parallel resonant inductor capacitor (LC) circuit. This resonant circuit is tuned to the frequency of interest and sustains the RF waveform during the non-conducting part of the cycle. The non-conducting portion of the cycle can be seen in Figure 6. Typically, the output matching is a parallel resonant circuit that is designed to provide an output signal that is proportional to the input signal at the resonant frequency of interest.

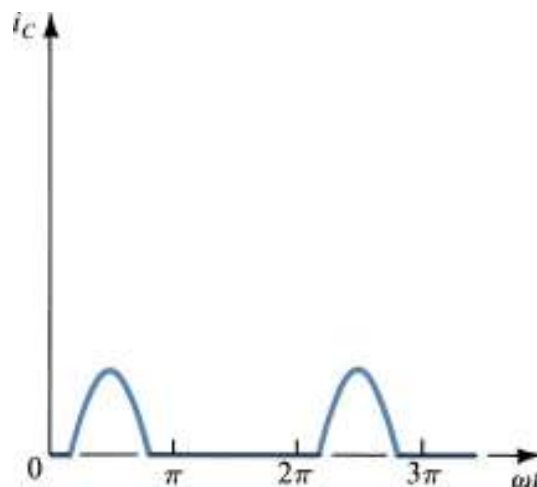


Figure 6: Collector Current Waveform for Class C Operation

2.1.5 CLASS D, E, F, J, S, AND OTHERS

These classes of amplifiers can be represented as switching amplifiers where their mode of operation is depicted by a switch where the current source is either delivering power to the load or is in an off mode. These classes of amplifiers can achieve very high efficiencies and with additional supporting

circuitry can be configured to operate in a more linear mode. There has been a great amount of literature published on these [14-16] as well as other classes of high efficiency amplifiers but they will not be covered here.

2.2 Figures of Merit

Besides amplifiers being described by their class of operation, they are also described by Figures Of Merit (FOM). Generally speaking the FOM characteristics are based on the performance of the amplifier under specific test and measurement conditions. Thus these specified conditions need to be well documented and held stable for the measurement to accurately compare the strengths or weaknesses of the device under test (DUT). The following FOM's are used:

- Power-Added-Efficiency
- Linearity: Output referred third-order intercept point, and 1-dB compression point
- Maximum Output Power
- Stability
- Maximum available gain and maximum stable gain
- Breakdown voltage
- Matching Technique

2.2.1 POWER-ADDED-EFFICIENCY

Power-Added-Efficiency (PAE) is a measure of a device's ability to convert the applied DC power to an RF power for a given fundamental frequency. Calculating PAE accounts for the input power (P_{RFin}) to the device as shown in Equation 1:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}} \quad [1]$$

For devices where there is low to moderate gain the inclusion of the P_{RFin} can be significant. In devices with fairly large gain, roughly in excess of 28 dB, the P_{RFin} becomes a small percentage of the overall value.

2.2.2 LINEARITY

The information gained from the DUT operating in the linear region is helpful in identifying the characteristics and behavior of the DUT. This information is also used to extrapolate into other FOM parameters. As can be seen in Figure 7 there are several characteristics of the DUT that can be extracted from a Pout versus Pin graph.

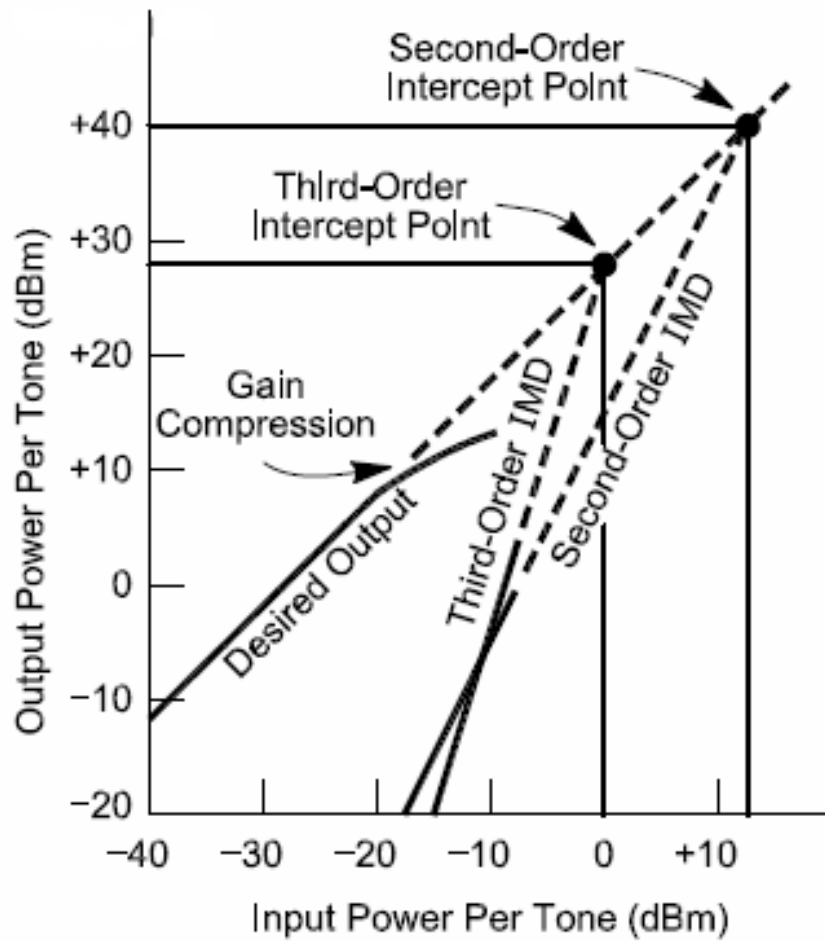


Figure 7: Pout versus Pin Graph Illustrating Intercept Points

This information can be used as the design of the amplifier is evaluated.

2.2.2.1 OUTPUT REFERRED THIRD-ORDER INTERCEPT POINT

While the output third order intercept point is not directly measured in devices with good linearity, it is used to assess the distortion products of the device. It is an indicator of the intermodulation distortion (IMD) that exists in non-linear systems. It should be noted that not only are harmonic frequencies generated, but the sum and difference frequencies are generated as well. A two-

tone test is used to determine the value of the intercept point as can be seen in Figure 8.

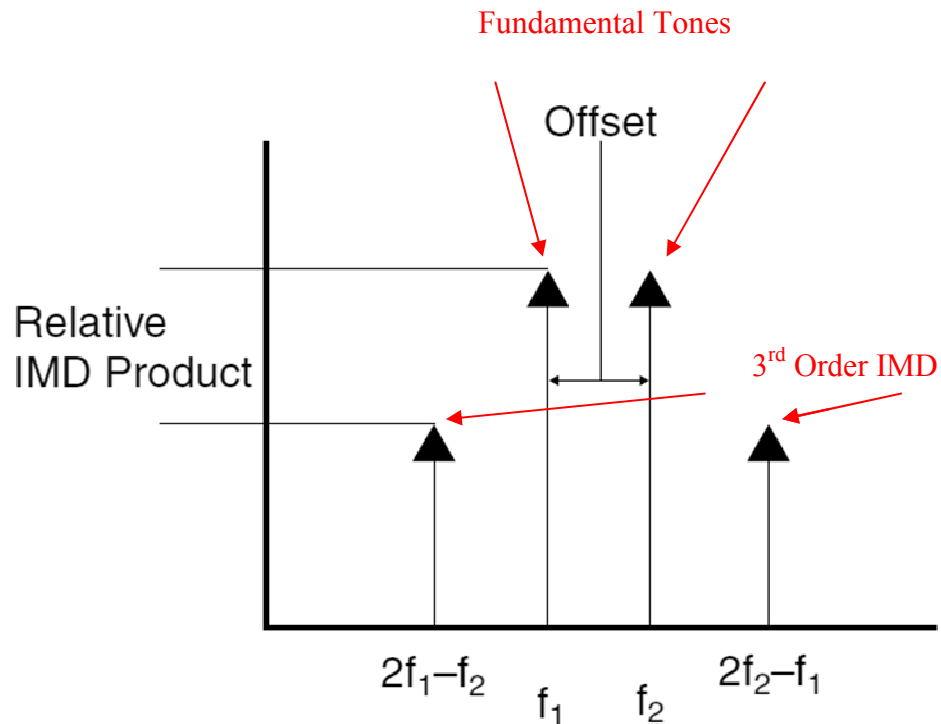


Figure 8: Frequency Graph of a Two-Tone Measurement

The third order IMD product will increase in magnitude as the input power of the fundamental tones increases. This increase will depend upon the offset spacing and the gain of the device at the frequencies used.

2.2.2.2 1dB COMPRESSION POINT

The 1dB compression point is defined by extrapolating the linear gain curve beyond its measured saturation region and then determining the point where the measured gain is one dB below the extrapolated linear gain point. This can be seen in Figure 9.

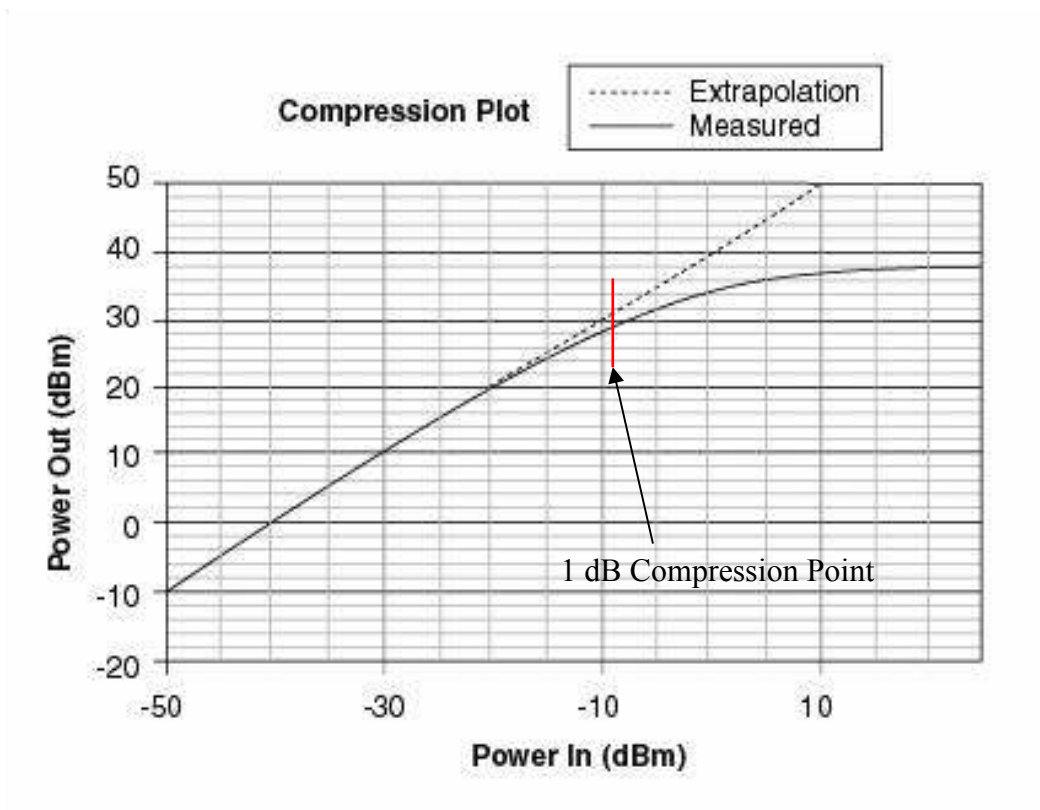


Figure 9: Measured and Extrapolated Gain Compression Plot of an Amplifier

Other compression points such as 0.5 dB and up to 3 and 5 dB can be determined in the same manner as necessary up to where the amplifier is fully saturated.

2.2.3 MAXIMUM OUTPUT POWER

The maximum output power region is where the device is saturated and the device cannot output any additional power into the load. This condition is where the efficiency of the device is high and the output voltage is severely clipped. This condition can be seen in Figure 10. The graph shows what the ideal output waveform may look like compared to the saturated condition.

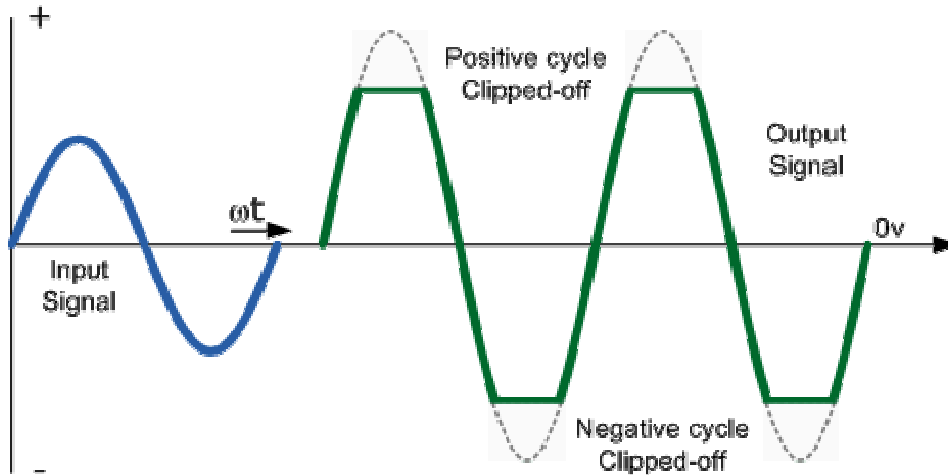


Figure 10: Ideal Waveform Compared to Compressed Amplifier Output

2.2.4 STABILITY

The stability of a device is one of the key elements to a successful design. The traditionally accepted FOM for stability is the Rollet stability factor K , where a value greater than one signifies that the device or design is unconditionally stable. This is determined from s-parameter data where;

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|}, \text{ where } \Delta = S_{11}S_{22} - S_{12}S_{21} \quad [2]$$

Typically, $|\Delta| < 1$ condition for stability is satisfied and we will discuss only the $K < 1$ condition.

2.2.5 MAXIMUM AVAILABLE GAIN AND MAXIMUM STABLE GAIN

The use of FOMs Maximum Available Gain (MAG) and Maximum Stable Gain (MSG) has been helpful in determining the frequency range which the device or design has adequate gain and under specific stability conditions. MSG is defined as $|S_{21}|/|S_{12}|$ when $K < 1$. Here the device is referred to as being potentially unstable. For MAG, which is also referred to as G_{\max} , K is greater

than 1 and the device is considered unconditionally stable. Equation 3 shows the mathematical calculation for G_{max} .

$$G_{MAX} = (K - \sqrt{K^2 - 1}) \times \frac{|S_{21}|}{|S_{12}|} \text{ for } K > 1 \quad [3]$$

When a device is unconditionally stable it will not oscillate under any load impedances.

When considering the performance of a device a typical S-parameter sweep over frequency is taken and plotted. This shows not only the gain of the device under a set of specific bias conditions, but also the transitions from a potentially unstable device to an unconditionally stable region. This is illustrated in Figure 11 where there is an abrupt change in the curve of the plot.

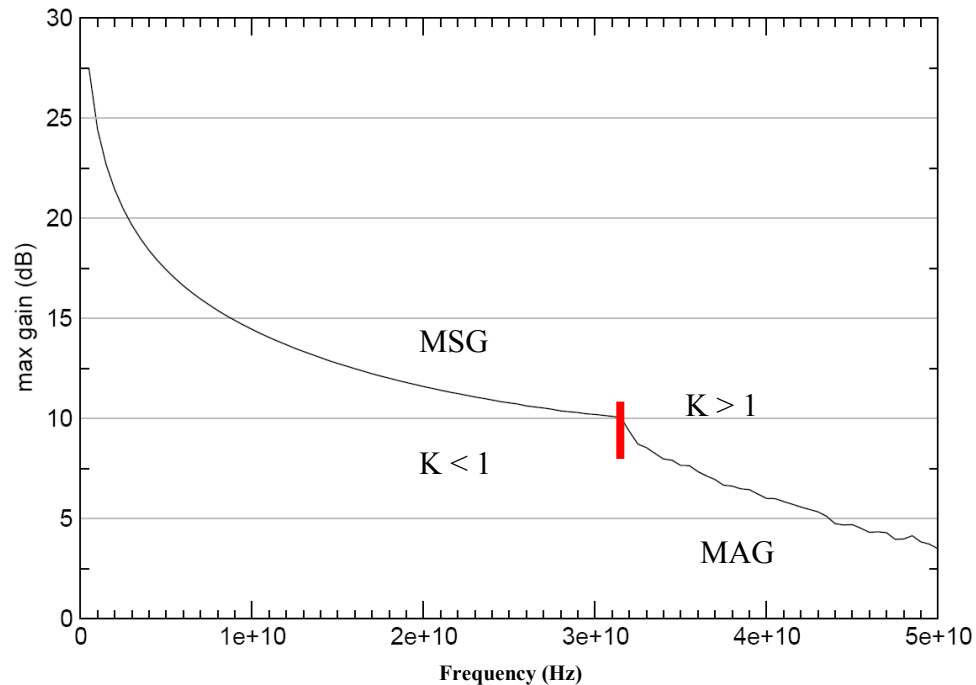


Figure 11: MSG to MAG Inflection Point Plot

2.2.6 BREAKDOWN VOLTAGE

One of the important parameters of a device is its breakdown voltage. When selecting a technology for a specific application the breakdown voltage must be considered. If this voltage is not sufficient to handle the voltage swings for the design space, then either another process must be selected or precautions must be taken to preclude the device from being subjected to these conditions. This may be accomplished by a change in the bias condition if other specifications are not too severely compromised by this change or by limiting the breakdown voltage by either topology and/or component changes and/or device enhancements. A device experiencing an electrical overstress (EOS) is seen in Figure 12. This is an example of where the device could not handle the high current under a non-typical test condition.

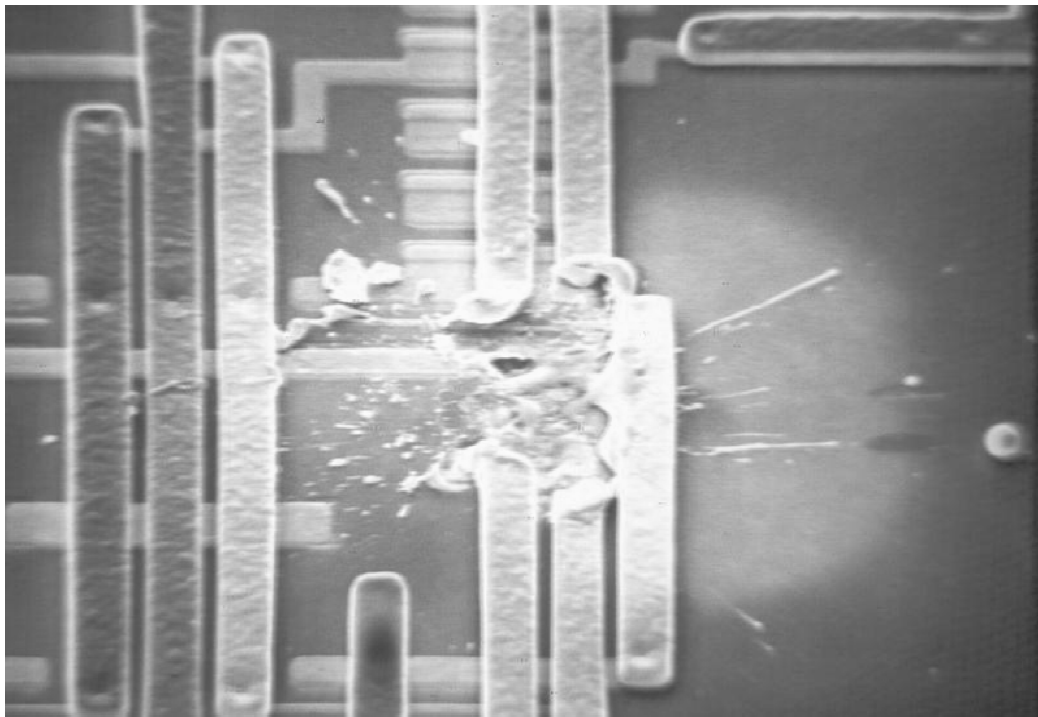


Figure 12: SEM Photograph of FET EOS Failure

2.2.7 INPUT, INTERSTAGE, AND OUTPUT MATCHING

The ability to properly interface the design and devices both on and off die is of the utmost importance. However determining the design approach, topology, and interconnect mechanisms involves numerous tradeoffs. Even choosing the technology contributes to the degree of freedom that may exist. For some technologies there are an adequate number of metal layers in the process to allow sufficient flexibility in the type and size of device interconnect. Other technologies may offer fewer metal layers and thus a limited number of interconnect options exist.

These connection options may also involve the type of material that the design will be physically attached to that will allow it to interface with the final assembly. Thus some of the matching may be incorporated on the substrate that the semiconductor die is attached to. This matching might be either discrete components or a combination of discrete and transmission line structures.

Typically, the interstage matching is done entirely on the semiconductor die. However, the type of matching structures may be dictated by the semiconductor technology used. Whether coplanar waveguide, microstrip, or stripline structures are used is dependent on the metal stackup of the process. Additionally, the frequency of operation may also help determine whether Metal-Insulator-Metal (MIM) capacitors or stub elements are used. More information regarding this will be presented in the following design section on transmission line analysis.

2.3 S-Parameters

The use of Scattering (S)-parameters typically differentiates between designs implemented at low frequencies where Z and Y parameters are used and those at radio frequencies (RF) and higher. Like Z and Y parameters, S-parameters have a set of conditions that define the data presented. The complex information is usually expressed as magnitude and angle or real and imaginary values. Also, a Smith Chart at some point in the design is usually used to interpret this information and could also help determine an appropriate matching network. Two-port network theory is well documented in the literature and will not be repeated here.

The four components of the S-parameters, however, will be briefly reviewed. S_{11} is referred to as the input reflection coefficient and is an indicator of how well the input of the DUT is matched to the source driving it. It is usually expressed in dB and its best value is obtained for conjugate matching the input. S_{12} is the reverse transmission coefficient and is an indication of how well the input and output ports are isolated. If they are perfectly isolated then S_{12} would be zero and the DUT would be referred to as being unilateral. S_{21} is commonly referred to as the gain of the DUT and lastly S_{22} is referred to as the output reflection coefficient and is an indicator of how well the output of the design is matched to the load it is driving.

Chapter 3

Semiconductor Process, Device, and Model Overview

3.1 Semiconductor Technology

The TriQuint TQP15 process is an optical lithography refractory gate technology that is processed on 150 mm GaAs substrate with vias on 4 mil thinned wafers. The TQP15 process is an extension of the work performed to develop the TQP25 process [17] and the earlier work involved on the TQP13 process [18]. These processes use I-line steppers and sidewall spacer technology for high throughput manufacturing. This spacer technology is also widely used in the silicon CMOS industry where it is implemented using etching steps that take the gate's larger drawn dimension down to the final target length. This is covered in detail in reference [17].

The high frequency 40 GHz markets typically require a higher breakdown voltage on the process side and also a less expensive packaging solution similar to those in the more commercial 1 - 2 GHz range. These two requirements have been implemented in the process to fit well with the commercial needs of the marketplace at this frequency. A summary of the process parameters is presented in Table 2.

Table 2: TQP15 Process Summary

Process Specifications, Vds = 3.0 V		
Parameter	Typical Value	Units
Gate Length	0.15	um
Pinch-off Voltage	-1.0	V
On Resistance	1.0	Ω -mm
Off Capacitance	250	fF/mm
Breakdown Voltage	14	V
I _{max} /I _{dss}	550 / 300	mA/mm
G _m	400 @ I _{dss}	mS/mm
F _t / F _{max}	50 / 125 @ I _{dss}	GHz
Process Passive Elements		
Parameter	Typical Value	Units
Resistors	50 / 100	Ω /sq
BLMET (0.62um)	50	m Ω /sq
Met 2 (4um)	6	m Ω /sq
MIM Cap	0.62	fF/um ²
MIM Cap BV	> 40	V

This optical lithography process allows for a less expensive solution for the design space where gate lithography is essential. Optical lithography allows for faster processing time when compared to traditional electron beam (e-beam) writing technologies. The refractory gate enhances the thermal stability and the long term reliability of the transistor. The classical benchmark for device reliability is defined by gate sinking [19]. However, with the refractory gate this phenomenon is not observed in standard accelerated life tests. This could allow for a higher operating junction temperature and thus a higher current density. A scanning electron microscopy image of the gate structure is seen in Figure 13.

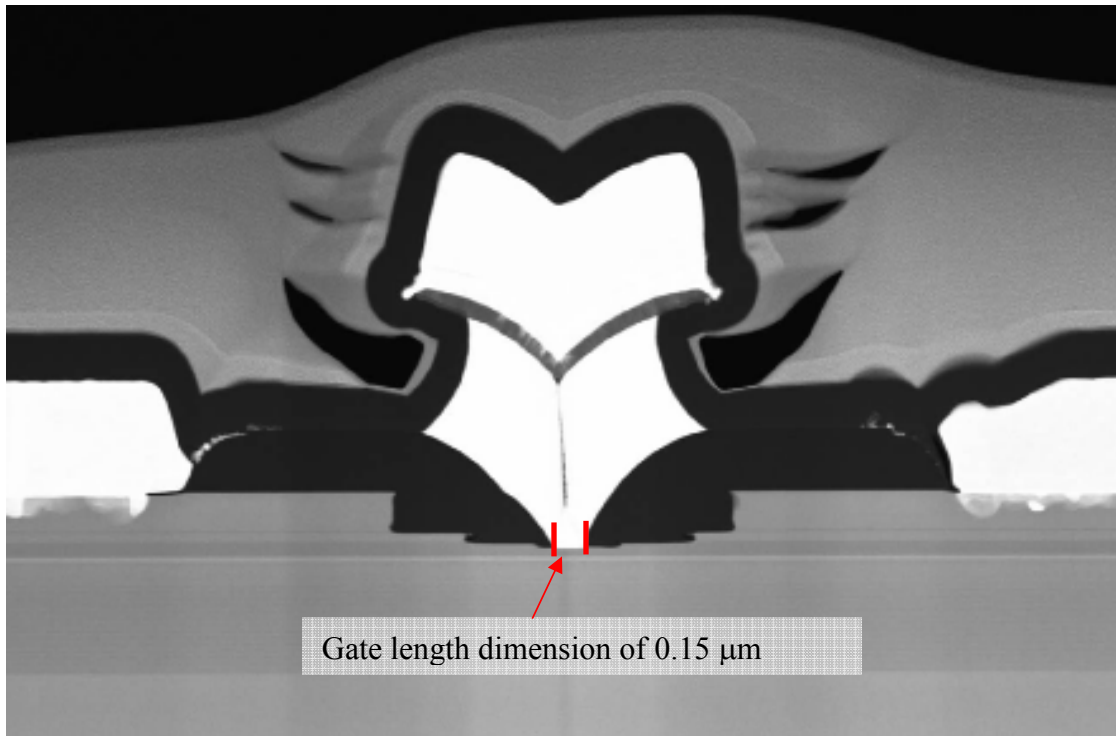


Figure 13: Cross-Section Image of the Gate Structure

The transition from an air-bridge process like TQP13 to a planarization layer of benzocyclobutene (BCB) allows for a more uniform electrical performance under different packaging conditions. For a typical airbridge process the packaging needs to be more expensive to prevent degradation of the performance of the device. Thus a hermetic or air cavity package is necessary to maintain performance. The BCB, while further protecting the die, also contributes to degrading the F_t and F_{max} performance of an airbridge process transistor. However, the BCB helps to maintain the frequency performance after a standard overmold package is used. Thus a less expensive package can be used while still maintaining the performance of a standard BCB process. A pictorial of the process cross section is depicted in Figure 14 which also identifies the circuit passive elements.

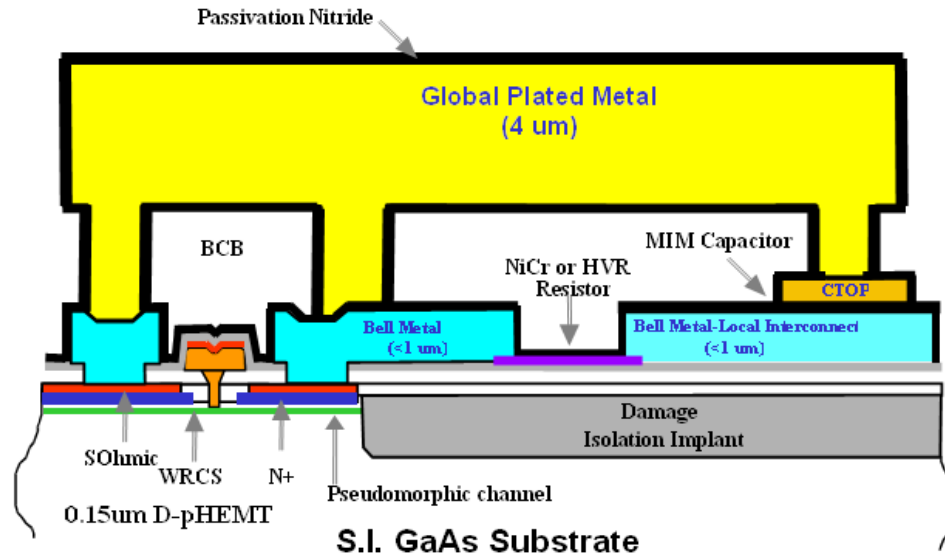


Figure 14: Process Cross-Section of TQP15

Another contributor to the low cost of the process comes from the incorporation of a two layer metal interconnect. These interconnect metals consist of an evaporated lower level metal that is also used for the bottom plate of the capacitor structure and an electroplated thick Metal 2 layer. The combination of these metal layers could also be used for the formation of an inductor structure, but typically is used to form the thick microstrip transmission line (TL).

The initial device characterization for the preliminary model development was performed in a coplanar waveguide (CPW) with a Ground-Signal-Ground (GSG) test pad configuration. This configuration allows for design layouts to be automatically generated internally from some simulators and incorporated into the design flow. A picture of the structure is seen in Figure 15.

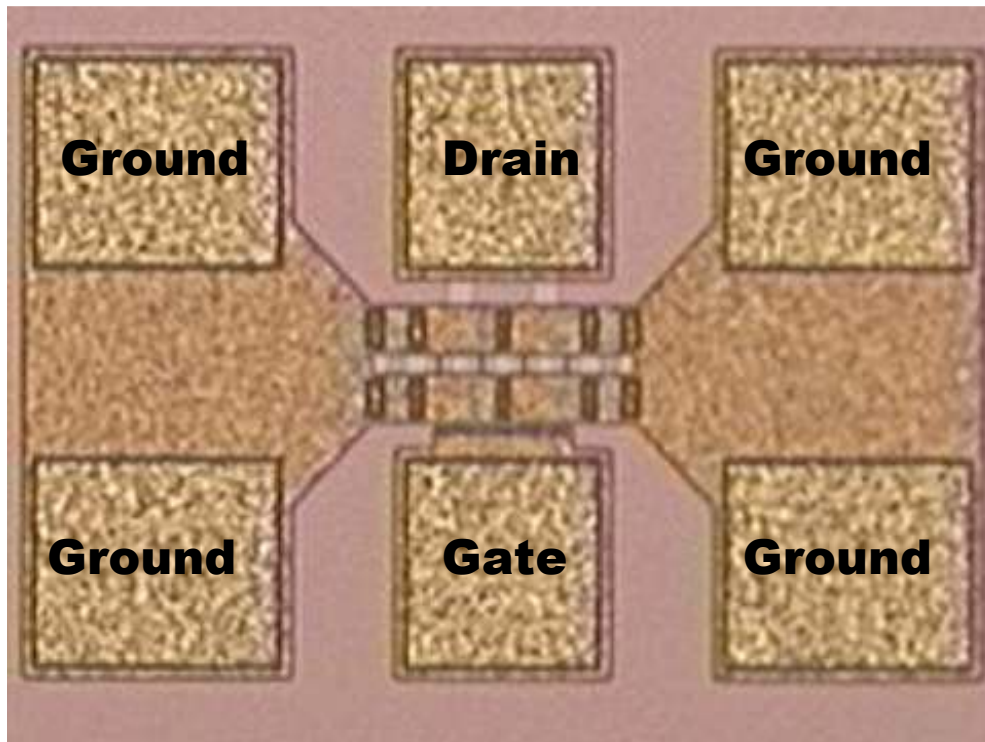


Figure 15: 4x50 FET in a CPW Test Structure

For other on wafer measurements such as noise and breakdown voltage, devices were used that would model the environment they would be incorporated in. Besides the devices having the substrate vias integrated into the device layout, calibration structures were used to perform an on wafer Line-Reflect-Match (LRM) calibration. These calibration structures use the same style GSG launch structures, as shown in Figure 15, that all the measured devices use regardless of the device size. The substrate vias are also integrated into these launch structures to provide a controlled environment and also maintain the capability to de-embed their parasitic effects out of the measurement. Figure 16 shows a ten finger device with a gate width of 60 μm .

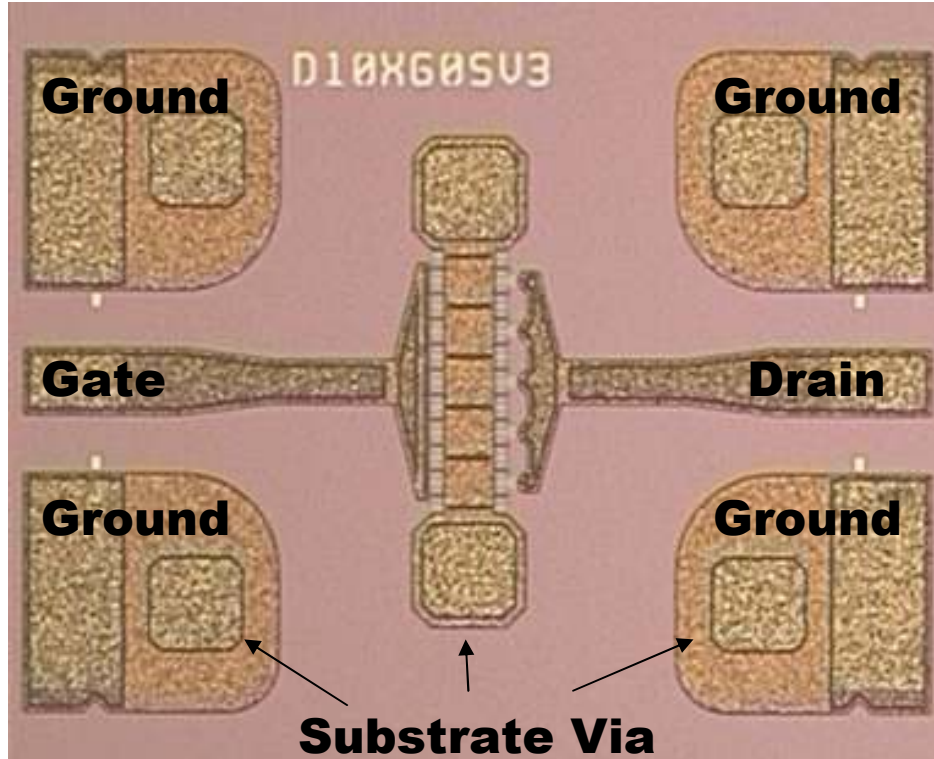


Figure 16: 10x60 FET in Microstrip GSG Test Structure

The characterization of passive components is typically done in a microstrip environment. Thus the GSG launch structures that have been previously used in the calibration procedure are used to evaluate an inductor as shown in Figure 17. While typical higher frequency designs do not use a standard coil inductor, there are lower frequency applications that do.

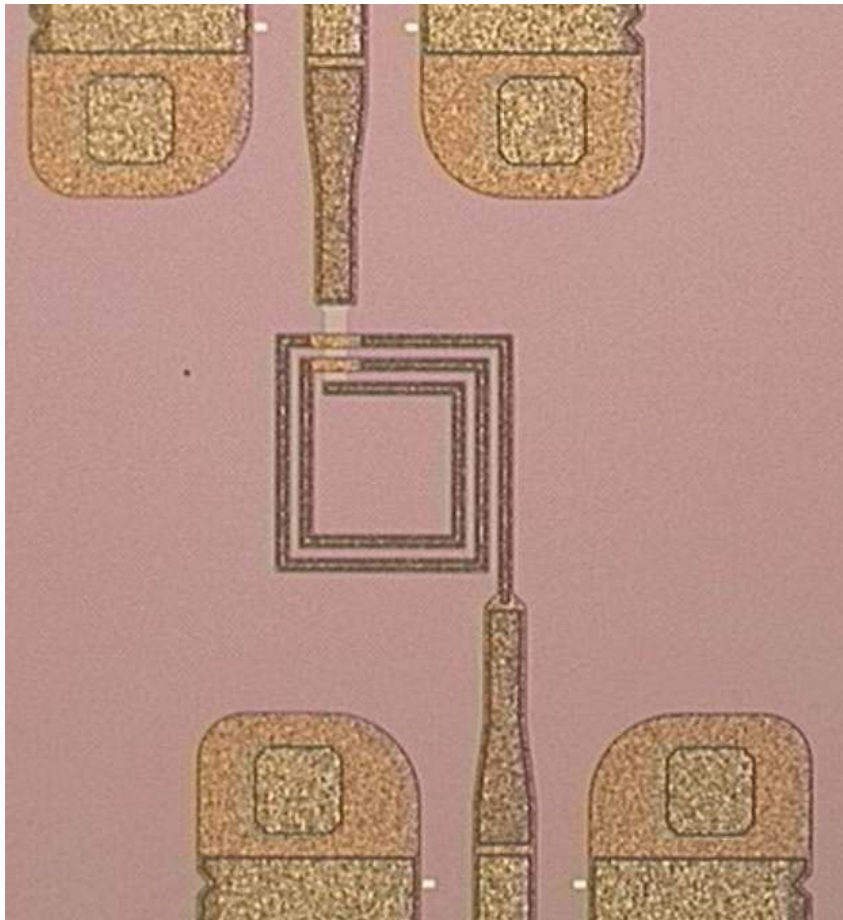


Figure 17: Passive Inductor Element Characterization Structure

3.2 Transistor Performance

Examination of measured performance of a wide variety of device sizes and configurations was undertaken. A measurement matrix included device periphery, gate pitch, internal via construction, and gate manifold. The device level data has been collected by the modeling groups in both TriQuint facilities located in Richardson Texas and Hillsboro Oregon.

The DC measurements are compared to the TOM4 extracted model. For the scalable TOM4 model the agreement tracks well with the measured data as

seen in Figure 18 below. These measurements were taken in the TriQuint Modeling Lab on a nominal full thickness wafers at room temperature.

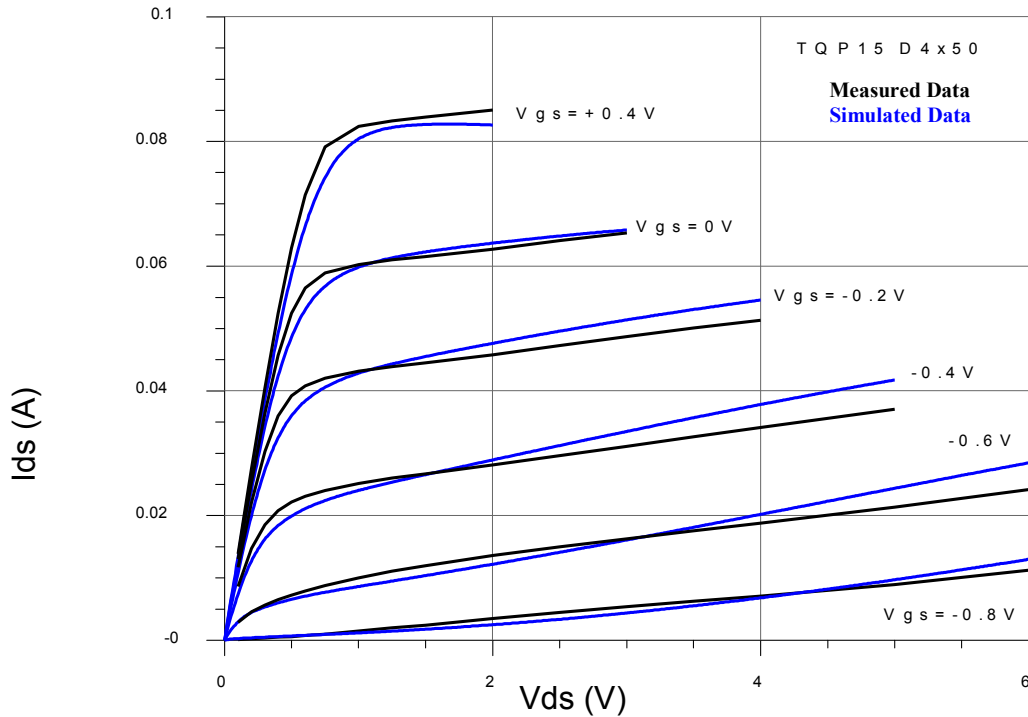


Figure 18: I-V Curves for the 4x50 Depletion Mode pHEMT FET

Data has been plotted comparing the measured and modeled transconductance G_m and drain current I_{ds} over a V_{gs} range of -1.2 to 0.8 volts, as seen in Figure 19. The comparison shows that the model data is slightly more optimistic at a slightly lower V_{gs} but then becomes slightly more pessimistic after the G_m peak. As more statistical data is collected over several process runs the model will be reevaluated by the modeling teams to reduce the model versus measurement error.

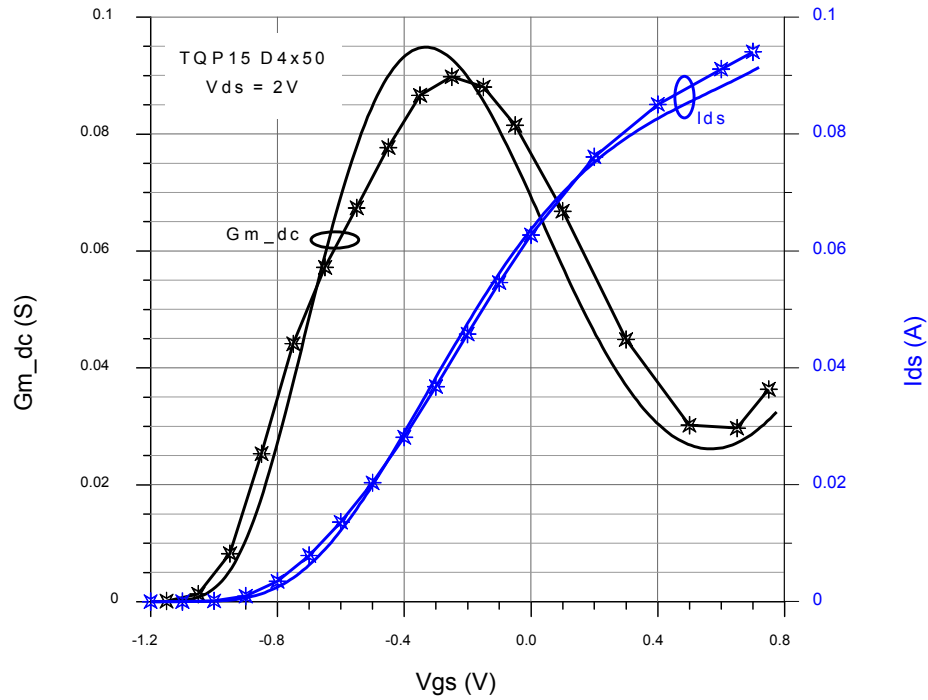


Figure 19: DC Ids and Gm Plots (Measured Data Marked with Symbols)

Additionally, S-Parameter measurements have been plotted for three volt operation up to 50 GHz as shown in Figure 20. This data is representative of the numerous data points collected under a wide range of Vdd and Ids bias points. As the process has matured over time a structured effort was maintained to continually collect data not only over different bias conditions but also over additional wafer and lot runs.

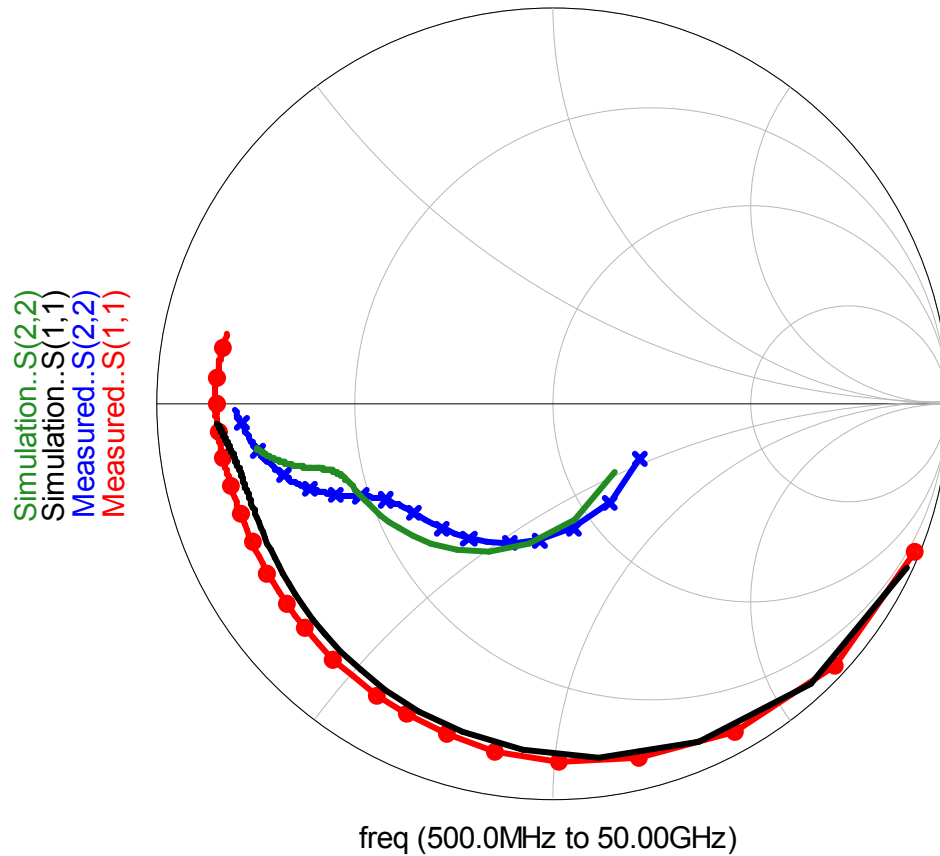


Figure 20: Measured versus Modeled Data for S11 and S22

For this study, other devices were tested on a wafer probe stage that was configured with RF GSG probes using 2.4 mm connectors. Measurements have been taken on full thickness wafers and also on thinned wafers with substrate vias that are attached to a 200 mm gold plated disk. Additionally, sawn parts were epoxy attached to gold flashed carriers and measured as well. These parts were used to also help assess the self-heating characteristics of the device that cannot be fully appreciated in a full wafer test environment.

A gain and stability factor plot from 500MHz to 50 GHz of a standard cell device is illustrated in Figure 21 showing the MSG/MAG transition above 30 GHz under 50 Ohm wafer probe conditions.

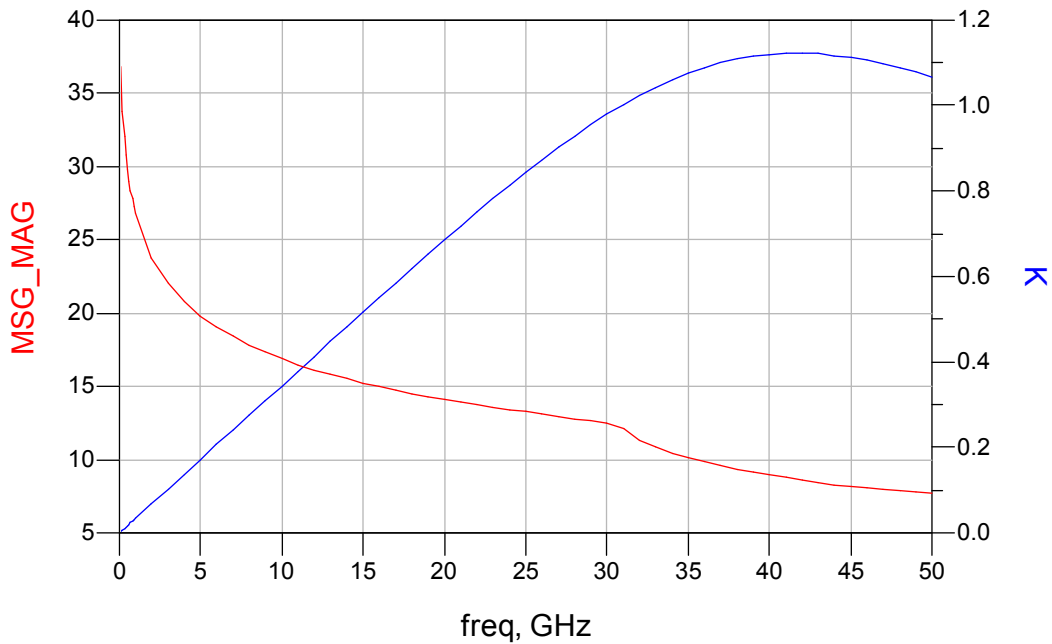


Figure 21: Maximum Gain and Stability Factor K of Standard Cell

Load pull analysis is used to help determine the best operating point for the unit cell in a design. This data can be plotted to help determine the trade-offs between competing specifications. Figures 22, 23, and 24 summarize the measured device performance for the technology at 21 GHz illustrating the tradeoffs between gain and PAE versus the output and input power. Wafer numbers are identified on individual plots.

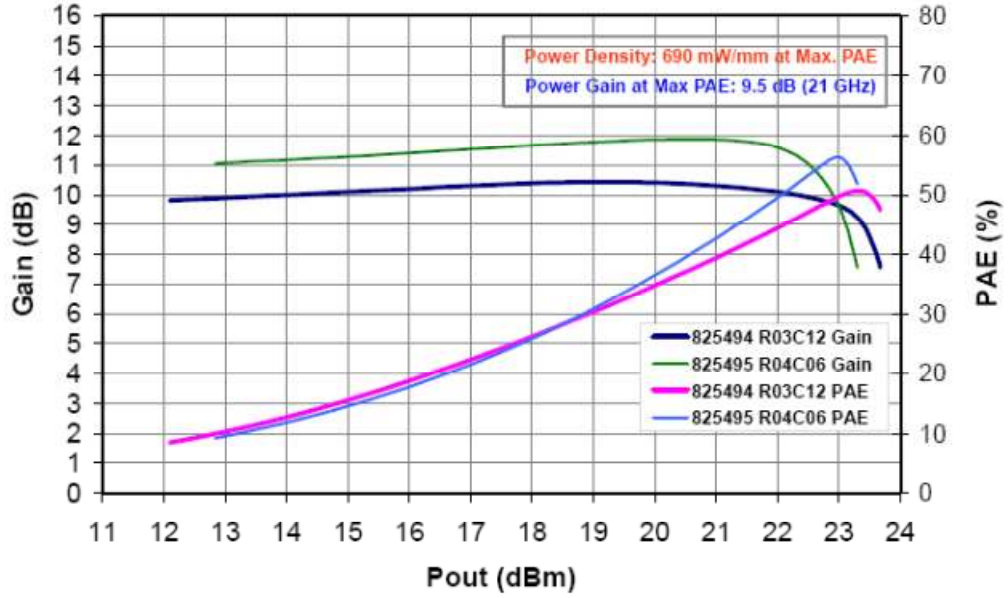


Figure 22: Measured Gain and PAE versus Pout

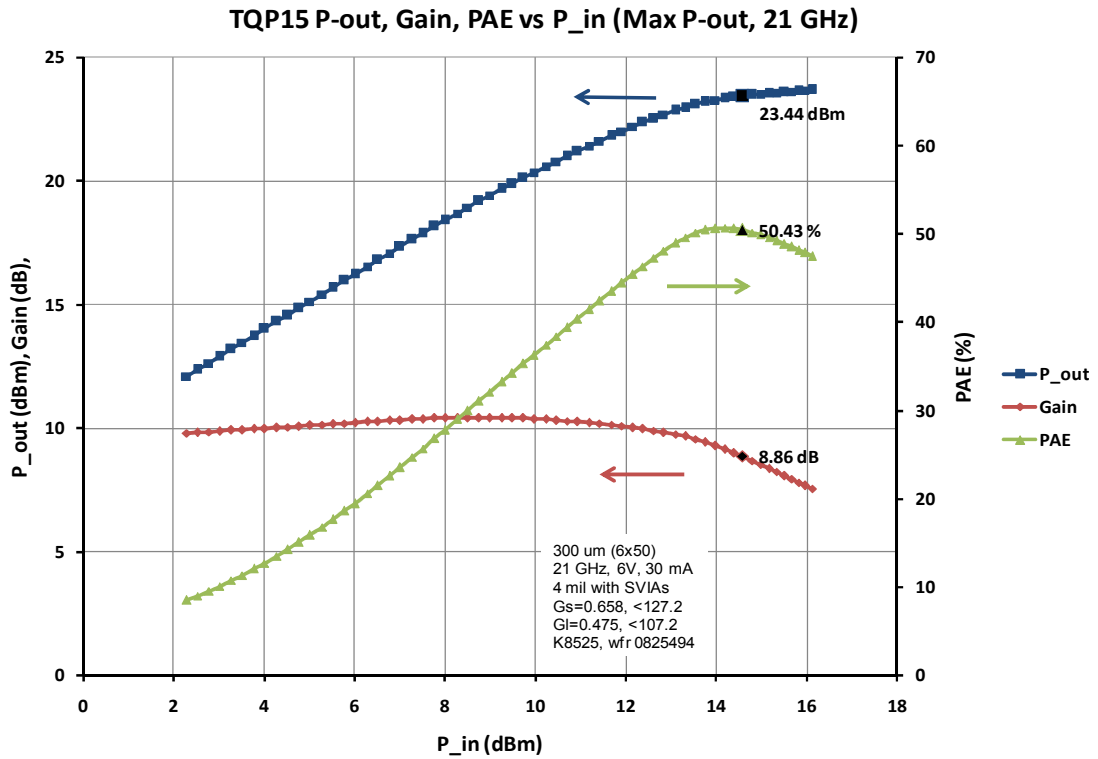


Figure 23: Gain, Pout and PAE versus Pin tuned for Maximum Pout

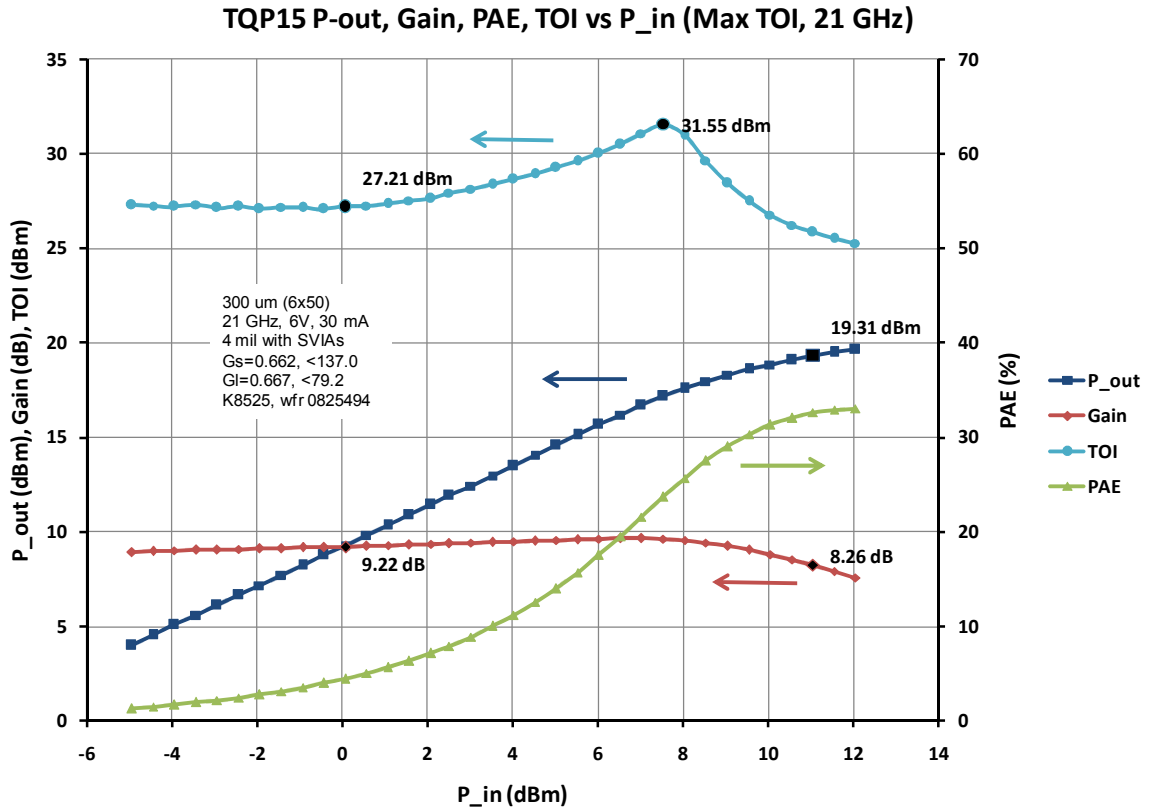


Figure 24: Gain, Pout and PAE versus Pin at 21 GHz for Maximum Pout

3.3 Transistor Model

The model used in the design kit is called TOM4 (TriQuint's Own Model) and is the fourth revision to the general topology illustrated in Figure 25.

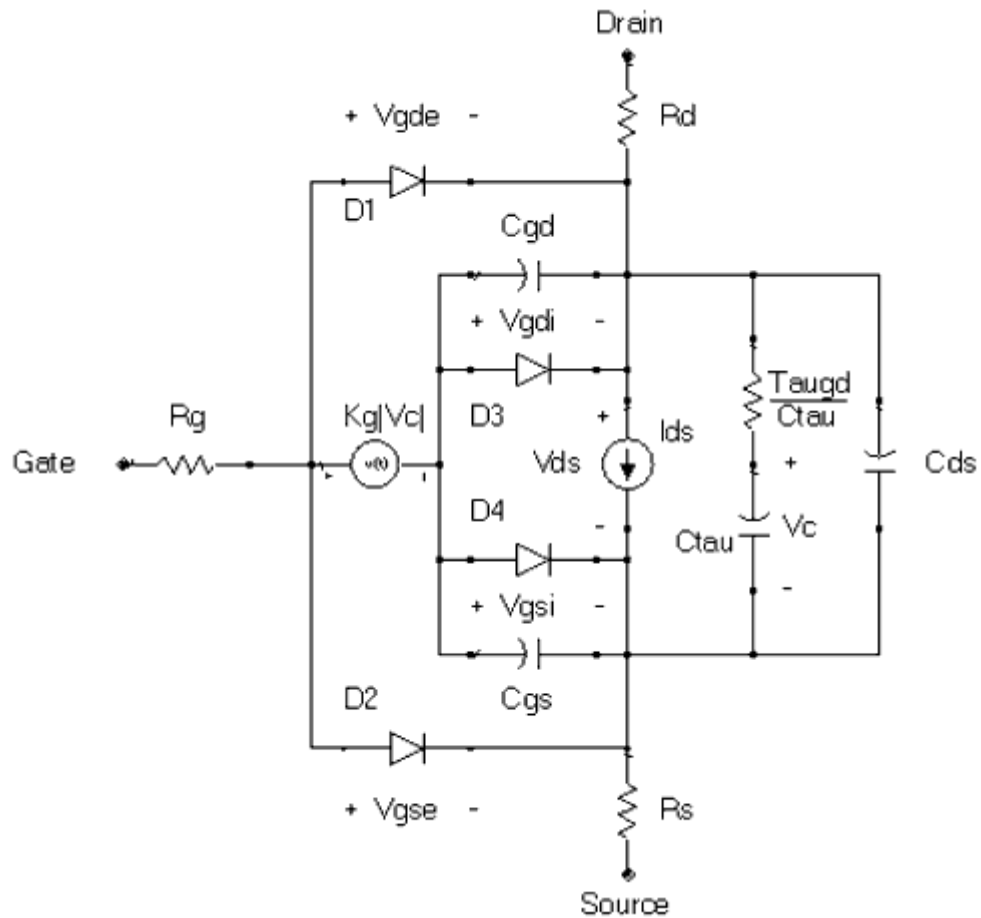


Figure 25: TOM Equivalent Circuit Topology

This architecture has been implemented to link the large and small signal performance into one model [20]. For improved simulation accuracy the effects of frequency dispersion and g_m compression have been refined in the charge functions and the voltage derivatives. Parameters for the model are extracted from both small and large signal S-parameters biased in a stable and safe operating region. The model parameters are then extracted from the measured data by fitting to the model equations.

Chapter 4

Circuit Design Process and Methodology

4.1 Design Overview

Generally, the design parameters of an amplifier, or any device, are specified by either a data sheet or a compliance matrix which explicitly identifies the conditions and limits that the design must conform to. Once these parameters are understood then the design process can proceed by first selecting the semiconductor process.

The initial design of the PA was based on the scaled model extracted from our early small signal S-parameter measurements performed on devices in a CPW environment. Using the model extracted from an early run of material has given us a good assessment of the general capability of the process. It is recognized that over the course of this design the process will be refined to improve the device performance and high volume process repeatability. However, this design methodology does allow for an early evaluation of the process to be used for the preliminary design cycle with the understanding that not all of the specifications will be initially met. Further changes to both the process and design can be incorporated into the subsequent evaluation of the material and thus the final process performance can be finalized from the early evaluation vehicles designed and fabricated. The simulation tool used for this design is Agilent's Advanced Design System (ADS).

There are different approaches regarding the design methodology. While much has been published in the literature [1] – [12] there are some

commonalities that exist. The general amplifier design approach presented here starts by determining the class of operation to use that will achieve the specified performance goals. After this, an assessment of the circuit architecture that best fits the combination of performance specifications and process capabilities is completed. Also, the matching networks are evaluated to determine the best approach to achieving performance and behavior within the specification parameters.

Initially we set out to design an amplifier at 40 GHz frequency, with 20 dB of gain, 30 dBm of output power, at a 3 V supply voltage. Die area was to be minimized and preferably less than 10 mm². The general specifications were to look similar to an existing TriQuint part, TGA4516.

Table 3: Amplifier Specifications

Frequency	Pout	Die Area	Power Density	Small Signal Gain	PAE	Vds	Idsq
(GHz)	(dBm)	(mm ²)	(mW/mm ²)	(dB)	(%)	(V)	(mA)
40	30.0	7.5	183	15	17.5	3.0	1500

For this design we organized the design flow as follows:

- Determine device sizes for biasing requirements
- Optimize output stage for power requirements
- Optimize output stage's power combining network
- Size and bias 2nd and 1st stages for gain and linearity
- Optimize interstage and input matching networks

The design flow was an iterative process that also required the use of EM simulations, especially as the layout evolved to incorporate biasing components and other elements to help with stability.

4.2 Device Size Selection

For designs operating at higher frequencies it is necessary to determine the base device cell size that will be repeated through the particular stage of a multi-stage design. Selecting the proper size requires either a good scalable simulation model that works well over a selected bias range or measured data over several sizes and bias points. This information can then be evaluated over the requirements for the design. An example of this information can be seen in Figure 26.

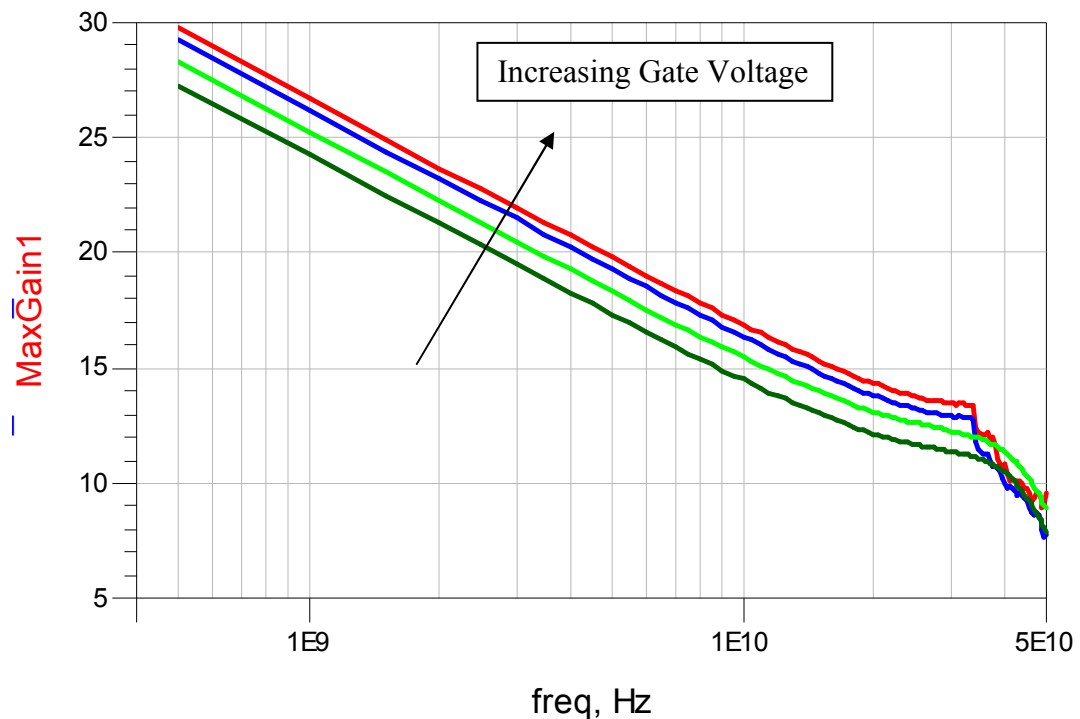


Figure 26: Plot of Measured MSG versus Frequency Over Bias

This information will help define how much gain is expected from the cell at the frequency of interest. It is also necessary to evaluate the current handling capability of the device to determine how much periphery will be necessary to drive the load presented to the stage to deliver the necessary output power.

Another area of importance is associated with the source inductance of the device. Usually at higher frequencies the device is modeled with the source grounding via incorporated within the model reference plane. During the model extraction procedure this source inductance can be removed to allow for an intrinsic model implementation using different layout techniques. However, this source inductance does have a significant influence on the frequency dependence of gain of the device. Also associated with the source inductance are the metal interconnect straps that tie the individual transistor source contacts together. These source straps are adjusted in size related to the size of the device. Figure 27 shows the simulated gain vs. frequency of an eight finger, 150 um device plotted with and without the source substrate vias.

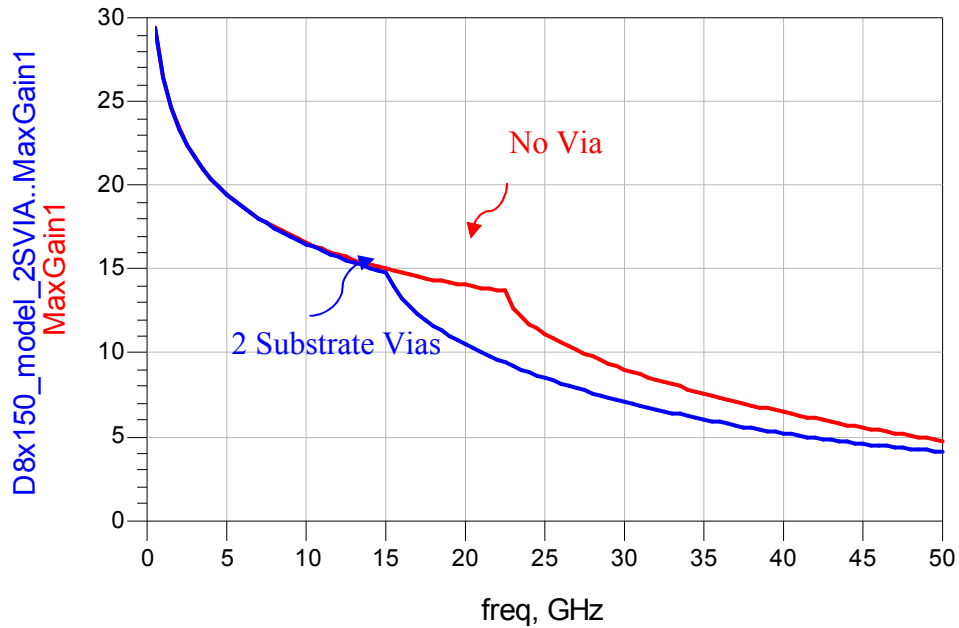


Figure 27: Simulated MSG Source Inductance Comparison

This plot clearly shows the influence on MSG versus frequency for two devices with the same periphery but different source inductances. When two substrate vias are measured with the transistor then the inflection point where K becomes greater than one occurs earlier in frequency.

Also to be considered is the load and source pull information that can be obtained from the device. While this information can also be simulated, for a new process it is best to rely more on the measured data. The load and source pull data can show the desired data typically plotted on a Smith Chart where the power and efficiency contours are displayed. This information also helps in determining the capabilities of the DUT which in turn maps into the design requirements. Measurements for a typical load pull plot of power, PAE and drain current is shown in Figure 28.

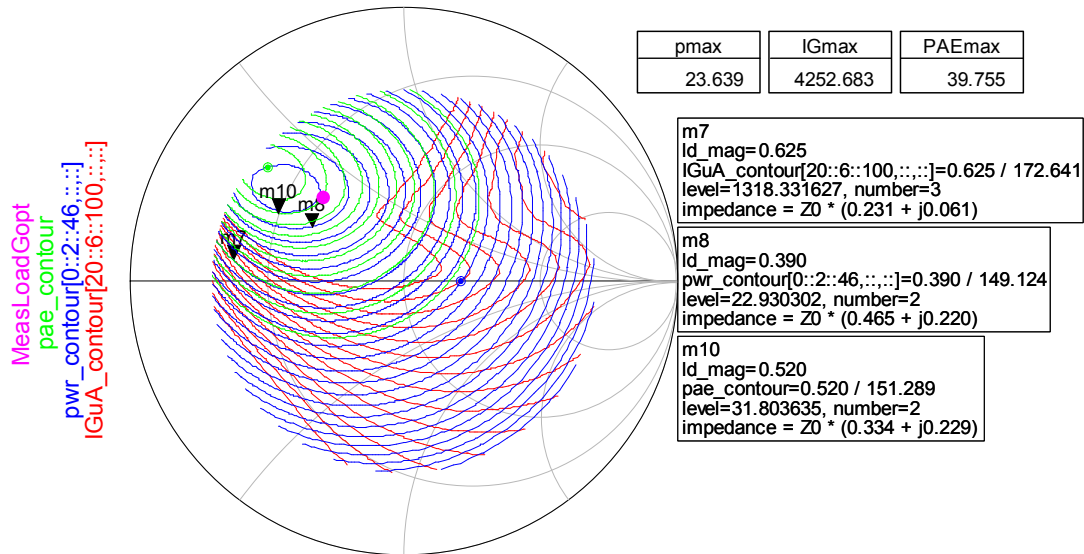


Figure 28: Load Pull Contours Representing Power, PAE and Current

The intersecting contours will help in assessing the trade-off between different specifications. Once we know these trade-offs, the design can be optimized for best performance over the design window.

The information in Figure 28 can be used to determine the number of transistor cells necessary to deliver enough power for a given design. Using the power level data from marker M8 displays a value of 22.93 dBm. Thus if a power level of 1 watt (30 dBm) is necessary the device cell would need to be replicated 8 times to provide greater than a 9 dB increase in power. Some margin should be included to allow for losses associated with input and output matching, however the output power using 8 cells would approach almost 32 dBm of power. Also, the corresponding impedance of the transistor stage is going to be decreased as well. This makes for a larger loss associated with the matching network. To remedy this either another bias point for the cell should be selected or using a smaller unit cell should be considered.

4.3 Stage Design

For a multistage design each stage has its own unique requirements to allow for a successful amplifier design. Each stage must have adequate performance for gain, power, efficiency, quiescent current, and other parameters specified for the design. These then help determine the envelope of operation each stage needs to perform within and what adjustments and trade-offs need to be made.

Assessing the stage's operating region also requires knowledge of the input, output, and biasing conditions. While the input and output stages typically interface with a 50 Ohm environment, they will still need another impedance transformation for their interstage match. Also required for the output stage will be an understanding of the layout and size requirements since at least one die size dimension is usually determined by this stage.

Typically the output stage is designed first by determining the frequency and power requirements. The periphery of the stage is sized for an appropriate output power in the class of operation. For a saturated amplifier design the class of operation may be closer to B or C compared to class A biasing. A class AB operating point is more typical since most saturated power amplifiers are also required to have some linear characteristics in a backed off power out condition. For a linear amplifier where PAE may be a more heavily weighted specification, a class AB operation closer to class A is a familiar choice.

The preceding input or driver and pre-driver stages are then typically designed to provide enough gain and power to achieve the overall output power

specification with adequate efficiency as well. These stages are also biased to not saturate before the output stage, if at all.

Our final design was a three-stage design with an input stage utilizing 4 devices with a gate width of 80 μm for 10 gate fingers resulting in 2.4 mm of periphery. The second stage used twice the number of devices for a larger periphery of 4.8 mm. The output stage used eight devices with a larger gate width of 80 μm and 10 fingers, resulting in a periphery of 6.4 mm.

4.4 Biasing Circuits

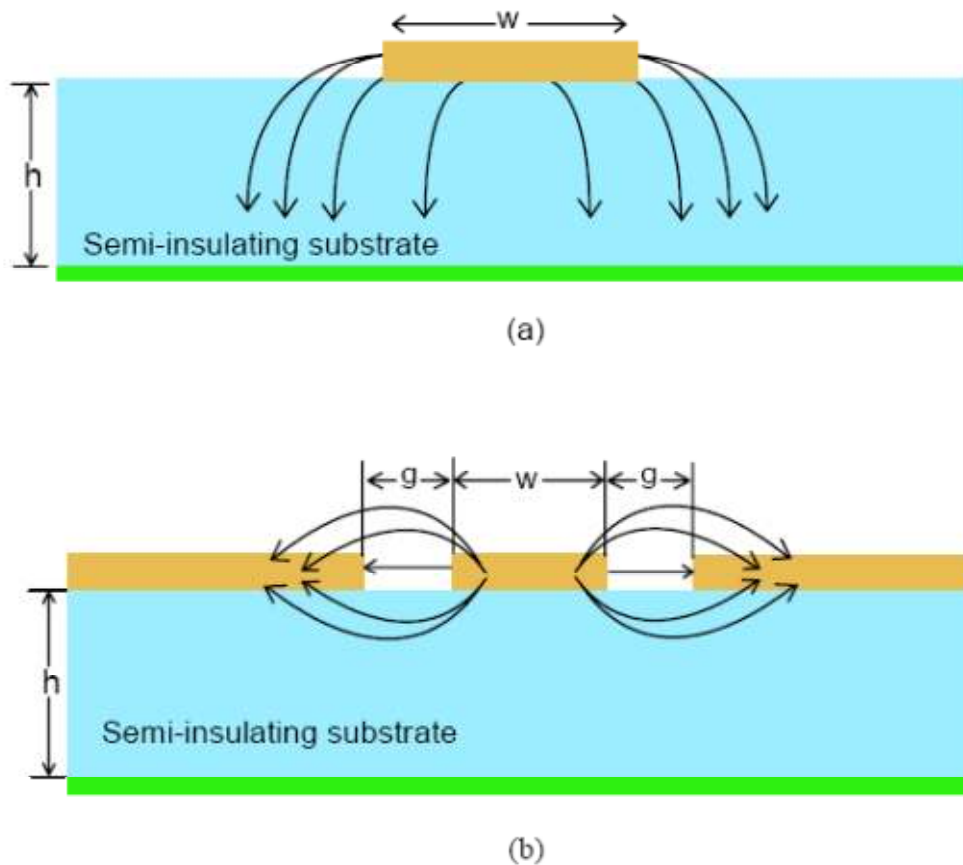
Biasing circuits for higher frequency devices are usually designed to be implemented external to the die. The more common method is to use an external bias supply that is split to supply a symmetric connection to either side of the die. This is complimented by using transmission line sizes and some on-die capacitive bypassing to provide an RF short impedance that will be seen by the gate and drain at the frequencies of interest. Unlike at lower frequencies, at 40 GHz these transmission lines can be made to present open or short impedances without a significant sacrifice in layout area. The biasing transmission lines were designed to provide a short on the die by using quarter lambda lengths and capacitors tied to ground by substrate vias.

Also necessary will be the design of structures to account for the even and odd modes prevalent in higher frequency designs that affect the stability and PAE performance of the design. On die resistors and TL structures have been used to address the mode and stability issues.

4.5 Matching Networks

The matching networks are necessary to translate the impedance of the devices with as little insertion loss as possible and provide a good match for best gain and/or power handling capability.

While there are choices as to the transmission line structure to use, most higher frequency designs use either microstrip or CPW, both of which are shown in Figure 29 [21]. While CPW has advantages of less dispersion and improved isolation, there is a size advantage to using microstrip lines. As the wafer thickness is decreased, as it is done for a substrate via process, the microstrip line width will decrease to maintain the same impedance value. On the other hand, CPW dimensions will stay the same. Thus a microstrip line approach was used instead of a CPW design. This avoids the necessity for excessive metallization that some processes require and also undesired slotline mode suppression techniques.



**Figure 29: (a) Standard Microstrip with Backside Ground Plane;
 (b) Standard CPW with Backside Ground Plane**

In order to find the best performance and lowest insertion loss a determination of the proper impedance presented to the devices needs to be evaluated. This evaluation can be initially simulated using an amplifier S-Parameter simulation DesignGuide template out of ADS called “S-Params., Noise Fig., Gain, Stability, Circles, and Group Delay”. This template’s schematic needs to be modified to reflect the device and technology of the design. The hierarchical schematics are shown in Figures 30 and 31.

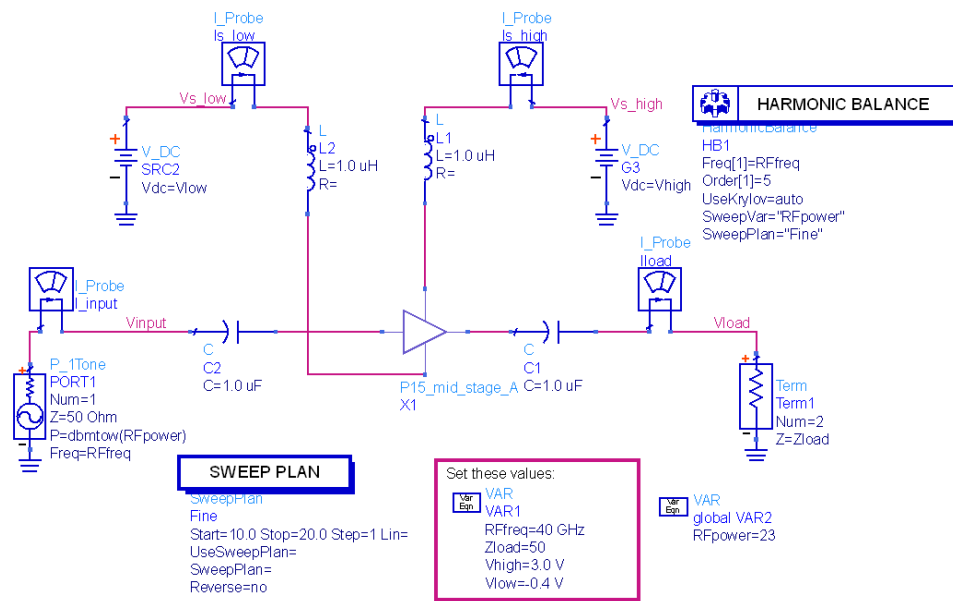


Figure 30: ADS Schematic Generated from DesignGuide

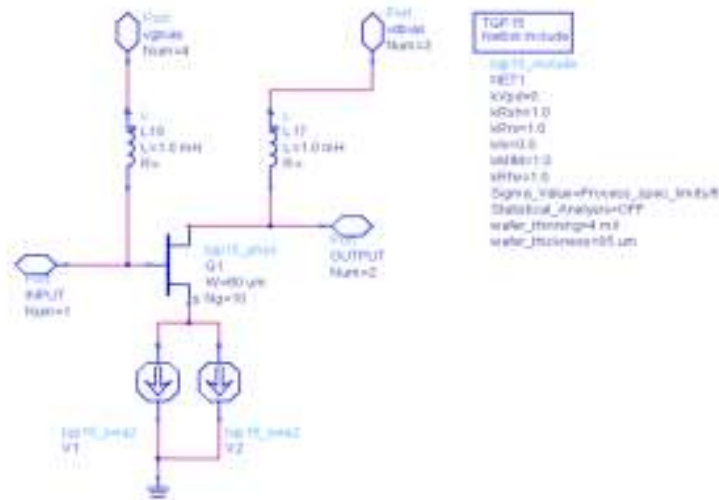


Figure 31: Symbol Topology from the Top-Level Schematic

Also, a portion of the template's display is shown in Figure 32. Within the Data Display Sheets there are several parameters plotted on multiple sheets that in this particular Design Guide are frequency dependent.

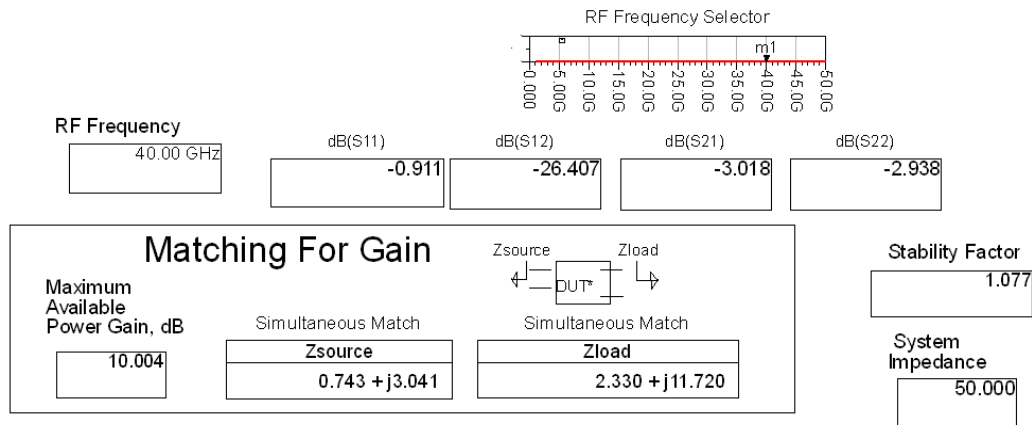


Figure 32: Data Display Generated from Simulation Template

With this information an initial design of the matching network can be performed. First a simple matching topology can be determined by plotting on the Smith Chart what the transformation needs to look like. The transformation from the low impedance output stage to a 50 Ohm environment needs to be achieved. This can be seen in Figure 33.

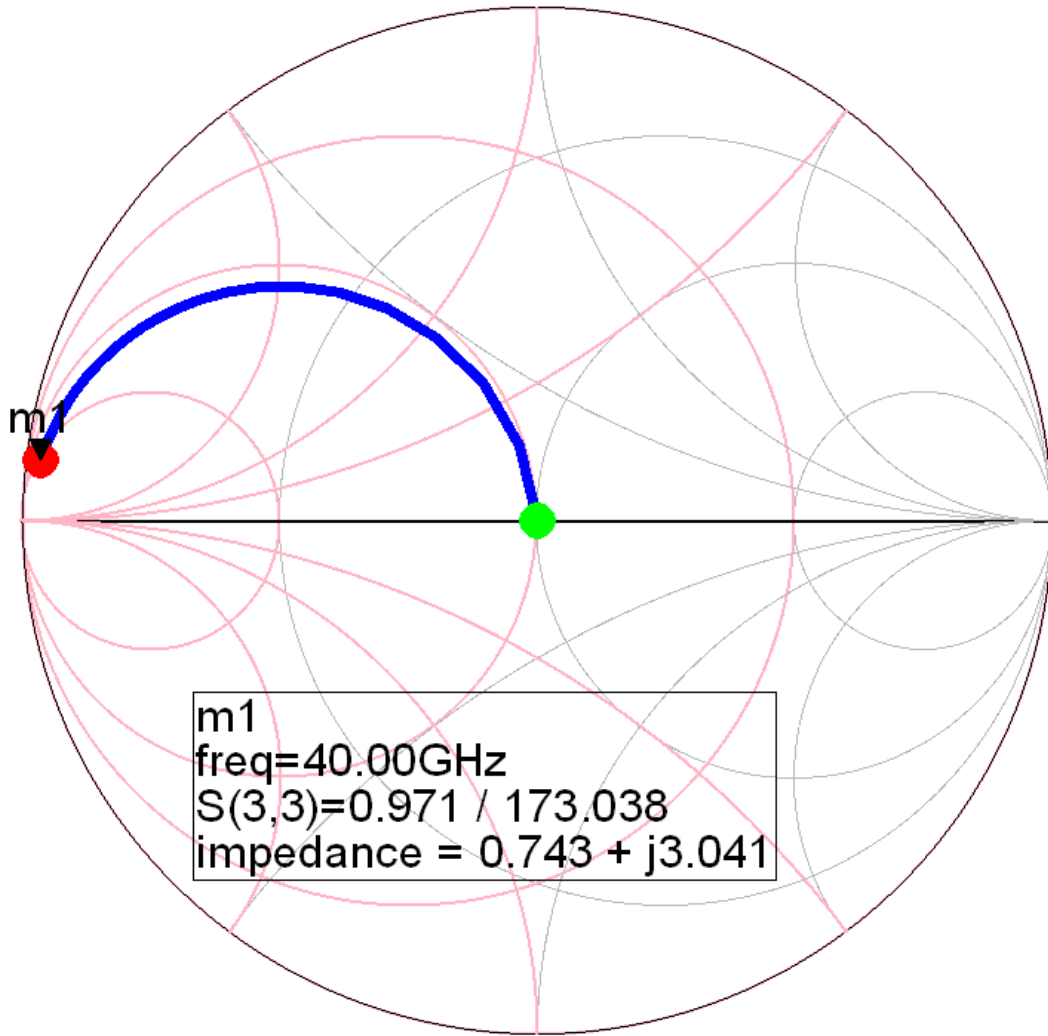
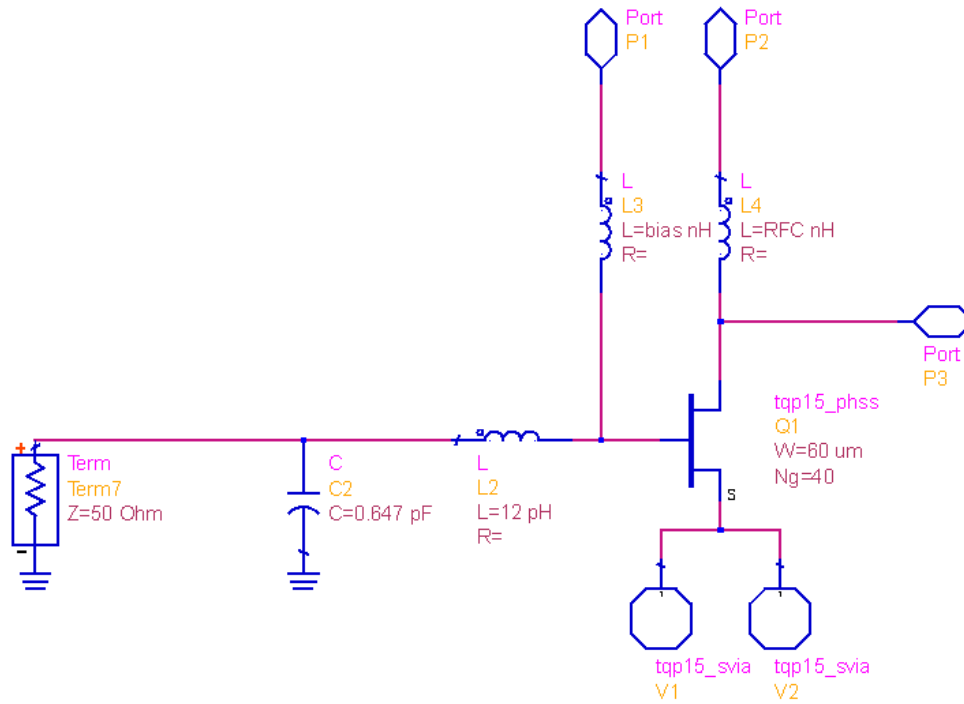


Figure 33: Simulation Determining Matching Network for a Device

In the case where the amplifier's input or output matching network is being evaluated, one termination is set to 50 Ohms. As seen in Figure 34 a simple schematic combines the peripheries of the device cell sizes into a single element. This single cell's impedance is used to determine what the impedance transformation needs to be.



**Figure 34: Simple Schematic for Designing Matching Network
(note: $N_g = 40$)**

Once a simple topology has been proven then further steps need to be undertaken to develop a workable solution. It can be noted that in Figure 34 there will need to be a blocking capacitor inserted on the input port to isolate the DC component from the test equipment and from the driving circuitry that will be present in the preceding stages.

Additionally, load pull data can be used to determine the necessary transformation for best performance for a specific bias. The contours shown in Figure 35 show the relationship between measured TOI, PAE, and P1dB over much of the Smith chart.

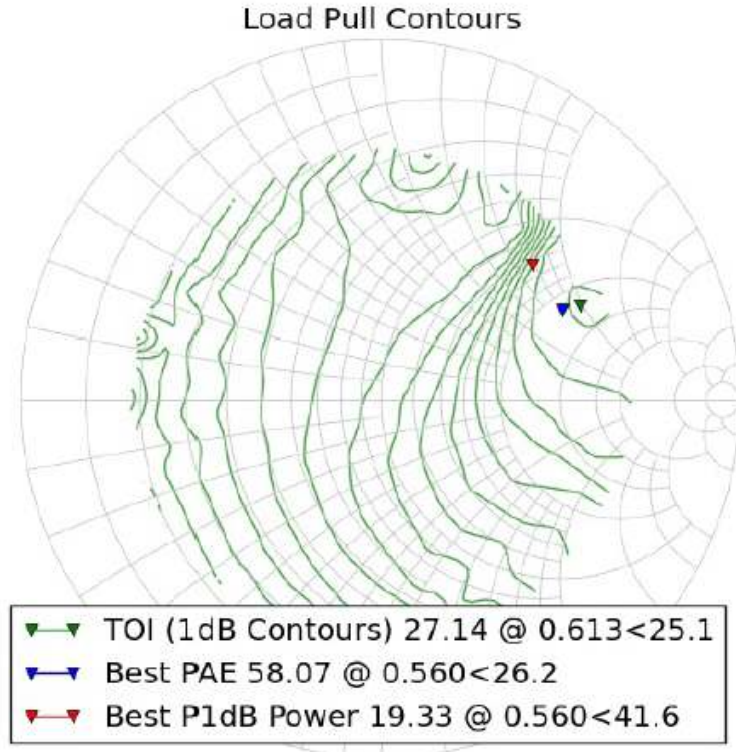


Figure 35: Load Pull Contours for Measured TOI, PAE, and P1dB

Depending upon the design specifications this simple topology may be implemented in discrete components off die or integrated on die in one of several configurations. For higher frequency implementation, as is the case in our design, the standard practice is to use transmission lines, either microstrip or CPW elements. However, making the transition from a lumped element design to a transmission line design, where the transistors are distributed, requires some additional simulation details. These include using transmission line interconnect components as well as additional resistors and capacitors to account for stability issues at higher frequencies.

An equivalent circuit comparison was used to translate the lumped element simulation to the embedded TL model structures developed for the process. These models are implemented in the design kit as elements pulled from the design palette. An intermediate step was also used since early in the design process, before all the models were verified, a generic microstrip model was used. Figure 36 shows the three different implementations of a matching network simulated using the simple discrete network, the built-in TL model, and finally to the process specific TL models that were eventually used.

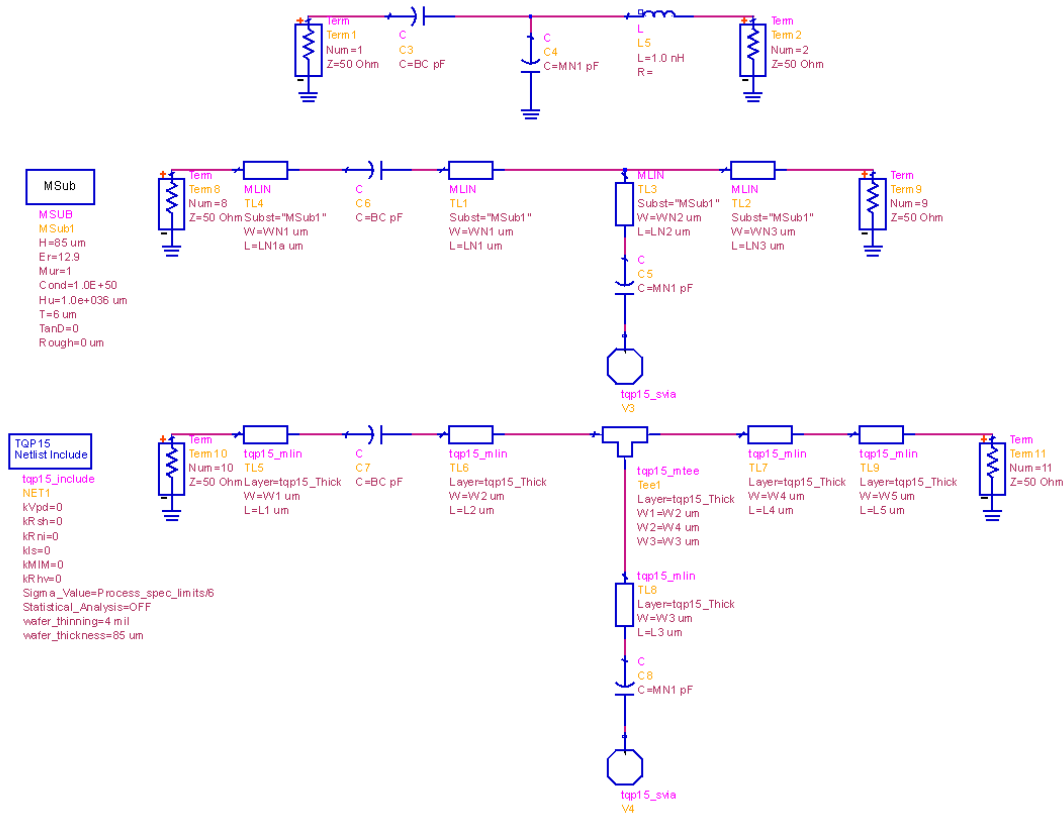


Figure 36: Progression of Lumped Element Components to TL Model

The networks described in Figure 36 can be used as simple lumped element networks where the multiple device impedances and TL structures are

collapsed to a single embodiment. This allows for a more readable schematic and also reduces the simulation time. However in the final schematic and layout, the impedance of every active device is presented to all the distributed microstrip lines. Thus a better method must be used. In Figure 37 the conjugate match of the device is used in the simulator's terminal component to present the proper impedance to each microstrip line implementation. Also, a more accurate representation of the TL structures is used. This becomes even more critical when both the input and output of the matching network is not in a 50 Ohm environment.

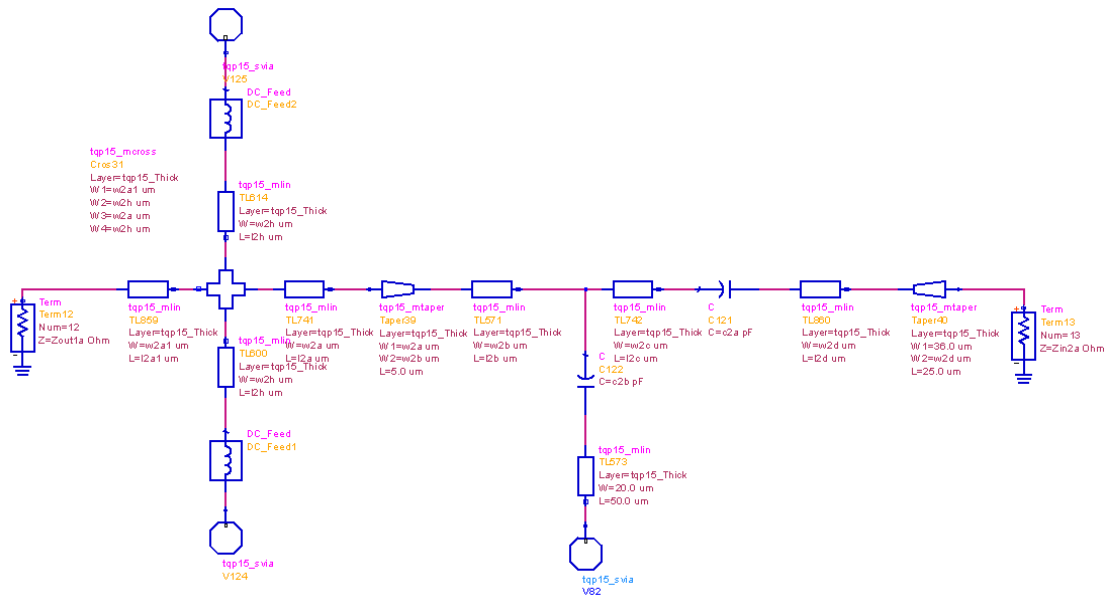


Figure 37: Matching Network Schematic with Non-50 Ohm Terminations

The layout of the interstage match as it is implemented from the simulation results is shown in Figure 38. This figure shows that for the interstage match the

structures are symmetric embodiments of the individually simulated matching networks.

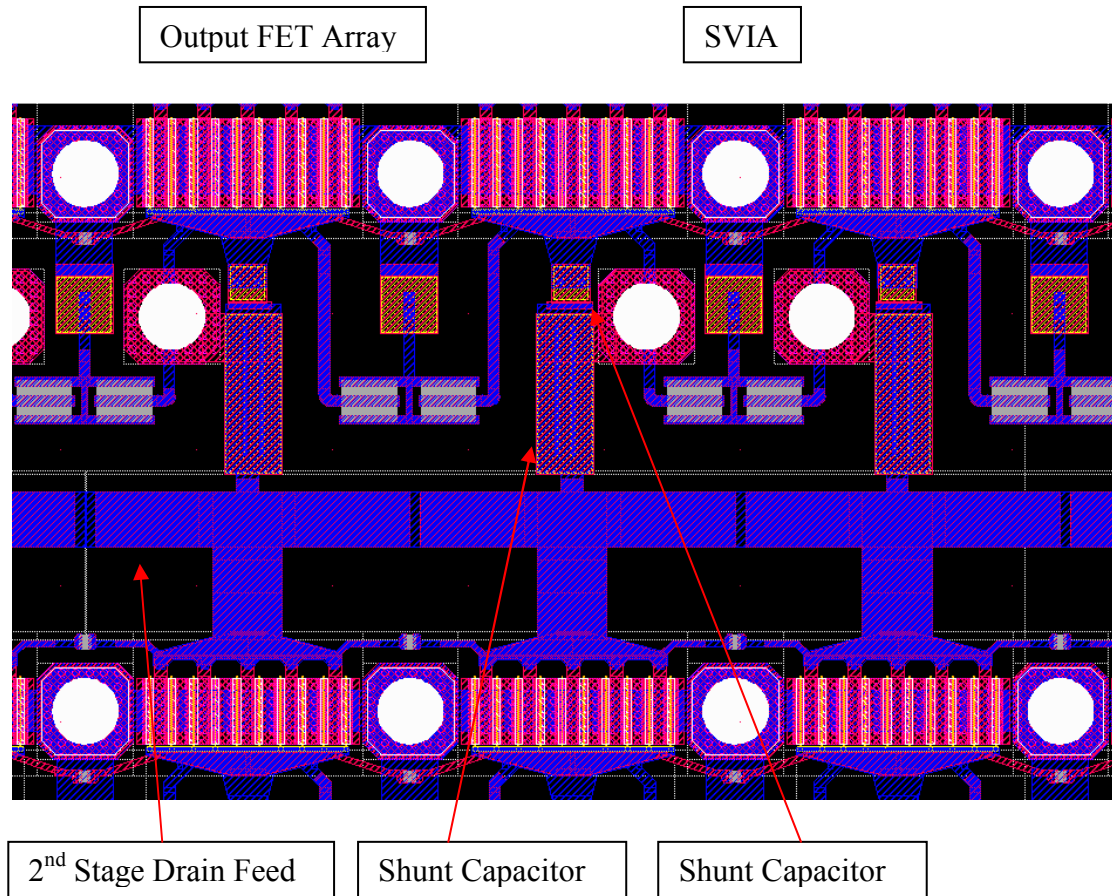


Figure 38: Layout of the Interstage Matching Network

There are many trade-offs to be considered when deciding on the best option to transform the low impedance output cell to the nominal 50 Ohm test and measurement environment. Considerations include but are not limited to bandwidth, loss, size, and flexibility.

The ability to incorporate electromagnetic (EM) simulations into the circuit simulation is a necessity. Most harmonic balance simulation software has either a resident EM simulator or the ability to import EM simulation results. The EM simulation, whether 2D or 3D, allows for another level of refinement within the simulation environment. This also allows a view of the layout that helps to visualize the port interaction. Figure 39 is a 3-D view of the layout as generated from using the layer definitions from the simulation design kit. The EM simulations are used after the layout has been roughly defined. The simulations can address coupling issues associated with the layout space constraints. The EM simulations also help determine if there are critical grounding and/or feedback issues that need to be addressed.

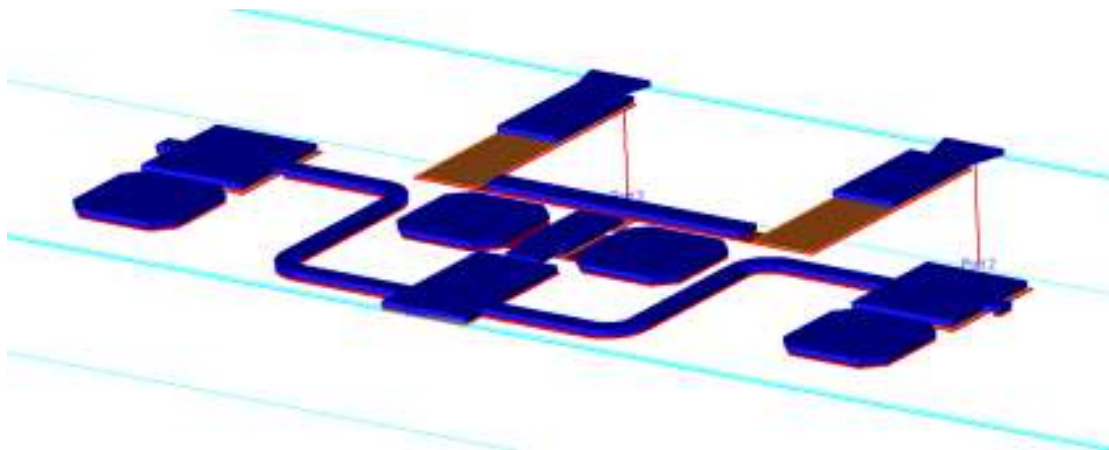


Figure 39: 3-D Pictorial of the Interstage Matching Network

4.6 Power Combining

The power combining network for an output stage needs to be designed to make the proper impedance transformation to 50 Ohms as well as handling the

required power while maintaining a low insertion loss. There are several techniques to accomplish this transformation. The design of the power combining network can take on several different topologies depending upon what specification is most important.

For an array of several parallel devices that share a common drain node, as is the case in our design, a compromise between simplicity of design and robust performance is made. A traditional two port output matching network could be constructed that can adequately perform the impedance transformation and handle the output power. However, this network relies on all the devices to see the same output matching network. This load sharing, where all the devices are directly connected to the same load, causes the devices to become susceptible to any changes from the other parallel devices.

While there are many methods of implementing a power combiner, for high frequency designs a hybrid combiner method is typically used. A hybrid combiner can be designed using several different topologies. Some embodiments are classically known as n-way power combiners or quarter-wave transformers; the type of combiner selected for this design is more commonly referred to as a corporate combiner [22] where the microstrip transmission lines are designed to perform the power combining and impedance transformation. The transmission lines were synthesized to minimize the losses associated with the microstrip structure by limiting the minimum width of the line.

The schematic of the output combiner can be examined in Figure 40 where the symmetric quarter-wave length drain bias feed (approximately 680 μm)

is also included along with its bypassing network. The output combiner was simulated and optimized by using non-50 Ohm impedances at each of the input ports. Each input port impedance was determined by measured load pull data.

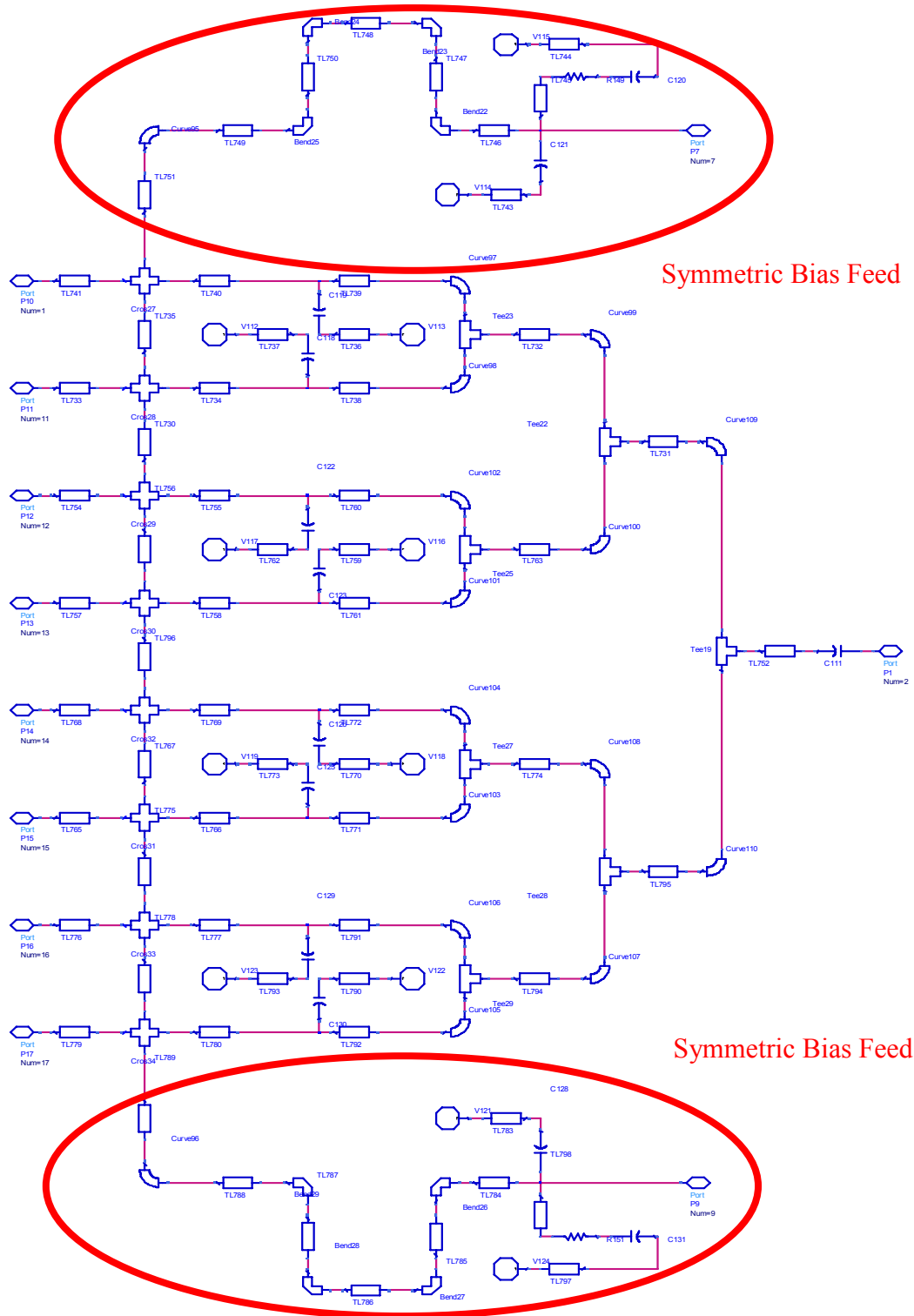


Figure 40: Multi-Port Transmission Line Simulation Schematic

Also plotted in Figure 41 are the S-Parameter simulations of the network where the ports are a conjugate match to the impedance expected at the input ports. These show a good match centered at 40 GHz as evidenced by S11 and S22 approaching -40 dB.

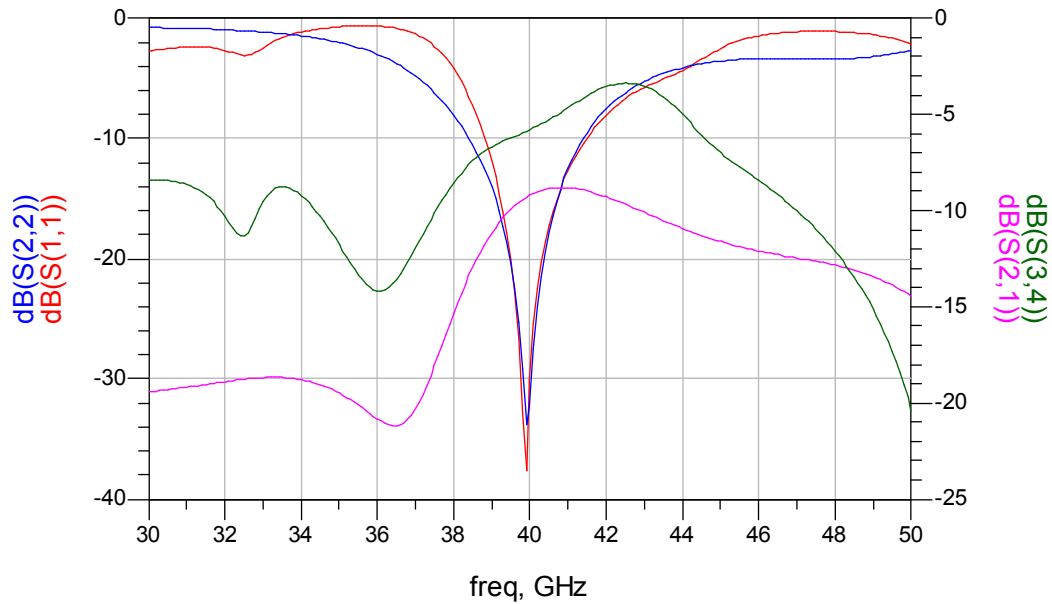


Figure 41: S-Parameter Simulations of the Power Combining Network

4.7 Final Design

The final power amplifier is based on a three-stage design. The output stage was designed to deliver over 28 dBm of output power with eight unit cells of 10 gate fingers by 80 μm . The input stage uses four unit cells and the second stage uses four. Each cell is 10x60 μm for good gain and power handling performance. The periphery of the input stage is 2400 μm^2 with periphery ratios for the three stage amplifier of 1:2:2.75. The total die size of 2.8 mm by 2.4 mm is mainly determined by the output stage's periphery and aspect ratio.

Biasing is performed external to the die where it can be controlled to account for changes in the threshold voltage of the devices. The input stage is designed to be biased as Class A for good linearity and gain. The second and output stages are biased more toward Class AB for better efficiency and power.

The output impedance of the power amplifier is low which is determined by a combination of the delivered power and also the drain voltage. At higher frequencies even more care has to be taken to consider the effects from process and power supply variations. Microstrip transmission lines were designed to provide the proper impedance transformation between stages and also for matching to the 50 Ohm environment on input and output.

The high current requirements for the drain feeds require that attention is given to the proper sizing for maximum current carrying capability and also for proper impedance characteristics. The biasing network is also symmetrically fed to minimize phase differences between the symmetric bias feed structures. The network utilizes the thin film capacitors and resistors available in the TQP15 process.

The thin film resistors are also used to suppress and prevent in-band and odd mode oscillations from occurring, especially in power combining configurations as described in [2]-[3], [7]. These resistive elements are used in series between the parallel gate terminals of the output cell array to attenuate the gate currents caused by the self resonance associated with the intrinsic parasitics of the device and its interconnect.

The layout density of the design must account for the coupling that arises in high frequency operation. Matching network topologies using microstrip line structures and a lumped element approaches are more susceptible to the coupling associated with elements in close proximity.

A low voltage high power design at high frequencies is complicated by the steep load line restrictions and the low impedance required for obtaining the required output power. The gate voltage is adjusted which determines the drain current and thus the overall system efficiency. Operation in this region as well as the matching and bandwidth limitations is more thoroughly addressed in [4].

In our final design we reached a good compromise between all of the competing requirements and managed to control all of the potential problems which were discussed above. The final block diagram of the circuit is given in Figure 42.

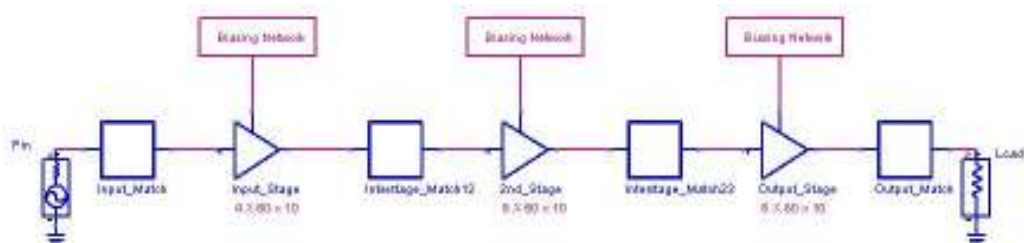


Figure 42: Simplified Block Diagram of the 3 Stage Amplifier

4.8 Layout

The final design iteration is dictated by the physical layout of the die. For a design where the size of the output stage determines one dimension of the die size, this also restricts the range of transmission line length interconnects and matching networks. And for higher frequency operations where phase is

important, the need to symmetrically distribute the bias must be properly accommodated.

Layout of the symmetrical bias network is important for the testing of the design. The pad placement must conform to the type of testing probes and also to the insertion of the device into either an automated testing fixture or mounting into a packaged environment. A picture of the die is shown below in Figure 43.

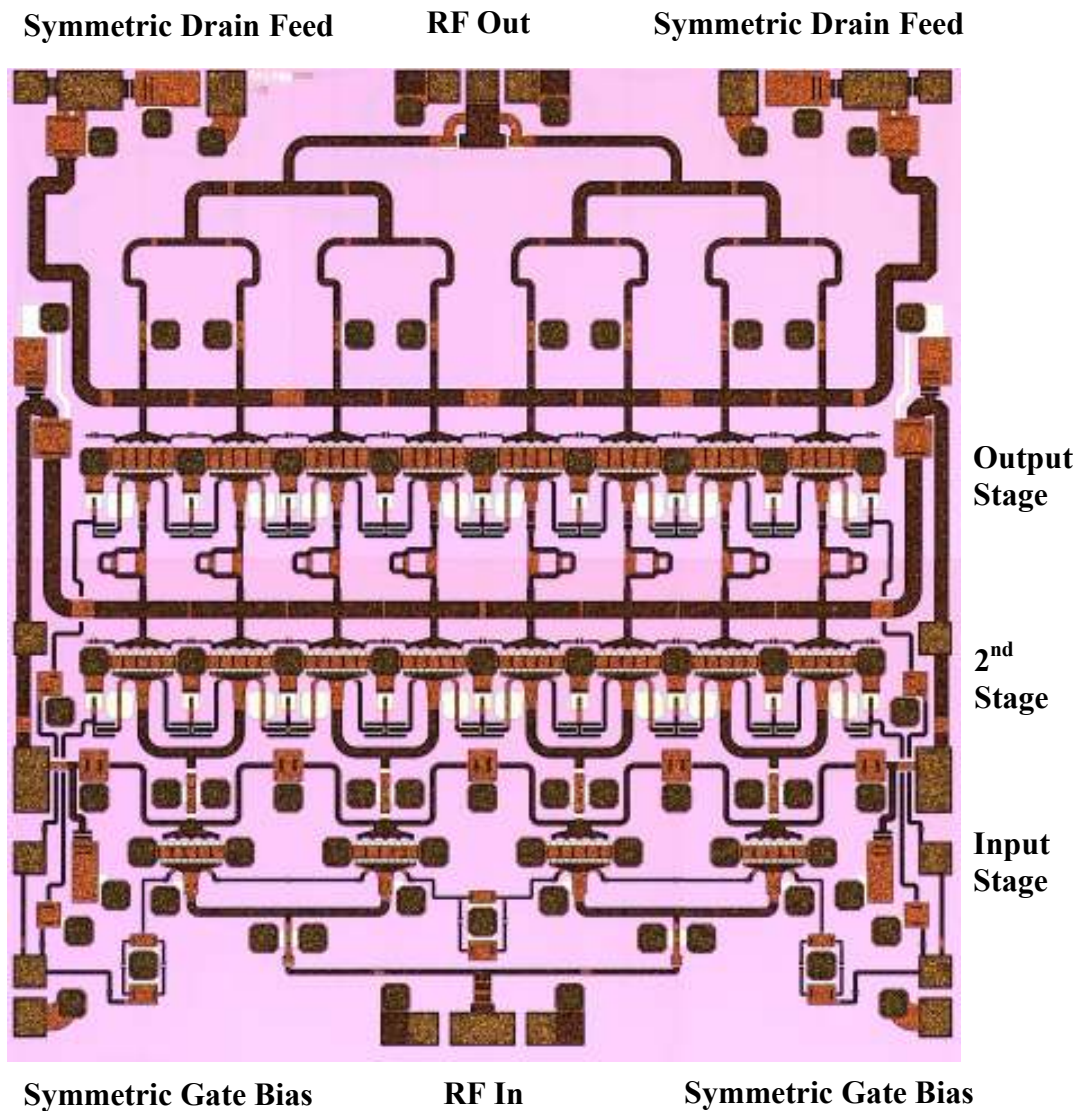


Figure 43: Photograph of the Power Amplifier MMIC, die size is 2.4x2.8 mm

Chapter 5

Power Amplifier Measurements

5.1 Testing

The design was fabricated on a standard 150 mm GaAs wafer that was processed with backside substrate via grounding structures. The dice on these wafers were sawn using a standard mechanical sawing process. Standard testing was performed on the wafers to verify the performance of the devices by evaluating the specific devices within the Process Control Monitor (PCM). The data collected from the PCM structures are published. Critical information such as the threshold voltage has been mapped as illustrated in Figure 44.

This specific wafer has an average threshold voltage that is more positive than the nominal target of -1.0 volts. Early wafer runs of an unreleased process should be expected to have some variation. For the TQP15 process the variation was within the process parameters. As the process is stabilized and centered the standard deviations will decrease and an acceptable yield will be established.

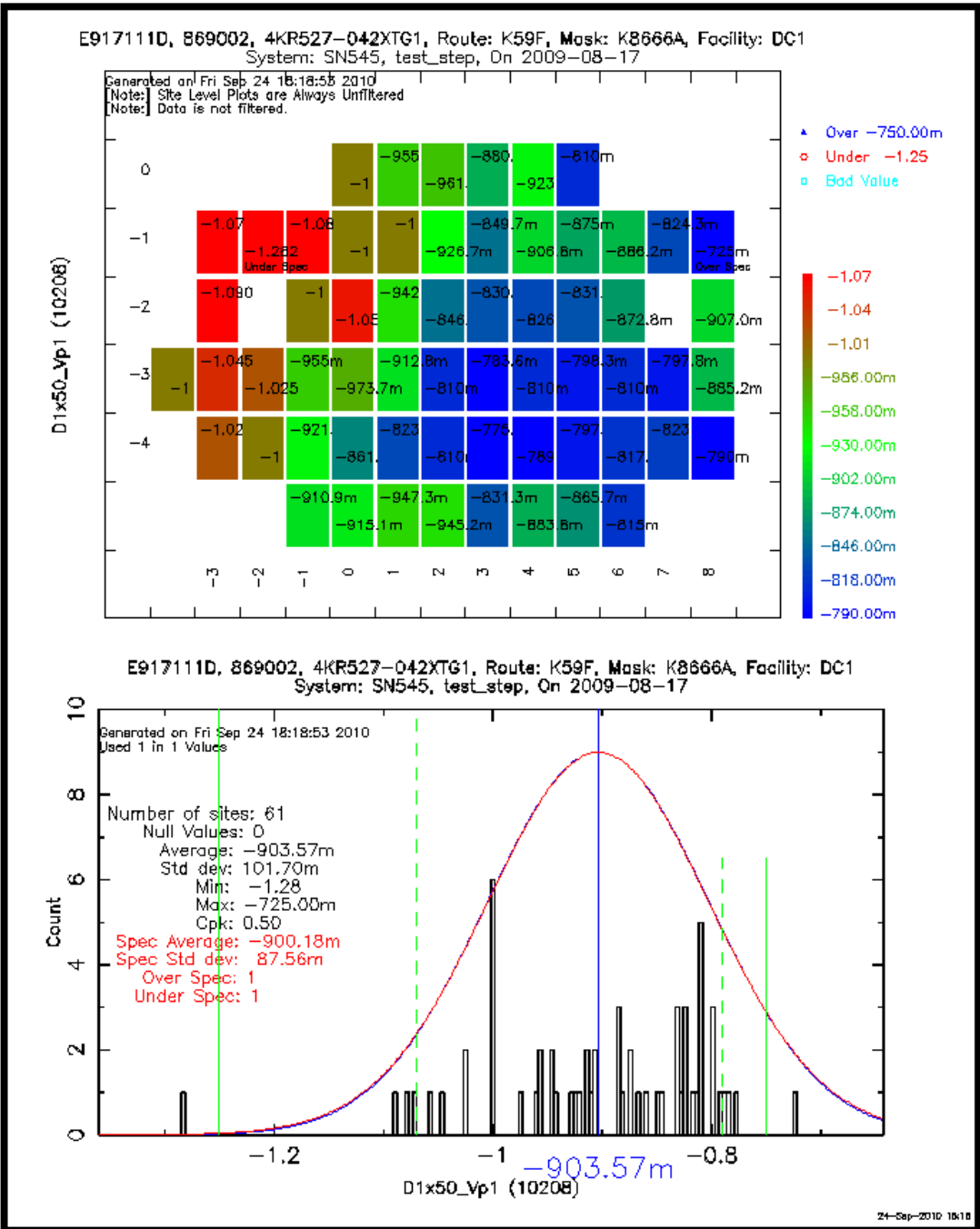


Figure 44: Wafer Map Plot of Threshold Voltage on PCM Device

The designs tested from this wafer were selected to be close to the specified nominal threshold voltage of -1.0 volts. These dice were located as close to the center of the wafer as possible.

The amplifier was tested on a wafer probe stage that was configured with RF probes where biasing was performed with both DC probes and also hard wired to DC sources. A picture of the die in its test fixture assembly where it is epoxy attached on a gold flashed carrier with epoxy grounded wire bonded bypass capacitors and probe pads is shown in Figure 45.

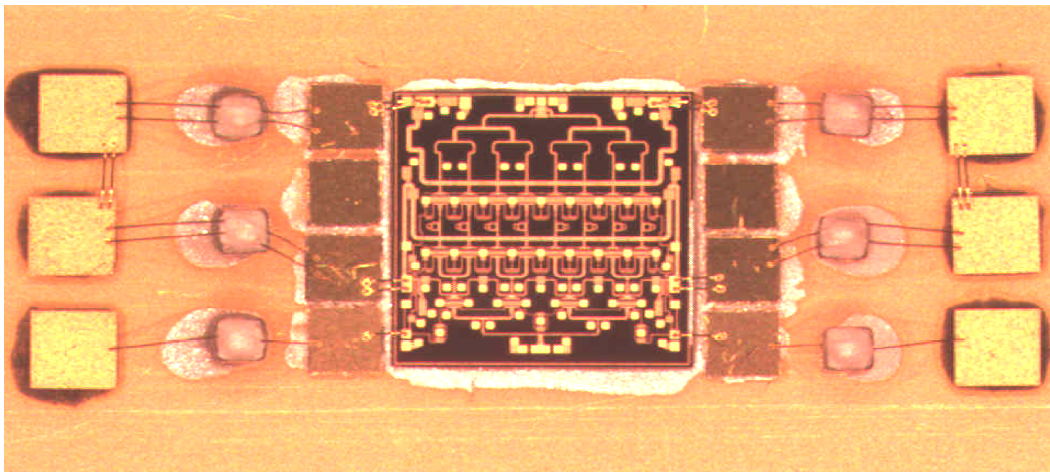


Figure 45: A Picture of the Die in Its Test Configuration

The test configuration presented an issue with losses being high enough that a reasonable 1-dB compression point could not be achieved. The RF source power at 40 GHz was not adequate and the source was entering compression before the amplifier. The measurement capability will need to be re-assessed to obtain adequate input power at a high frequency to properly determine the performance of the amplifier. Figure 45 shows a plot of the expected P_{out} versus P_{in} .

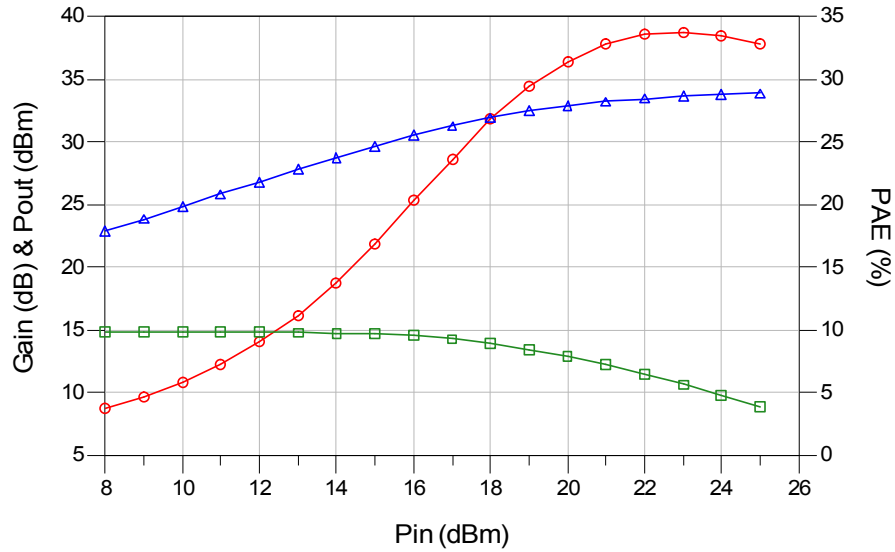


Figure 46: Simulation of Gain (squares), PAE (circles) and Pout (triangles)

Table 3: Simulated Amplifier Specifications

Frequency	Pout	Die Area	Power Density	Small Signal Gain	PAE	Vds	Idsq
(GHz)	(dBm)	(mm ²)	(mW/mm ²)	(dB)	(%)	(V)	(mA)
40	32.45	9.58	183	15	29.5	3	1655

The data plotted is the simulation of a single-ended three stage high power amplifier operating at 40 GHz from a three volt power supply. The design uses a low cost two metal layer microstrip line matching with standard MIM capacitors and 90 um substrate vias.

The amplifier was measured on a probe station where the bias lines were hardwired to the on-substrate bypassing capacitors. The equipment used was an Agilent E8257 Signal Generator, an E4448 Spectrum Analyzer, and two power supplies. The system was calibrated using an Impedance Standard

Substrate (ISS) calibration technique to de-embed the losses of the cables and interconnect up to the 40 GHz center frequency. The power measurements were recorded and plotted as shown in Figure 47.

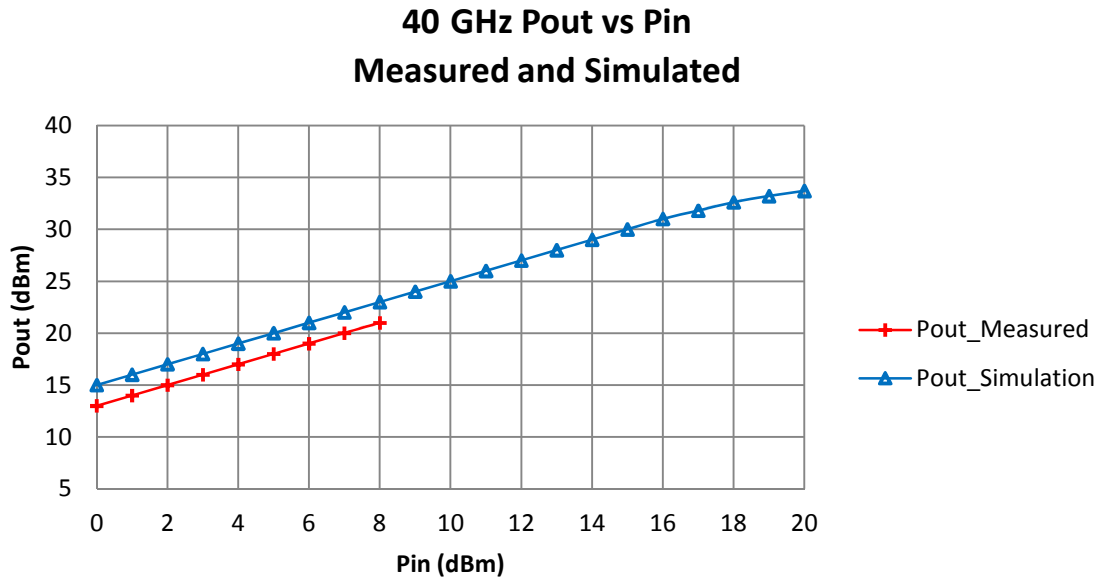


Figure 47: Measured and Simulated Pout Plot at 40 GHz

As can be seen on the plot in Figure 47 the compression point could not be achieved due to the losses inherent in the measurement system at the fundamental frequency of 40 GHz. A driver amplifier will need to be implemented on future testing. S-parameter data is not currently available since the analyzer in-house that can test to 40 GHz is heavily utilized for other projects at this time. For the limited set of data the measurements and simulations correlate well.

Chapter 6

Discussion, Conclusions, and Future Work

6.1 Discussion

The design of a high frequency power amplifier presented many challenges that were addressed outside the scope of this work. Some of these were anticipated such as the final epitaxial GaAs substrate wafer material not being defined until much later in the design. Unknown challenges such as those related to simulation were thought to be addressed but we needed some additional work to understand the model parameters that were affecting performance.

Another issue that was not expected to cause problems was related to testing the device. The high frequency equipment could not provide enough power because cabling and connector losses were higher than expected at 40 GHz plus additional padding was necessary to protect the spectrum analyzer. Also, different equipment was used at various times due to the testing time demands for the equipment. Thus new calibration files were necessary for each test configuration.

As mentioned earlier when designing a high power device at a relatively low drain voltage the load line of the device becomes more challenging to generate enough current into a low impedance. This was difficult especially when testing the device and not initially accounting for the thermal excursions of the design. It was serendipitous that the gate metallurgy provided more than

adequate margin to survive at a high junction temperature without a large performance degradation.

Another observation relates to the test environment. The initial design required several probe micromanipulators to bias and measure the amplifier. More thorough planning on the next design iteration for the test pad, both in placement and shared common pads, helped alleviate many of the testing challenges associated with the many probes and wiring harness.

6.2 Conclusions

The amplifier designed to operate at 40 GHz and at a drain voltage of 3 volts performed well and initial results were reported in [23]. While there were iterations of the design kit model during the design and manufacturing phase, these improvements help to predict the final performance of the amplifier. While no large signal measurements could be performed at this time, the goal was to achieve a working design that could be measured at the frequency of interest. Based on the available measurements for output power vs. input power we observe good agreement between predicted and measured performance. Our simulations predicted 15 dB of small signal gain and we measured 14 dB.

This project provided the opportunity to examine many different areas related to power amplifier design. In this thesis an effort has been made to touch on the most significant areas of this design such as biasing, matching and power performance. The most significant items addressed in this work include:

- Device size selection from model and load pull data

- Output combining network for power handling capability
- Interstage matching networks for proper impedance transformations
- Biasing networks for stability
- EM simulations to optimize the matching with TL structures

These challenges provided an opportunity to show methods that could result in a solution to the difficult problem of designing power amplifiers for 40 GHz and higher frequencies. The design methodology presented here can be used as a starting point for future more specialized and targeted applications.

6.3 Future Work

While this thesis has presented many different phases from background information to the design aspects related to a high frequency power amplifier, there remain many areas that can be expounded upon. There still remains many aspects of the power combiner that can be optimized and improved to allow for better insertion loss and broadband capability.

Another area to explore is the interstage matching for improved efficiency. While currently the design provides for an adequate impedance transformation it is not very process variation tolerant. This is even more critical at higher frequencies where a change in capacitance value or transmission line impedance can shift the matching enough to seriously degrade the performance. The matching could also be implemented using stub microstrip line structures, however an evaluation to assess the area increase and resulting coupling issues may be too costly or too impractical.

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