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A PWM Method for Reducing dv/dt and Switching Losses in Two-Stage Power Converters

Mahima Gupta
Portland State University, mahima@pdx.edu

Abhijeet Prem
Portland State University

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A PWM Method for Reducing dv/dt and Switching Losses in Two-Stage Power Converters

Mahima Gupta, *Member, IEEE,* Abhijeet Prem, *Student Member, IEEE*

***Abstract*—Today's semiconductor devices are accompanied by high switching frequencies (> kilo-hertz) and small transition times (< micro-seconds). Such fast transition times are accompanied by undesirable effects such as voltage overshoots at the load terminals, ground leakage currents, wide-band electromagnetic noise, etc. With the advent of wide band-gap devices, several applications are moving towards higher switching frequency operation with at-least an order of magnitude reduction in transition times. While these characteristics are considered necessary to break the next-generation barriers in power density, efficiency and applicability, the undesirable effects due to faster transitions are expected to present obstacles. This work proposes a PWM approach to modify the shape of the switching voltages to overcome the disadvantages of the fast transition times without any increase in switching losses. In fact, several of the switching transitions feature ZVS operation, resulting in reduced switching losses. The paper discusses the analytical details of the approach using a simple DC-DC boost-buck converter and extends it to a DC to three-phase AC converter using the principles of space vector modulation. The paper presents detailed simulation and comparative results in terms of voltage over-shoots over long cables, loss calculations and electromagnetic noise. Results from a laboratory-scale working prototype confirm the benefits of the proposed approach in terms of EMI and loss reduction.**

***Index Terms*—AC-DC power conversion, Capacitors, Electromagnetic interference, Losses, Pulse width modulation**

I. Introduction

THE advancements in power semiconductor devices have led to the ubiquitous presence of power electronic converters in several applications including electric drives, electrified transportation, renewable energy integration and so on for high efficiency, high performance and wide range of operation. With the emergence of wide band-gap (WBG) semiconductor devices, power electronic converters are expected to break the next barriers in power density, efficiency, and applicability. Since the 1990s, switching frequencies of 1-20kHz and switching transitions of $<1\mu s$ have been possible due to the commercial availability of silicon MOSFETs and IGBTs. In recent years, progress in silicon carbide based MOSFETs have permitted much higher switching frequency and shorter switching transitions with at least two orders of magnitude reduction [1], [2].

Due to the inherent switching operation of power electronics, the converter operation imposes high dv/dt effects as a trade-off on the applications under consideration. The high voltage stress on the converter source or the load results in several challenges including motor winding failures, bearing currents, high-frequency ground leakage currents and wide-band electromagnetic issues [3]–[6]. The state-of-the-art solutions include slowing the switching transitions by increasing the gate resistor or adding RCD snubber circuits across the switching devices. These solutions lead to increased system losses and contradict the motivation to apply fast switching devices. Other mitigation techniques such as increasing the insulation strength of the motor cables to withstand high dv/dt or utilizing switches with higher voltage safety margin have also being adopted. The most widespread solution utilizes advanced filter designs such as LCR filters [3], [7], [8], active filter designs [9]–[11], etc. The filter designs typically account of 2-3% of system losses, can occupy up-to 30% of the overall system volume, and increase system cost [1], [12]–[15]. Further, complex design processes using either computational algorithms or experimental work may need to be employed with these approaches to achieve the desired performance [16], [17].

Soft switching snubber techniques have also been studied for three-phase PWM inverters [18], [19]. In certain approaches, circulating currents from an energy recovery unit can affect the overall inverter efficiency and interfere with normal operating conditions [18]. Other approaches utilize many additional auxiliary devices including inductors, diodes, capacitors, and push-pull transformers that lead to additional losses and affect overall system volume [19]. Other solutions present the control of dv/dt rate of the semiconductor switching devices [20], [21]. In [20], external Miller capacitance control circuitry is added in order to control the dv/dt rate and an optimized weighting factor is electronically selected for loss optimization. In [21], intermediate gate voltage levels are introduced in order to control the transient rates. In these studies, trade-off exists between switching loss reduction and electromagnetic noise reduction and improvement in one specification leads to poor performance in the other. A variety of soft-switching resonant circuit techniques have been explored in the literature, which are expected to reduce the dv/dt noise [22] [23]. These techniques feature addition of capacitors, controlled switches, diodes, and inductors with complex operating modes restricting the operation boundary and limited results on quantification of EMI reduction. The class of multilevel converters including diode-clamped voltage source converters and active neutral-point clamped converters are expected to reduce electromagnetic interference issues by introducing multiple levels to the switching pole voltages [24], [25]. Hence, the dv/dt rates are reduced by reducing the numerator value, which is determined by the number of levels in the converter design. In contrast, this paper proposes

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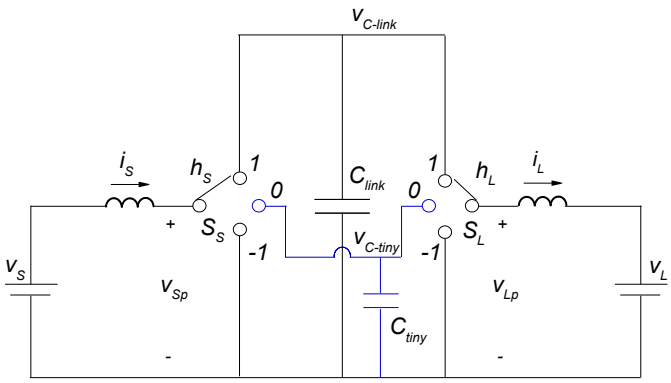

Fig. 1. Proposed topology for a DC-DC converter example. Note that the circuit modifications are highlighted in blue traces.

a PWM method with conventional two-level converters by increasing the denominator value of the dv/dt rates while reducing system losses. Note that the dv/dt rate can be tuned based on the converter design.

EMI mitigation at the EMI source, that is the semiconductor switch, is considered the most attractive pathway. This paper proposes a PWM modulation approach in order to inherently modify the shape of the switching voltages, without slowing down the semiconductor switches or increasing switching losses. In fact, the proposed approach is expected to reduce the number of instances of hard switching operation and introducing zero-voltage switching operation (ZVS). Note that the proposed PWM method can be applied to two-stage converters where the source and the load nodes connect to the intermediate energy storage element using active devices. The paper discusses the analytical details of the approach using a simple DC-DC boost-buck converter and extends it to a DC to three-phase AC converter using the principles of space vector modulation. The paper also presents the comparative results in terms of voltage over-shoots over long cables, loss reduction, and electromagnetic noise reduction.

II. DC-DC Converters

The principal ideas of the proposed approach are first described using a simple DC-DC boost-buck converter example of Figure 1 [26]. Section III discusses the details for a DC-AC converter example.

The proposed approach utilizes single-pole triple-throw (SPTT) switches, instead of the classical single-pole double-throw (SPDT) switches, to connect the source and the load to the intermediate DC-link capacitor (C_{link}), annotated as S_S and S_L in the figure. The additional throw of the switches, annotated with state "0", connects to a *tiny* capacitor (C_{tiny}) and is utilized to smoothen the high dv/dt transitions of the switch pole voltages, v_{Sp} and v_{Lp}, without additional switching losses, as described in the next few subsections.

A. Operation

1) Boost Operation: In contrast to the classical PWM approach where the source and load switches, S_S and S_L,

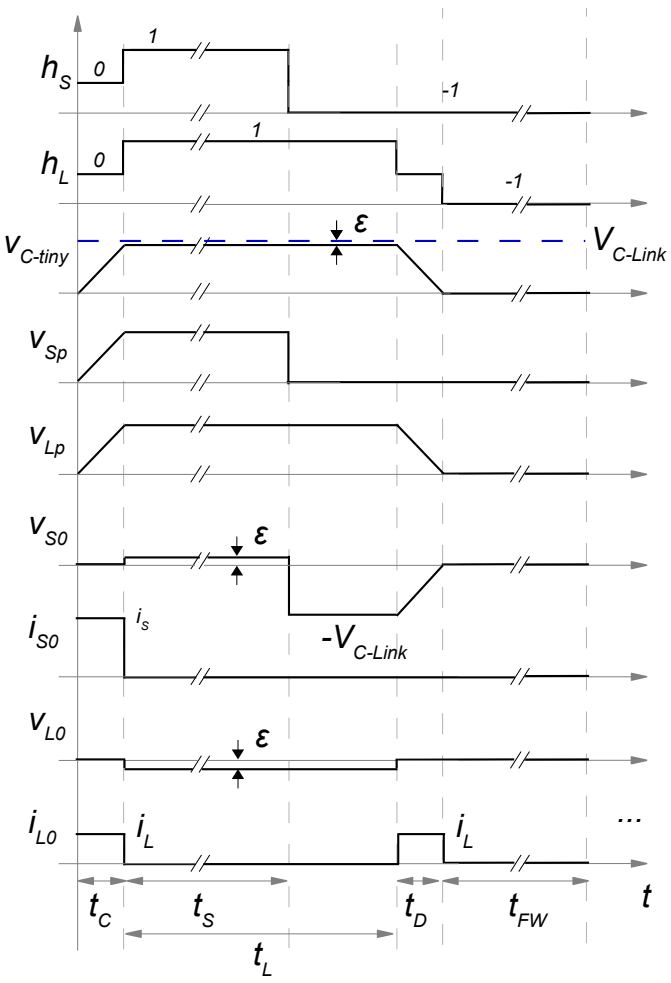

Fig. 2. Waveforms of the switching functions (h_S and h_L), tiny capacitor voltage (V_{C-tiny}), source and load side pole voltages (v_{Sp} and v_{Lp}), and voltage, current waveforms of state "0" throws (v_{S0}, i_{S0} and v_{L0}, i_{L0}) during boost mode of operation.

may or may not be synchronized, the switches are sequenced and synchronized as illustrated in Figure 2. At the start of the switching interval, during charge time t_C, the switch poles first connect to throw "0" and C_{tiny}, which is at zero volts. The net capacitor current ($i_S - i_L$) charges the tiny capacitor from zero voltage until the voltage is approximately equal to the DC-link voltage V_{C-link}. Hence, the switch pole voltages, v_{Sp} and v_{Lp}, feature a low *tunable* dv/dt rising edge, also highlighted in Figure 2. Next, the switches transition to "1" state where they connect to the DC-link capacitor C_{link} for the conventional power transfer operation. Note that this transition from state "0" to state "1" happens with zero-voltage switching (ZVS) at the source and the load, since $v_{C-tiny} \approx V_{C-link}$. The difference in the voltages between v_{C-tiny} and V_{C-link} at this instant is denoted as ϵ. The magnitude of $\epsilon \to 0$ and will be determined based on the control and hardware implementation. In the figure, the DC-link capacitor voltage V_{C-link} features low voltage ripple since the DC-link capacitor is assumed to be large enough for stiff operation.

While the source transfers the power for t_S duration, the load remains connected for t_L duration in order to complete

the power transfer process for boost operation. These time-intervals are predominantly determined by the conventional PWM operation, also discussed in Section II-B. Under boost operation, the source switch has a shorter active interval and enters the inactive freewheeling state after t_S duration. Subsequently, the load transitions to state "-1" from state "1" through state "0" where C_{tiny} is discharged to zero by the load current i_L. During the active to the inactive freewheeling state transition, only the load switch dv/dt transition edge features a low dv/dt rate. The source switch witnesses a hard high dv/dt transition. The remaining period (t_{FW}) is completed by the inactive freewheeling state where both the source and load remain in switch state "-1" and freewheel. The time intervals of the low dv/dt transitions, t_C and t_D, have been exaggerated in Figure 2 for illustration purposes only.

2) Buck Operation: Under buck operation, the source switch has a longer active interval as compared to the load switch. In addition, the net current ($i_S - i_L$) is a negative value. Hence, in contrast to the boost mode of operation, the buck mode begins by the connection of only the source switch to the throw "0" and C_{tiny}, which is at zero volts. The net capacitor current during t_C, which is i_S, charges the tiny capacitor from zero voltage until the voltage is approximately equal to the DC-link voltage V_{C-link}. Hence, the source switch pole voltage, v_{Sp}, features a low dv/dt rising edge, also highlighted in Figure 3. Next, the switch transition to "1" state where it connects to the DC-link capacitor C_{link} for the conventional power transfer operation. Note that this source transition from state "0" to state "1" happens with zero-voltage switching (ZVS) since $v_{C-tiny} \approx V_{C-link}$.

While the source transfers the power for t_S duration, the load connects to the DC-link voltage V_{C-link} for t_L duration. During the zero to active state load transition, the load switch witnesses a hard high dv/dt transition. After the completion of the power transfer process, both the source and the load transition to state "-1" from state "1" through state "0", where C_{tiny} is discharged to zero by the net negative current of (i_S-i_L). During the active to inactive freewheeling state transition, both the source and the load switch dv/dt transition edge features a low dv/dt rate. The remaining period (t_{FW}) is completed by inactive freewheeling state, where both the source and load remain in switch state "-1" and freewheel. Again, the time intervals of the low dv/dt transitions, t_C and t_D, have been exaggerated in Figure 3 for illustration purposes only.

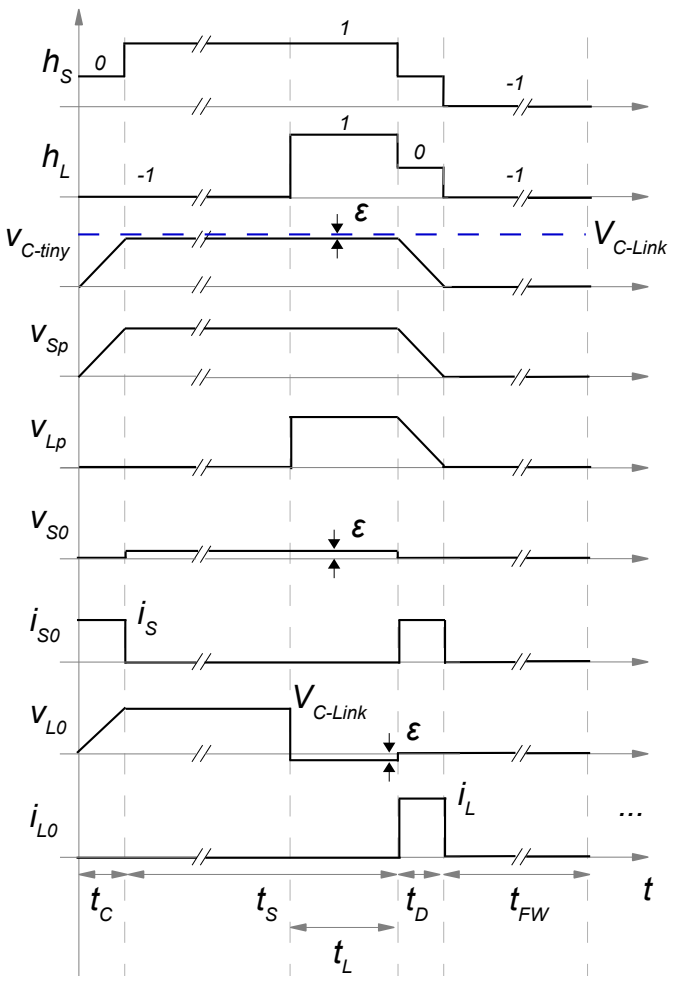

Fig. 3. Waveforms of the switching functions (h_S and h_L), tiny capacitor voltage (V_{C-tiny}), source and load side pole voltages (v_{Sp} and v_{Lp}), and voltage, current waveforms of state "0" throws (v_{S0}, i_{S0} and v_{L0}, i_{L0}) during buck mode of operation.

Boost:

$$t_C = \frac{d_C}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_S - i_L} \tag{1}$$

$$t_D = \frac{d_D}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_L} \tag{2}$$

Buck:

$$t_C = \frac{d_C}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_S} \tag{3}$$

$$t_D = \frac{d_D}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_L - i_S} \tag{4}$$

where, f_{SW} is the switching frequency, V_{C-link} is the DC-link capacitor voltage, i_S and i_L are the source and load currents respectively and d_C and d_D are the corresponding duty ratios of the charge and discharge time intervals. A selected value of C_{tiny} will impose a range of values for the tuned transition rates dv/dt and the t_C and t_D time intervals that are also a function of the operating conditions of the converter. In order to account for the t_C and t_D intervals in the source and the load duty ratios, equations (5)-(8) can be calculated as shown using linear duty ratio expressions.

B. Duty ratio calculation

With the proposed approach, the dv/dt rate can now be designed based on overall application requirements. To emphasize, the switching losses do not increase due to dv/dt tuning and will be discussed in detail in Section II-E and Section III. The transition time intervals t_C and t_D will determine the rate of rise of the switching pole voltages (v_{Sp} and v_{Lp}) and can be calculated based on the capacitor equation, $C_{tiny}\frac{dv_{C-tiny}}{dt} = i_{tiny}$, as shown in (1)-(4).

Boost:

$$t_S = \frac{d_S}{f_{SW}} \approx \frac{v_S}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C}{2}}_{\text{small}} \tag{5}$$

$$t_L = \frac{d_L}{f_{SW}} \approx \frac{v_L}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C + t_D}{2}}_{\text{small}} \tag{6}$$

Buck:

$$t_S = \frac{d_S}{f_{SW}} \approx \frac{v_S}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C + t_D}{2}}_{\text{small}} \tag{7}$$

$$t_L = \frac{d_L}{f_{SW}} \approx \frac{v_L}{f_{SW} V_{C-link}} - \underbrace{\frac{t_D}{2}}_{\text{small}} \tag{8}$$

where, v_S and v_L are the source and load voltages respectively and d_S and d_L are the corresponding duty ratios to time intervals t_S and t_L as annotated in Figure 2 and Figure 3. While the t_C and t_D time intervals could be designed based on application specifications, they are expected to be relatively small as compared to the power transfer time intervals of the source (t_S) and the load (t_L) and could potentially be ignored. Equation (1)-(4) can be rearranged to obtain Equation (9)-(10) to design a value of C_{tiny} and tune the dv/dt rate for the desired transition times and as per the specifications of the application under consideration.

Boost:

$$C_{tiny} \approx \frac{t_C(i_S - i_L)}{V_{C-link}} \approx \frac{t_D i_L}{V_{C-link}} \tag{9}$$

Buck:

$$C_{tiny} \approx \frac{t_D(i_L - i_S)}{V_{C-link}} \approx \frac{t_C i_S}{V_{C-link}} \tag{10}$$

C. Device Ratings

The proposed additional throw with state "0" of the two SPTT switches can be realized using the conventional power semiconductor switches such as MOSFETs, IGBTs and diodes but with significantly lower overall ratings. In order to determine the optimized realization, Figure 2 and Figure 3 also illustrate the voltage and current waveforms of the throw "0", as annotated by v_{S0}, i_{S0} and v_{L0}, i_{L0} for the source and the load respectively. Figure 4 illustrates the switch realizations for the two modes of operation for unidirectional and bidirectional power flow using MOSFETs and diodes. Table I lists the peak voltage and RMS current ratings of the additional devices in order to optimize device VA ratings.

Considering the boost mode of operation, the source throw "0" blocks bidirectional voltage. Hence, the throw may be realized using a series connection of a MOSFET and a diode. While the diode will be rated for the voltage blocking capability of V_{C-link}, the voltage rating of the MOSFET is $\epsilon \to 0$. In contrast, the load throw "0" witnesses negative blocking voltage. Hence, the load throw is realized using only a diode with minimal blocking voltage requirement of ϵ. Similarly, considering the buck mode of operation, the source throw "0" blocks positive voltage of ϵ. Hence, the throw may be realized using a single MOSFET. The load throw "0" witnesses bidirectional blocking voltage and requires a series connected MOSFET and a diode. Again, the diode will be rated for the voltage blocking capability of V_{C-link}. Irrespective of the mode of operation, the RMS current ratings of the devices are determined by the source and the load currents. It may be noted that the RMS currents are significantly smaller than rated current magnitudes since the throw "0" conducts for a very small time interval, also discussed in Section II-B. For converters requiring bidirectional power flow, two transistor devices with anti-parallel diodes are necessary, also shown

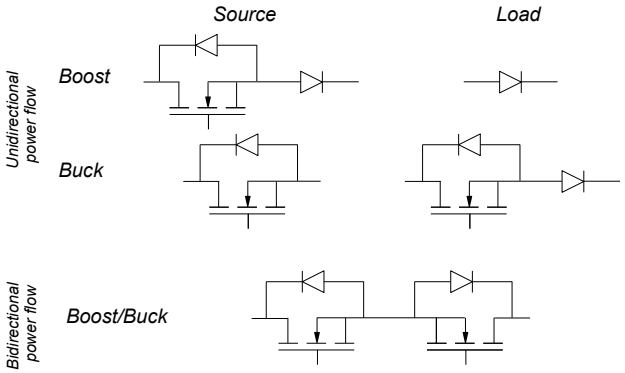

Fig. 4. Switch realizations for the state "0" throw for boost and buck mode of operation with unidirectional and bidirectional power flow.

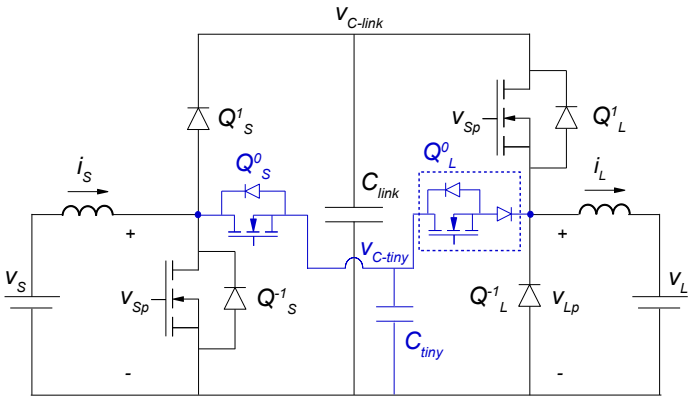

Fig. 5. Circuit schematic of the proposed DC-DC converter with buck mode of operation and unidirectional power flow. Note that the switch additions are highlighted in blue traces.

TABLE I
PEAK VOLTAGE AND RMS CURRENT RATINGS OF THE SWITCHES OF THE ADDITIONAL THROW FOR BOOST AND BUCK MODE OF OPERATION.

Mode		Source throw "0"		Load throw "0"	
		MOSFET	Diode	MOSFET	Diode
Boost	Voltage	$\epsilon \to 0$	V_{C-link}	-	$\epsilon \to 0$
	Current	$i_S\sqrt{d_C}$		$i_L\sqrt{d_C + d_D}$	
Buck	Voltage	$\epsilon \to 0$	-	V_{C-link}	$\epsilon \to 0$
	Current	$i_S\sqrt{d_C + d_D}$		$i_L\sqrt{d_D}$	
				Note: $d_C, d_D << 1$	

TABLE II
VA RATING OF THE SEMICONDUCTOR DEVICES WITH BUCK MODE OF OPERATION PER-UNITIZED OVER THE INPUT POWER.

Device	Voltage	Current	VA (p.u.)
Conventional Devices			
Q_S^1	V_{C-link}	$\sqrt{d_S}I_S$	$\frac{1}{\sqrt{d_S}}$
Q_S^{-1}	V_{C-link}	$\sqrt{d'_S}I_S$	$\frac{\sqrt{d'_S}}{d_S}$
Q_L^1	V_{C-link}	$\sqrt{d_L}I_L$	$\frac{1}{\sqrt{d_L}}$
Q_L^{-1}	V_{C-link}	$\sqrt{d'_L}I_L$	$\frac{\sqrt{d'_L}}{d_L}$
Additional Devices			
Q_S^0	ϵ	$\sqrt{d_C+d_D}I_S$	$\frac{\epsilon}{V_S}\sqrt{d_C+d_D}$
Q_L^0	V_{C-link}	$\sqrt{d_D}I_L$	$\frac{\sqrt{d_D}}{d_L}$
			Note: $\frac{\epsilon}{V_S} << 1$, $\frac{d_D}{d_L} << 1$

in Figure 4. Figure 5 illustrates the circuit schematic of the proposed DC-DC converter with buck mode of operation and unidirectional power flow. Note that the switch additions are highlighted in blue traces. Similar circuit schematics can be derived using Figure 4 and Table I for various other design scenarios.

Table II details the VA calculation comparison for buck mode of operation by extending the results obtained in Table I. The table lists the VA ratings of the conventional and the additional devices per-unitized (p.u.) over the input power. Note that while the peak voltage ratings of the additional devices can be as high as the DC voltage value, RMS current ratings will be a fraction of the ratings of the existing switches. Considering the design example analyzed in the study, the transition times are tuned to approximately $1\mu s$ for a 15kHz switching frequency. Hence, $\frac{d_D}{d_L} << 1$. Further, $\epsilon \rightarrow V_{C-link}$ Hence, $\frac{\epsilon}{V_S} << 1$. In summary, the net VA rating of the additional devices are expected to be a fraction of the conventional devices. Section IV details the numerical results for the design example under consideration.

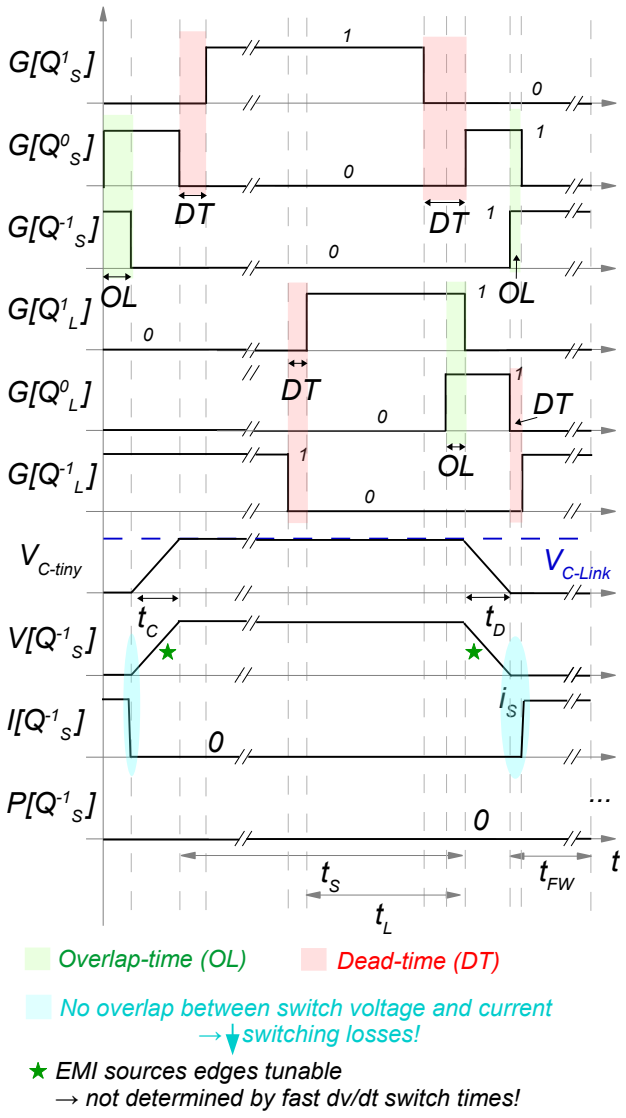

Fig. 6. Waveforms of the gate signals of the source and load switches ($G[Q_y^x]$, where $x = -1, 0, 1$ and $y = S, L$), tiny capacitor voltage (V_{C-tiny}), and the voltage, current and power waveforms of the source side bottom transistor ($V[Q_S^{-1}], I[Q_S^{-1}], P[Q_S^{-1}]$) with buck mode of operation.

D. Commutation during states "1" ↔ "0" ↔ "-1"

Figure 2 and Figure 3 illustrate simplified switching functions of the SPTT switches of Figure 1 where the focus is on basic converter operation. This section discusses commutation strategies with the proposed PWM method. Figure 6 demonstrates the gate drive signals for the transistor realizations using a buck mode of operation and circuit schematic of Figure 5. Similar extensions are feasible for boost operation (not included in the paper for brevity). Here, Q_y^x refers to device Q with state x, where $x = -1, 0, 1$, and y refers to source or the load side where $y = S, L$. The devices may be realized either using a single MOSFET device, a diode device, or their series combination. The commutation strategy of the figure assumes the use of common-source connected bidirectional MOSFET devices of Figure 4 for universal power flow. Optimized switch configurations are feasible, in which case certain controlled gate driver signals will be redundant and may not be used.

During the buck mode of operation, the charge interval of the tiny capacitor (t_C) involves the transition of S_S : " -1" $\rightarrow$ "0" $\rightarrow$ "1". Considering the direction of the source current, the device transition involves the turning-off of the Q_S^{-1} transistor and the turn-on of the anti-parallel diode of Q_S^1. Soon after $G[Q_S^{-1}] = 0$, if the state "0" transistor is not turned-on, the anti-parallel diode of Q_S^1 will begin to conduct to provide a path for the stiff pole current. Hence, the transition from state " -1" $\rightarrow$ "0" involves an overlap time (OL), as noted in the figure. It may be worth noting that only after $G[Q_S^{-1}] = 0$, the tiny capacitor begins to charge. The end of the charge interval is marked by when, $V_{C-tiny} \approx V_{C-Link}$ after which the anti-parallel diode of Q_S^1 becomes forward-biased and turns-on. Consequently, $G[Q_S^1] = 1$ after a dead-time (DT) interval.

The discharge interval of the tiny capacitor (t_D) involves the transition of both S_S and S_L : "1" $\rightarrow$ "0" $\rightarrow$ " -1".

TABLE III
ZERO-VOLTAGE SWITCHING INSTANCES WITH THE PROPOSED APPROACH FOR BOOST AND BUCK MODE OF OPERATION.

Mode	State	Source side	Load side
Boost	$S_{-1} \rightarrow S_0$	S_{-1} ZVS off, S_0 ZVS on	
	$S_0 \rightarrow S_1$	S_0 ZVS off, S_1 ZVS on	
	$S_1 \rightarrow S_{-1}$	Hard switching	-
	$S_1 \rightarrow S_0$	-	S_1 ZVS off S_0 ZVS on
	$S_0 \rightarrow S_{-1}$	-	S_0 ZVS off S_{-1} ZVS on
Buck	$S_{-1} \rightarrow S_0$	S_{-1} ZVS off S_0 ZVS on	-
	$S_0 \rightarrow S_1$	S_0 ZVS off S_1 ZVS on	-
	$S_{-1} \rightarrow S_1$	-	Hard switching
	$S_1 \rightarrow S_0$	S_1 ZVS off, S_0 ZVS on	
	$S_0 \rightarrow S_{-1}$	S_0 ZVS off, S_{-1} ZVS on	

First, considering the load side switch, the device transition involves the turn-off of the Q_L^1 transistor and the turn-on of the anti-parallel diode of Q_L^{-1}. Soon after $G[Q_L^1] = 0$, if the state "0" transistor is not turned-on, the anti-parallel diode of Q_L^{-1} will begin to conduct to provide a path to the stiff load current. Hence, the transition from state "1" $\rightarrow$ "0" involves an overlap time (OL), as noted in the figure, followed by the dead-time for $G[Q_L^{-1}]$. At the source side switch, even after $G[Q_S^1] = 0$, the anti-parallel diode will continue to conduct. Hence, $G[Q_S^1]$ and $G[Q_S^0]$ feature a dead-time. When $G[Q_S^0] = 1$, the top diode becomes reverse-biased and Q_S^0 begins to conduct. Finally, $G[Q_S^0]$ and $G[Q_S^{-1}]$ feature an overlap time to prevent the turn-on of the top anti-parallel diode like in the conventional case. The discharge interval (t_D) begins with the turn-off of Q_L^1 after which the load current begins to discharge the tiny capacitor via Q_L^0. The end of the discharge interval is marked by when, $V_{C-tiny} \approx 0$ after which the anti-parallel diode of Q_L^{-1} turns-on and takes over. Note that the role of the diode device of Q_L^0 in Figure 5 is to block the small voltage difference ϵ during the load side active state, also noted in Figure 3. The next section discusses zero-voltage switching operation illustrated by the remaining bottom switch waveforms of the figure and summarizes the results.

E. Summary

As noted in Section II-A, several of the switch transitions occur under ZVS. Figure 6 highlights ZVS operation for source bottom switch, Q_S^{-1}, during buck mode of operation. Considering the capacitor charge operation, Q_S^{-1} is "on" prior to the t_C and conducts the source current, I_S. When Q_S^{-1} is turned-off, switch Q_S^0 takes over and Q_S^{-1} blocks V_{C-tiny} which is slowly charged from 0V. Hence, the switching time instants with simultaneously high current conduction and high voltage blocking are eliminated, resulting in ZVS operation.

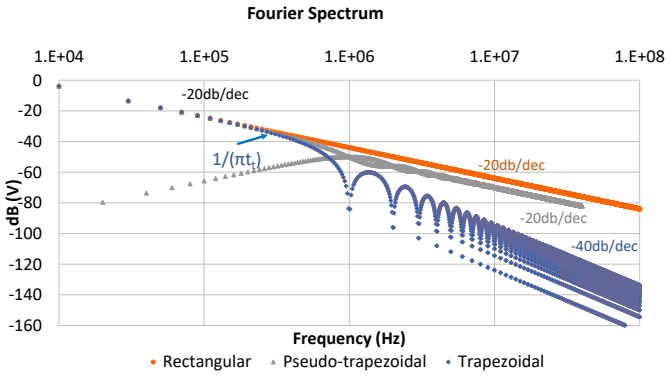

Fig. 7. Fourier spectrum of pole voltages with rectangular, pseudo-trapezoidal and trapezoidal shapes.

Similarly, during the capacitor discharge operation, Q_S^{-1} is "off" prior to the t_D and blocks the bus voltage, V_{C-bulk}. Q_S^{-1} is turned-on only after Q_S^0 and Q_L^0 are utilized to discharge the tiny capacitor to 0V. Again, the switching time instants with simultaneously high current conduction and high voltage blocking are eliminated. Similar extensions are possible for other switching transitions and modes of operation. Table III provides a comprehensive summary. It can be observed that out of a total of seven switching instances between states "-1", "0" and "1", six instances are under ZVS. In other words, out of the four fast transitions of the switching voltages v_{Sp} and v_{Lp} with conventional PWM, three transitions can be shaped with the desired dv/dt rate. On the other hand, in the conventional case, all the switching instances are hard-switching. In summary, together with reduction in EMI noise, the proposed approach results in switching loss reduction. The analytical results are verified using a laboratory-scale working prototype and are discussed in Section IV.

Equation (11) characterizes the noise spectrum and illustrates the advantages of tuning the transition time intervals. In contrast to the conventional case when the transition time t_t is determined by the switch inherent rise/fall time, with the proposed PWM method, it can be *tuned*. Hence, the magnitude of the harmonic spectrum, which is indirectly proportional to the transition time, can be designed and reduced.

$$V[Q_S^{-1}] = \underbrace{d_S V_{C-Link}}_{\textit{power transfer}} + \sum_{n=1}^{\infty} 2 d_S V_{C-Link} \left|\frac{sin(n\pi d_S)}{n\pi d_S}\right| \underbrace{\left|\frac{sin(n\pi t_t/T_{SW})}{n\pi t_t/T_{SW}}\right|}_{\substack{\textit{Conv.: } t_t=\textit{rise/fall time} \\ \textit{Prop.: } t_t=\textit{tuned interval}}} cos(n\omega t+\phi) \tag{11}$$

Figure 7 illustrates the Fourier spectrum of a per-unitized rectangular, a pseudo-trapezoidal and a trapezoidal waveform representing an ideal switching voltage, and the proposed v_{Sp} and v_{Lp} waveforms of Figure 2 and Figure 3. While the rectangular and pseudo-trapezoidal waveform spectrum fall at 20db/dec, the trapezoidal waveform begins to fall at 40db/dec

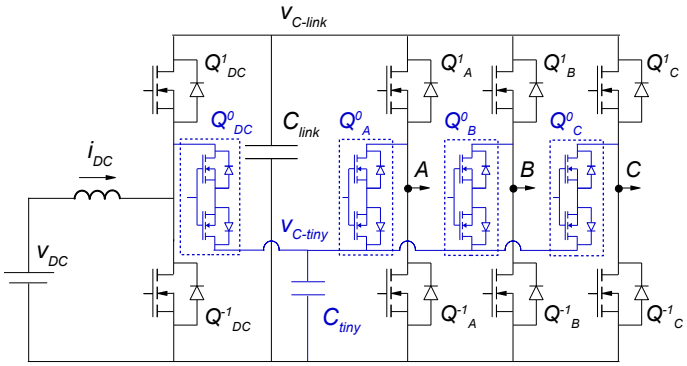

Fig. 8. Circuit schematic for DC-AC power conversion. Note that the circuit modifications are highlighted in blue traces.

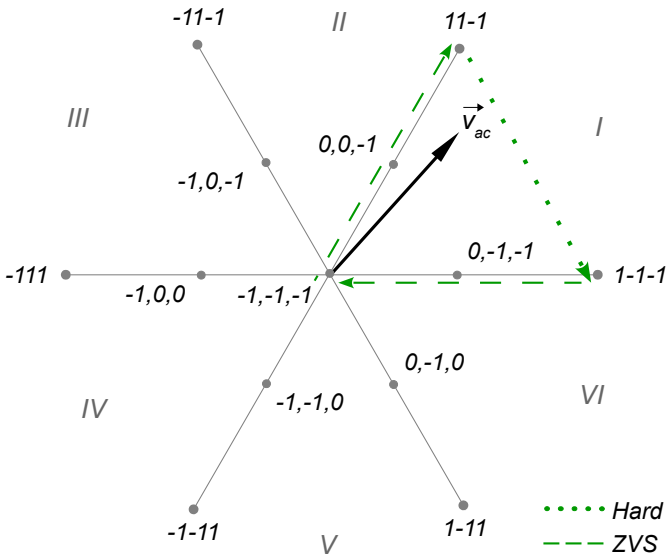

Fig. 9. Space vector diagram for the AC inverter operation with the proposed PWM method.

after the cut-off frequency of $\frac{1}{\pi t_t}$ (where, t_t represents the transition time). Here, $t_t = 1\mu s$. It may be concluded that the proposed approach will result in reduction of electromagnetic noise in the overall system. Due to the unsymmetrical nature of voltage v_{Sp} of Figure 2, while its spectrum is noisier than v_{Lp}, it is still about $5dB$ lower. The analytical results are verified using a laboratory-scale working prototype and are discussed in Section IV.

III. DC-AC Converters

The proposed approach presented in Section II can simply be extended to two-stage DC-AC power converters, as illustrated in Figure 8. This topology is commonly found in transformer-less photovoltaic systems, traction applications and so on. The blue traces highlight the addition of the throw to the DC and AC side switches, which are derived from the analytical results presented in Section II-C and Figure 4. The throws can be realized using a transistor and a diode or two transistors for unidirectional and bidirectional power flow respectively. The figure illustrates the throw "0" switch realization for bidirectional power flow. While the additional devices have to be rated for the full DC-link voltage, the current rating is expected to be a fraction of the rated value since time intervals t_C and t_D are expected to be $< 1\mu s$.

A. Operation

The principles of space vector modulation can be extended to incorporate the additional switch state "0". Figure 9 illustrates the space vector diagram with the proposed additional state vectors. The AC phase A is aligned with the horizontal x-axis of the diagram, and the AC vector $v_{ac}^{\rightarrow}$ is shown in Sector I of operation. In addition to the conventional space vectors illustrated on the outer edges with states "1" and "-1", the figure also illustrates the proposed space vectors with "0" state.

Considering the conventional operation, during sector I, the nearest space vectors [11-1] and [1-1-1] are typically selected. With the proposed approach, additional space vectors with "0" state are appended during the beginning and the end of the active space vectors. For example, during sector I, the state vector sequence can be [-1-1-1] → [00-1] → [11-1] → [1-1-1] → [0-1-1] → [-1-1-1]. The transition between several

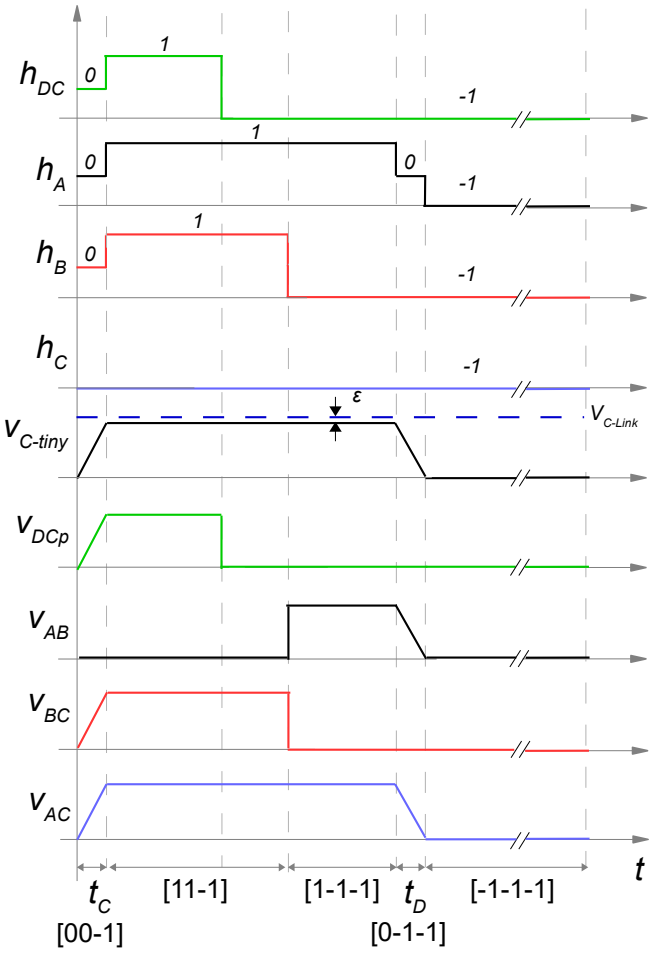

Fig. 10. Switching waveforms for DC-AC conversion for one sector of operation.

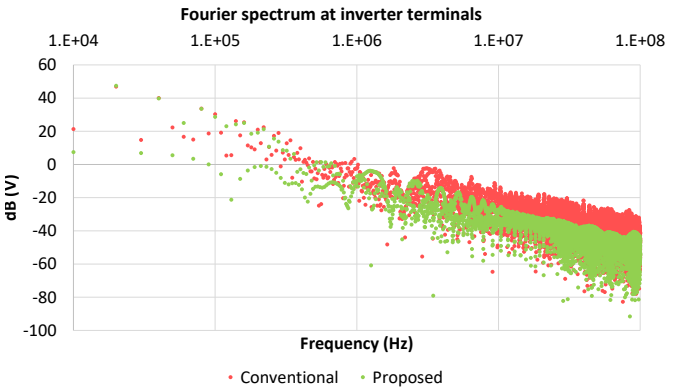

Fig. 11. Fourier Spectrum at the inverter terminals with the conventional (red) and the proposed approach (green).

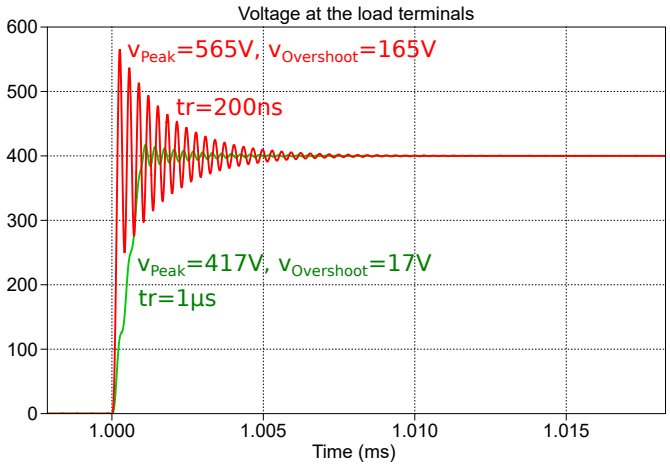

Fig. 12. Switching voltage transient at load terminals with the conventional (red) and the proposed approach (green).

state vectors is also highlighted in the figure using dotted and dashed green arrow lines. The state vector transition on the outer edge is under hard switching condition, also shown by the dotted line. In contrast, the remaining transitions have been tuned for low dv/dt rate and ZVS operation. The space vector transitions can be clockwise or counterclockwise and are based on minimizing DC-link capacitor voltage ripple, reactive power minimization, loss minimization and other conventional optimized functions.

Figure 10 illustrates the switching functions that are translated from the state vector diagram of Figure 9 and the pole voltage of the DC and AC switches for the first sector of operation. The figure details the addition of the switch state "0" with the DC and AC phases, where the "0" state is appended during the beginning or the end of the switching functions (h). The figure also illustrates the AC line-line voltages. It may be observed that four out of the six switching transitions have been selected to be tuned by utilizing the C_{tiny} capacitor. The DC switching state is sequenced with the first active AC state vector to charge the tiny capacitor C_{tiny}. Similar analysis can be extended for the remaining sectors of the space vector diagram.

B. Design Example

In order to verify the proposed work, results from an example DC-AC converter design are presented. The design parameters include power throughput $P = 3kW$, DC voltage $V_{DC} = 200V$, AC voltage $V_{AC} = 208V$ with 60Hz output frequency, DC-link voltage $V_{C-link} = 400V$ and $f_{SW} = 15kHz$. With the design choice values of the charge and the discharge time intervals to be $\approx 1\mu s$, C_{tiny} is sized to be $20nF$. Detailed simulation models have been developed in PLECS circuit simulator environment. Figure 11 to Figure 12 detail the comparison between the conventional and the proposed PWM approaches.

Figure 11 compares the Fourier Spectrum of the inverter terminal voltages where the proposed PWM approach results in reduced electromagnetic noise due to significantly reduced dv/dt rate, while reducing switching losses. While Figure 11 illustrates the results at the inverter terminals, the load may be connected to the inverter with long cables. High dv/dt transitions can cause significant voltage overshoots due to cable parasitics. Figure 12 compares the switching voltage transient at the load terminals between the conventional and the proposed PWM method when the load is connected to the inverter with a 10 ft (ca. 3 m) long cable. The results clearly illustrate the high voltage over-shoot due to cable parasitics (where, cable inductance is $0.25\mu H/ft$ and capacitance is $100pF/ft$) in the conventional case where the voltage overshoots can be $> 40\%$. The proposed approach limits the voltage overshoot to $< 4.5\%$.

Table IV details the VA calculation for DC-AC operation for the conventional and the additional devices. Here, $m = \frac{V_{AC}}{V_{C-link}}$ refers to the modulation index and ϕ refers to the AC power factor. Note that the VA rating is per-unitized over the input power. Similar to the DC case, while the peak voltage ratings of the additional devices will be the DC voltage value, RMS current ratings will be a fraction of the ratings of the existing switches. Simulation results verify the analytical results presented in the table. In the simulated design example, the net VA rating of the conventional devices is 7.54p.u., per-unitized over the input power. In contrast, the net VA rating of the system with additional devices is 8.23p.u.. In summary, the net VA rating of the converter design increases by 10% of this design example.

IV. Experimental Results

A laboratory-scale working prototype has been developed in order to confirm the feasibility of the proposed analytical approach. To enable universal power conversion operation which includes step-up mode, step-down mode, unidirectional power flow, and bidirectional power flow, the additional throw with state "0" is realized using two MOSFET devices in common-source configuration in the prototype. It may be noted that based on specific power converter design requirements, optimized switch realizations are possible, also discussed in Section II-C. The component list can be found in Table V of Appendix A. Figure 13 shows a photograph of the laboratory-scale prototype featuring a modular design which implements the circuit schematic of Figure 8. Each of the half-bridges

TABLE IV
VA RATING OF THE SEMICONDUCTOR DEVICES WITH DC-AC POWER CONVERSION.

Device	Voltage	Current	VA (p.u.)
Conventional Devices			
Q^1_{DC}	V_{C-link}	$\sqrt{d_{DC}}I_{DC}$	$\frac{1}{\sqrt{d_{DC}}}$
Q^{-1}_{DC}	V_{C-link}	$\sqrt{d'_{DC}}I_S$	$\frac{\sqrt{d'_{DC}}}{d_{DC}}$
Q^1_x/Q^{-1}_x	V_{C-link}	$\frac{I_{AC}}{\sqrt{2}}$	$\frac{1}{\sqrt{6}mcos(\phi)}$
Additional Devices			
Q^0_{DC}	V_{C-link}	$\sqrt{d_C}I_{DC}$	$\frac{\sqrt{d_C}}{d_{DC}}$
Q^0_x	V_{C-link}	$\approx \sqrt{d_D}I_x$	$\frac{\sqrt{d_D}}{\sqrt{3}mcos(\phi)}$
			Note: $\frac{d_C}{d_{DC}} << 1$

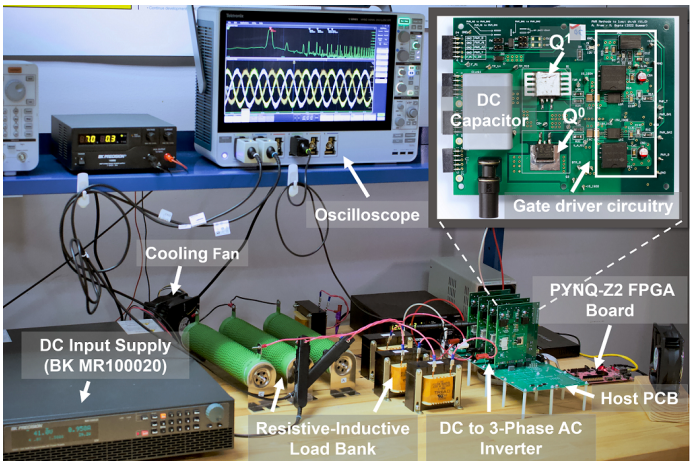

Fig. 13. Photograph of the laboratory-scale prototype setup.

of the DC to AC converter are mounted vertically on a host PCB, which also connects to the controller. The zoomed-in front view of the half-bridge board is shown on the top-right of the figure. The shared tiny capacitors are distributed and mounted on the host PCB near each half-bridge module. The modulation approach is implemented on a PYNQ-Z2 FPGA development board, based on Xilinx Zynq 7000 SoC. The converter is operated under the conventional and the proposed PWM modulation approach in order to compare the performance in terms of EMI noise and overall efficiency. Figure 14 to Figure 19 illustrate the experimental results for DC-DC and DC-AC operation and correspond to the circuit schematics of Figure 5 and Figure 8 respectively.

Figure 14 illustrates the switch turn-off (left) and turn-on (right) transitions with the conventional (red) and the proposed (green) PWM method. The DC-DC converter of Figure 5 is operated under buck mode of operation with input voltage $v_S = 175V$, input current $i_S = 2.2A$, capacitor voltage $V_{C-link} = 350V$, output voltage $v_L = 88V$, and switching frequency, $f_{SW} = 15kHz$. In contrast to the conventional PWM where the switch transition time is determined by the device characteristics, with the proposed approach, the switch transition time is *tuned*. The figures illustrate the results where the dv/dt rate is tuned at 350V/1μs. Without the proposed approach, the switch voltage falls at 350V/50ns (or 7.5kV/1μs) and rises at 350V/52ns (or 6.8kV/1μs) which are close to the switch inherent transition times from the manufacturer's datasheet (Table V). The effect of high dv/dt rate is readily observed in the pole current (bottom waveforms) where the EMI noise is coupled. Note that in this design example, the net VA rating of the conventional devices is 8.26p.u., per-unitized over the input power, also detailed in Table II. The net VA rating of the additional devices are 0.56p.u.. In summary, the net VA rating of the converter design increases by 7% of this design example.

Figure 15 and Figure 16 illustrate the Fourier spectrum of the source-side switch voltage (Q_S^{-1}) and the pole current (i_S) for the entire switching period of 15kHz with the conventional PWM (red) and the proposed PWM method (green) respectively. Focusing on the switch voltage (also the pole voltage, v_{Sp}, of Figure 5), in the conventional case, the transition time is roughly 50ns (Table V). Hence, the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\frac{1}{\pi t_t}$ (roughly 6.4MHz). On the other hand, with the proposed PWM method, the transition time is tuned to $1\mu s$ due to which the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\approx$ 310kHz. In summary, it can be concluded that the proposed PWM approach results in significantly reduced EMI noise. Figure 16 illustrates the Fourier spectrum of the pole current, i_S, of Figure 14 (bottom plots). The EMI noise reduction observed in the time-domain waveforms is readily confirmed in the Fourier spectrum.

The DC-AC converter of Figure 8 is operated with input voltage $v_S = 100V$, capacitor voltage $V_{C-link} = 200V$, AC output RMS voltage of $100V$, and switching frequency, $f_{SW} = 15kHz$. Figure 17 illustrates the Fourier spectrum of an AC side switch voltage for the entire switching period of 60Hz with the conventional space-vector PWM (red) and the proposed space-vector PWM method (green) respectively. Similar to the DC-DC case, the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\frac{1}{\pi t_t}$ (roughly 6.4MHz). On the other hand, with the proposed space-vector PWM method, the AC pole voltages feature pseudo-trapezoidal or trapezoidal shapes, as discussed in Section III-A. The transition time of the tuned edges are designed to have a transition time of $1.2\mu s$. The analytical results presented in Figure 11 are readily confirmed by the experimental results presented in Figure 17. Figure 18 presents the three-phase AC currents with the conventional (top plots) and the proposed (bottom plots) modulation strategies. The total harmonic distortion in the AC currents is measured to be 8.9% and 8.4% for the conventional and the proposed case respectively. The effect of EMI noise reduction due to tuning of the pole voltages is also observed in the pole currents which have reduced high-frequency noise during switching instances.

In contrast to classical EMI reduction approaches which result in increased system losses, the proposed approach enables switching losses reduction due to zero-voltage switching operation, also verified with the experimental waveforms and illustrated in Figure 19. While the switch voltage is measuring using voltage probes, the switch current is measuring using

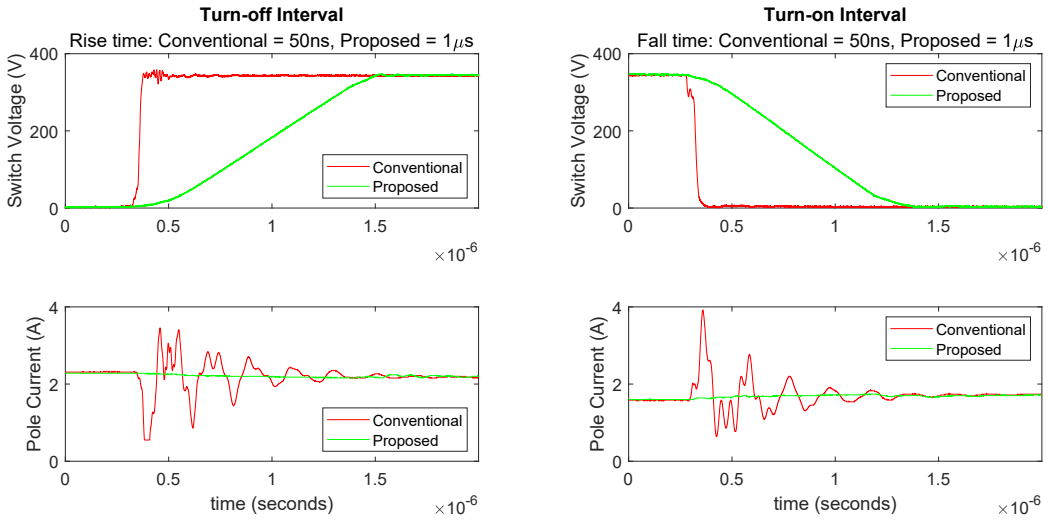

Fig. 14. Experimentally measured Q_S^{-1} switch turn-off (left) and turn-on (right) transition with the conventional (red) and the proposed (green) approach where the voltage transition time is 50ns and 1μs respectively. The bottom waveforms illustrate noise propagation to the pole current (i_S) with the conventional (red) and the proposed (green) PWM method.

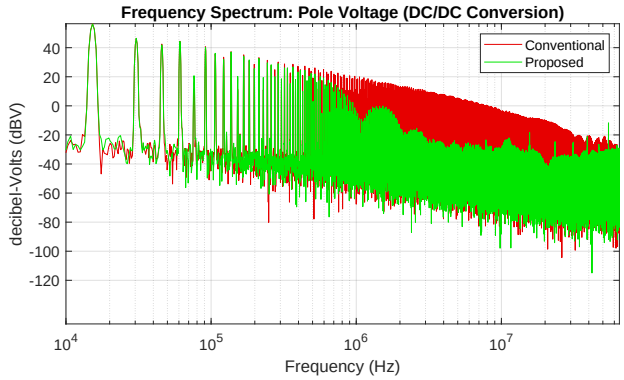

Fig. 15. Experimentally measured frequency spectrum of the trapezoidal-shaped switch voltage (green) compared against the conventional case (red).

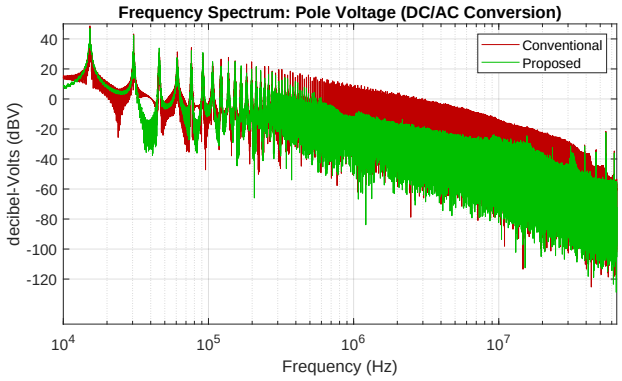

Fig. 17. Experimentally measured frequency spectrum of the AC pole voltages with the trapezoidal shaped pole voltages (green) compared against the conventional case (red).

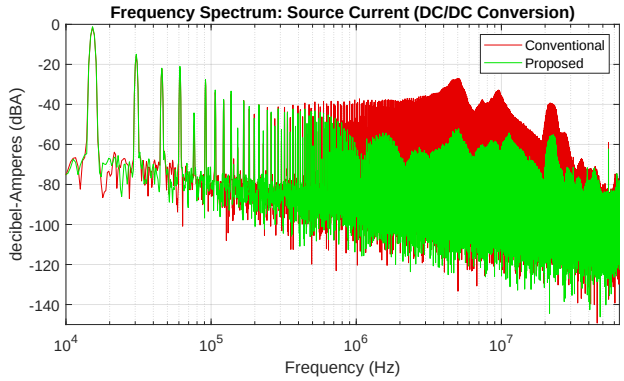

Fig. 16. Experimentally measured frequency spectrum of the source current with trapezoidal shaped pole voltages (green) compared against the conventional case (red).

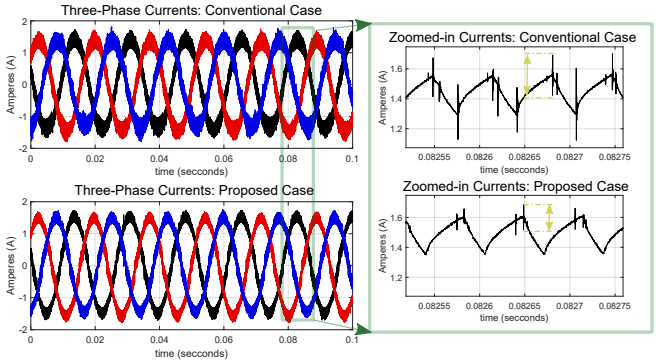

Fig. 18. Waveforms of the three-phase AC currents with the conventional (top) and proposed (bottom) modulation strategy.

a sense resistor. For the turn-off instant, the switch voltage transitions from the conduction state to voltage blocking state using the tiny capacitor. During the transition instant, the pole current flows through the tiny capacitor, consequently eradicating any time instant with high current and high blocking voltage. Similarly, for the turn-on instant, the switch voltage transitions from the voltage blocking state to the conduction state using the tiny capacitor. Again, during the transition instant, the pole current flows through the tiny capacitor (and switch current is zero) eradicating any time instant with high current and high blocking voltage. In the case of DC-DC buck conversion, net efficiency improvement of 12% was measured with overall converter efficiency of 90% with the proposed PWM method. For DC-AC conversion with space-vector modulation, efficiency improvement of 9.5% was obtained with overall converter efficiency of 88% with the proposed PWM method. While in the case of DC-DC conversion, 75% of the edges are tuned, in the case of DC-AC conversion, 62.5% of edges are tuned. Hence, higher efficiency improvements with DC-DC conversion are expected.

Lastly, it may be noted that while silicon MOSFET devices have been used for the laboratory-scale prototype validation, use of other commercially available or future device technologies including IGBT devices and silicon carbide (SiC) MOSFETs are also feasible with the proposed method. SiC MOSFET devices are already expected to improve system efficiency due to lower conduction losses and faster transition times as compared to silicon counterparts in conventional system designs. With the proposed methodology, SiC based inverters are expected to yield even higher efficiencies due to ZVS operation with simultaneous reductions in electromagnetic issues due to reduced dv/dt rates.

V. Conclusion

This work presents a PWM approach which inherently modifies the shape of the switching voltages to a trapezoidal or pseudo-trapezoidal waveform, instead of near-rectangular waveforms with sharp dv/dt transitions. These waveforms are tuned by additional throws which connect to a tiny capacitor ($< 0.1\mu F$). The principles of space vector modulation are utilized to append additional state vectors and accommodate the switching states of the additional throw. The additional throws are active only during turn-on or turn-off transition and utilize the charging and discharging of the tiny capacitor to smoothen the dv/dt rate to be $\approx 1\mu s$ while enabling ZVS operation. The paper discusses the analytical details of the approach using a simple DC-DC boost-buck converter and extends it to a DC to three-phase AC converter, in a progressive manner.

Detailed studies on a design example indicate overall reduction in electromagnetic noise by at least 10db in the case of three-phase inverter operation. The voltage overshoot at the load terminals that is connected to the inverter with a 10 feet (ca. 3 m) long cable can be limited to $< 4.5\%$ without additional losses. Experimental results on a laboratory scale prototype indicate up-to 35dB reduction with the proposed method featuring trapezoidal pole voltages in the conducted EMI spectrum window of 150kHz to 30MHz. Second-order effects include reduced noise coupling at the pole currents resulting in up-to 30dB reduction in the conducted EMI spectrum window of 150kHz to 30MHz. Introduction of ZVS operation leads to a decrease in system losses where the net system efficiency measured during experiments improved by 12% in the case of DC-DC conversion and by 9.5% with DC-AC conversion. As a trade-off, the proposed PWM method leads to addition of semiconductor switches with increase in VA rating of up-to 10% in the design examples under consideration. However, it may be noted that the approach utilizes a simplified control strategy to operate these additional controlled devices. Further, these devices conduct only during the transition times leading to minimal additional semiconductor cooling requirements and net reduction in system losses. Researchers continue to make progresses in development of truly bidirectional four-quadrant switches which are expected to be commercially available in the future [27]. Advancements in this focus area are expected to improve the commercial viability of the proposed approach for EMI reduction. Lastly, to understand the cost implications of addition of silicon

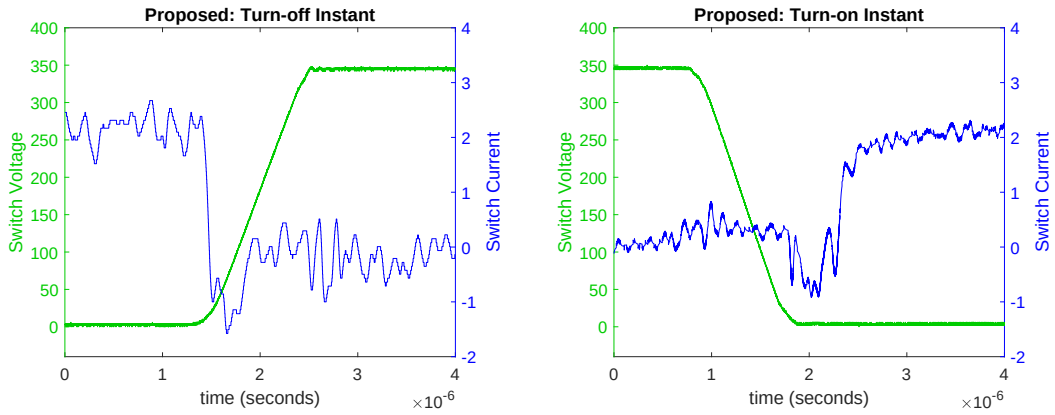

Fig. 19. Experimentally measured switch voltage (green) and current (blue) waveforms during turn-off transition (left) and turn-on transition (right) illustrating zero-voltage switching operation.

devices with advantages due to reduction in EMI filter sizing, system–specific and application–specific cost benefit analysis would be beneficial and would be undertaken in the future.

APPENDIX A
DETAILS OF THE PROTOTYPE COMPONENTS

TABLE V
LIST OF THE MANUFACTURER PART NUMBERS USED IN THE LABORATORY-SCALE PROTOTYPE

Parameter	Manufacturer Number	Key Ratings
MOSFETs	STB36NM60ND	650V, 29A, $R_{DS} = 0.11\Omega$, $t_r = 53.4ns$, $t_f = 61.8ns$, $t_{rr} = 175ns$
Gate Driver	NCD57090CDWR2G	Isolated, 6.5A Output
Bulk Capacitor	ALA7DA331CE500	500VDC, $330\mu F$
Tiny Capacitors	R76TF12705050J	650VDC, $2.7nF$
Filter Inductors	C-59U	10mH, 12.5A

REFERENCES

[1] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-si, si-sic, and all-sic device combinations," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2393–2407, 2014.

[2] P. Yi, Y. Cui, A. Vang, and L. Wei, "Investigation and evaluation of high power sic mosfets switching performance and overshoot voltage," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2589–2592.

[3] L. Palma and P. Enjeti, "An inverter output filter to mitigate dv/dt effects in pwm drive system," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, vol. 1, 2002, pp. 550–556 vol.1.

[4] A. von Jouanne and P. Enjeti, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in asd applications," *IEEE Transactions on Industry Applications*, vol. 33, no. 5, pp. 1138–1145, 1997.

[5] G. Skibinski, R. Kerkman, and D. Schlegel, "Emi emissions of modern pwm ac drives," *IEEE Industry Applications Magazine*, vol. 5, no. 6, pp. 47–80, 1999.

[6] L. Middelstaedt, B. Strauss, A. Chupryn, and A. Lindemann, "Investigation of the root causes of electromagnetic noise of an interleaved dc–dc converter with gan or si transistors and corresponding optimization strategies," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2759–2774, 2020.

[7] C. Choochuan, "A survey of output filter topologies to minimize the impact of pwm inverter waveforms on three-phase ac induction motors," in *2005 International Power Engineering Conference*, 2005, pp. 1–544.

[8] M. Ali, F. Jens, and A. Mertens, "Design and comparison of output filter configurations for sic-mosfet-based automotive dc-ac inverters," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–8.

[9] Y. Son and Seung-Ki Sul, "A new active common-mode emi filter for pwm inverter," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1309–1314, 2003.

[10] I. Takahashi, A. Ogata, H. Kanazawa, and A. Hiruma, "Active emi filter for switching noise of high frequency inverters," in *Proceedings of Power Conversion Conference - PCC '97*, vol. 1, 1997, pp. 331–334 vol.1.

[11] B. Narayanasamy and F. Luo, "A survey of active emi filters for conducted emi noise reduction in power electronic converters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 6, pp. 2040–2049, 2019.

[12] D. O. Boillat, F. Krismer, and J. W. Kolar, "Emi filter volume minimization of a three-phase, three-level t-type pwm converter system," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2473–2480, 2017.

[13] D. Shin, J. Kim, C. Son, S. Jeon, B. Cho, and J. Han, "A simple low-cost common mode active emi filter using a push-pull amplifier," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–5.

[14] L. Dai, W. Chen, Y. Yang, R. Wang, and X. Yang, "Design of active emi filters with the integrated passive component," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 640–643.

[15] H. Li, Y. Ding, C. Zhang, Z. Yang, Z. Yang, and B. Zhang, "A compact emi filter design by reducing the common-mode inductance with chaotic pwm technique," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 473–484, 2022.

[16] G. Ala, G. C. Giaconia, G. Giglia, M. C. Di Piazza, and G. Vitale, "Design and performance evaluation of a high power-density emi filter for pwm inverter-fed induction-motor drives," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2397–2404, 2016.

[17] Y.-C. Son and S.-K. Sul, "Conducted emi in pwm inverter for household electric appliance," *IEEE Transactions on Industry Applications*, vol. 38, no. 5, pp. 1370–1379, 2002.

[18] L. Chen, A. Joseph, Q. Tang, and F. Z. Peng, "Development and test of a 260 kva inverter with a passive soft-switching snubber," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 2007, pp. 1721–1726.

[19] Z. Zhang, X. Yang, T. Q. Zheng, and J. Zhang, "A passive soft-switching snubber with energy active recovery circuit for pwm inverters," *IEEE Access*, vol. 8, pp. 100 031–100 043, 2020.

[20] J. D. Kagerbauer and T. M. Jahns, "Development of an active dv/dt control algorithm for reducing inverter conducted emi with minimal impact on switching losses," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 894–900.

[21] N. Idir, R. Bausiere, and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 849–855, 2006.

[22] M. Cai, O. Wasynczuk, and M. Saeedifard, "A voltage-edge-rate-limiting soft-switching inverter based on auxiliary resonant pole," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 736–744, 2019.

[23] Q. Wang, X. Jiang, and Y. Wang, "An efficient three-phase resonant pole inverter with low conduction loss of switching devices," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 1512–1516, 2022.

[24] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, D. J. Costinett, and B. B. Choi, "Coupled inductor design for interleaved three-level active neutral point clamped inverters considering emi noise reduction," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 257–264.

[25] J.-i. Itoh, H. Dang Minh, and D. Sato, "Experimental verification of conduction noise of three-level v-connection rectifier-inverter system," in *2014 16th International Power Electronics and Motion Control Conference and Exposition*, 2014, pp. 558–563.

[26] M. Gupta, "A pwm control method for reducing dv/dt in cascaded power converters," in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 3308–3315.

[27] Transphorm, Inc. (2022, aug) Transphorm Wins ARPA-E Contract for Novel Four Quadrant GaN Switches with Bidirectional Current and Voltage Control. Aug. 2022. [Online]. Available: https://www.transphormusa.com/en/news/arpae_four_quadrant_switch/