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This thesis describes a digital control system used by the Network Analog Group of the Bonneville Power Administration. This system, the Random Sequence Closing Control System, provides automatic control for a special purpose analog computer used in the study of switching surge overvoltages on power transmission lines. This system, which uses pseudorandom data, has made it feasible to analyze switching surge phenomena on a statistical basis.

THE RANDOM SEQUENCE CLOSING CONTROL SYSTEM

by

HENRI BERNARD JOYAUX

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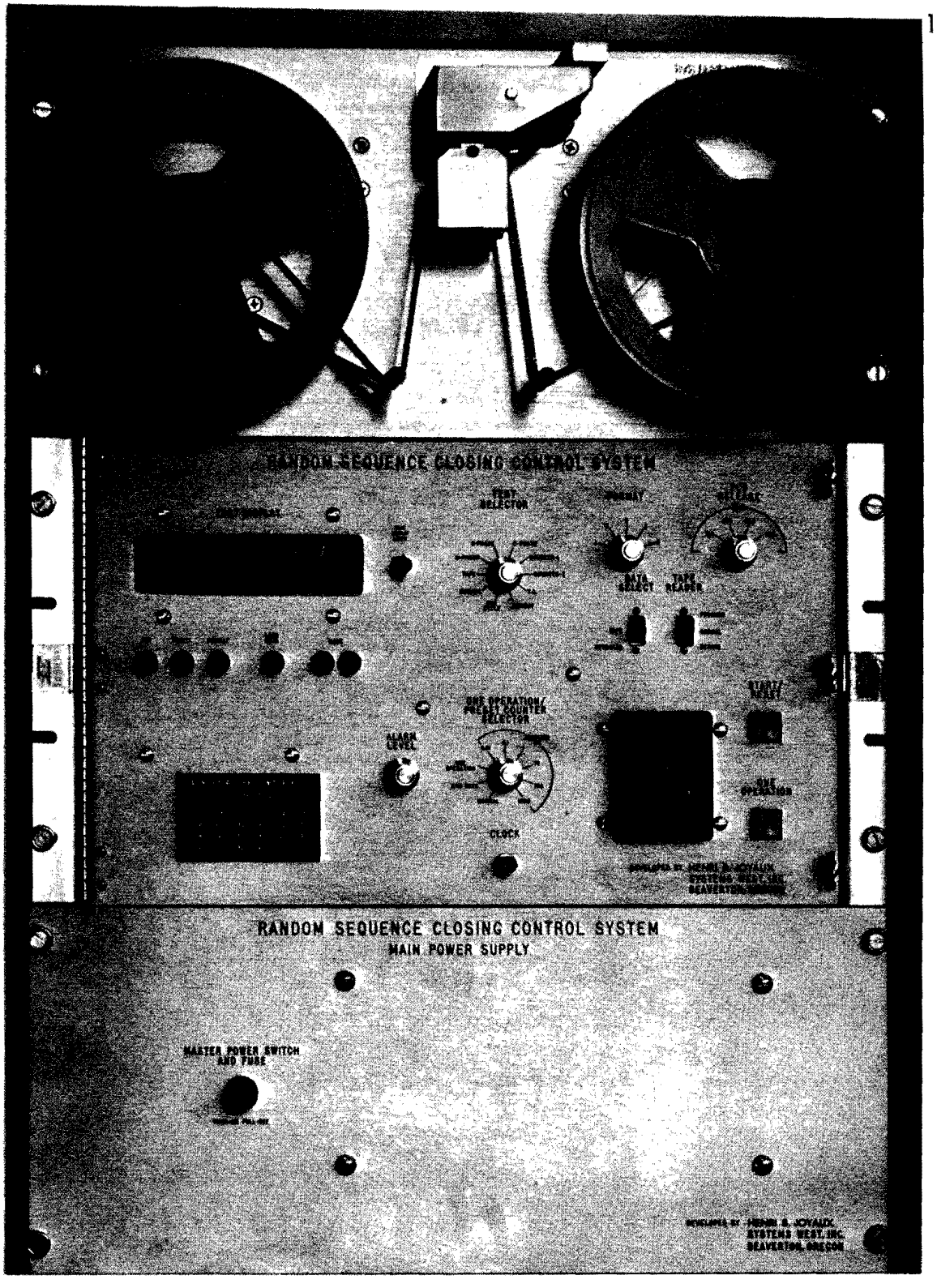


Figure 1. The Random Sequence Closing Control System

INTRODUCTION

1. THE TRANSIENT NETWORK ANALYZER

The Network Analog Group of the Bonneville Power Administration has developed the Transient Network Analyzer for conducting studies of switching surge overvoltages on power transmission lines. The Transient Network Analyzer is a special purpose analog computer, which consists of a model power circuit breaker and a model transmission line. Switching surge investigations are made by varying the closing times of the individual poles of the model power circuit breaker within the manufacturer's pole span specifications.

In 1969 the model power circuit breaker was expanded to include five sets of contacts for each phase. This gives it the capability to be programmed to simulate newly developed power circuit breakers with pre-insertion resistors. Figure 2 is a schematic representation of the model power circuit breaker with four pre-insertion resistors per phase.

The contacts for each phase of the model power circuit breaker are closed in a phase dependent asynchronous sequence, beginning with the $S_{1\varphi}$ contacts and ending with the closure of the $S_{5\varphi}$ contacts. Typically, the closing sequence begins 8 ± 4 ms (milliseconds) after the initiating closing command. Successive contact closures occur at nominal 8 ± 4 ms intervals. The closure of any set of contacts is independent of any closures on the other two phases. Thus, it is possible, as an example, for contacts S_{2B} to close after contacts S_{3A}.

Past studies were directed toward the determination of the maximum overvoltages that could occur on a system. The higher insulation costs of the 500 kV (kilovolts), 760 kV, and 1000 kV systems have made it economically attractive to study switching surge phenomena on a statistical basis. The objectives of these studies then becomes the empirical determination of the probabilities of the overvoltage magnitudes exceeding specific limits.

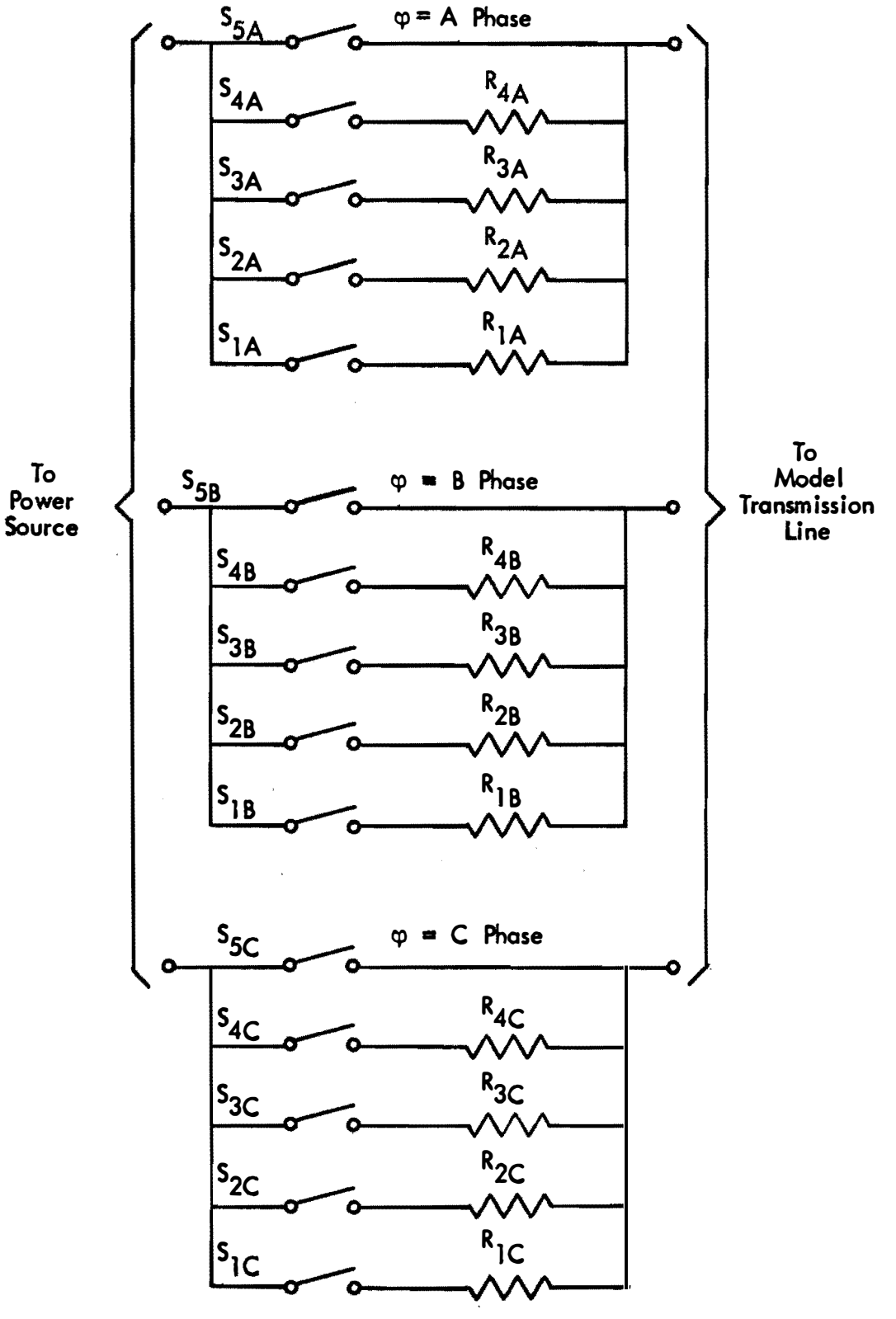


Figure 2. Model Power Circuit Breaker

II. AUTOMATIC CONTROL

Since each complete closure of the model power circuit breaker involves up to fifteen time delays, it has become necessary to provide an automatic system for generating these delays and for controlling the closing sequence of the model power circuit breaker. The Random Sequence Closing Control System has been developed to provide these control functions.

The Random Sequence Closing Control System can provide up to fifteen time delayed closing commands to the model power circuit breaker. In addition, it can provide trapped charge selection commands for the Transient Network Analyzer prior to the power circuit breaker closing sequence, thus permitting the simulation of the static or induced charges, normally found on open transmission lines.

THE RANDOM SEQUENCE CLOSING CONTROL SYSTEM

The primary purpose of the Random Sequence Closing Control System is to provide time delayed closure commands to the model power circuit breaker. For statistical studies, these time delays should have random values within their specified tolerances. By using computer generated pseudorandom numbers as data for generating the time delays, two main advantages may be realized:

1. The type of statistical distribution can be specified for each study.
2. The results are repeatable, simply by re-using the same set of data.

I. GENERAL DESCRIPTION

The Random Sequence Closing Control System is designed as a precision data controlled system. Basically, the system consists of a punched tape reader for data input, memory for storing the time delay data, trapped charge data registers, a precision clock oscillator, a counter, three data buffer registers, three comparators, three delay output registers, and control logic. See Figure 3.

The system has a four-mode operational sequence in converting the data into Transient Network Analyzer control functions.

During the first mode of operation, trapped charge data is read by the tape reader and stored in the trapped charge registers, thus initiating the trapped charge commands. This data is followed by the time delay data which is stored in the memory.

The second mode is initiated at the completion of a data string for one model power circuit breaker closing sequence. The trapped charge registers are cleared and the first time delay data for each phase is loaded into the data buffer registers. The system is held in this mode for a period of 8 ms to allow the trapped charge relays sufficient time to disconnect from the model power transmission line.

The third mode is initiated at the completion of the 8 ms delay of the second mode. During this mode the counter is held in the cleared condition and the system is held in a ready condition for a sequence initiation command at time t_0 from the Transient Network Analyzer. At the reception of the t_0 command, the

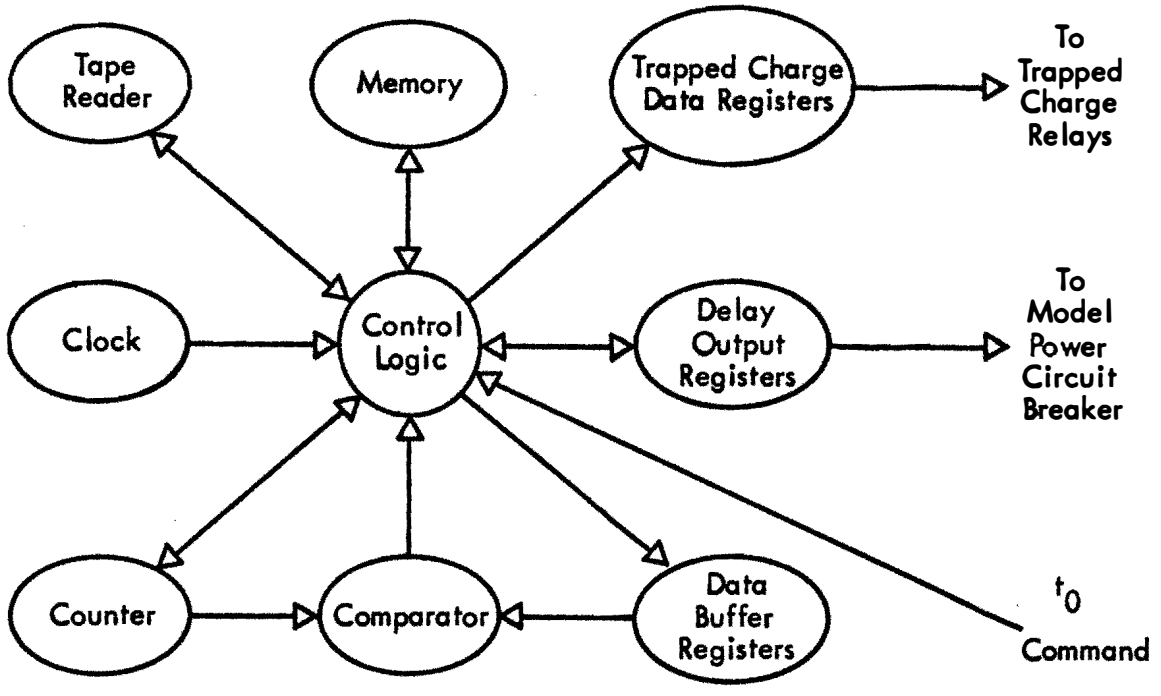


Figure 3. Functional Organization of the Random Sequence Closing Control System.

system goes into its fourth mode.

The system's primary function, that of generating time delayed commands, is performed during the fourth mode. The counter provides a digital time base by counting pulses from the clock. When the counter reaches a reading equal to the contents of any data buffer register, the comparator for that phase signals its respective delay output register. The delay output register changes state, thus generating a closing command for the model circuit breaker. The new state of the delay output register provides the memory address for that phase's next time delay data. This data is then accessed and loaded into the data buffer register. This process continues for each phase until the closing sequence is completed. Later, at a predetermined time, all registers and the counter are cleared and the system returns to its first mode for more data. This is continued until the system runs out of data or it is manually stopped.

II. DETAILED DESCRIPTION

Tape Reader and Data Format

This system uses a Talley Model 424 tape reader. The tape reader reads

eight channel USASCII (United States of America Standard Code for Information Interchange, X3.4-1967) encoded tape with even parity. The reader reads at the rate of sixty characters per second. The tape reader spools have a capacity of one thousand or more sets of closing sequence data. The reader is controlled by the control logic portion of the system.

The data tape may be prepared on a standard Model 33 Teletype, which is readily available as a computer time-share terminal or as an input/output device for most small computers.

The data must be prepared in accordance with one of five formats. Each format is used for a different configuration of the model power circuit breaker. These formats are:

Format One. $Q_A, Q_B, Q_C, t_{5A}, t_{5B}, t_{5C}, ?$

Format Two. $Q_A, Q_B, Q_C, t_{4A}, t_{4B}, t_{4C}, t_{5A}, t_{5B}, t_{5C}, ?$

Format Three. $Q_A, Q_B, Q_C, t_{3A}, t_{3B}, t_{3C}, t_{4A}, t_{4B}, t_{4C}, t_{5A}, t_{5B}, t_{5C}, ?$

Format Four. $Q_A, Q_B, Q_C, t_{2A}, t_{2B}, t_{2C}, t_{3A}, t_{3B}, t_{3C}, t_{4A}, t_{4B}, t_{4C}, t_{5A}, t_{5B}, t_{5C}, ?$

Format Five. $Q_A, Q_B, Q_C, t_{1A}, t_{1B}, t_{1C}, t_{2A}, t_{2B}, t_{2C}, t_{3A}, t_{3B}, t_{3C}, t_{4A}, t_{4B}, t_{4C}, t_{5A}, t_{5B}, t_{5C}, ?$

Q_A, Q_B, and Q_C are the trapped charge data for phase A, phase B, and phase C respectively. They may each have a value of 0, 1, or 2 for no trapped charge, positive trapped charge, or negative trapped charge respectively. The magnitude of the trapped charge is preset in the Transient Network Analyzer. The data term, $t_{n\varphi}$, is the time delay for closing contacts $S_{n\varphi}$ of the model power circuit breaker. Each delay is represented as a four digit number, with the least significant digit representing increments of 10 μs (microseconds). Thus, the time delays may have any value t, such that:

$$00.00 \text{ ms} \leq t \leq 99.99 \text{ ms}.$$

The only other restrictions on the time delay data are:

1. Each delay must contain four digits. Delays which are less than 10 ms must have leading zero (es) to satisfy this requirement.

2. The time delays must have ascending values in accordance with their sequence for each phase.

A question mark (?) is used to signify the end of a data string. Figure 4 shows the USASCII characters used by this system. With the exception of the characters, (: ; < = >) , all other characters are ignored.

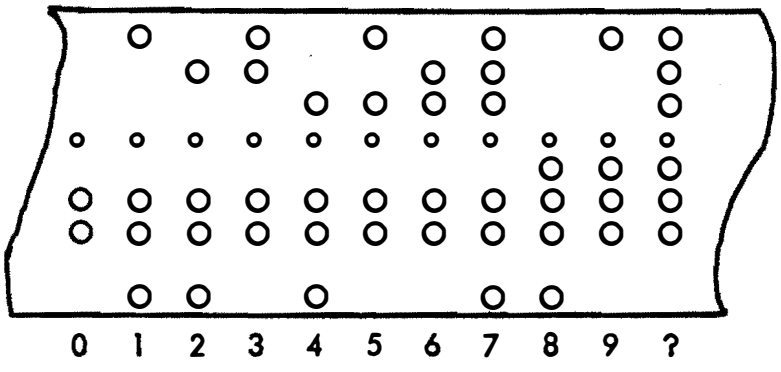


Figure 4. Punched tape characters as used by the Random Sequence Closing Control System.

Trapped Charge Registers

The three trapped charge registers consist of two flip-flops each. The outputs of these registers are decoded into two outputs each for energizing the trapped charge relays in the Transient Network Analyzer. The sequential loading of data into these registers is controlled by the control logic section.

Memory

The time delay data is stored in a 256 bit random access, bi-polar memory. The memory is organized as a four by four array of sixteen bit words. Each word is divided into four bytes of four bits each. Each data word is stored as four binary coded decimal digits. Table I gives the memory addresses for the time delays. Since the system is involved with a maximum of fifteen time delays, memory location 00 is not used.

TABLE I
MEMORY ADDRESS MATRIX

Phase (φ =)	$t_{1\varphi}$	$t_{2\varphi}$	$t_{3\varphi}$	$t_{4\varphi}$	$t_{5\varphi}$
A	01	10	13	22	31
B	02	11	20	23	32
C	03	12	21	30	33

Clock and Counter

An Electra/Midland model FC70T5P crystal oscillator module is used as the system clock. The clock frequency is 1.0000 MHz (megahertz) ± 0.005%.

The counter consists of six binary coded decimal decades. In addition to providing the time base for the delayed output signals, the counter provides multi-phase timing for the control logic. The operation of the counter is controlled by the control logic section.

Data Buffer Registers and Comparators

Since only one data word may be accessed at a time in a random access memory, three data buffer registers are provided for simultaneous comparison of time delay data for all three phases. Each data buffer register has a comparator circuit for comparing its contents with the contents of the second through fifth stages of the counter. The control logic section controls the loading of data from the memory into the data buffer registers. The outputs of the comparators signal the control logic when the contents of the counter equal that of their respective data buffer registers.

Delay Output Registers

Each of the three delay output registers contain five flip-flops. Each of these flip-flops control one set of contacts of the model power circuit breaker. These registers operate as variable length shift registers. The length of these registers is determined by a preset format function in the control logic. The flip-flops which control the unused contacts of the model power circuit breaker are held in the cleared condition. The delay output registers change state on commands from

the control logic section. Table II describes the state sequence of these registers and their relationships with the format function and the model power circuit breaker contacts.

TABLE II

DELAY OUTPUT REGISTER SEQUENCE

Format	Time	Delay Output Register	Model Power Circuit Breaker Contacts Closed				
			$S_{1\varphi}$	$S_{2\varphi}$	$S_{3\varphi}$	$S_{4\varphi}$	$S_{5\varphi}$
1	t_0	00000					
	$t_{5\varphi}$	00001					X
2	t_0	00000					
	$t_{4\varphi}$	00010				X	
	$t_{5\varphi}$	00011				X	X
3	t_0	00000					
	$t_{3\varphi}$	00100			X		
	$t_{4\varphi}$	00110			X	X	
	$t_{5\varphi}$	00111			X	X	X
4	t_0	00000					
	$t_{2\varphi}$	01000		X			
	$t_{3\varphi}$	01100		X	X		
	$t_{4\varphi}$	01110		X	X	X	
	$t_{5\varphi}$	01111		X	X	X	X
5	t_0	00000					
	$t_{1\varphi}$	10000	X				
	$t_{2\varphi}$	11000	X	X			
	$t_{3\varphi}$	11100	X	X	X		
	$t_{4\varphi}$	11110	X	X	X	X	
	$t_{5\varphi}$	11111	X	X	X	X	X

(X) denotes closed contacts.

Control Logic

The control logic section, as its name implies, provides the main functions for coordinating and controlling the other sections. A primary function of this section is mode control. Mode control is provided by a two flip-flop mode counter. Each of the mode counter's four binary states corresponds to one of the operational modes. Most of the major subsections of the control logic are mode oriented and will be discussed under their respective mode headings.

Mode 00. Whenever the mode counter is cleared to binary state 00, the system is placed in the data input mode. The tape reader is under the control of this logic. The tape is advanced by a 4.5 ms pulse, which is generated by a monostable multivibrator. The multivibrator is triggered by a 60 Hz half-wave rectified signal taken from one of the system's 60 Hz line operated power supplies. The multivibrator can be disabled by the actuation of either of two tape sensing switches.

A data input control circuit provides a means of synchronizing the 60 Hz pulses with the system clock. This circuit also provides the sequential tests and operations for accepting and storing data. Sequential control of this circuit is provided by a three flip-flop, self-restoring, Johnson counter. Table III shows the operations performed for each of the counter's six states.

TABLE III

DATA INPUT CONTROL CIRCUIT OPERATIONAL SEQUENCE

State *	Operation
000	If 60 Hz pulse is not present, advance to the next state (100).
100	If the 60 Hz pulse is present, advance to the next state (110). Energize "Data Load" indicator.
110	Perform parity test. If test passes, go to next state (111). If test fails, advance tape, sound alarm and energize "Parity" indicator, and stop.
111	Data acceptance test. If test passes, go to next state (011). If test fails, advance tape and go to state 000.
011	If numeric field is 1111 (?) and the memory address counter reads 0000 (00), advance mode counter to mode 01. If address is wrong, stop, advance tape, sound alarm and energize "Format" indicator. If numeric field is not 1111, then go to state 001.
001	Write data into memory, advance memory address counter, advance tape, and return to state 000.

*All state transitions are synchronous with the system clock.

States 000 and 100 provide an escapement-type action for the sequence, to prevent multiple recording of the same data into memory before the reader completes its tape advance.

Memory Address Counter. The memory address counter has three sections. The first section is a two flip-flop counter, whose first three states direct the incoming data to the three trapped charge data registers in the proper sequence. This section stops in its fourth state, and transfers control of the incoming data to the remaining two sections.

It may be recalled that each time delay data word consists of four binary coded decimal digits (four bytes). The time delay data must be serially written into the memory, a byte at a time. The next two sections are connected as a six flip-flop binary counter. The outputs of the first two flip-flops are decoded to provide sequential control of four write enable inputs (one for each byte) of the memory. The remaining four flip-flops provide the memory addresses in sequence.

The outputs of the last four flip-flops are connected to a four-line address bus, through open-collector output NAND gates. These gates are enabled only during mode 00. The memory address bus is terminated with decoding circuitry which converts the binary address into a modulo four address ("one-of-four" code) for the memory.

The first two sections of the memory address counter are cleared whenever the mode counter is cleared. The third section is preset to a value determined by the format control as follows:

Format 1 - Address is preset to 1101 modulo 2 (31 modulo 4).
Format 2 - Address is preset to 1010 (22).
Format 3 - Address is preset to 0111 (13).
Format 4 - Address is preset to 0100 (10).
Format 5 - Address is preset to 0001 (01).

The format is controlled by a switch located on the front control panel. The last time delay data entry is always stored in location 33.

It has already been mentioned that an alarm is given if the parity or format tests fail. This alarm is also activated when either of the tape sensing switches is actuated. This also halts the system and provides the proper visual indication. The alarm signal is gated from the second flip-flop of the third decade of the system's binary coded decimal counter. The frequency composition of the alarm signal, as shown in Figure 5, consists of 2.5 kHz, 1.67 kHz, 1.25 kHz, 1 kHz, and their harmonics. This frequency mixture gives the alarm a characteristic sound, which is quite discernible from most background noises.

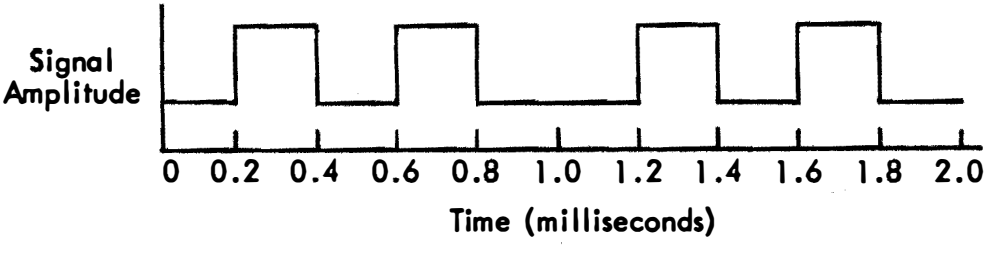


Figure 5. Alarm signal waveshape

The alarm signal is amplified to provide a maximum output of 250 milliwatts peak at the loudspeaker. The Alarm Level control on the front panel can provide a maximum attenuation of 20 decibels.

Mode 01. The counter is cleared at the initiation of this mode. As mentioned before, the trapped charge registers are cleared and the system remains in this mode until the counter reaches the 8 ms count. During this interval, the first time delay data words are sequentially loaded into the data buffer registers. There is a memory address decoder circuit for each of the three delay output registers. The outputs of these address decoders are connected to the memory address bus through opened collector output NAND gates. The first two flip-flops of the first counter decade provide the sequential control for enabling each address decoder onto the memory address bus.

Mode 10. This state of the mode counter holds the system's binary coded decimal counter in the cleared condition. The Transient Network Analyzer provides a continuous string of 60 Hz pulses, which is not synchronous with this system's clock. The first such pulse (leading edge), which occurs in this mode, will enable the mode counter to advance to mode 11 at the next clock pulse. Therefore, the timing sequence begins within one microsecond of the t_0 command.

Mode 11. During this mode, the counter is operational. The first two flip-flops of the counter not only provide sequential control for the delay output register's address decoders, but also, in their 00 state, enable the comparators. Since the lowest ordered digit of a time delay is compared to the second decade of the counter, the first decade flip-flops will all be in the 0 state when an equality occurs. The delay output registers will change their states at the beginning of this microsecond interval.

The comparator circuit also sets a fundamental mode latch, which will enable its data buffer register to load data when that phase's delay output register's address decoder is enabled to the memory address bus. The latch is reset during the second half of that phase's data buffer register load cycle. Thus, if all three have an identical time delay, their delay output registers will change states simultaneously, while their data buffer registers will be loaded sequentially. Table IV illustrates the memory addresses as generated by the delay output registers' decoders. Note that no address is necessary when the delay output register has reached its final state.

TABLE IV

DELAY OUTPUT REGISTER STATES AND ADDRESS DECODER OUTPUTS

Format	Output States	Address Decoder		
		A Phase	B Phase	C Phase
1	00000	31	32	33
	00001	.	.	.
2	00000	22	23	30
	00010	31	32	33
	00011	.	.	.
3	00000	13	20	21
	00100	22	23	30
	00110	31	32	33
	00111	.	.	.
4	00000	10	11	12
	01000	13	20	21
	01100	22	23	30
	01110	31	32	33
	01111	.	.	.
5	00000	01	02	03
	10000	10	11	12
	11000	13	20	21
	11100	22	23	30
	11110	31	32	33
	11111	.	.	.

The system will remain in this mode for the time specified by the PCB Release (power circuit breaker release) switch on the control panel. This switch enables the appropriate counter outputs to clear the mode counter at the

indicated time.

Control Panel

The control panel for the Random Sequence Closing Control System is shown in Figure 6. The manual controls and visual indicators for the system are located on this panel. These controls include the format selector switch and the power circuit breaker (PCB) release switch, whose functions have already been discussed. The visual indicators include the end-of-tape (EOT), parity, format, and load data, which also were previously mentioned. The status of the mode counter is displayed by the mode indicators.

The test display provides a four decimal digit readout with seven segment indicators. The test display lamps' push button energizes all segments to test for filament failures. The test selector switch selects the information to be displayed. The state of the memory address bus is displayed by the two right hand digits in the one cycle, normal, and tape positions. The one cycle position prevents the mode counter from clearing when the power circuit breaker release occurs. Depressing the start/reset button will return the system to mode 00 for more data. The normal position is self-explanatory. The tape position will display the eight tape channels on the left two digits. The seven segment display will show information which is not binary coded decimal as illustrated in Figure 7. The A phase, B phase, and C phase positions are for displaying the contents of the data buffer registers. The

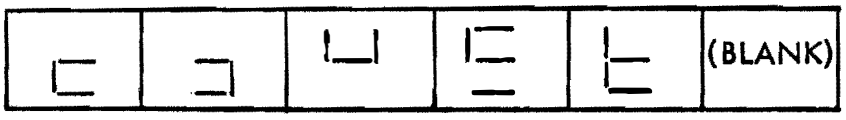


Figure 7. Seven segment display of four bit binary information greater than nine.

counter-1 position displays the first and last decades of the counter. The counter-2 position displays the four decades of the counter which are compared to the data buffer registers. The contents of the three trapped charge registers are displayed in the T. C. position. The memory position displays the contents of a memory location, which is addressed by the keyboard.

The data select switch permits the keyboard to be used as an alternate data source. The tape reader switch is self-explanatory. The system clock may be

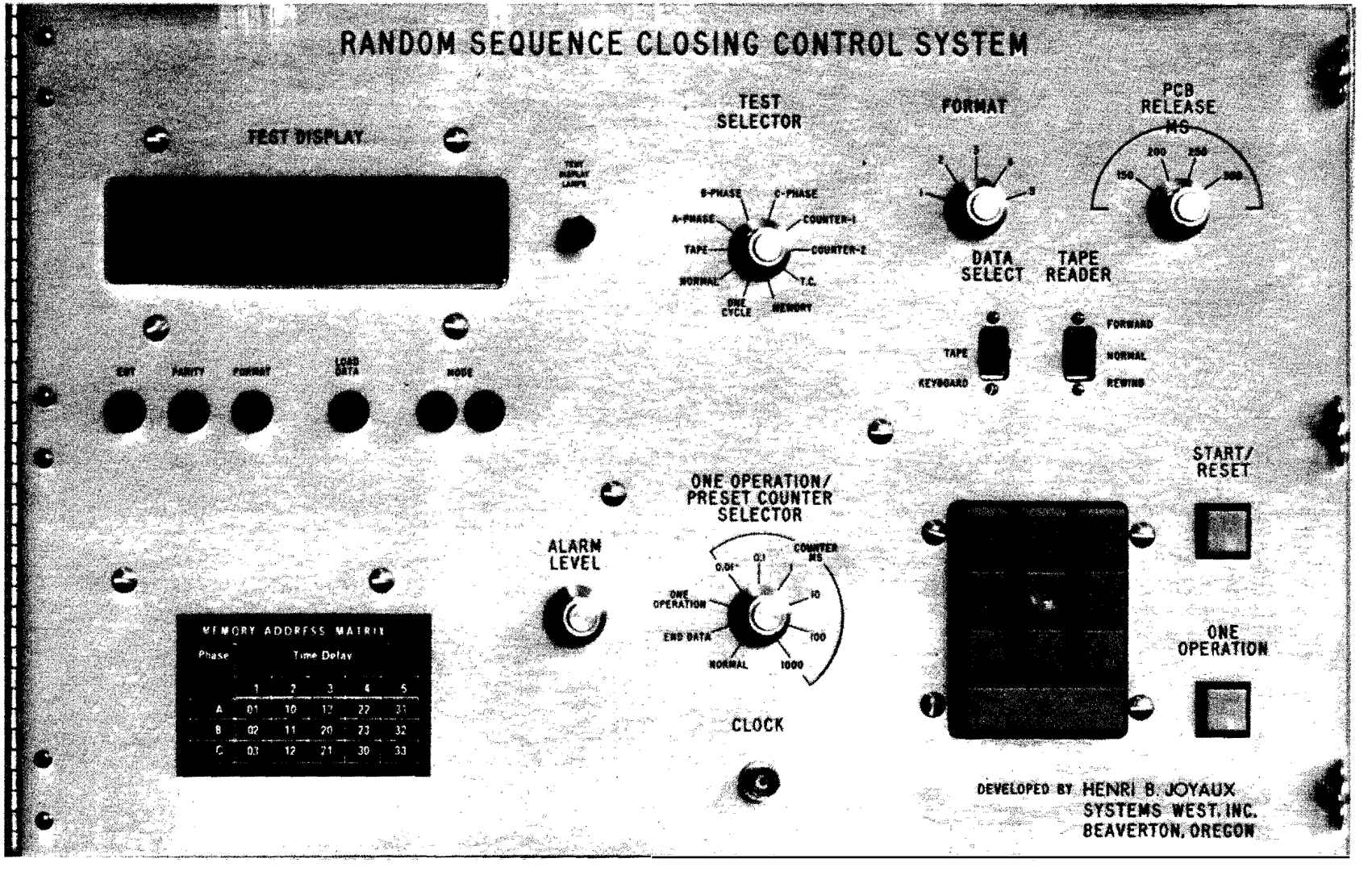


Figure 6. The Random Sequence Closing Control System Main Control Panel

monitored at the clock connector.

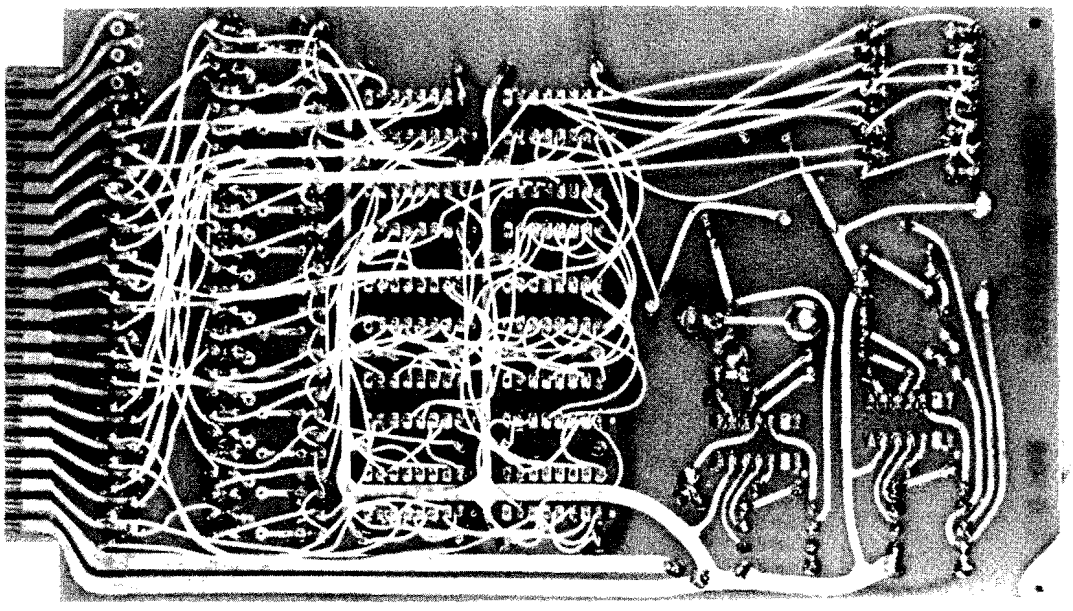
The one operation/preset counter selector switch selects the functions for the one operation push button. The push button is disabled in the normal position. The end data position permits the manual generation of the end of data string character. The one operation position permits the push button to replace the 60 Hz pulses in the data entry mode, and to replace the clock pulses in all other modes. The remaining six positions permit the one operation push button to be used to preset each of the six counter decades.

Thus, the control panel not only provides for the normal operation of the system, but also for diagnostic analysis of the system.

Construction

The TTL (Transistor Transistor Logic) family of integrated circuits were used throughout this system. With the exception of the tape reader interface and the system clock circuit boards, all circuits were fabricated by the wire-wrap method. Figure 8 shows both sides of the system clock circuit board, which has both etched and wire-wrapped circuitry.

The system has two power supplies. One supply, which is located on the tape reader interface circuit board, provides a regulated and passively protected 24 V dc for the tape drive solenoids. The second supply provides primary regulated power at 14 V dc; this is the required voltage for the visual indicators on the control panel. This primary power is distributed to the circuit boards, where secondary regulators provide passive current limited 5 V power for the logic circuits. Most of the circuit boards have their own regulators. This provides dynamic decoupling between circuits. These 5 V regulators are referenced to a master regulator, located on the system clock circuit board. The system is also protected by a circuit breaker.



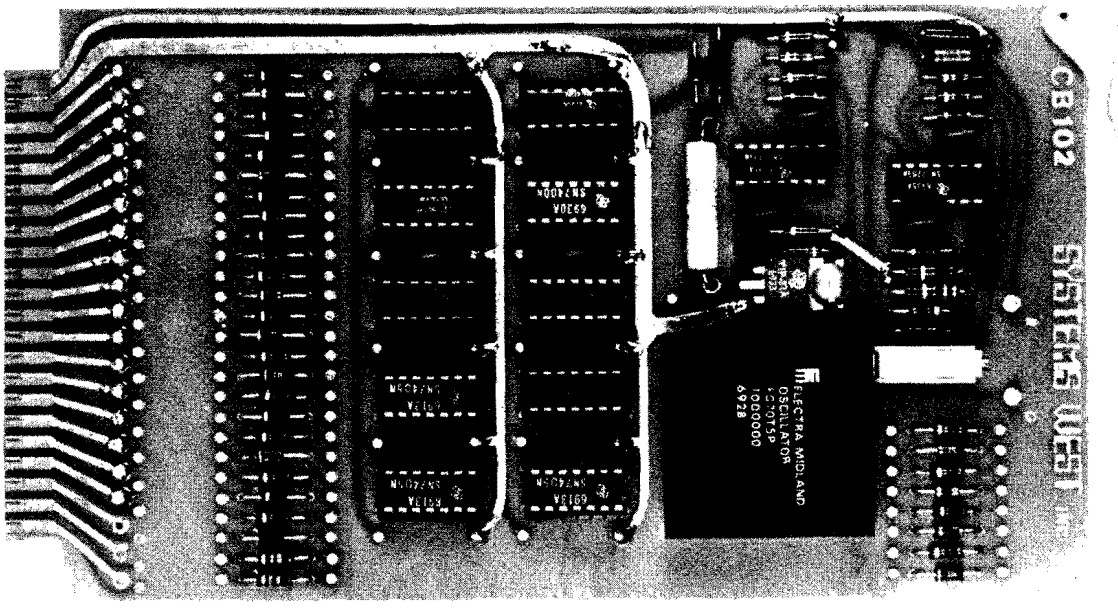


Figure 8. The System Clock Circuit Board

SUMMARY

It has been attempted to show the simplicity of the logical organization of the Random Sequence Closing Control System. The System has proven its reliablity inasmuch as it has needed servicing on only two occasions since it became operational two and one-half years ago (Fall, 1970).

This system has permitted the Network Analog Group to conduct studies with the Transient Network Analyzer, that were not economically feasible before.

It is not the intent of the author to present this system as a final solution to a research problem. Rather, it is hoped, this system will be instrumental, by performing its specific functions, in developing better models of power systems. The knowledge gained from the use of the Transient Network Analyzer has already helped in the development of more accurate mathematical models of switching surge phenomena. Ironically, this could eventually produce computer simulation programs which would replace these hybrid techniques.

BIBLIOGRAPHY

Joyaux, H. B. 1971, "Random Sequence Closing Control System Instruction Manual," BPA Contract No. 85122.

Kimbark, E. W. and A. C. Legate 1968. "Fault Surge Versus Switching Surge: A Study of Transient Overvoltages Caused by Line-to-Ground Faults," IEEE Transactions, Power Group, Vol. 87, pp. 1762-1769.

Legate, A. C. 1970, "Comparison of Switching Surge Measurements With Transient Network Analyzer Measurements," IEEE Winter Power Meeting Conference Paper, No. 70CP36PWR.