Spring 5-26-2015

Constant Interface Temperature Reliability Assessment Method: An Alternative Method for Testing Thermal Interface Material in Products

Christian Amoah-Kusi
Portland State University

Constant Interface Temperature Reliability Assessment Method:

An Alternative Method for Testing Thermal Interface Material in Products

by

Christian Amoah-Kusi

A thesis submitted in partial fulfillment of the
requirements for the degree of

Master of Science
in
Mechanical Engineering

Thesis Committee:
Gerald Recktenwald, Chair
Faryar Etesami
Derek Tretheway

Portland State University
2015

Abstract

As electronic packages and their thermal solutions become more complex the reliability margins in the thermal solutions diminish and become less tolerant to errors in reliability predictions. The current method of thermally stress testing thermal solutions can be over or under predicting end of life thermal performance. Benefits of accurate testing and modeling are improved silicon yield in manufacturing, improved performance, lower cost thermal solutions, and shortened test times.

The current method of thermally stress testing is to place the entire unit in an elevated isothermal temperature and periodically measure thermal performance. Isothermally aging is not an accurate representation of how the unit will be used by the customer and does not capture the thermal gradients and mechanical stresses due to different coefficients of thermal expansion of the materials used in the thermal solution.

A new testing system, CITRAM which is an acronym for Constant Interface Temperature Reliability Method, has been developed that uses an electronic test board. The approach captures the thermal and mechanical stresses accurately and improves test time by 20-30% as a result of automation. Through this study a difference in the two methods has been identified and the new CITRAM method should be adopted as current practice.

Table of Contents

List of Tables

List of Figures

Glossary

CITRAM: Constant Interface Temperature Reliability Assesment Method

cRIO: Compact Reconfigurable Inputs and Outputs

*PCIe: Peripheral Component Interconnect Express

SKU: Stock Keeping Unit

TIM 1: Thermal Interface Material between Silicon and a heat spreader

TIM 2: Thermal Interface Material between the heat spreader and the heat sink

TMTB: Thermal Mechanical Test Board

* Third party trademarks are property of their owners

Introduction

The goal of this study is to investigate a new method for reliability testing of Thermal Interface Materials (TIM's) used in high performance computing hardware. The new method is compared to the traditional methods used today to test if end-of-life performance is predicted more accurately. The current practice of thermally aging TIM's is to stress the TIM material by placing it in an elevated isothermal chamber for extended times and then periodically removing it for performance testing. The proposed method uses heaters on a mechanically representative version of the end product and subjects the TIM to the temperatures and heat flux that will be experienced over the useful lifetime of the hardware. This proposed method is a closer approximation to how the product will be used by the customer.

Thermal Interface Materials enhance thermal contact between adjoining parts along a heat flow path. TIM's are an essential component in the cooling system designed to keep the operating temperature of the modern microprocessor at acceptable levels while dissipating power levels under heavy computational load. This enables the microprocessor to run cooler which improves efficiency and reliability or it allows the microprocessor to run at a higher frequency than would be allowed without the TIM. Asperities between the surface of the microprocessor and the heat spreader or the heat spreader and the heat sink, inhibit the transfer of heat. The main function of the TIM is to fill the voids between the two interfaces with a higher conductivity material than the air that occupies the void. This provides better heat transfer from the electronic component to the heat spreader or heat sink.

There are many different categories of TIM's and the major factors in choosing a TIM for the final product are based on cost, performance, and overall reliability. For this study we will focus on thermal greases because greases typically have a low standard deviation of variability and a predictable degradation. The well-behaved performance degradation of greases allow greater precision in evaluating the differences between the two methods in comparison of failure modeling, that are the subject of this research.

Thermal Performance Characterization of a TIM

The performance of a TIM is measured by applying a known power to one side of the TIM and measuring the temperature delta across the TIM. The performance of the thermal solution is characterized by the case-to-ambient resistance

$$\psi_{ca} = \frac{T_c - T_a}{P} \qquad (1)$$

where T_c, T_a, and P are the center case temperature, ambient temperature, and power applied, respectively (Sauciuc, 2005). In current designs of high performance CPU cooling there are two TIM's. TIM 1 interface is located between the silicon and the heat spreader. TIM 2 interface is located between the heat spreader and the heat sink pedestal. From the TIM manufacturer, the performance of TIM's are determined in a controlled ideal environment between two coupons as shown in Figure 1.

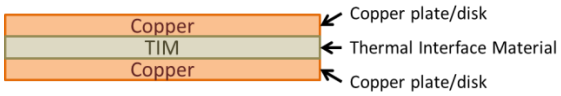

Figure 1: Typical copper coupon TIM sample used for thermal performance testing

A known power is applied to one of the copper sides of the coupon and the temperature delta is measured across the TIM. This performance number is typically what is published by the TIM manufacturer in their data sheets. In many cases the electronic product is mechanically and thermally more complex than the test coupons used by the TIM manufacturer (D. DeVoto, 2014). Because not all the degradation modes is understood, this causes the customer of the TIM to validate that the performance of the TIM is sufficient for the intended product. The TIM will need to be validated independently at the beginning of the product's life and at the end of the product's useful life for all stresses it will be exposed to by the customer during reasonable use.

Arrhenius Model for Accelerated Life Testing

For the purposes of this study we will use the Arrhenius life-temperature relationship, a model widely used to model product life as a function of temperature. The Arrhenius rate law correlates a simple first order chemical reaction to temperature by

$$R = A'\exp[-E_a/kT] \tag{2}$$

where R is the reaction rate, A' is a constant that is a characteristic of the product, E_a is the activation energy, k is the Boltzmann constant, and T is the absolute temperature

(Nelson, 2004). With this theory the modeling of the degradation rate of the thermal resistance at a specific use temperature can then be constructed with

$$\psi_{ca}(t) = b + Rt = b + A'\exp[-E_a/kT]t \tag{3}$$

where b is the initial performance, R is the rate as described in Equation (2) and t is time, typically in hours. An end of life performance is predicted if the activation energy for the mechanism causing the degradation is determined. In industry, this is typically done by placing two to three populations of assemblies in an oven to bake at a constant temperature, with each assembly at different temperatures than each other and higher than the use case temperature. Performance measurements are made by periodically removing assemblies at specified time intervals and testing on an apparatus that excites the TMTB (Thermal Mechanical Test Board) to customer use conditions. The degradation rates by temperature are measured at two elevated bake temperatures and an acceleration factor is determined between the elevated temperatures as the ratio of rates

$$A_F = \frac{R_{T_{High}}}{R_{T_{Low}}} = \exp\{(E_a/k)[(1/T_{High}) - (1/T_{Low})]\} \tag{4}$$

Here A_F is the acceleration factor, E_a and k are the activation energy and the Boltzmann constant, respectively, T_{High} is the absolute elevated high test temperature, and T_{Low} is the product's absolute use temperature or the absolute lower bake temperature. From the two temperatures used in the testing the activation energy is found by

$$E_a = \frac{ln\left(R_{T_{High}}\right) - ln\left(R_{T_{Low}}\right)}{\frac{1}{k}\left(\frac{1}{T_{High}} - \frac{1}{T_{Low}}\right)} \tag{5}$$

The rates, $R_{T_{Low}}$ and $R_{T_{High}}$, are found by the slope of the fit curve through the data collected from the testing. Once the activation energy is computed, an end of life thermal performance is predicted using Equation (3). Alternatively, an equivalent time of life testing is done at an elevated temperature using the acceleration factor by

$$t_{test} = \frac{t_{use}}{A_F} \tag{6}$$

Here t_{test} is the time under test and an elevated temperature, t_{use} is the expected life of the product, and A_F is the acceleration factor computed from Equation (4).

Reliability Testing with Uniform Thermal Bake

The thermal solution assembly with the board attached is stressed by placing the assembly in an oven at an elevated temperature and then periodically testing the performance as a function of time at a particular ambient temperature. This is known as thermal bake where the TIM's performance is degraded through the exposure of the elevated temperature. The degradation is then recorded as the increase in the thermal resistance over time as measured by the initial performance measurement

$$\hat{\psi}_{ca}(t_n) = \psi_{ca}(t_n) - \psi_{ca}(t_o) = \frac{\left(T_c(t_n) - T_s(t_n)\right)}{P(t_n)} - \frac{\left(T_c(t_o) - T_s(t_o)\right)}{P(t_o)} \tag{7}$$

The lower case "t" in Equation (7) is with respect to time and the subscripts "n" and "o" are with respect to time greater than zero and time at zero, respectively. In this way

the performance of the CPU, frequency and voltage, is set for an accepted end of life performance based on the different stresses their TIM will see, typically five to seven years.

Over time the thermal solutions and their loading mechanisms have become more complex. The use of materials with differing coefficients of thermal expansion have also been implemented in many of today's designs. With the thermal solution becoming more complex, simply placing the entire assembly in an oven and elevating the temperature is not an accurate representation of how the assembly is stressed in actual use conditions. In customer like conditions the heat is being generated by several components in the product and not by its environment. The product is also not at one isothermal temperature when in use.

There may be many degradation modes dependent on temperature and interactions between those modes that cause thermal degradation of the TIM selected. For the thermal grease in the study, this includes a pump out failure mode where the TIM is evacuated by the mechanical motion created by temperature cycling of the product at the TIM Interface. The grease can release volatiles while thermally elevated essentially drying out the TIM and not allowing it to flow into the voids. The filler material or conducting material in the TIM could oxidize lowering the effective bulk conductivity of the TIM. There is an entire industry dedicated to TIM development to improve thermal performance and reliability.

Creating a degradation model using the Arrhenius modeling approach discussed earlier in an isothermal bake environment could over or under predict the thermal

performance of the product at the end of its useful life with both having negative implications on the performance and cost of the product. If the degradation of the TIM selected is over predicted, the performance could be limited by that manufacturer so that the product will continue to work to the expected life of the product or a more expensive and exotic TIM may be selected that will meet the products performance needs. If the degradation of the TIM selected is under predicted, the performance of the product could be throttled due to over temperature during normal use or the product will not survive to the expected life and the manufacturer of that product would have a reliability issue with that product.

CITRAM Testing Method

In this study the traditional method, oven bake method, is compared to a direct measurement of thermal resistance during an accelerated life test. The new method is called CITRAM, which is an acronym for Constant Interface Temperature Reliability Assessment Method. A diagram of arbitrary thermal gradients expected throughout the thermal solution is shown in Figure 2:

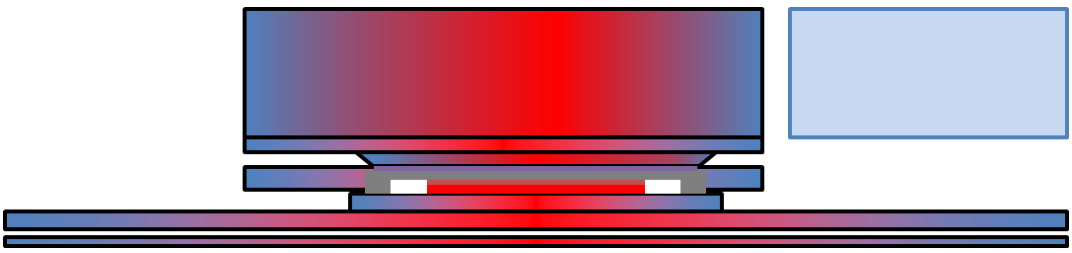

Figure 2: Vertical cross section of card with assumed temperature gradients contours

During an isothermal bake test the normal thermal stresses are not accurately simulated. The purpose of the new proposed method is to more closely match the thermal conditions experienced by the actual product during customer use.

The product studied in this thesis is a PCIe add-in card that is used in servers and workstations for co-processing. Rather than using a fully functional card, the experiments are conducted with a TMTB, a geometrically accurate representative of the production card that is made from the same materials with the exception that the co-processor is a resistive heater created in silicon, but otherwise thermally and mechanically the same. The voltage regulators on the board are simply wired backwards through rerouting of traces in the test board. This causes the diodes in the FET's (Field Effect Transistor) to heat up such that they will produce the same amount of heat as the production card during testing. Additional board traces are embedded in the board to add a heat load in the board to simulate the I^2R losses in the board. The size and power of the TMTB has enabled this study to be feasible economically. Previous attempts have used lower power products that needed supplemental heating by raising the ambient temperature to elevate the TIM interface temperature.

Using the TMTB and the product thermal solution the temperature of the TIM interface is controlled and the behavior when compared to the production card will be a better representative than the isothermal method. In parallel we will take the same type of assembly and place it in an oven at an elevated isothermal temperature to compare with the new proposed CITRAM method.

Converting Testing Requirements to Design and Operation of CITRAM

Temperature Targets

The reason for the proposed new test is due to the complex nature in which the heat sink and board are mechanically loaded. Figure 3 is a diagram of the different components typically seen in a PCIe add-in card.

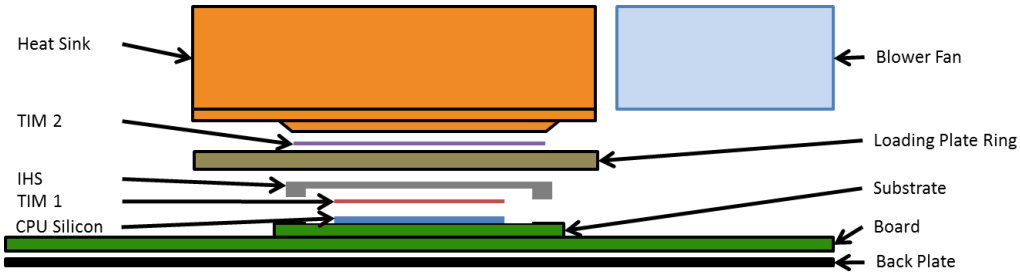

Figure 3: Exploded cross flow view of card with components labeled

Starting from the bottom of the assembly and working up, there is typically a back plate and loading plate ring that the board is sandwiched in between, with fasteners going through all three components. The heat sink is then attached to the loading plate ring with a spring latching mechanism to apply a load on the TIM 2 material, which sits on top of the IHS (Integrated Heat Spreader), which has TIM 1 underneath, TIM 1 rests on top of the CPU silicon, that is soldered to the substrate, which is also soldered to the board. What is also not pictured is a sheet metal structure called the fuselage that usually is attached to the back plate through the topside of the board. The fuselage locates the blower fan and provides an enclosure to shield the entire product from the environment. The purpose of this illustration is to make obvious to the reader how complex the thermal solution is when assembled to the board.

The complex mechanical assembly creates multiple parallel heat flow paths from the CPU silicon to the immediate environment. By design, most of the heat is rejected by the heat sink and therefore that heat passes through TIM 1 and TIM 2. Some of the heat generated by the CPU silicon is conducted down through the substrate, board and back plate. Some heat is convected laterally through the IHS, loading plate ring, and ultimately convected from the side of the assembly, not through the heat sink. The thermal stability and reliability of CPU benefits from the heat flow paths that are parallel to the primary path. However, these parallel paths complicate in situ ψ_{ca} measurements by CITRAM.

Assume that during the assembly process everything is flat and there is no warping due to the stresses of the heat sink loading. If this were true, as the temperature of the different components in the assembly increases, additional mechanical stresses are induced by different thermal expansions of materials with different CTE (coefficient of thermal expansion) in the assembly. From the mechanical stresses there will be elastic and plastic deformation in the thermal solution that will change the interface between TIM 1 to the interface between IHS and silicon, and the TIM 2 and the pedestal and IHS. The greater the CTE differences between these components the larger the stress as the temperature rises causing a greater flatness differences between the interfacing parts.

The conventional method of reliability testing uses an isothermal bake in which the entire thermal assembly is raised to a uniform elevated temperature. The conventional method causes a higher mechanical distortion between parts than the actual product would see in normal operating conditions. This makes long term modeling of

performance degradation more difficult because the conventional testing method does not induce the failure mechanism stress realized in normal operation. The purpose of CITRAM is to simulate similar temperature gradients as seen during normal operation while also elevating the interface temperature of the TIM2. By stressing the thermal solution closer to customer use conditions, there will be more confidence in the projected reliability estimates.

The thermal requirements for the test method are based on data collected on a thermal mechanical test board that is used to simulate a functional card. Estimates are made of the final power consumption of each of the components on the functional card based on computer simulation of the functional silicon at the performance requirements set by the marketing team. The power specifications are used as set points for each of the components on the thermal mechanical test board. The board being tested is available in several different SKU's (Stock Keeping Units) or configurations. The SKU chosen to validate this new testing method is the 300W version running a simulated CPU intensive design load. This is usually the SKU and workload with the highest demands on the thermal solution.

This study focuses on inducing a thermal gradient similar to customer use conditions in the vertical column that encompasses the heat sink loading mechanism indicated by the translucent red box in Figure 4.

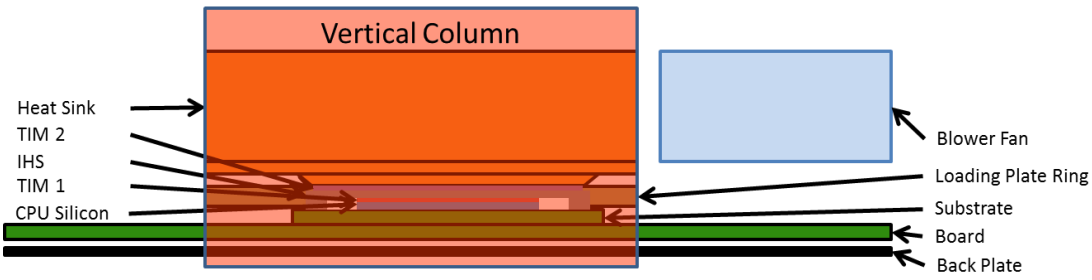

Figure 4: Cross flow view of card with vertical column of thermal importance highlighted

The interface temperature of the TIM will be elevated above normal use conditions to induce an accelerated degradation that can then be modeled using an Arrhenius relationship.

The temperature gradient requirements were derived using a representative electronics test board with the thermal solution attached and was tested using the power predicted for each component on the board. Temperatures were then recorded throughout the vertical column highlighted in Figure 4 and the gradients measured were used as the initial requirements. In addition to the thermal gradients, maintaining a stable thermal ambient environment was added as a requirement.

Testing was performed in the lab to match the temperature difference in reference to the TIM 2 interface temperature. The results of the settings is seen in Figure 5.

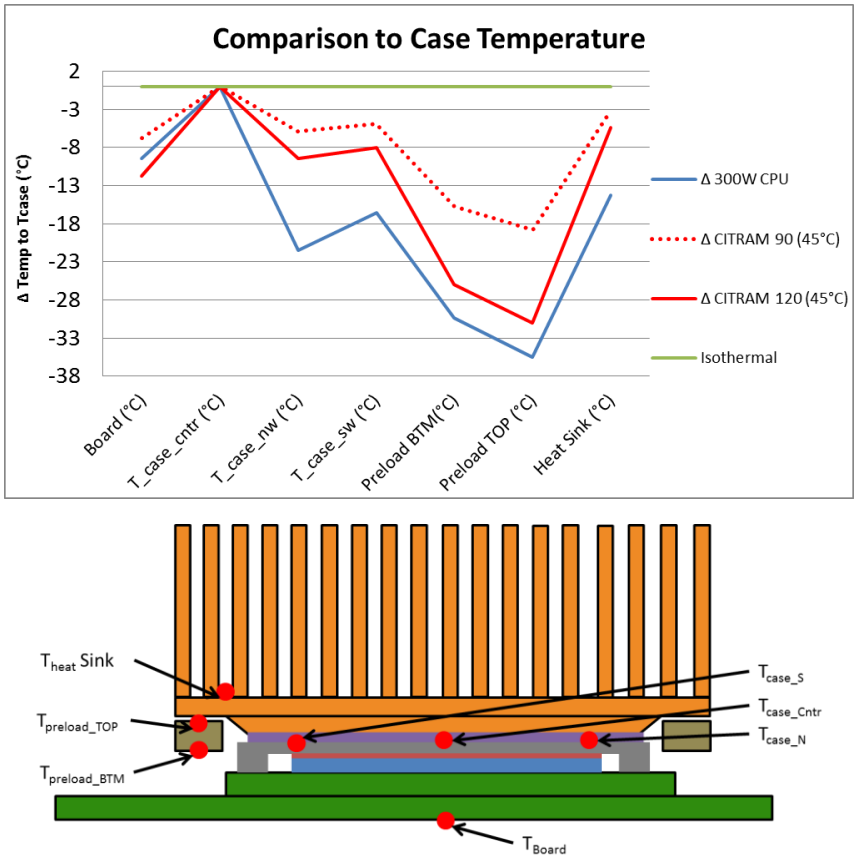

Figure 5: Parallel to air flow view of card with measurement points identified and measured temperature difference compared to center case temperature

Both the upper and lower temperatures considered for the testing were used to bracket the range of gradients expected. In Figure 5 the gradients within the vertical column of the cards within the CITRAM test are closely matched to the 300W CPU intensive loaded card.

System Design

To improve the testing method, design requirements were generated for improved reliability predictions from the thermal stress test. These include:

1. Create an industrial testing apparatus that can test at minimum of 20 cards simultaneously.

2. Utilize TMTB to replicate thermal and mechanical stresses seen in use conditions.
3. Maintain elevated case temperature to within ±0.1°C.
4. Maintain an ambient temperature to within ±4.0°C for all cards in the system.
5. Enable in situ thermal testing to improve testing efficiency.
6. Have the same precision in performance measurement or better than the current isothermal test.

The first thing to solve is how to reject the heat that is generated by the test samples. Collaboration with the building facilities manager was required and a margin was found in the HVAC system so that excess heat could be rejected directly into the building HVAC without elevating the temperature of the lab or the ambient temperature for the environment enclosing the cards. A simple resistance model of the proposed method is seen in Figure 6.

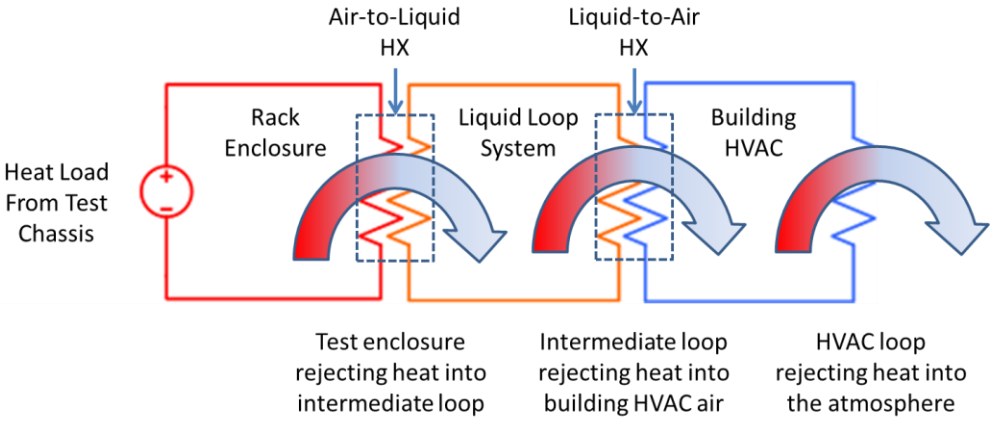

Figure 6: System level heat flow path of CITRAM test system

Beginning from left to right: All the test samples need to be in a temperature controlled enclosure represented by the first loop. The enclosure needs to reject its heat input from

the 24 test cards into an intermediate loop that is controlled to maintain the temperature within the rack enclosure. The intermediate loop needs to reject the excess heat into the building's HVAC system which then finally rejects heat into the atmosphere.

Rack Systems

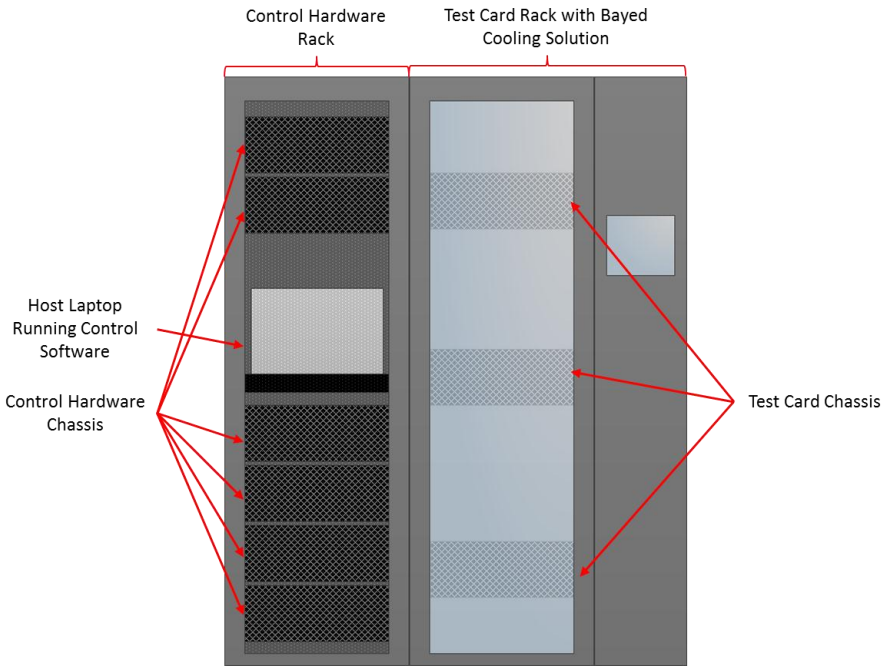

Figure 7: Front view diagram of CITRAM test system

Figure 7 is a front view of the two racks used to separate the control hardware from the test cards. One rack houses the data acquisition equipment and the power supplies, and the other rack houses the units under test. The control and the data acquisition system are separated from the test units because the elevated ambient temperatures would affect the long term reliability of the control hardware. The six control hardware chassis are set in a standard 19 inch wide, 42u tall rack with 70% perforation front and rear doors. The heat generated from the control hardware chassis is exhausted directly into the lab with little impact on the temperature of the lab. The control hardware rack has a

local network hosted by a laptop positioned in the middle of the rack. This allows all six chassis to communicate with overarching software on the laptop and to communicate data to be saved on an external hard drive.

The test card chassis are in a fully enclosed rack manufactured by RITTAL Incorporated. This system has attached to its fully enclosed 19 wide 42u tall rack, a 12 inch wide, 42u tall rack that houses a liquid-to-air cooling package. In this configuration the ambient temperature inside the rack is actively controlled by adjusting the flow rate of the water into the liquid-to-air heat exchanger and the velocity of the air inside the rack.

Intermediate Loop

An intermediate liquid loop was designed to reject the excess heat generated by the RITTAL system into the buildings HVAC system. This system is controlled by the host laptop using an expansion chassis hosted on the same local network to control the temperature and flow rate of the water.

Figure 8 is a diagram of the liquid loop that is located directly behind the two testing racks:

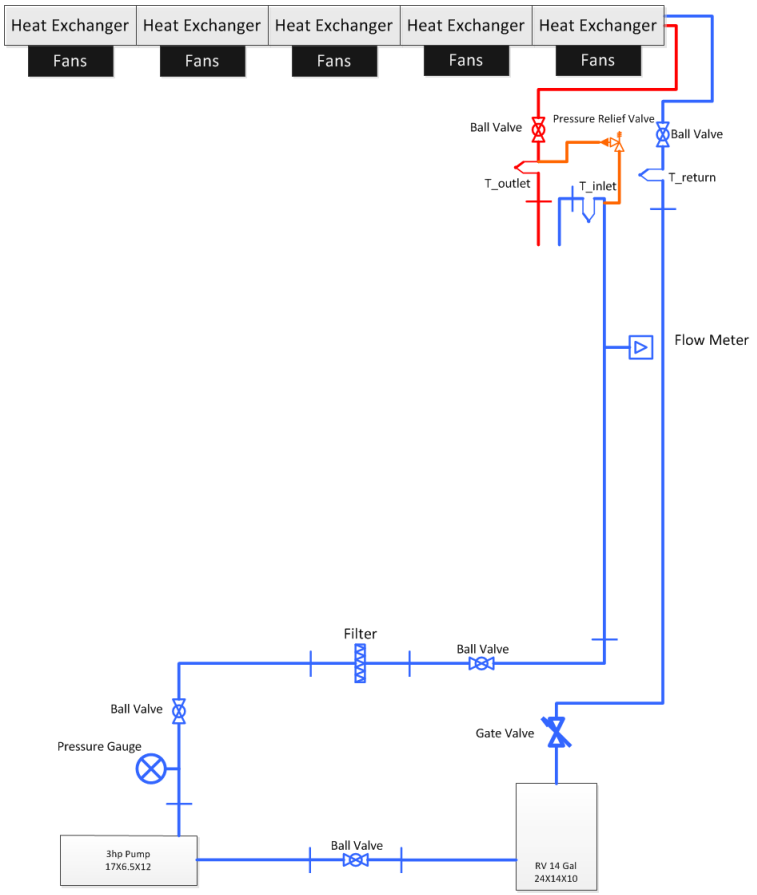

Figure 8: Pipe diagram of intermediate liquid loop used to manage heat rejected from the system

This simple design uses five parallel liquid-to-air heat exchangers to reject the system heat load into the return plenum of the buildings HVAC system. Along the liquid path are temperature sensors to monitor the inlet and outlet temperatures of the heat exchangers, both in the CITRAM system and the heat exchangers rejecting heat into the HVAC system. A filter, pressure gauge, and a flow meter were added to the liquid loop for reliability and added monitoring. There are also various valves for maintenance and troubleshooting components.

Test Card Chassis

The decision was made to design a chassis system to house the test cards in a 19 inch wide server form factor. The cards are separated into PCI Express volume specifications to normalize each card regardless of location within the chassis. With these constraints eight cards could be placed within a 19 inch wide, 4u tall chassis that is 28 inches deep. Figure 9 shows an exploded view of the chassis that encloses the test cards:

Within that chassis there are eight break out boards (BOBs) with a PCIe connector that allows power to be wired to the card and thermal data to be collected from the test card below a false floor that does not violate the PCIe volume specification. A cross section of the chassis is shown in Figure 10 with the break out board and the PCIe test card in place.

The false floor exists directly beneath the card where the BOB is concealed from interfering with the PCIe volume. Wiring for thermal sensors, power, and fan control is routed underneath the test card to minimize any flow variations from card to card. The top cover of the chassis is not shown in Figure 10. The ambient temperature in the test rack is controlled by reclaiming the heat generated by the test cards. Exhaust air from the cards passes over the air-to-liquid heat exchanger within the rack system, and is returned to the front of the rack system at the desired inlet temperature. A top view diagram of how the air is recirculated inside the rack is shown in Figure 11.

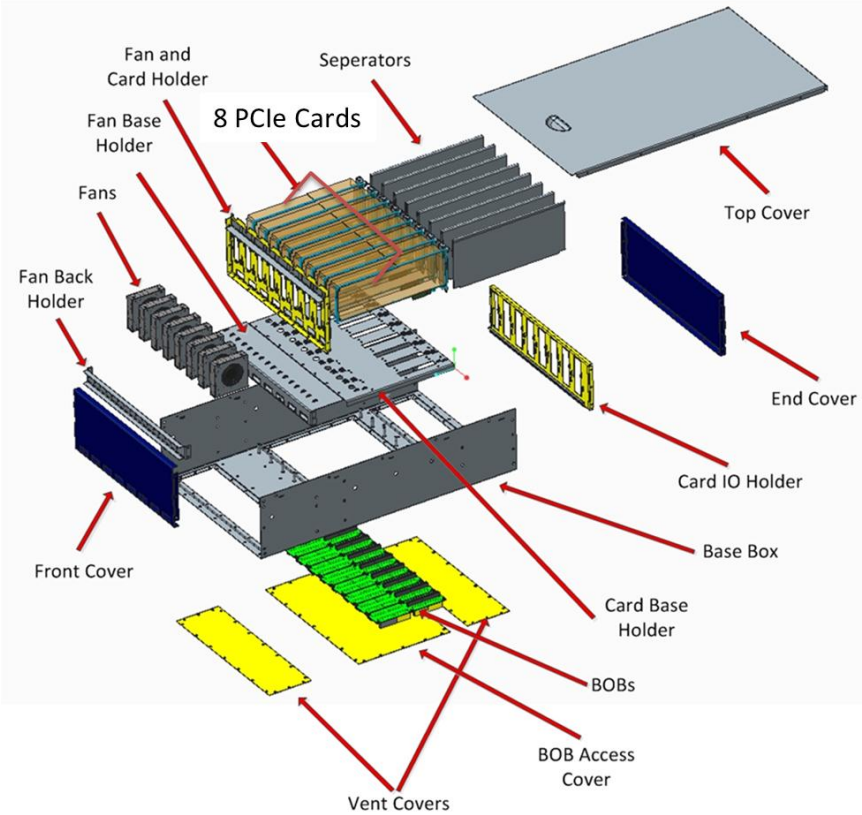

Figure 9: Exploded view of test card chassis

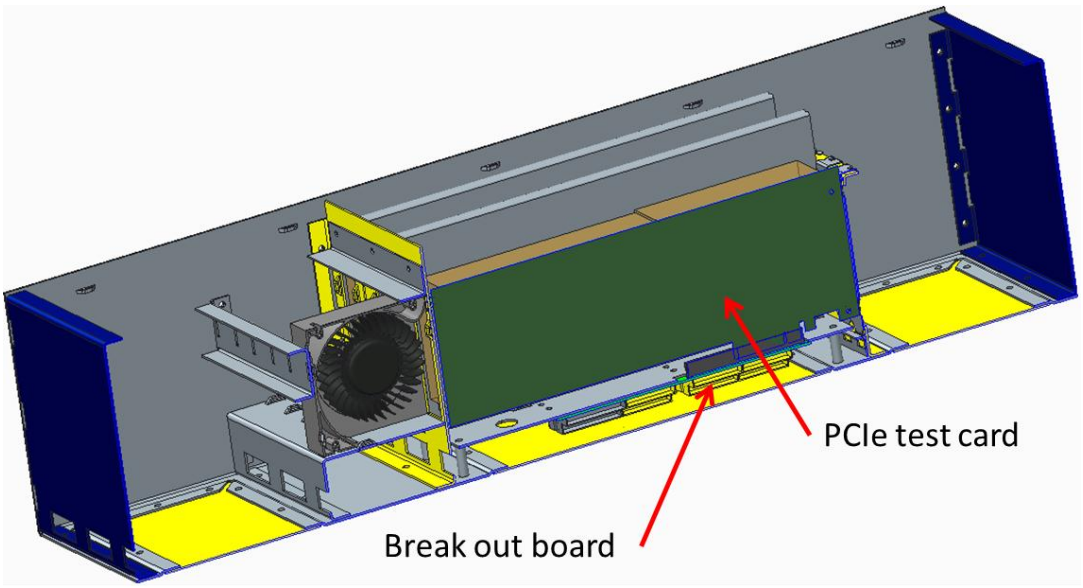

Figure 10: Cross section of test card chassis showing single PCIe slot

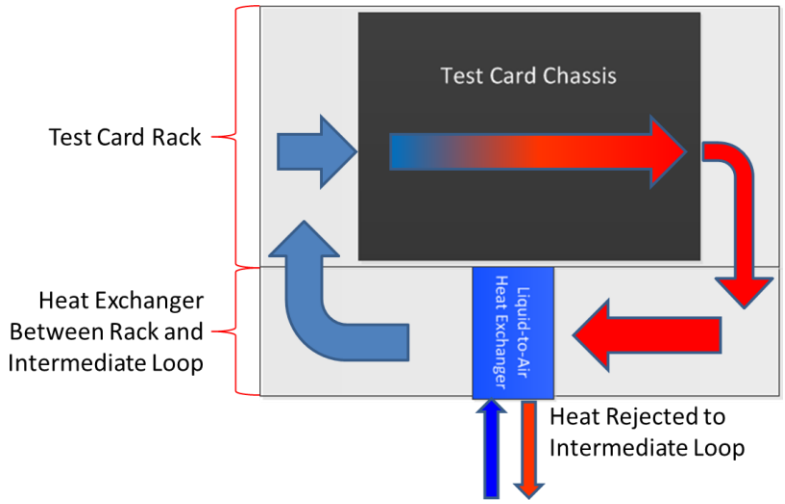

Figure 11: Heat flow diagram of ambient temperature management within RITALL rack

Control Hardware Chassis

A second chassis was designed to house the control hardware and power supplies in the same form factor as the chassis for the test cards. The electronics in this chassis controls the interface temperature of the TIM, performs the data logging, and the periodic performance testing.

The control hardware chassis was designed to fit eight 0-135VDC power supplies, one 12VDC power supply, and a National Instruments cRIO (Compact Reconfigurable Inputs and Outputs) 9074. Each control chassis controls four PCIe test cards. A total of six chassis are required to control all 24 test cards for this study. An exploded view of the control hardware chassis is shown in Figure 12. This configuration allows for two power supplies, four T-type thermocouples, two 4-wire sensors, and two fan controls to be dedicated to each card.

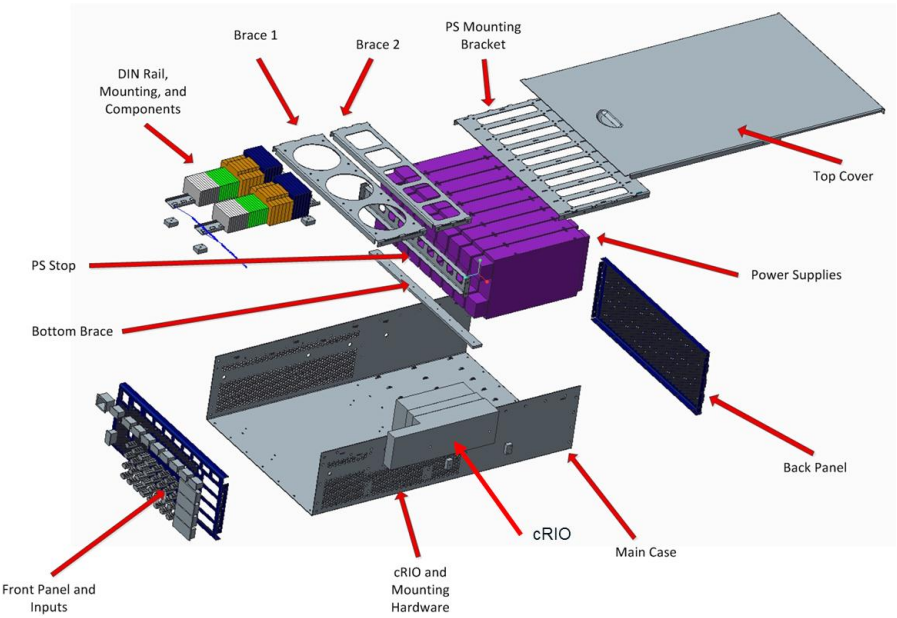

Figure 12: Exploded view of control hardware chassis CAD model

Control Software

The control software is based on the National Instruments LabVIEW software. The software was created at three different layers: FPGA, Real Time OS, and Windows OS. The layout of the software was chosen to recreate the resolution of the current isothermal test apparatus. On the lowest level, the PWM generation for fan control, tachometer readings from the fans, relay switching for on/off control of the power supplies and fans were written on the FPGA layer on the cRIO because of the time critical operations. On the real time operating layer, sensor readings, control signals, and network shared variables are updated. The Real Time OS performs critical operations that can run independently if the host laptop is to crash. The highest level of code is written on the

windows operating system hosted by the laptop. The Windows layer controls the user interface and records and writes to the network shared variables that the user can control. If the laptop crashes, the last settings will be maintained by the Real Time OS and data collection is resumed once the lap top is reset. All three layers of code communicate with each other through the network shared variables accessed over the local network of the system.

Shakedown Test Runs

Shakedown runs were used to optimize the operation of the CITRAM system to meet the design requirements to make the system successful. Many features of the system were discovered that help understand the stability of measurement capabilities when judging performance and degradation of the thermal solution during the shakedown runs. These were eventually controlled or understood, such that their impact on uncertainty and measurement error were eliminated or minimized.

Performance Testing vs. Constant Interface Temperature

The initial test profile ran cards with their fans turned off while controlling power input to maintain a desired TIM 2 interface temperature. At specified random time intervals, the card entered a performance test with fixed power and fixed fan speed. It was discovered that when this occurred the neighboring card's temperature were also influenced as shown in Figure 13.

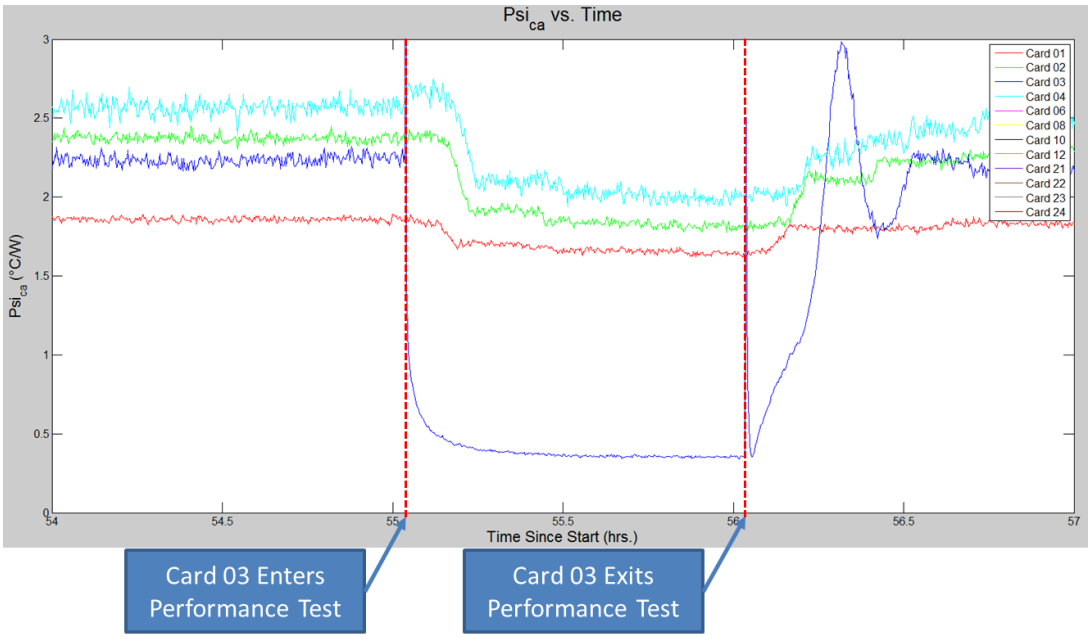

Figure 13: Performance impact on neighboring cards as a result of Card 03 fan speed increase

In Figure 13, card 03 enters a performance test at the 55th hour and the effect of the neighboring three cards is present as a decrease in ψ_{ca} resistance. At 56th hour, card 03 exits the performance test and again the effect is seen as an increase in the ψ_{ca} resistance on the neighboring three cards.

Because the performance test affected the ambient temperature and ψ_{ca} of the neighboring cards the performance testing was eliminated. In a new protocol the ψ_{ca} of each card is directly measured from the constant interface temperature parameters. This stabilizes the system as the power states and fan settings on the card stay fixed throughout the test.

Card Fan Impacts on ψ_{ca} Measurements

The noise in ψ_{ca} measurements using the constant interface temperature parameters was a concern as the expected degradation was within the measurement noise. To reduce

the noise, the card fans were turned on and set to the minimum speed to generate a higher forced convection than allowed by the system fan attached to the RITTAL rack. In Figure 14 the fan was turned on and set to the minimum fan speed 906 hours into the test for card one and the effect of the amplitude in noise is seen with and without the fan.

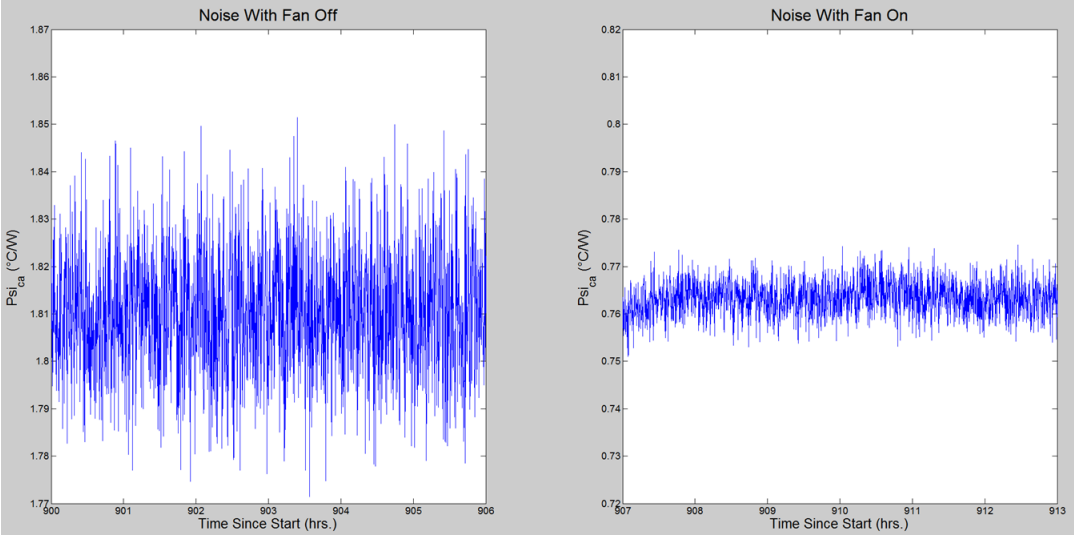

Figure 14: Side-by-side comparison of performance measurement noise with card fan off vs. card fan on

Both subplots have the same range in ψ_{ca} and a reduction in noise is seen with the fan on. The reduced noise will give higher confidence in any TIM 2 degradation. However, turning on the fans comes with the higher risk of heater failure due to the increase in power needed to maintain the same interface temperature.

System Fan Impacts on ψ_{ca} Measurements

Two control systems were initially used to maintain the ambient temperature within the RITTAL rack: the temperature control system that came with the RITTAL rack, and the control system used to control the temperature of the water in the intermediate liquid loop. The RITTAL system will first change its water valve position to 100% open and if

that is insufficient at reducing the ambient temperature the speed of the system fans is increased, which increases the air velocity in the rack. The second system controls the speed of the fans attached to the ceiling heat exchangers responsible for rejecting heat into the HVAC system.

The problem with the system for controlling air temperature inside the RITTAL rack is that the water temperature increased to a point where the ambient temperature could not be maintained. When that happened, the speed of the system fan in the rack was increased. This increased the forced convection within the rack and reduced the ψ_{ca} measured on all cards within the system. This is seen in Figure 15.

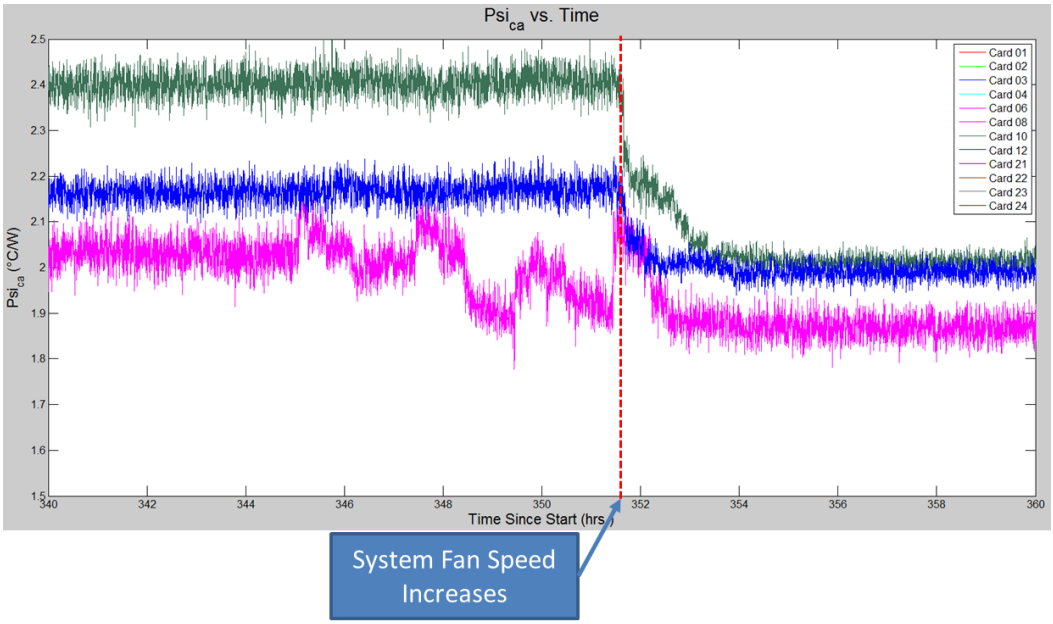

Figure 15: Impact on performance measurement as a result of increase in system fan speed

To eliminate the effect of the system fan, the RITTAL control loop was turned off and put into manual mode. The RITTAL system fans were set to the minimum speed and the control valve in the RITTAL system was opened to 100%. The ambient temperature

in the rack would strictly be controlled by the water temperature alone from the heat exchanger rejecting heat into the building's HVAC system.

Building HVAC Impacts on ψ_{ca} Measurements

The water temperature in the intermediate liquid loop controls the local ambient air temperature for the cards being tested. Initially, the goal was a high local ambient temperature. A simple resistance model of the parasitic losses and the measured heat flow path from which we take measurements from is shown in Figure 16.

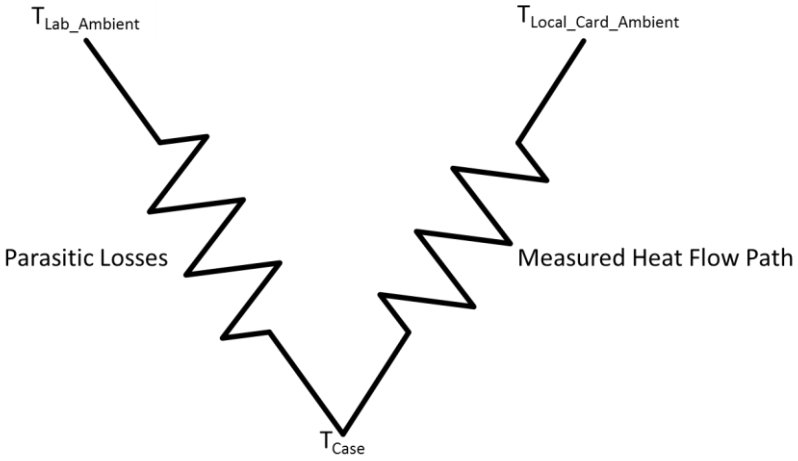

Figure 16: Two resistor model of measured heat flow path and parasitic losses

With the resistance path through the intermediate water loop being large due to the higher local ambient within the rack, the parasitic losses significantly impacted ψ_{ca} measurements as the temperature in the lab fluctuated by a degree or so over the course of 24 hours. Only the difference between the case temperature and the local card ambient temperature are accounted for in the main heat path of the system when measuring ψ_{ca}. As the temperature in the lab decreased, more power was needed to maintain the same interface temperature due to an increase in heat flow through the parasitic losses. This

results in a perceived improvement in the ψ_{ca} measurement. Because of the power fluctuation this shows up in the ψ_{ca} measurements as an oscillation with a period of 24 hours as shown in the Figure 17.

Reducing the local card ambient temperature and bringing it closer to the lab ambient temperature minimized the effect of the parasitic losses, but did not eliminate it. The result of this is shown in Figure 18.

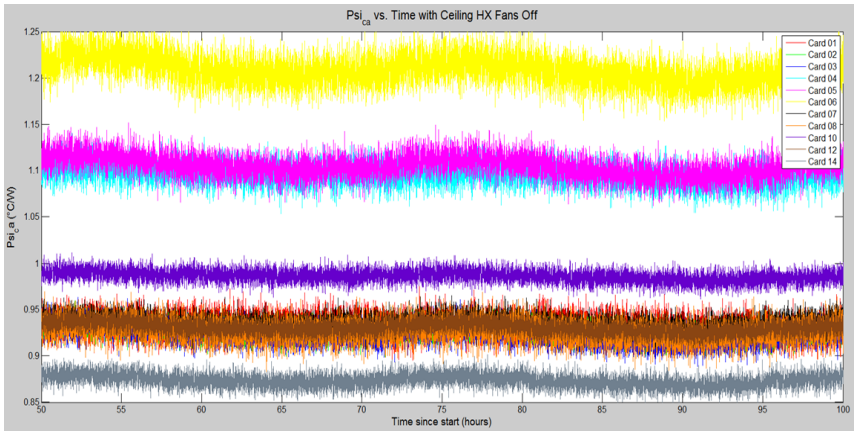

Figure 17: Performance measurement fluctuations with high ambient temperatures

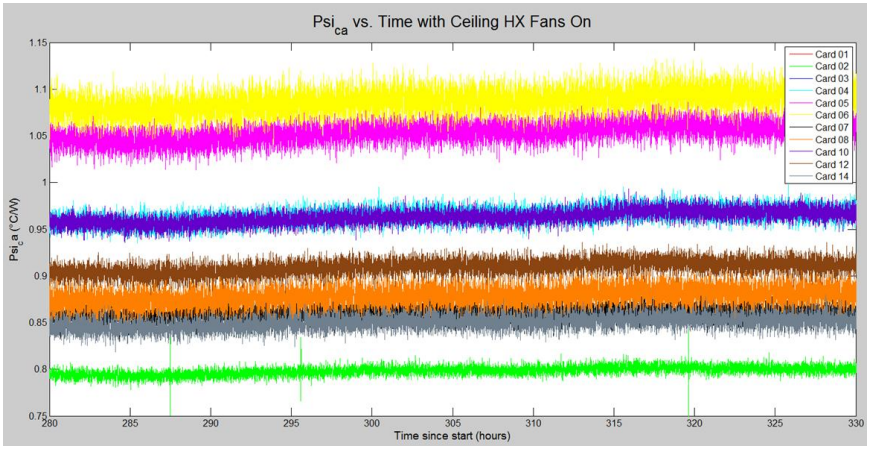

Figure 18: Performance measurement fluctuations with lower ambient temperatures

Card-to-Card Coupling

The extent of card-to-card coupling was realized when intermittent heater function was observed to have an impact on the remaining cards in the rack. Figure 19 shows the layout and location of the 24 cards in the system and highlights cards 01 and 03 that had heater failures early in the testing.

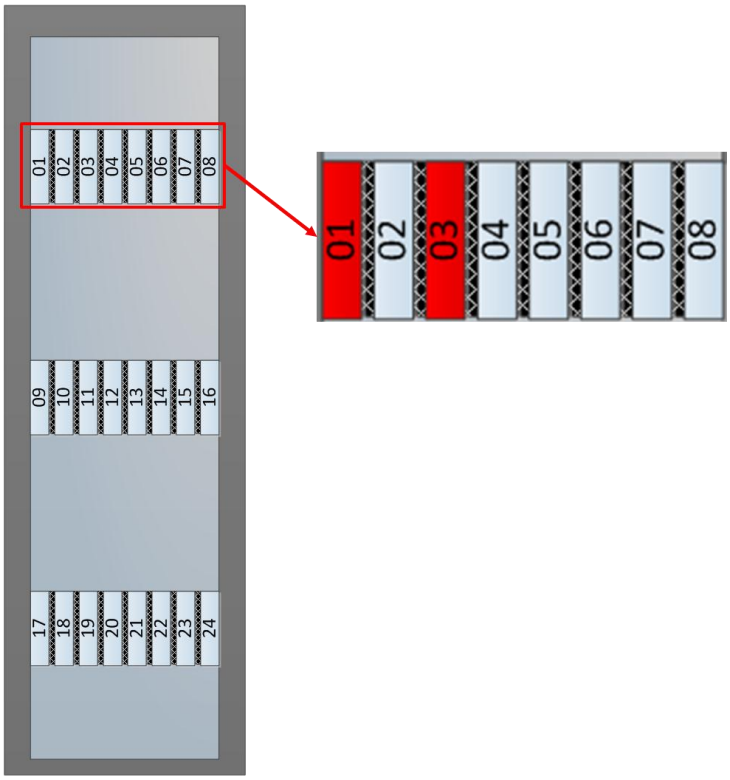

Figure 19: Card layout within RITTAL rack highlighting problem cards

The partial failures of cards 01 and 03 and their influence on the remaining 6 cards in the chassis were noticed. An isolated failure occurred in card 03 that caused a temporary low power setting followed by a recovery as shown in the power graph in Figure 20.

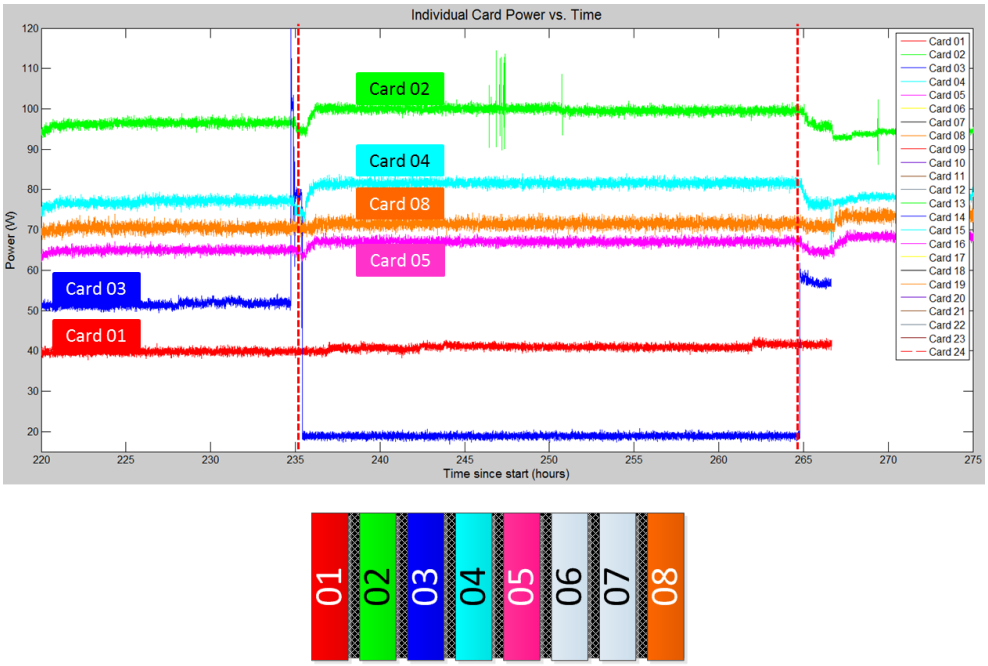

Figure 20: Power setting impacts on neighboring cards as a result of Card 03 heater failure

Card 03 is shown as the blue line in Figure 20. Within the same eight card chassis an impact exists as an adjustment in power to maintain the interface temperature. The influence of one card on another within this system is similar to the effect described by the superposition calculation of influence coefficients for individual components on an electronic board (Muzychka, 2006). The CITRAM system is viewed as a large electronic board in this instance where each card is coupled to the other 23 cards in the system to varying degrees. Knowing the influence coefficients and the power of all 24 cards within the system the resulting case temperature is determined by

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \vdots \\ \Delta T_{23} \\ \Delta T_{24} \end{bmatrix} = \begin{bmatrix} \psi_{1,1} & \psi_{1,2} & \cdots & \psi_{1,23} & \psi_{1,24} \\ \psi_{2,1} & \psi_{2,2} & \cdots & \psi_{2,23} & \psi_{2,24} \\ \psi_{3,1} & \psi_{3,2} & \cdots & \psi_{3,23} & \psi_{3,24} \\ \vdots & \vdots & \cdots & \vdots & \vdots \\ \psi_{23,1} & \psi_{23,2} & \cdots & \psi_{23,23} & \psi_{23,24} \\ \psi_{24,1} & \psi_{24,2} & \cdots & \psi_{24,23} & \psi_{24,24} \end{bmatrix} \cdot \begin{bmatrix} \mathrm{P}_1 \\ \mathrm{P}_2 \\ \mathrm{P}_3 \\ \vdots \\ \mathrm{P}_{23} \\ \mathrm{P}_{24} \end{bmatrix} \quad (8)$$

The first number in the subscript of ψ is the temperature delta of the card that is being solved for and the second number in the subscript is the influence of that card on the card being solved for. Throughout the testing it was discovered that each card has a unique influence on its neighboring cards and is not only contained within one test card chassis.

Results

Isothermal Bake Analysis

In parallel an isothermal bake was conducted to compare to the CITRAM testing. The bake temperatures used were 120°C and 100°C for the high and low temperature bake legs, respectfully. The data were normalized and then averaged by bake leg temperature and the degradation results in Figure 21.

The best fit curve through the data uses a natural log transformation of time to linearize the data and the Arrhenius model is applied. By transforming the time axis the linearization of the data are put in the same form as the Arrhenius equation described in Equation (3) as shown in Figure 22.

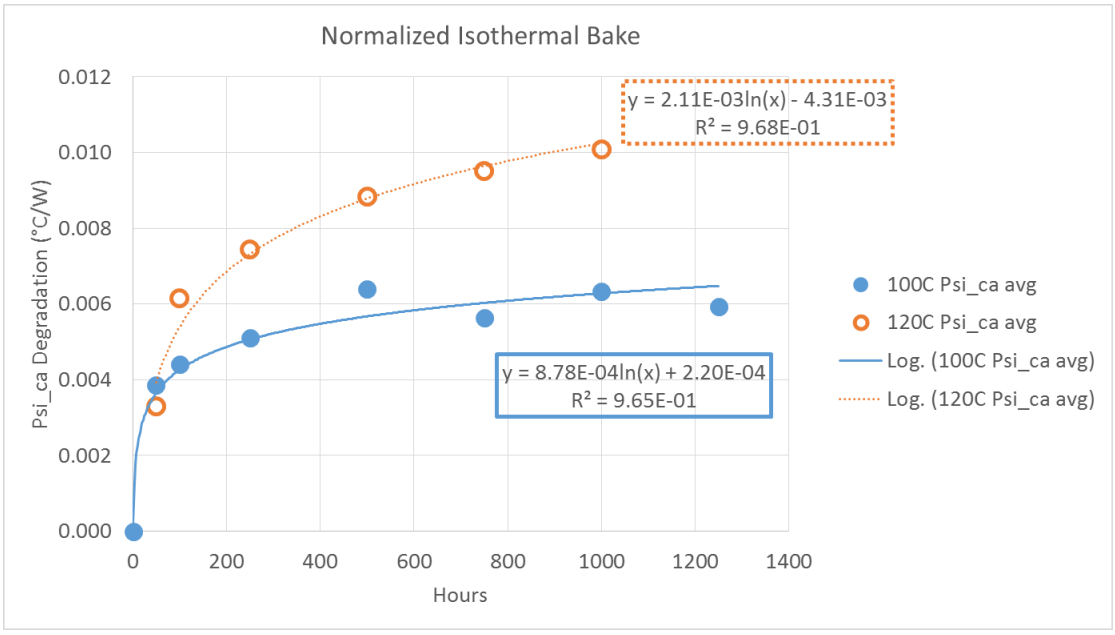

Figure 21: Isothermal data normalized to time zero performance

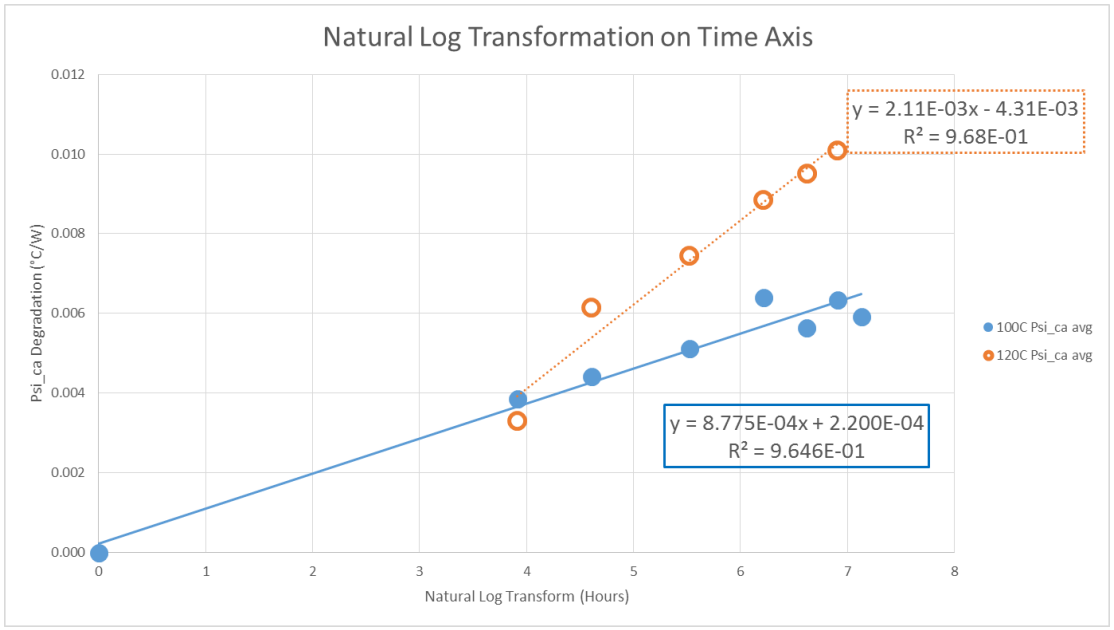

Figure 22: Isothermal data with natural log transformation of time to linearize data

The Arrhenius modeling can now be performed with the data linearized. The parameters needed to calculate the activation energy are shown in Table 1.

Table 1: Parameters to Calculate Activation Energy

Bake Temp	1/kT	R	ln(R)
100°C	47264	8.775E-04	-7.04
120°C	44860	2.108E-03	-6.16

The activation energy can now be computed using Equation (5).

Now that the activation energy is known the expected acceleration factor from 120°C case temperature to the use case temperature was determined with the use of Equation (4). For the purpose of this study, the use case temperature is assumed to be 90°C, which is the lower temperature used in the CITRAM study. An equivalent time tested at an elevated temperature was calculated using

$$t_{test} = t_{use}^{\frac{1}{A_F}} \tag{9}$$

Equation (9) differs from Equation (6) because of the natural log transformation on time. Simple algebra was used to find the equivalent time.

Plugging in all variables and solving for the unknown parameters yields Table 2.

Table 2: Isothermal Arrhenius parameter analysis results

Parameter	Value	Units
Ea	-3.64E-04	W/m^2*K^3
AF	3.9	--
t_{test}	15.11	hours

From the isothermal bake, assuming a use case of 90°C and a 5 year life at 80 % on time, an equivalent test time at an elevated test temperature of 120°C was reached in about 15 hours. This is a typical result expected from an isothermal elevated temperature bake.

Using the Arrhenius equation we can determine the fit curves for a 90°C and 110°C bake. This is shown below in Figure 23 and will be used later to compare against the equivalent test temperatures in CITRAM testing.

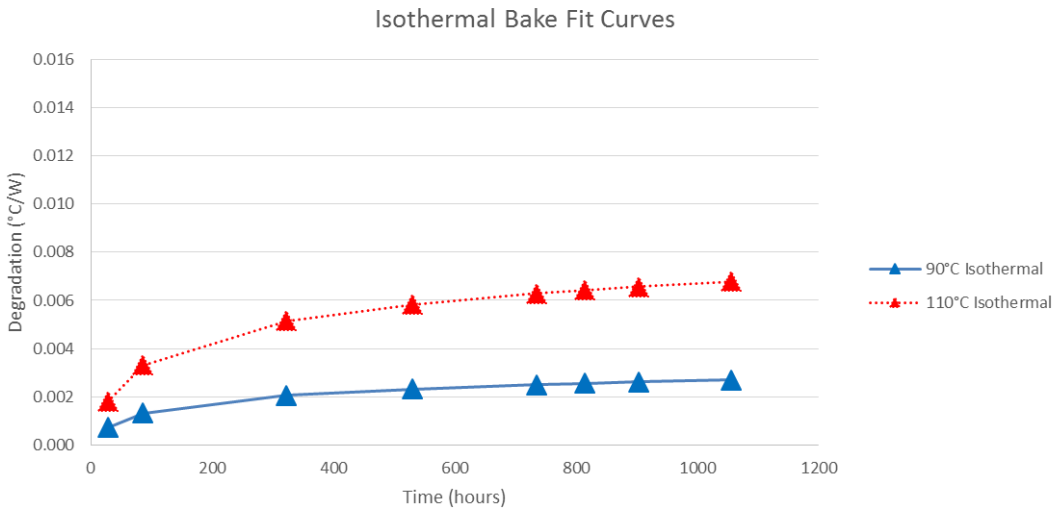

Figure 23: Isothermal fit curves for 90°C and 110°C case temperatures for comparison to CITRAM data

Next, a technique used in weather data analysis is performed to look at just the difference in degradation between the predicted temperatures of 110°C and 90°C of both methods (Michaels, 2008). This will be used to compare to the same data analysis in the CITRAM data. The results of this data manipulation is shown in Figure 24.

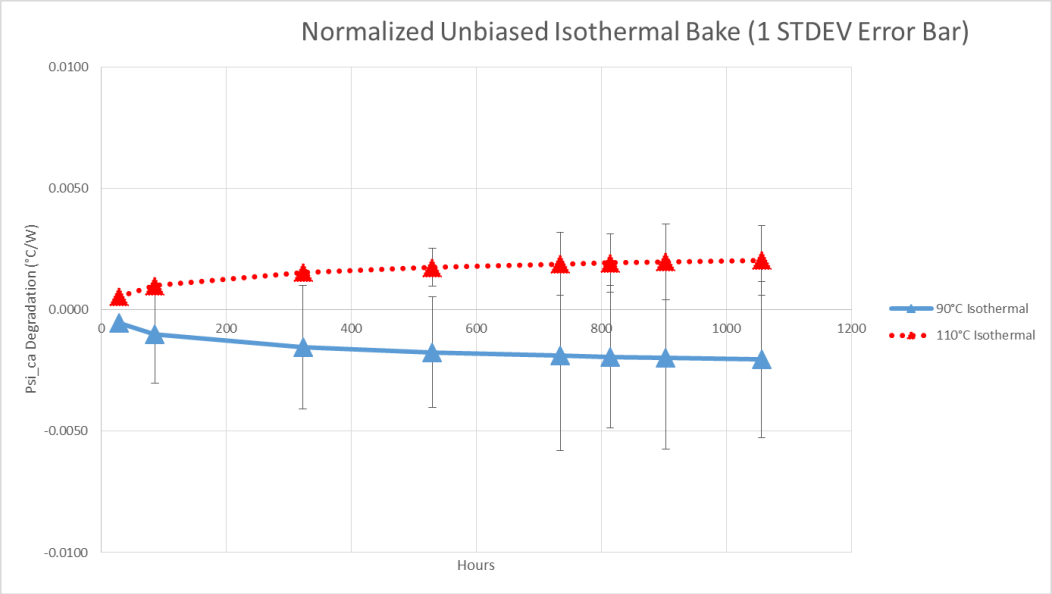

Figure 24: Normalized and unbiased Isothermal bake data to compare differences in bake temperatures

At each time the average of both upper and lower bake leg temperatures are subtracted from each of the bake legs. The result is an equal and opposite degradation between the two bake temperatures about the X-axis. This removes all global effects and absolute degradation in the testing and allows comparison of the different bake legs within the test. Performing the same analysis on the CITRAM will allows a comparison between the test methods.

CITRAM Test Analysis

Looking at Equation (3) used to model TIM degradation an assumption is made that the ambient temperature the card is tested in has a negligible effect on the degradation. This assumption assumes that the mechanical stresses caused by CTE mismatches and the small thermal gradients within the TIM have no impact to ψ_{ca}degradation. With the complexity of the thermal solution this assumption is no longer valid. The Arrhenius

model for TIM degradation has been rewritten below with an additional term that includes an affect for the ambient temperature the TIM is tested in.

$$\psi_{ca}(t) = b + t * \left(e^{\left(\frac{E_a}{k \cdot T_c}\right)} + e^{\left(\frac{E_a}{k \cdot T_a}\right)} \right) \tag{10}$$

In Equation (10), b is a constant that is the initial performance, t is time, and there are two exponent terms, one with respect to the absolute case temperature and the second with respect to the ambient temperature. The model in Equation (10) has the same form $\psi_{ca}(t) = b + Rt$, where the rate, R as described in Equation (2), is the sum effect of the case temperature and the ambient temperature. In the case of isothermal bake the ambient temperature is the same as the case temperature and in the CITRAM test configuration the ambient is much lower than the case temperature. Equation (10) shows that the absolute ψ_{ca} at any time greater than zero should be different between the two methods in this study given that the ambient temperatures are different at the respective case temperatures. If ambient temperature does not matter as is assumed in the current ψ_{ca} model, shown in Equation (3), the degradation prediction of the two methods should be equivalent. The analysis approach of Equation (3) is taken since Equation (10) would require a minimum three tests, 2 separate case temperatures, and 2 separate ambient temperatures at one of the case temperatures tested.

CITRAM Ambient Temperature Stratification

Within the CITRAM test apparatus a stratification of ambient temperatures within the test unit was observed as seen in Figure 25.

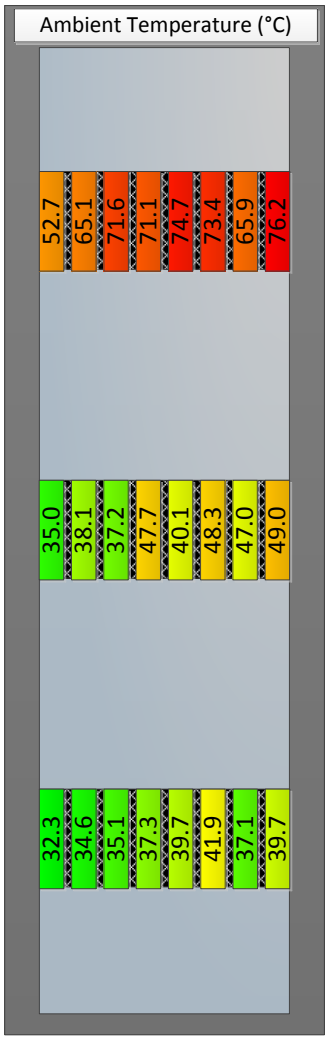

Figure 25: Ambient temperature variation within rack system for final run

Figure 25 is a frontal view of the CITRAM system with the respective ambient temperatures and color gradient applied to each card. The stratification exists from top to bottom in the entire system, with the top having an elevated temperature. Also within a test cards chassis there is a temperature variation from left to right with the right side

being hotter than the left. The point of the system is to have an isothermal ambient temperature for all cards under test. The poor reliability of the test cards forced system settings such that a lower power could be used to conduct the test to 1,000 hours. The TMTB failures and the change in system settings had the adverse effect of causing the stratification seen because the fans speed was also reduced to accommodate a lower power setting while maintaining the same case temperature.

As a result of the stratification, cards that were located in the middle chassis that had an ambient temperature within 2°C of each other were used in the analysis. There are two cards in each higher and lower case temperature tests. The selected cards are shown in Figure 26.

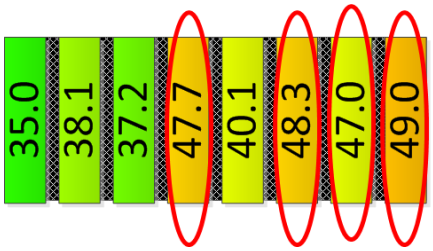

Figure 26: Selected cards for data analysis based on similar ambient temperatures

CITRAM Degradation Analysis

The degradation of the cards was normalized and averaged by case temperature with respect to their time zero performance. Refer to the raw data reduction described in the appendix. The results of this analysis follows in Figure 27.

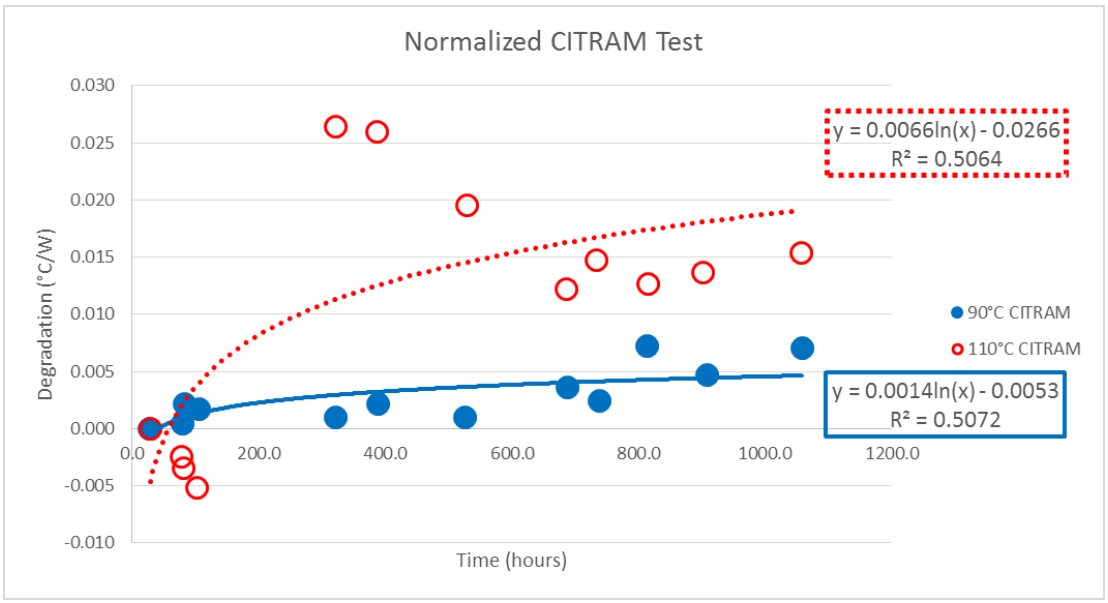

Figure 27: CITRAM data normalized to time zero performance

Performing the same natural log time transformation and adding fit curves yields Figure 28.

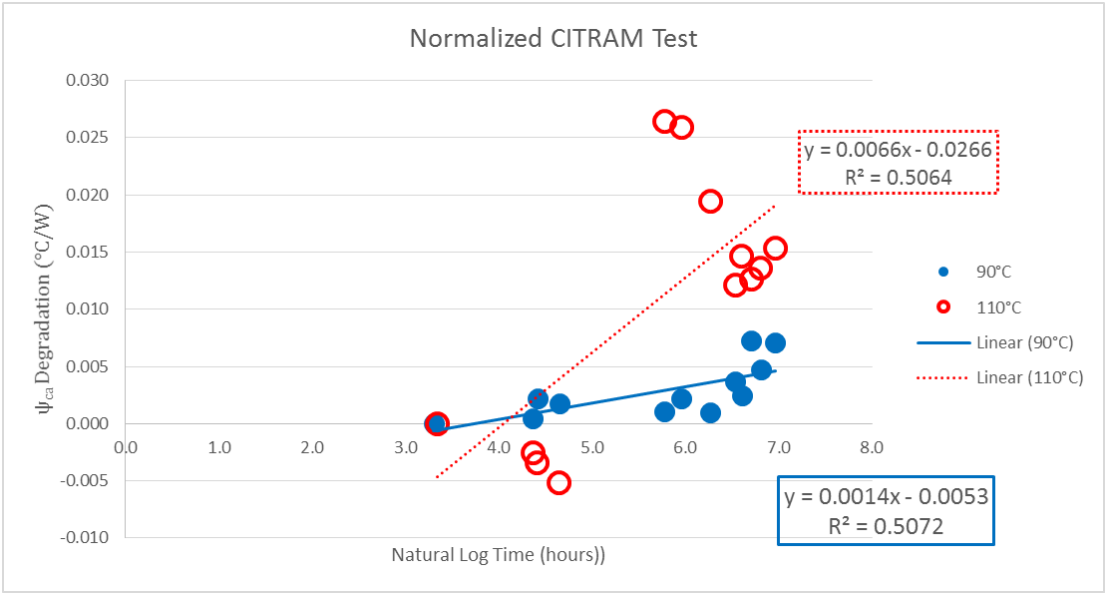

Figure 28: CITRAM data with natural log transformation of time to linearize data

Performing the same analysis on the CITRAM data set yields the parameters shown in Table 3.

Table 3: CITRAM & Isothermal Arrhenius parameter analysis results

Parameter	CITRAM Values	Isothermal Values	Units
Ea	-4.91E-04	-3.64E-04	W*s
AF	6.2	3.9	--
t_{test}	5.5	15.0	hours

Comparing the results of Table 3 and Table 2 there is a difference between the two different methods. This becomes apparent as well when the degradation trends of the two methods are laid on top of each other as shown in Figure 29.

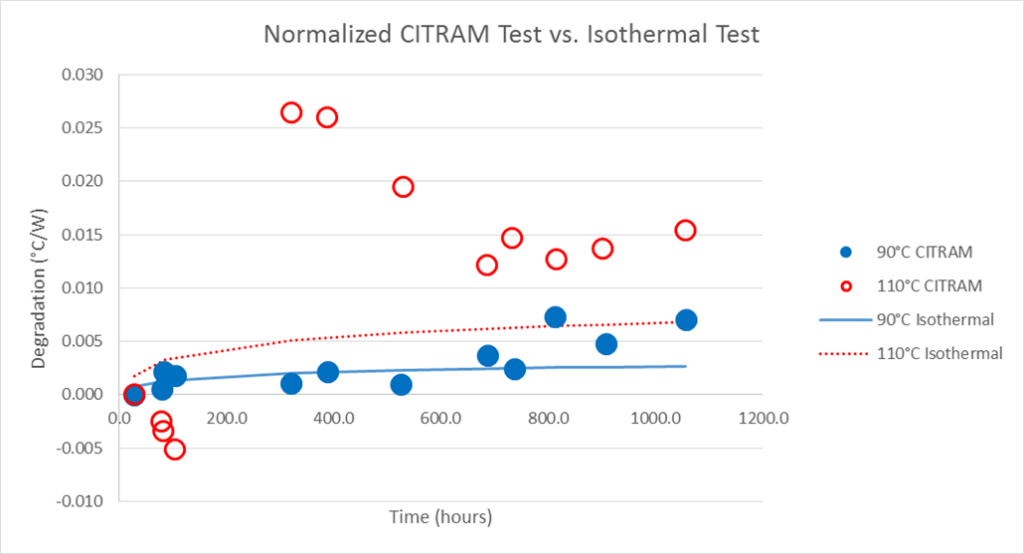

Figure 29: Isothermal bake and to CITRAM degradation rate comparison

However, the R^2 value for the fit curves are not acceptable. A second comparison approach was taken to correct for the variation of the ambient temperature. This method is commonly used in weather modeling and is used to compare the bias between two or more weather stations that should be equivalent (Michaels, 2008). The improvement of the TIM measured in the test was greater than the total resistance of the TIM and this

improvement is attributed to global effects affecting the system. This was seen in the raw data shown below in Figure 30.

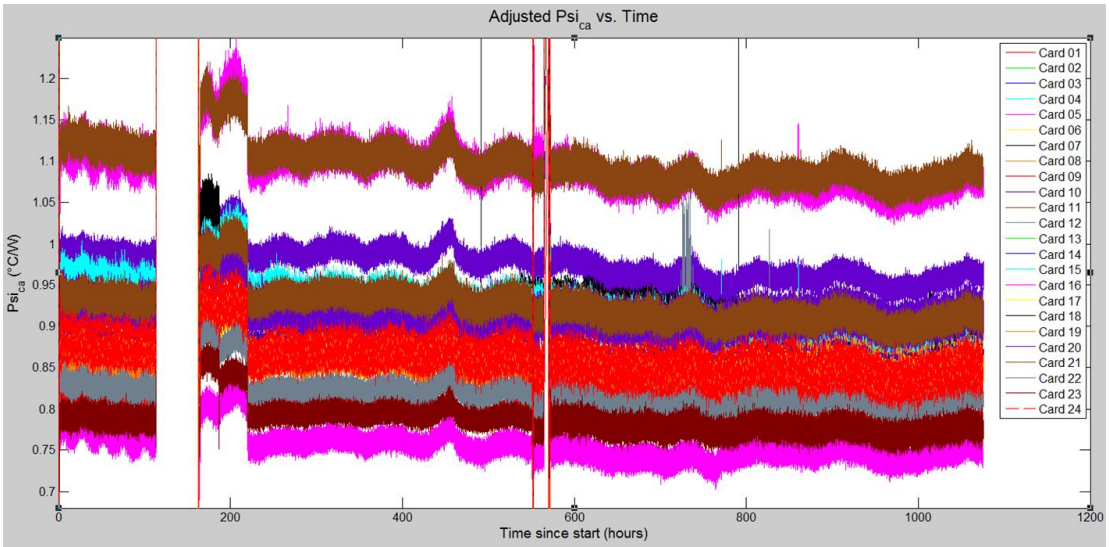

Figure 30: CITRAM data after adjustment to data to correct for card failures

The oscillations in the data in Figure 30 for all cards are identical in period and in magnitude indicating the global effects described earlier. In addition the spikes in the data align with HVAC system spikes.

The common trend of cards located in the middle chassis with ambient temperatures within 2°C are used to compare with isothermal bake. Selecting cards from the middle chassis removes the confounding of the upper chassis also being at a higher ambient temperature due to the variation shown in Figure 25. The results of the unbiased data analysis is shown in Figure 31.

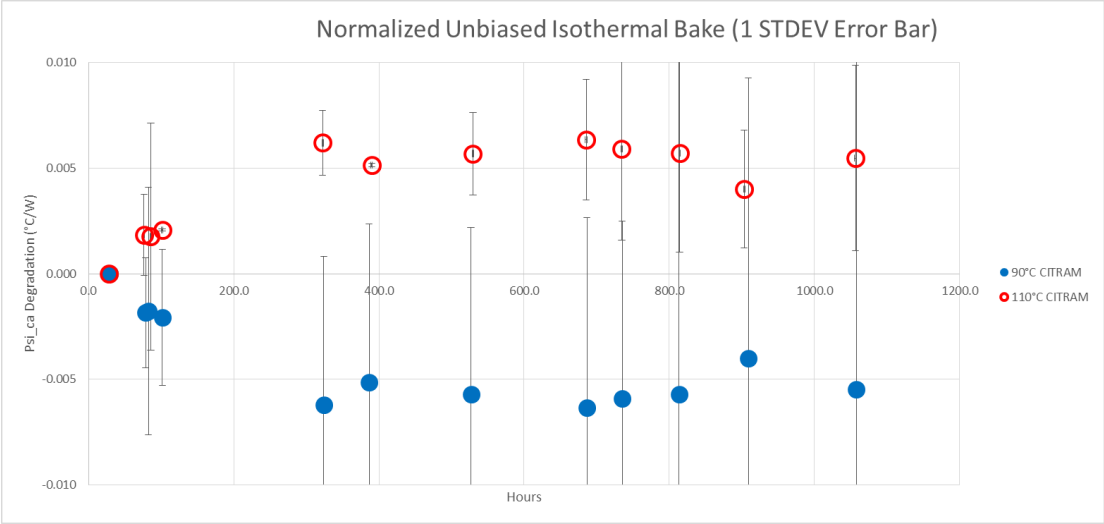

Figure 31: CITRAM data analysis using unbiased technique

When the data from the two different methods are plotted on the same graph, the data from the CITRAM test does not line up with the fit curves for the equivalent case temperatures from the Isothermal data as shown below in Figure 32.

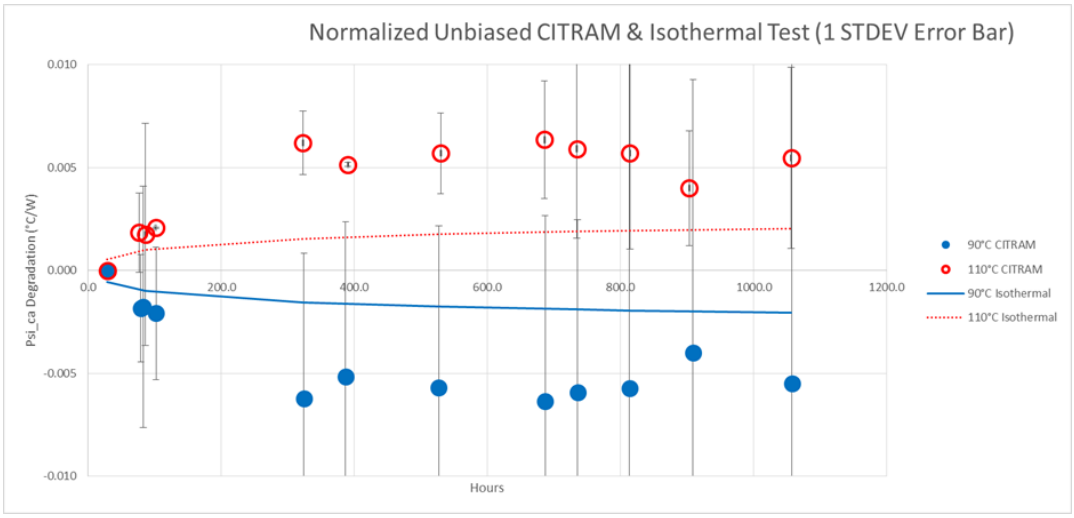

Figure 32: Isothermal comparison to CITRAM degradation using unbiased technique

The difference in the graph in Figure 32 indicates that there is a difference in the separation between the two temperatures. With this graph it would not be possible for the

predicted degradation and the acceleration factor between the two methods to be equivalent. CITRAM data are adjusted, maintaining the difference in higher and lower case temperature, such that the acceleration factor between the two methods are equivalent and the degradation prediction is plotted as shown in Figure 33.

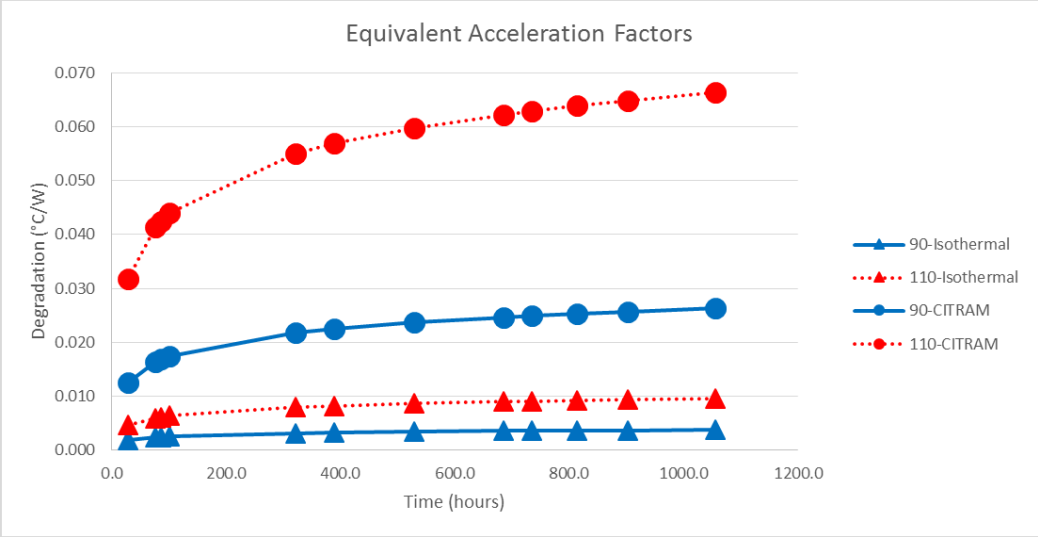

Figure 33: Comparing Isothermal and CITRAM degradation rates with an equivalent acceleration factor

Figure 33 shows that if the acceleration factors were equivalent between the two methods, the degradation would not be the same which is an indicator that there is difference between the two test methods.

Conclusion

The goal of this research is to develop CITRAM, a new method of reliability testing for TIMs, and to compare the reliability predictions from CITRAM to the reliability predictions from the conventional isothermal bake method of accelerated life testing. The reliability of a TIM is determined by measuring an increase in ψ_{ca}, the thermal resistance between the case and ambient. The increase in ψ_{ca} from the initial measurement at time zero is considered a degradation since higher ψ_{ca} means the thermal control system is performing worse over time. The increase in ψ_{ca} over time is caused by mechanical (e.g. reflow or delamination) or chemical (e.g. outgassing or crosslinking) degradation of the TIM. An Arrhenius model is fit to the $\hat{\psi}_{ca}(t)$ data measured to obtain an acceleration factor, by comparing the rates of change in $\psi_{ca}(t)$ in the two different temperatures.

CITRAM is an alternative test method designed to hold the computing modules in a more realistic non-uniform thermal environment during the long-term reliability tests. Throughout the testing period, the device under test is stressed with a steady case-to-ambient temperature gradient and ψ_{ca} values are measured continuously.

Unlike CITRAM, the steady bake method does not impose a thermal gradient across the TIM. With steady bake testing, the device under test is periodically removed from the high temperature environments (ovens) and then placed in a separate apparatus for a relatively short period of time to measure ψ_{ca}. In contrast, CITRAM measures ψ_{ca} continuously and does not require physical handling of the device under test during the test.

At the end of the test it was clear that there were two different responses from the performance measurements taken over time in the two test methods. It was predicted that there would be a difference in degradation rates because of the CTE mismatch of the several components that make up the total thermal solution for the card. Although the absolute degradation of the CITRAM test unit was not realized due to the poor reliability of the thermal test board and the global effects of the system, there was a definite difference between the two methods, indicated by the difference in separation of the two identical test temperatures.

It is the opinion of the author that CITRAM holds further potential for improving the long term reliability prediction of TIM performance. Isothermal bake testing has been utilized for these predictions due to the constraints of thermal test board and test facility capabilities. However, it has been demonstrated that an approach like CITRAM provides a closer approximation to customer use conditions, and the research described herein has shown that results between the two methods are statistically different. Further improvements in reliability of test boards to sustain high power at high temperature for extended durations are required to realize the full potential benefits of CITRAM.

References

D. DeVoto, P. P. (2014). Thermal Performance and Reliability Characterization of Bonded Interface Materials (BIMs). *NREL/CP-5400-61107* (pp. 1-2). Orlando, Florida: National Renewable Energy Laboratory (NREL) .

Michaels, P. J. (2008). Global Warming: Correcting The Data. *Regulation*, 46-52.

Muzychka, Y. S. (2006). *Influence Coefficient Method for Calculating Discrete* (Vol. 29). St. John's, Newfoundland, Canada: IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES.

Nelson, W. B. (2004). *Accelerated Testing Statistical Models, Test Plans, and Data Anaysis.* Hoboken, New Jersey, Unites States of America: John Wiley & Sons.

Sauciuc, I. (2005). Thermal Performance and Key Challenges For Future CPU Cooling Technologies. *IPACK2005-73242* (pp. 1-3). San Francisco: ASME InterPACK.

Appendices

A. CITRAM Data Reduction

With the poor reliability of the test boards and global effects on the measured $\psi_{ca}(t)$, data reduction and manipulation was done to perform the final data analysis.

The data manipulation was done based on the super position behavior in the measured $\psi_{ca}(t)$ as described in Equation 8. When a neighboring card died, an effect could be seen as a shift in $\psi_{ca}(t)$ as shown in Figure 34.

In this case the data collected after the neighboring card crashed is shifted up to match with the data before the crash. The measured ψ_{ca} values after the crash were simply shifted by the amount of the jump in ψ_{ca} that occurred at the time of the crash.

$$\acute{\psi}_{ca}(t_{crash}: t_{end}) = \psi_{ca}(t_{crash}: t_{end}) + (\psi_{ca}(t_{crash}) - \psi_{ca}(t_{crash-1})) \quad (11)$$

The result of this is a stitching effect that follows in Figure 35. The now adjusted data set is a continuous curve without the effect of the failed neighboring card. This adjustment was performed on all cards in the CITRAM test apparatus.

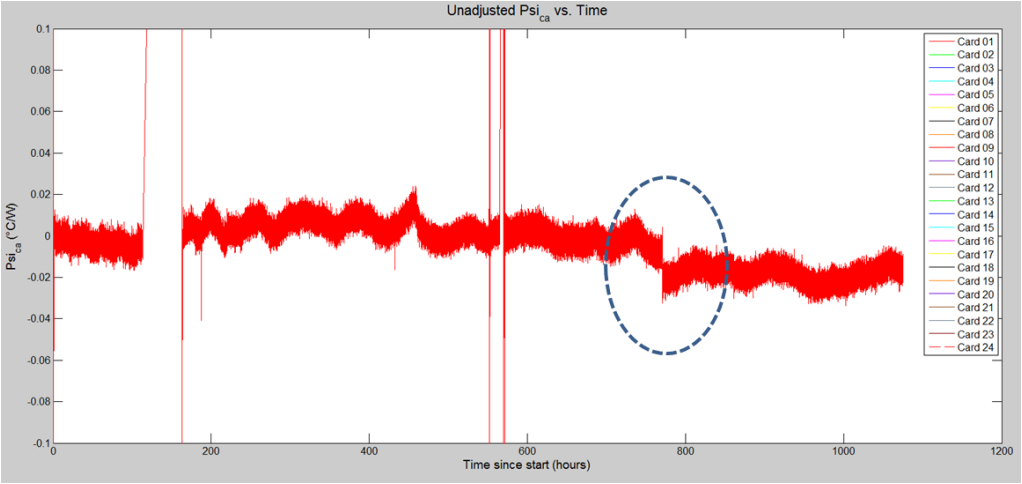

Figure 34 Measured ψ_{ca} for Card 09 showing the effect of a crash on card 04

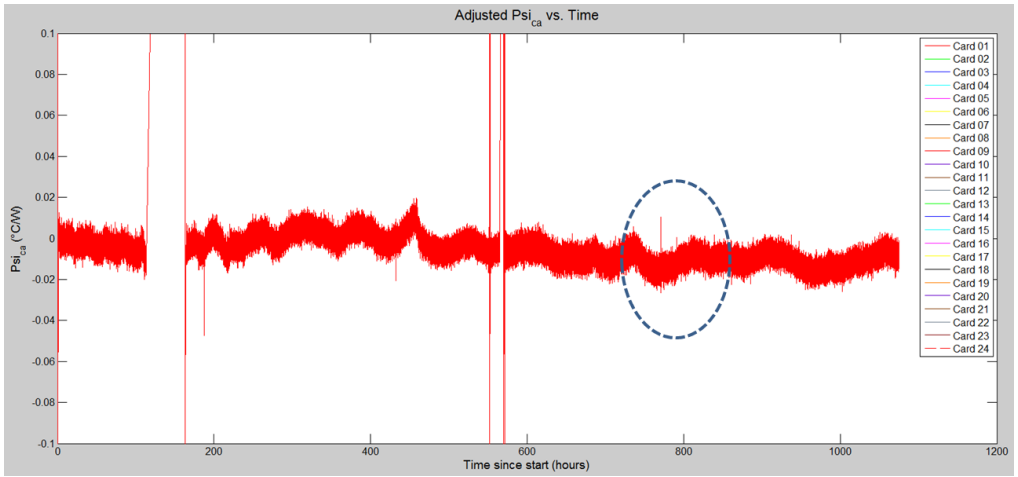

Figure 35 Values of ψ_{ca} for card 09 after correcting for the effect of the crash on card 04

Once the data were adjusted for card failures, windows of data were selected based on a single period of the oscillations and the maximum ψ_{ca} value was identified within that window. An average of 30 of the neighboring values around the identified maximum ψ_{ca} are recorded with the associated time of those 30 data points. An example of this is shown on the data set below in Figure 36.

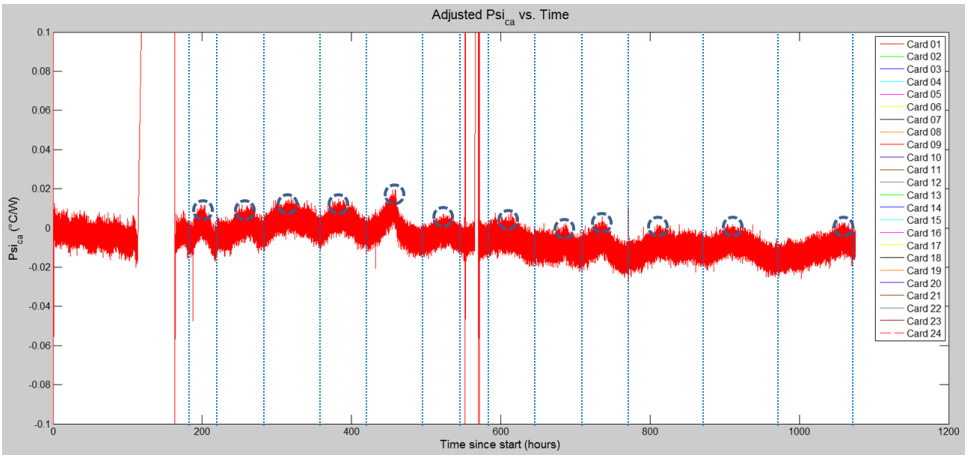

Figure 36 Windows and averaged data points for CITRAM data

The vertical lines in Figure 36 represent the separation of the windows and the dashed circles are where the data is averaged. To validate this approach an assumption that the oscillations in the data are equal in amplitude from period to period was made and any difference in data is a result of the degradation of the TIM.

The data shown in the body of this document is a result of the two steps described to compare to the isothermal data.

B. Removing Degradation and Global Effects

With the confounding of the global effects caused by the building HVAC system a second analysis approach was taken to compare the two test methods. The idea is to only look at the differences between the high and the low bake leg as

$$\acute{\psi}_{ca\_High}(t_n) = \psi_{ca\_High}(t_n) - \frac{\psi_{ca\_High}(t_n) + \psi_{ca\_Low}(t_n)}{2} \quad (12)$$

$$\acute{\psi}_{ca\_Low}(t_n) = \psi_{ca\_Low}(t_n) - \frac{\psi_{ca\_High}(t_n) + \psi_{ca\_Low}(t_n)}{2} \quad (13)$$

Here $\psi_{ca\_High}(t_n)$ is the ψ_{ca} average performance of the high temperature solutions and $\psi_{ca\_Low}(t_n)$ is the ψ_{ca}average performance of the low temperature solutions. The result of plotting $\acute{\psi}_{ca\_High}(t)$ and $\acute{\psi}_{ca\_Low}(t)$ are two curves that are equal and opposite across the x-axis that reflect only the differences in the two temperature bake legs.

Two arbitrary degradations rates are created with a sinusoidal effect imposed on the data shown in Figure 38

If the average of both curves are computed and plotted on top of the graph a resultant curve should be produced that splits the data evenly as shown in Figure 39

In the last step the average curve is used to subtract from each of the case temperature data sets to produce the final graph shown Figure 40

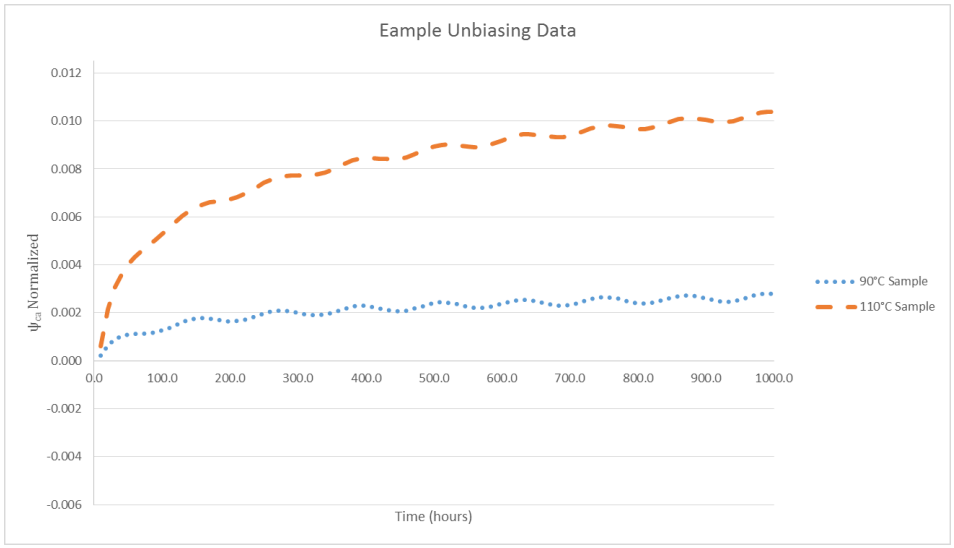

Figure 37: Simulated data with sinusoidal effect super imposed on top

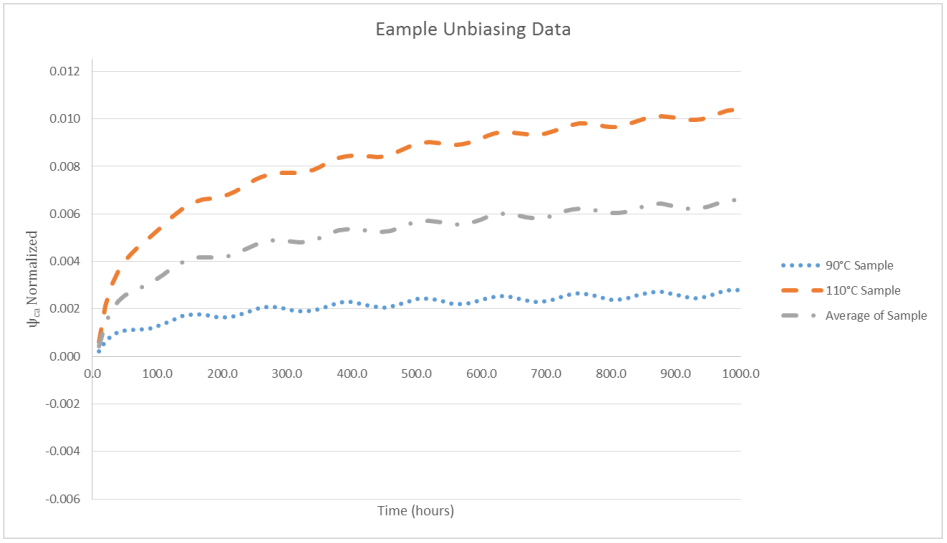

Figure 38: Average of simulated data included in graph

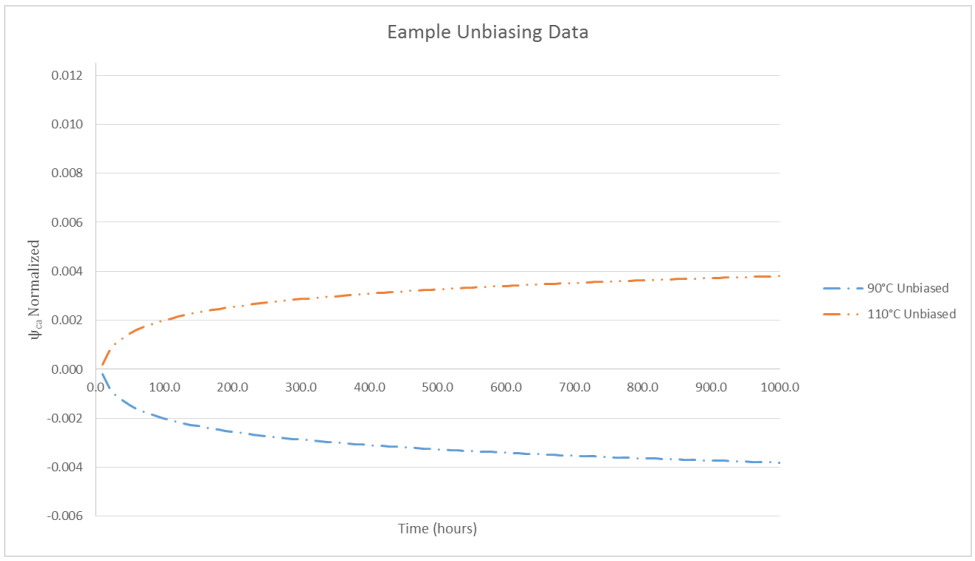

Figure 39: Final graph to compare both case temperature data sets to each other with degradation and global effects removed

By removing any confounding effects on the data both testing methods are compared to each other. If the two methods are equivalent then the data sets will line up with each other when overlaid on top of each other.