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Design of a Microprocessor Controlled Telecommunication System

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Recent advancements in Large Scale Integration Technology have made available devices, such as microprocessors, analog gates and "three state" logic, that provide the designer with a wide range of possibilities in the design of telecommunication systems. A microprocessor and analog gates are utilized in this design to demonstrate the feasibility of implementing a flexible Telecommunication System. The microprocessor is programmed to control, through software, the system functions. The feasibility of systems highly adaptable to the needs of individual

subscribers is thus demonstrated.

DESIGN OF A MICROPROCESSOR CONTROLLED TELECOMMUNICATION SYSTEM

by

GEORGE J. MAROUTSOS

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PREFACE

The objective of this project is to demonstrate the feasibility of implementing a flexible and easily expandable telephone system, that can be adapted to the needs of individual users, at low cost.

By utilizing advantages offered by analog gates, microprocessors and "Three State" logic, and because of the nature of the multiplexing/demultiplexing scheme used, the system described here can serve large numbers of subscribers.

Detailed discussion of the technical aspects of the design compromises will be taken up in the main body of this report. Suffice it to state here, however, that time division multiplexing and pulse amplitude modulation is used. The design approach is such as to reduce to acceptable levels the shortcomings, primarily excessive cross-talk, associated with these techniques. Although it can be argued that other multiplexing techniques could improve the cross-talk levels, the sacrifices in system flexibility and the increased complexity of control do not warrant their use at the clock rates utilized in this system.

The system will be controlled by microprocessor. The MOS Technology, Inc. MCS6502 microprocessor will be used.

I wish to express my sincere thanks to Dr. Harry S. White for pointing the way, to Mr. Jack C. Riley for encouraging me, and to Mr. Henri B. Joyaux for his boundless patience and his invaluable technical advice, without which I would have never begun this undertaking.

I also wish to thank Deena, my wife, for her understanding and for typing the manuscript.

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CHAPTER I

INTRODUCTION

In order to carry out Telecommunication, the audio signal must be converted to a form transmissible over the required distance, the means of transmission must be provided and reconversion of the signal to its original, audible form must be achieved at the receiving end. If this telecommunication is to be selective, that is only between selected participants, to the exclusion of everyone else, the means of selecting the recipient must also be provided.

When the first telephone exchange went into operation in New Haven, Conn., on Jan. 20, 1878, with only 20 subscribers, it was operated manually and the selection of the called party presented no insurmountable problem. Since that time, however, the number of subscribers has increased to well over 200 million, and the selection of the called subscriber presents the problem of designing into the telephone system the capability of addressing any and all other subscribers efficiently. Efficiency in this case implies the successful completion of calls without excessive delays and on the first attempt a good part of the time, but primarily it implies economical use of the telephone plant. Even though each subscriber must have the capability of addressing every other subscriber, in practice, the vast majority of "other" subscribers will never be called, a very small number of subscribers will be called very rarely, while a miniscule number of subscribers will be called with any regularity. However, even this regularity, which may amount to a

few times a day, adds up to a small percentage of the total time.

A number of schemes have evolved over the last hundred years, each of which attempts to provide reliable and economical telephone service. All of these utilize some mix of space and time division multiplexing of the audio path and also of the control function, the means of setting-up of calls, and of maintaining the audio path for the duration of the conversation. The rapid rate of increase in the demands placed upon the telephone system has forced the development of ever newer, faster, more compact and increasingly flexible systems. These systems, whether manual, step-by-step or register controlled make use of metallic cross-points. The metallic cross-point, though it represents a "slow" technology long superceded in most fields of electronic applications, offers the advantage of a low, linear impedance path through the telephone switching system. Also, because of its slow response time, it possesses the advantage of not responding to fast transients that may occur throughout the system. Because of these inherent advantages, and because of the relatively lower costs of manufacture of a system based on relay and reed-switch technology, but primarily because of the size of investment in this technology, which as measured by the existing equipment operated by the telephone companies, ranges into the billions of dollars, there exists great inertia to the urge to update. There is no inherent advantage in the elegance or originality of design. The final choice is that design approach which optimizes the objective function. In the case of a telecommunication system, the variables that constitute the objective function include: intelligibility of signal, cost, reliability, maintainability, adaptability of the system to different and varying sizes of serviced area,

etc. Cost includes, in addition to development, hardware and real estate costs, other indirect costs such as the cost of training personnel to maintain the new equipment, the cost of the impact of the new equipment on existing equipment (interfaces, obsolescence due to new services which the old equipment cannot provide at a reasonable cost)...etc.

However, the relative importance of the economic factors affecting the process of making the choice of designs change continuously. Rapid advancements in the development of the Large Scale Integration (LSI) technologies, decreased costs of LSI because of economies of scale, increases in labor costs, costs of space and power, the pace of increase of demand for new service as well as the ability of the new technologies to provide features to the telephone system which would allow it to be flexible enough to be adaptable to the needs of each individual subscriber, are tipping the balance in favor of the new technologies.

Analog gates that permit high speed multiplexing, and the development of the microprocessor that allows software programming of the control of the switching of the audio signals, make the design of relatively inexpensive, adaptable systems feasible. Up to the present, relatively small telephone exchanges, such as those used by business firms, schools, hotels, hospitals, etc., could not be economically designed to provide services adaptable to the needs of the subscriber. Flexibility and adaptability were characteristics associated with relatively large systems, with several thousands of subscribers, controlled by a minicomputer. The microprocessor permits the design of exchanges servicing only a few subscribers, with flexibility and adaptability, at low cost.

CHAPTER II

SYSTEM DESCRIPTION

System Concept

Figure 2 shows the general configuration of the system. All the "subscribers" are connected to the Central Switching Unit by means of their "subscriber's lines." The "subscriber's line" consists of wires carrying the Transmit and Receive audio signals, DC power and Ground. On/Off Hook signals, multifrequency tone dialing, as well as ringing signals are transmitted by the audio wires.

The Central Switching Unit contains the System Controller, a microprocessor, which sequentially polls each subscriber's line. Changes in status are detected by the Central Controller and programmed action is taken to provide the required service.

A Pulse Amplitude Modulation, Time Division Multiplexing Scheme is used. Time is subdivided into slots, Fig. 1, determined by the system clock.

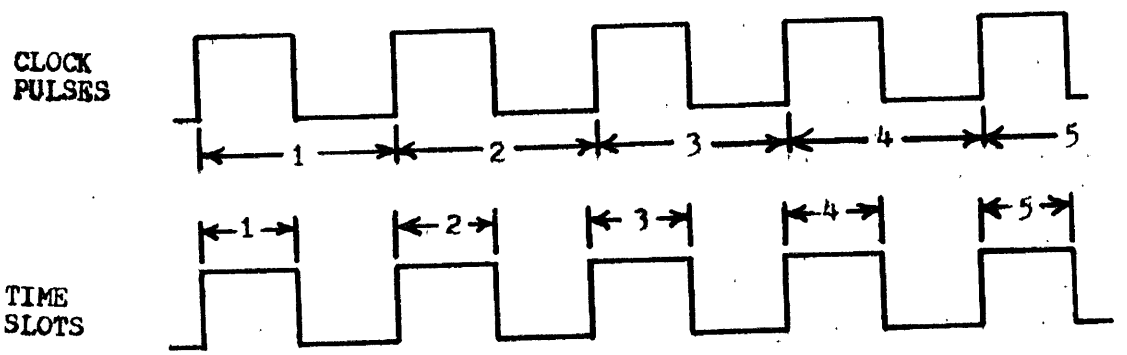


Figure 1. Clock Pulses and Time Slots.

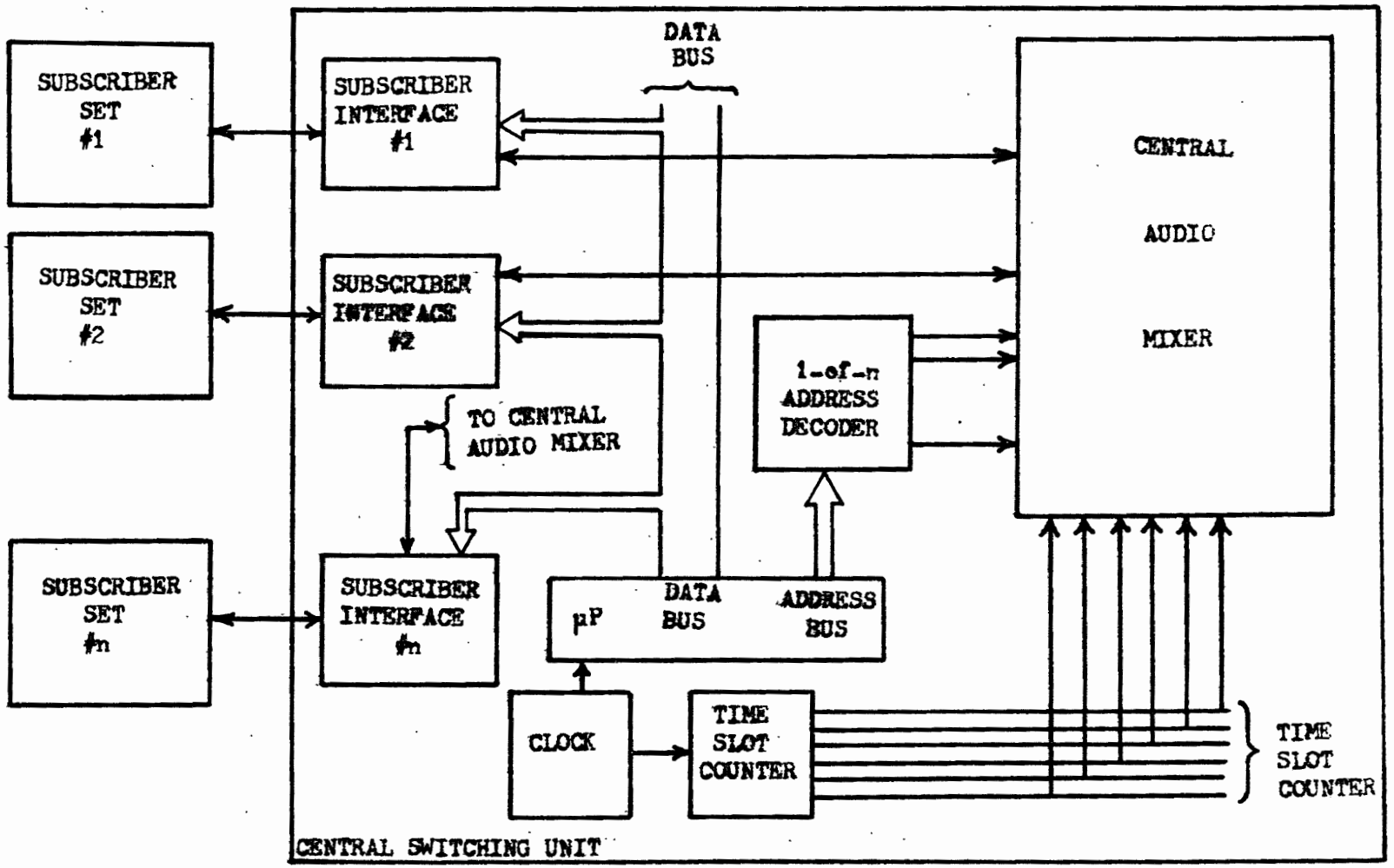


Figure 2. System Configuration

The clock pulses are counted by a 6-bit binary counter. This permits $2^6=64$ time slots. The time slots serve as trunks. Time slot 00 is not used, since it is assigned to those subscribers who are idle, therefore only 63 trunks are available. Subscribers can be programmed by the controller to the same trunk in order to conduct a conversation. That is, 63 simultaneous conversations can be in progress. This implies that 126 subscribers can be served without "blocking", that is, without any subscriber ever being inaccessible because of call congestion.

However, telephone traffic is random in nature. The number of calls initiated vary from day to day, hour to hour, and minute to minute, as well as from subscriber to subscriber. Fig. 3 shows a typical 24-hour distribution of calls in a 2000-line telephone exchange.

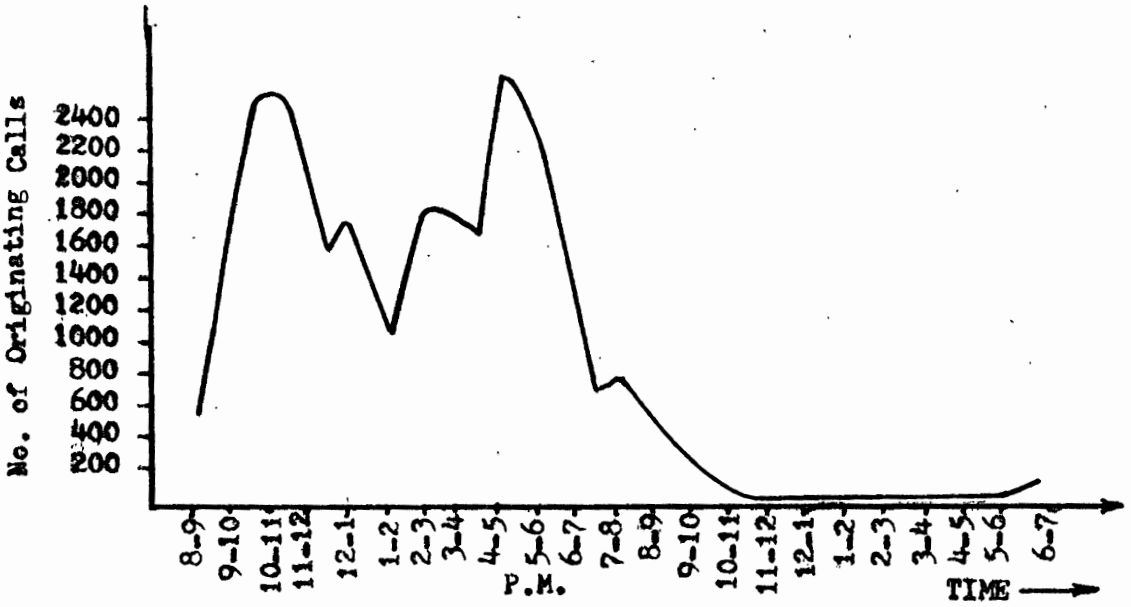


Figure 3. Typical 24-hour distribution of calls in a 2000-line telephone exchange.[1]

[1]Ramses R. Mina, Teletraffic Engineering (Chicago: Telephony Publishing Corp., 1974), P. 3.

In addition, the duration of calls is random, but it has been determined by actual measurements that short duration calls, 1-3 minutes, are more probable than calls of longer duration. The duration of calls display the probability distribution shown in fig. 4, with the average duration being 1.6 minutes.

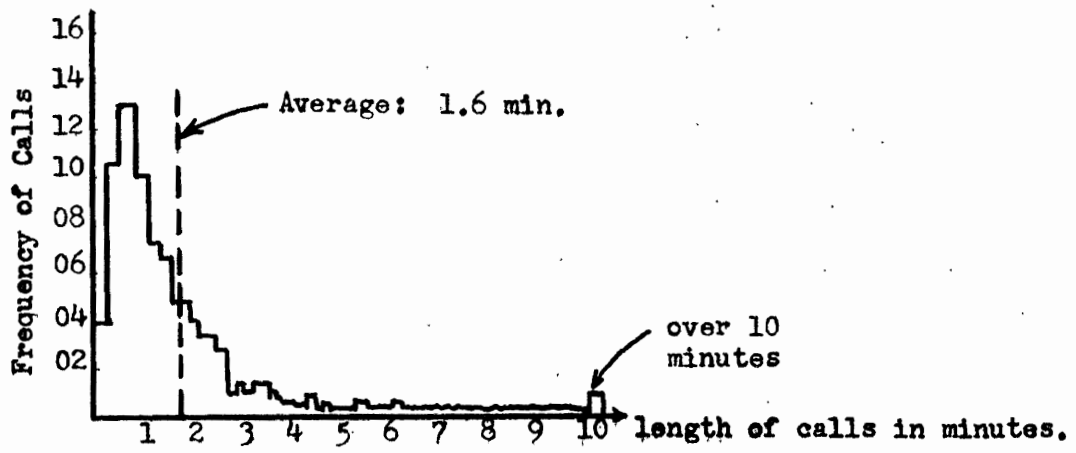


Figure 4. Probability distribution of call duration.[2]

Since each subscriber's line is used only during a small fraction of the time, the number of subscribers that can be accommodated is much larger than twice the number of trunks available. The term "grade of service" is used as an indication of the percentage of calls that are statistically prevented from completion, during the busy hour, due to the inadequacy of the equipment. Consequently, the actual number of subscribers that can be serviced depends on the permissible grade of service.

Each subscriber's line is terminated in the Subscriber's Interface. The Subscriber's Interface contains circuitry which determines the

[2]Ramses R. Mina, Teletraffic Engineering (Chicago: Telephony Publishing Corp., 1974), P. 4.

On/Off Hook status of the subscriber. This information is transferred to the "Status Register", Fig. 5, which is connected to the I/O data bus of the microprocessor. Through the Status Register, information is exchanged between the subscribers and the Central Controller.

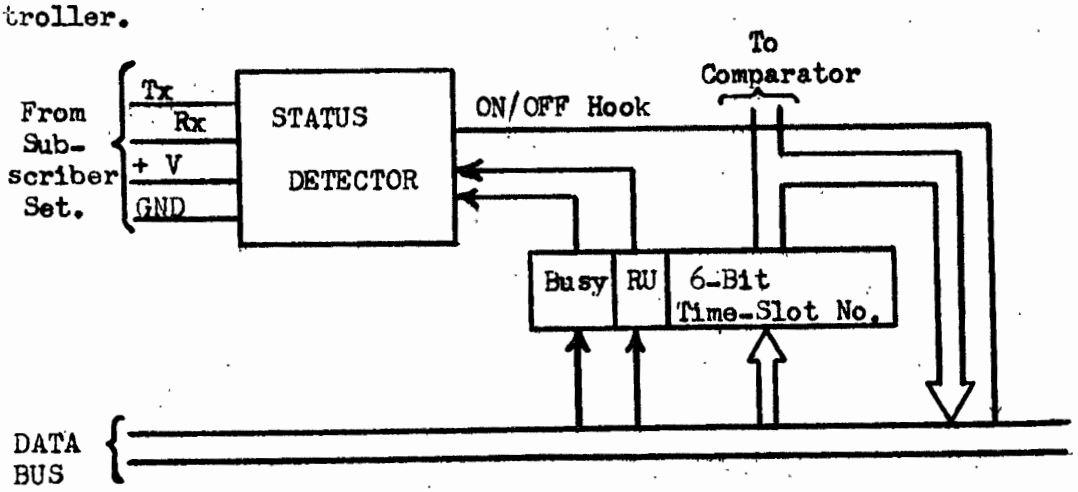


Figure 5. Subscriber Interface.

When a change in the status of a subscriber is detected, the Controller will proceed to service the subscriber according to the program which is stored in the ROM and directs the actions of the Controller. If the subscriber hangs up (On Hook) after conducting a conversation, the Controller will determine the trunk previously assigned to the subscriber and the subscriber will be dropped from the time slot. If no other subscriber is assigned the same time slot, the time slot will become available for a subsequent call by some other subscriber.

If a subscriber wishes to make a call (goes Off-Hook after being idle), the Controller will determine the next available time slot, assign it to the calling subscriber, determine the called subscriber and assign to him the same time slot. The Pulse Amplitude Modulation

technique with Time Division Multiplexing allows the simplest mixing of the audio signals, by taking advantage of the characteristics of the Summing Amplifier, Fig. 6. Thus, more than two subscribers can be assigned to the same time slot in order to conduct a "conference call".

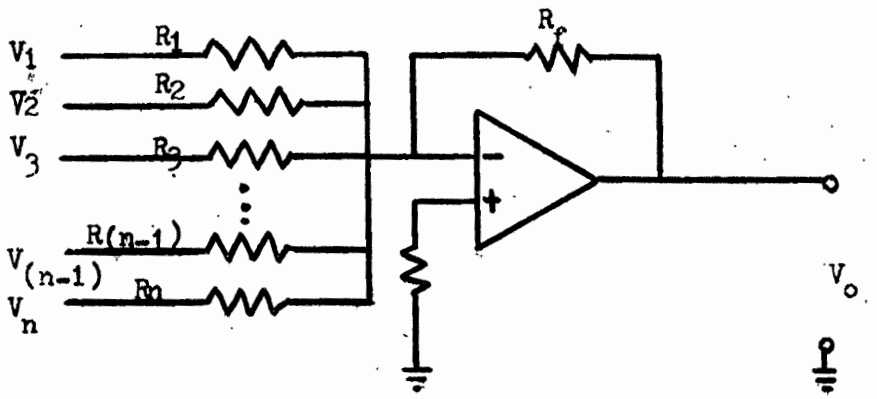


Figure 6. Summing Amplifier.

The transfer function of the Summing Amplifier is,

$$V_o = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n}\right)$$

That is, the output equals the weighted algebraic sum of all the input signals. If $R_1=R_2=R_3=\ldots=R_n$, the output will be

$$V_o = -\frac{R_f}{R_i}(V_1+V_2+V_3+\ldots V_n) \text{ where } R_i=R_1=R_2=R_3=\ldots=R_n.$$

If $R_f=R_i$, the output will be the inverted algebraic sum of the input voltages. If V_1, V_2, $\ldots V_n$ are the waveforms representing the audio input of the subscribers, the output will be the sum of these inputs. If more than one subscriber is speaking at any one time the output waveform will be as unintelligible as the audio is when two people are speaking simultaneously. If the amplifier is overdriven

and goes into saturation, the output will be distorted and totally unintelligible.

The Summing Amplifier is the heart of the Mixer. The Audio Transmit signal of each subscriber is applied through an analog gate to the input of the summing amplifier, ig. 7. The output of the summing amplifier is connected to the Audio Receive line of all the subscribers, also through an analog gate. During any particular time slot only those subscribers assigned by the Controller to that time slot will be gated on. Both input and output gates are on simultaneously.

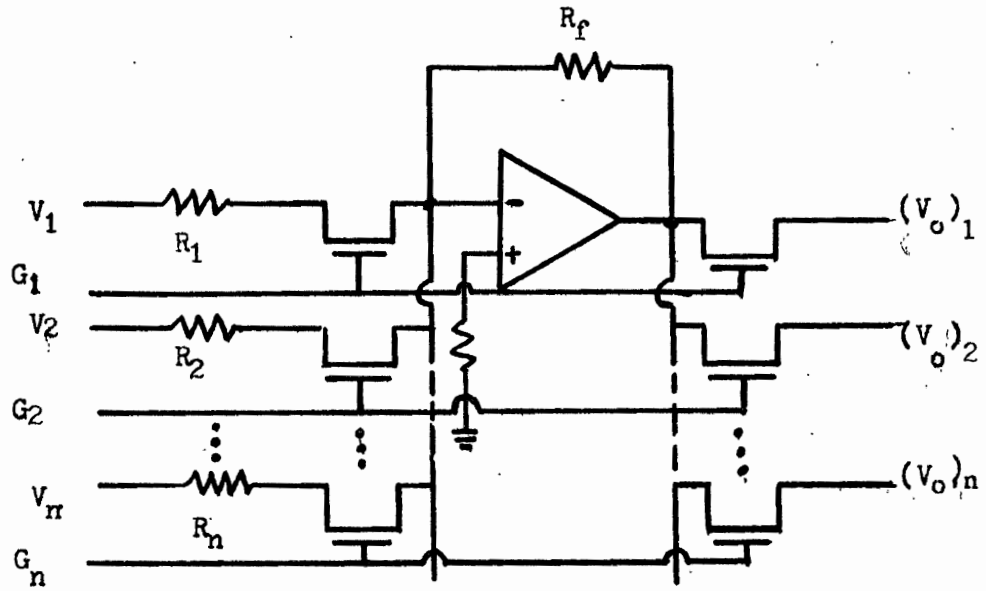


Figure 7. Audio Mixer.

In this manner they can listen to the other participants in the call. In addition, their own Transmit Audio signal is applied to their Receive Audio line, as Sidetone, which serves as audio feedback to the subscriber and prevents him from shouting into the microphone.

The gating of the inputs and outputs at the appropriate time slot

is achieved by a 6-bit comparator. The number, 1-63, of the time slot assigned to a subscriber who is a participant in a call, is applied to the comparator. The other set of inputs to the comparator is the output of the time slot counter. Time slot 00 is assigned to those subscribers who are idle. Consequently the time slot counter counts from 1 through 64 and then goes back to 1 without ever going through zero. When the output of the time slot counter coincides with the number of the time slot assigned to the subscriber the output of the comparator goes positive and is used to gate on the Transmit and Receive lines of the subscriber to the Summing Amplifier. Figure 8 shows the comparator.

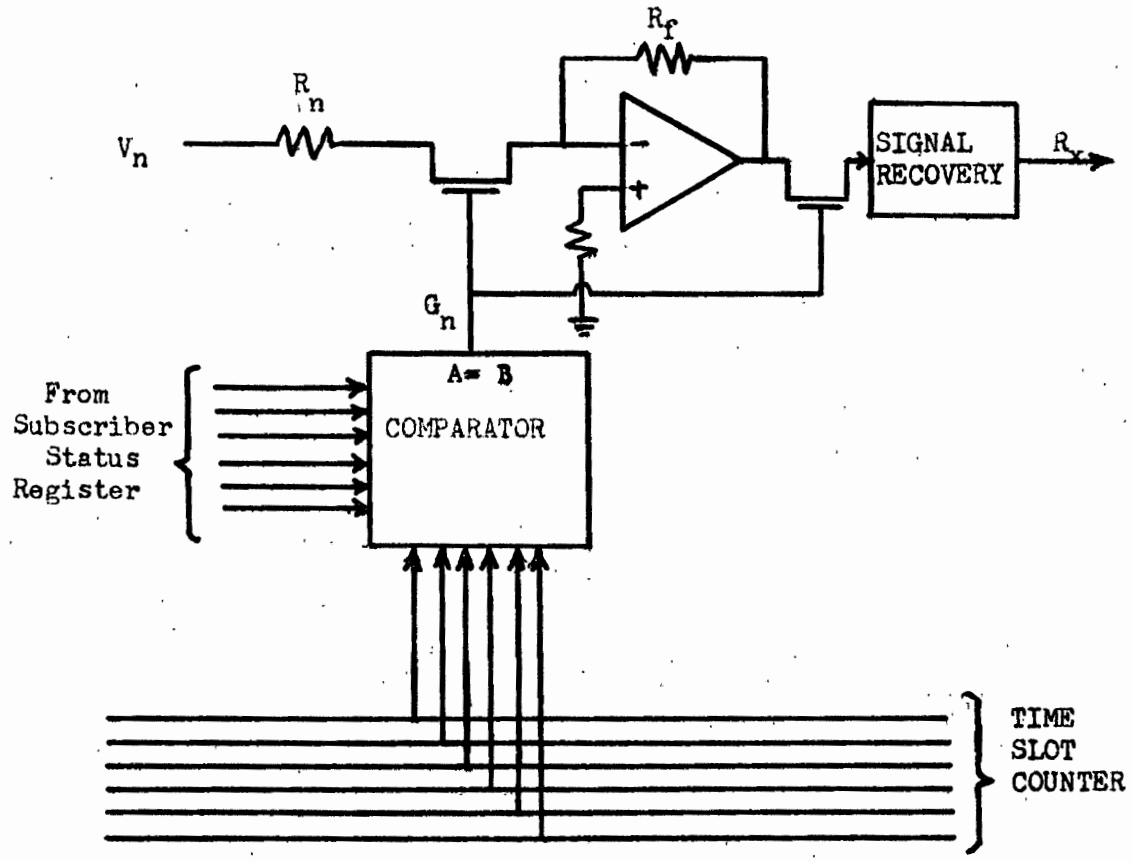


Figure 8. Gating of the audio signal to the Mixer.

System Component Description

Controller - Microprocessor. The microprocessor, used in this design to provide the system control, is the MOS Technology MCS6502 microprocessor. The pin-out for this device is shown in fig. 9.

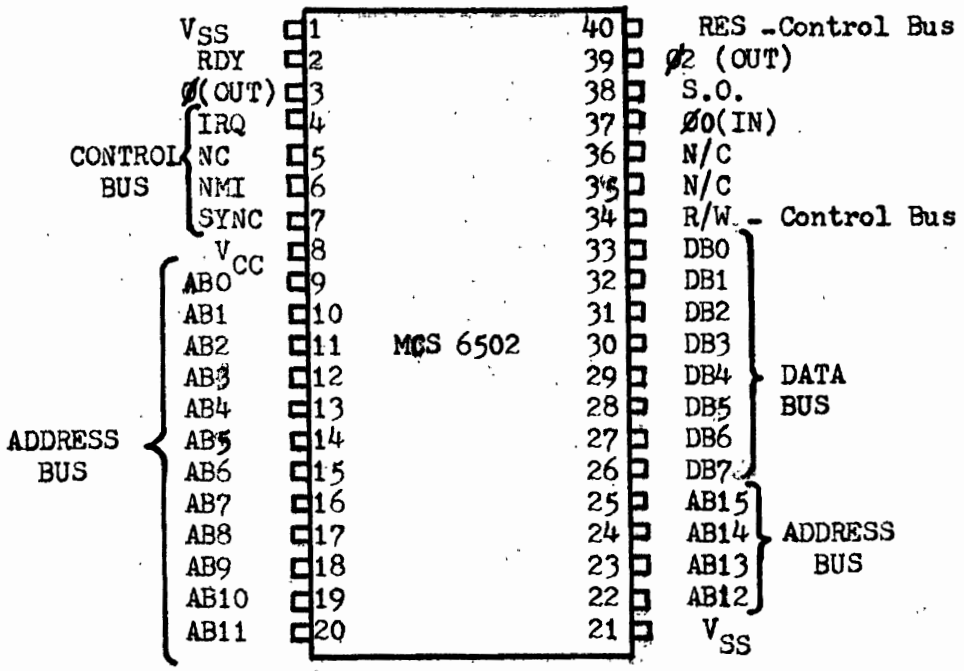


Figure 9. MCS6502 Microprocessor Pin-Out.[3]

This microprocessor was chosen because of its low cost and its organization. The MCS6502 is similar to the Motorola 6800 microprocessor, in that it handles all external Input/Output registers as part of its "memory space" which can be addressed by its Address Bus just like any RAM location, with the capability to write-in as well as read out data through its data bus, Fig. 10. The ROM which contains the program is

[3]Author unknown, MCS 6500 Microcomputer Hardware Manual (Norristown: MOS Technology, Inc., 1975), P. 42.

also part of the memory space.

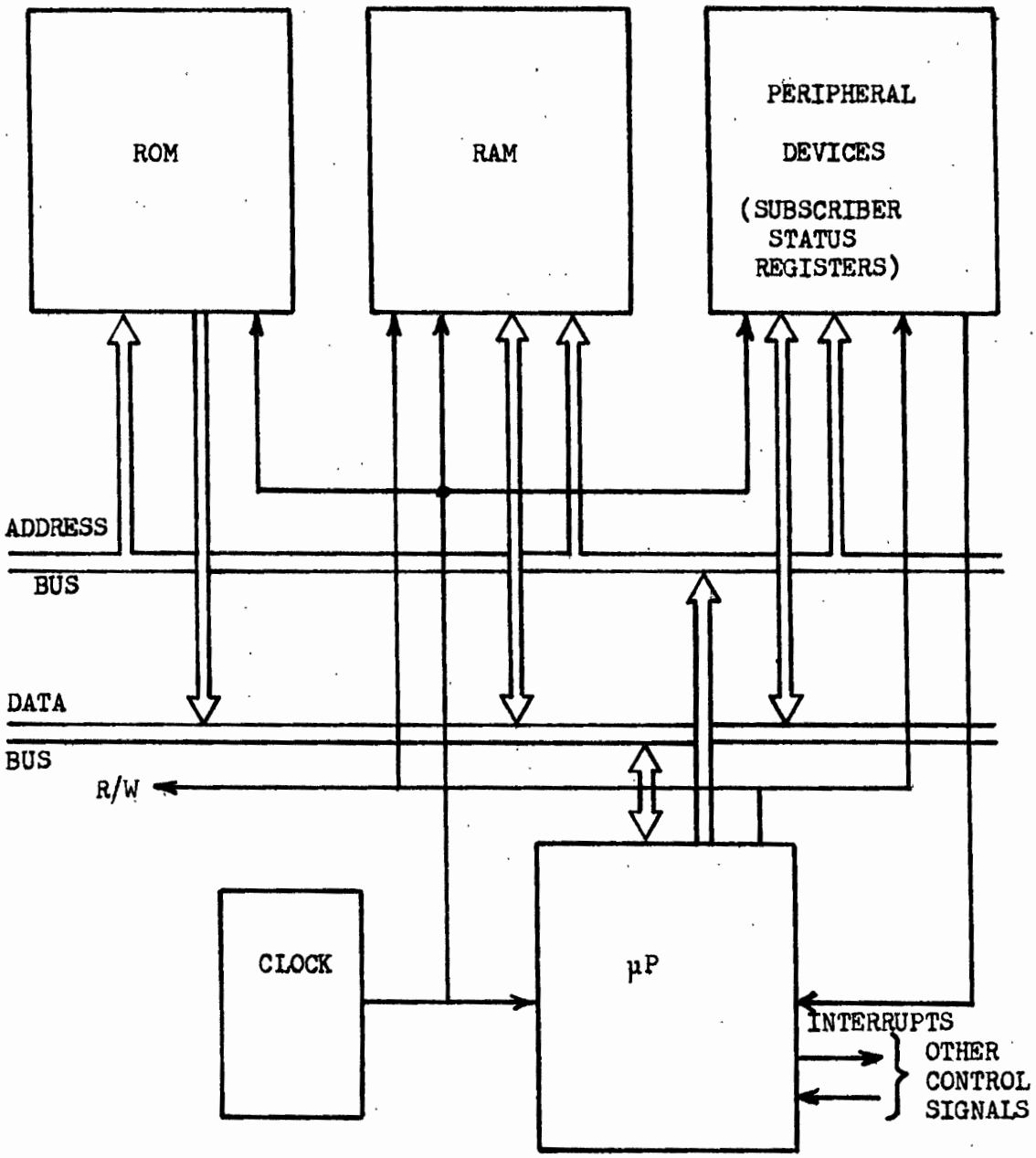


Figure 10. Organization of the MCS 6502 Microprocessor System.[4]

[4]Author unknown, MCS 6500 Microcomputer Hardware Manual (Norristown: MOS Technology, Inc., 1975), P. 5.

The MCS6502 has an 8-bit data bus and a 16-bit memory bus, which means that it can address a total of 65,536 memory words, each 8 bits wide. It has an 8-bit wide Accumulator, two Index Registers, X and Y, each also 8 bits wide, a program counter which is 16 bits wide, and a Processor Status Register. The Processor Status Register is 8 bits wide and each bit serves as a flag which is set or reset according to the contents of certain registers or bits. The 8 bits of the Processor Status Register are assigned as shown in fig. 11.

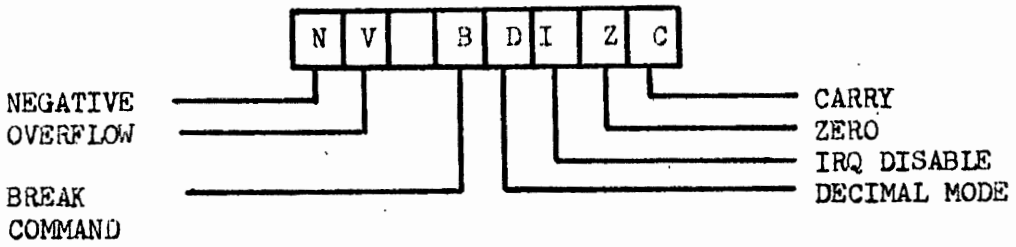


Figure 11. Processor Status Register.

The three bits of the Processor Status Register used in this design are bit #2, the Z-flag; bit #6, the V-flag; and bit #7, the N-flag. Bit #2, the Z-flag, is automatically set equal to 1 by the microprocessor after an operation involving data movement, if the contents of the Accumulator are equal to zero. Conversely, if the contents of the Accumulator are other than zero, flag Z is set equal to zero.

Bit #7, the N-flag, is automatically set equal to 1 by the microprocessor after an arithmetic operation, if the contents of the Accumulator are negative. Conversely, if the contents of the Accumulator are not negative the N-flag is set equal to zero. Since a negative number in the Accumulator is signified by setting the seventh bit of the Accumulator equal to 1, and conversely a positive number in the Accumulator is signified by setting the seventh bit of the Accumulator

equal to zero, flag-N is set equal to the seventh bit of the Accumulator, following any movement of data into the Accumulator.

Bit #6, the V-flag is set equal to 1, when an overflow has occurred following an addition or subtraction of two numbers. However, additionally, the MCS6502 Microprocessor has a unique feature that increases the flexibility of the device considerably. Following the instruction BIT, Test Bits in Memory with Accumulator, Flag V is set equal to the content of bit #6 in the Accumulator.

This capability to test bits #6 and #7 directly and then branch to subroutines according to the state of these bits makes the MCS6502 a very efficient microprocessor for this application. The reason is that the contents of bits #6 and #7 of the Subscriber's Status Register can be assigned to signify one of a number of states, eg. On/Off Hook, Being Rung-Up, etc., that the subscriber may be in. Since for the MCS6502 the external input/output registers are in the "memory space" of the microprocessor and therefore addressable like any other location in memory, the status of a subscriber can be ascertained with a minimum number of steps. Since for the vast majority of the time the subscribers will be idle, requiring no service, the microprocessor can proceed with the polling of the subscribers and with four instructions, as the flow chart shows, it can determine that a subscriber is idle. It can then go on to the next subscriber, until it comes up to one requiring service.

In addition to the Data and Address Buses, the MCS6502 has the Control Bus. The Control Bus as shown in fig. 9, is composed of the lines that control the flow of information between the microprocessor, the memory, and the peripheral devices. In this application, only the R/W, Read/Write, line will be used. This line controls the direction

of information transfer on the bidirectional Data Bus. This line is high when the microprocessor is reading data from memory and goes low when the microprocessor is writing data into memory.

The $\overline{\text{NMI}}$ (Non-Maskable Interrupt) and the $\overline{\text{IRQ}}$ (Interrupt Request) could prove very useful in controlling a system such as a telephone switchboard, where the requests for service are relatively infrequent occurrances. The use of the Interrupt capability could free the microprocessor to perform other tasks, unrelated to the servicing of telephone calls, such as arithmetic operations, control of other systems, etc. Through a hierarchy of Interrupts the microprocessor could return to service the telephone exchange whenever requested by a subscriber. This would be a very efficient use of the microprocessor capabilities. However, since in this application there are no requirements other than the control of the telephone exchange, the simpler approach is used. That is, the subscribers are sequentially polled to determine the status of each one, and when service is requested by a subscriber the microprocessor services the subscriber according to the program.

Interfaces and Information Exchange

Subscriber Interface. Fig. 5, on page 8, shows the Subscriber Interface. The Subscriber Interface terminates the subscriber's line in the Central Switching Unit and also contains the circuitry that determines the status of the subscriber. Additional circuit detail is shown on Fig. 12 below.

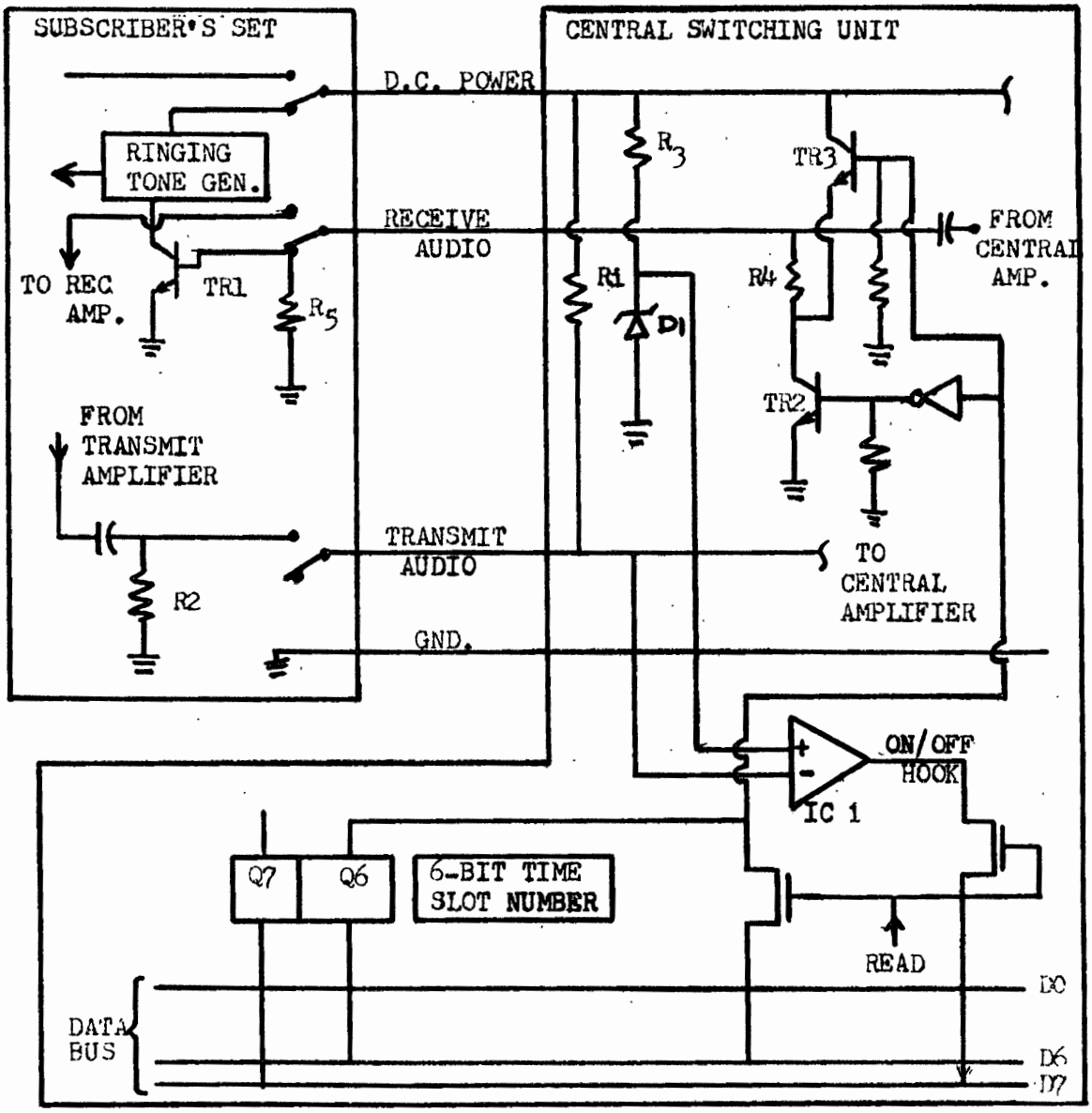


Figure 12. Subscriber Interface.

Zener diode D1, through resistor R3, provides a reference voltage to the noninverting input of comparator IC1. When the subscriber is On Hook, the voltage of the DC power bus is applied to the inverting input of the voltage comparator, through resistor R1. When the subscriber goes Off Hook, resistor R1 in the Central Switching Unit and resistor R2 in the Subscriber's Set form a voltage divider, so that a voltage lower than the power bus voltage is applied to the inverting input of the voltage comparator. If the zener voltage of diode D1 is chosen so that $V_{D1} > V_{DC}\ (R2/(R1+R2))$, when the subscriber is On Hook the output of the comparator IC1 will be a 0, and when the subscriber is Off Hook the output of the comparator will be a 1. The output of the comparator can be stored in the Subscriber Status Register. Since the Subscriber Status Register is on the microprocessor's Data Bus, it can be addressed by the microprocessor and data can be transferred in and out of it. If bit #7 of the Subscriber Status Register is assigned to provide the microprocessor information about the On/Off Hook status of the subscriber, information would be flowing only in one direction, from the Subscriber Interface to the microprocessor. Consequently bit #7 of the Data Bus would not be used to its full capacity. Conversely, when the called subscriber is Busy, a "Busy" Tone is to be added to the calling subscriber's Audio Receive line. An analog gate must be activated to gate the "Busy" Tone onto the subscriber's Receive line. When the calling subscriber goes On Hook in response to a Busy Tone, the microprocessor would reset to 0 the bit that would control the analog gate that, in turn, would control the "Busy" Tone. In this case, control information to the analog gate would flow only in one direction, from the microprocessor to the Subscriber Interface. Consequently, bit #7

of the Data Bus can be used to implement two functions. It can transfer subscriber status information from the Subscriber Interface to the microprocessor and "Busy" Tone control information from the microprocessor to the Subscriber Interface. Fig. 13 shows details of the circuit.

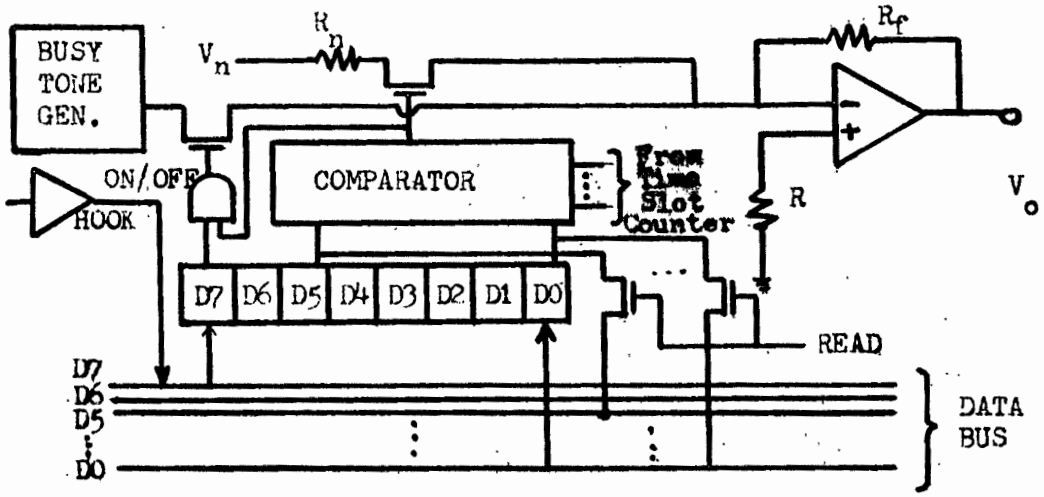


Figure 13. "Busy" Tone Control.

When the Central Controller wants to ring up a subscriber, a 1 is stored in bit location #6 of the Subscriber Status Register. The ringing-up is effected as follows. A Ringing Tone Generator is found in the subscriber's set. When the subscriber is On Hook, the power bus is connected to the Tone Generator, and ground is applied through transistor TR1. When bit #6 in the Subscriber Status Register is a 1, that is, when the subscriber is being rung-up, transistor TR2 is cut off and TR3 is saturated, thus applying a voltage V_{DC} $(R5/(R_4+R_5))$ to the base of transistor TR1, in turn causing it to saturate. This provides a ground to the Ringing Tone Generator which is then activated. When bit #6 in the Subscriber Status Register is a zero, 0, transistor TR3 is cut off and transistor TR2 is saturated. Thus, ground through R_4 is applied to the base of transistor TR1 driving it to cut off, and disabling

the Ringing Tone Generator. When the subscriber who is being rung up lifts his receiver off the hook to answer the call, power is disconnected from the Ringing Tone Generator and is applied to the Transmit and Receive Amplifiers in the Subscriber's Set. Also, the comparator in the Subscriber's Interface changes state and becomes a 1, since the subscriber is now Off Hook.

During the next polling of the subscriber, the microprocessor will detect the state of the subscriber as being Off Hook in response to a ringing signal and will change the contents of bit #6 of the Subscirber's Status Register to a 0.

Since the audio is A-C coupled to the Transmit and Receive lines the D-C signaling voltages do not affect the audio transmission. This is an extreme case of frequency multiplexing.

The Subscriber Status Register is 8 bits wide. The first six bits, D0-D5, are used to store the number of the time slot, 1-63, assigned to the subscriber during a call. If the subscriber is not a participant in a call, but is idle, the number 000000 will be stored in the first six bits of the register.

As shown in fig. 13, the output of the Subscriber Status Register is connected to the Data Bus of the microprocessor through analog gates. These gates are gated On to the Bus when the Address Decoder selects the subscriber and the Read/Write control line goes high. Fig. 14, shows the details of the circuit interconnection and an analysis of the control signals.

The 1-of-n Address Decoder is composed of National Semiconductor MM74C154 decoder/demultiplexer integrated circuits. When a binary input is applied to the decoder, the corresponding output goes low, while

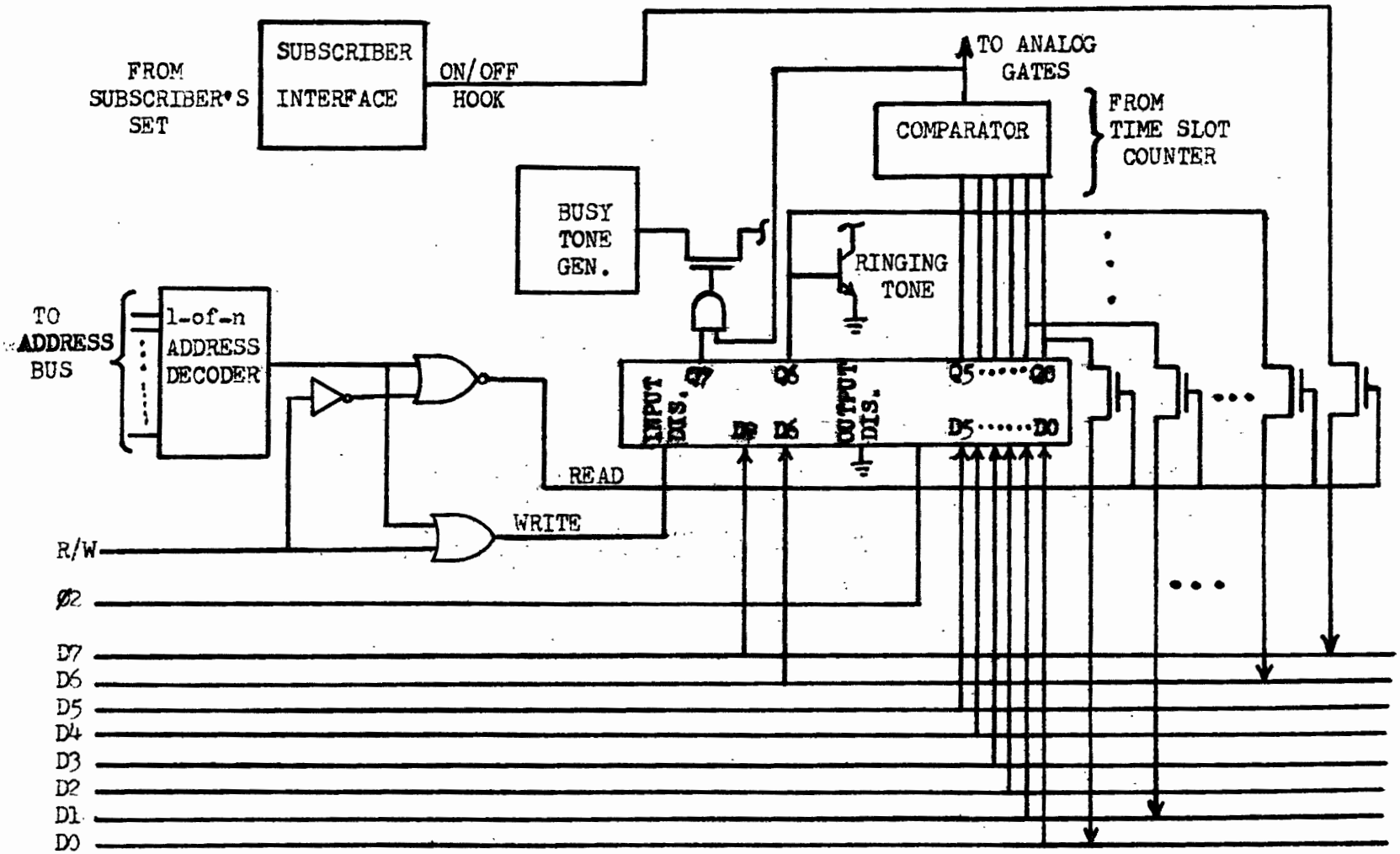
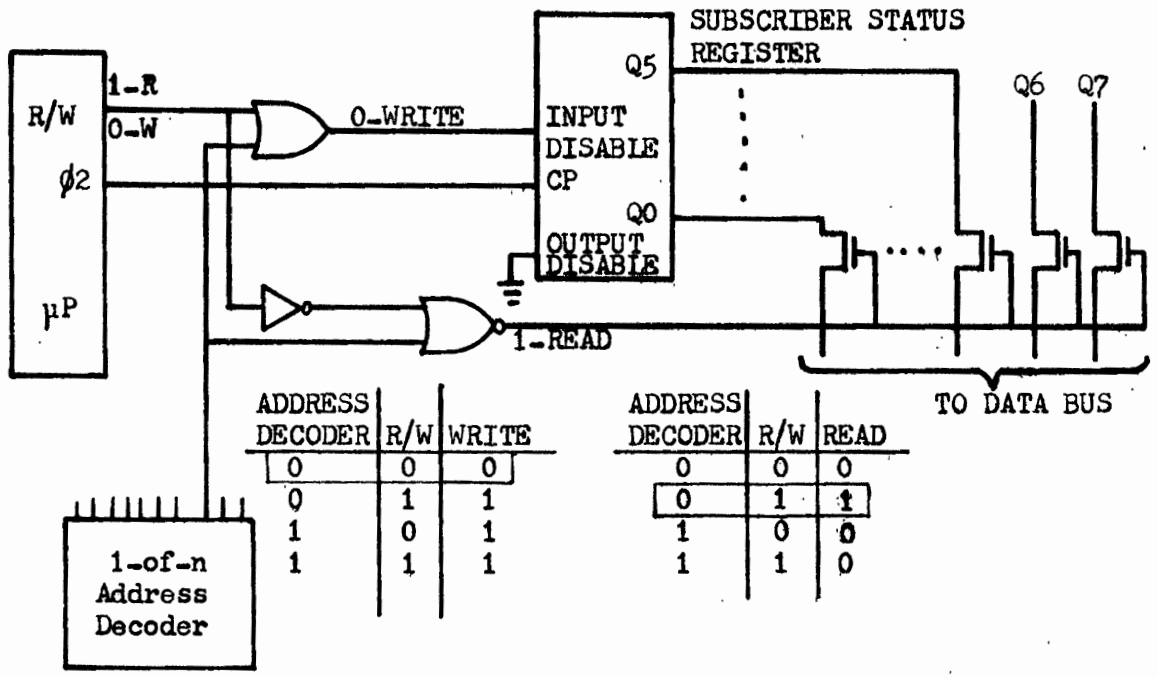


Figure 14. Subscriber's Status Register.

every other output remains in the 1-state. The Subscriber Status Register is composed of two National Semiconductor MM74C173 Tri-State quad-D flip-flops. These flip-flops, in addition to the Clock input, have an Input Disable and an Output Disable. The Output Disable input must be in the 0-stats, since the output of the register is continuously applied to the comparator in the Mixer. See Fig. 14. The appropriate output of 1-of-n Address Decoder must be logically combined with the R/W signal of the microprocessor, Fig. 15, to generate a 0 for the Input Disable input of the Subscriber Status Register, when it is desired to transfer data into the register, and to generate a 1 when it is desired by the microprocessor to read the contents of the Subscriber Status Register.



ADDRESS DECODER	R/W	WRITE
0	0	0
0	1	1
1	0	1
1	1	1

ADDRESS DECODER	R/W	READ
0	0	0
0	1	1
1	0	0
1	1	0

Figure 15. R/W Control Signals.

Tone Decoder. A Multifrequency Tone Generator in the Subscriber's Set generates the combinations of tones required to effect the dialing of the desired digits. In the Central Switching Unit, Tone Decoders

must be provided to decode the tones and translate them to binary digits. Since each subscriber uses his line during only a small fraction of the time, the system must be designed so that the subscribers share as much of the hardware as possible. The Tone Decoder is used only during the initial stages of a call, only during dialing. Consequently, a small number of Tone Decoders, assigned to the subscribers upon request, can adequately serve the system.

In this design approach, there are four Multifrequency Tone Decoders in the system. They have their own 8-bit Status Register. The first six bits, D0-D5 are used to store the number of the time slot assigned to the Tone Decoder. This number will be the same as that assigned to the subscriber who is initiating the call. When the microprocessor detects that a subscriber is initiating a call, having gone Off Hook, it will go through the process of determining whether a Tone Decoder and a time slot is available.

After the microprocessor determines that a Tone Decoder and a time slot are available, it proceeds to store the same time slot number in both the Tone Decoder and Subscriber Status Registers. Since both the calling subscriber and the tone decoder are on the same trunk, the multifrequency tones transmitted by the calling subscriber will be received and decoded by the decoder. When the decoding is completed the number dialed will be stored in binary form in a buffer register at the output of the Tone Decoder. This register is on the microprocessor's data bus and therefore addressable by the microprocessor. The contents of this register, the number of the called subscriber, will subsequently, upon interrogation as directed by the program, be transferred to the microprocessor for processing. Fig. 16, shows the details of circuit

interconnection for the Tone Decoder. The Decoder is gated on to the Audio Receive Bus like any subscriber when coincidence occurs between the time slot number stored in the status register and the number at the output of the time slot counter. In order to activate the tone decoding part of the circuit, the following events must take place. At the time that the Tone Decoder's time slot number is stored in the first six bits of the Status Register, D0-D5, a 1 is applied on line D6 of the Data Bus. The 1 on line D6, inverted, is applied to the Preset input of flip-flop FF1 and the Clear input of flip-flop FF2. Before the sequence of events that take place during the tone decoding can be described in detail,

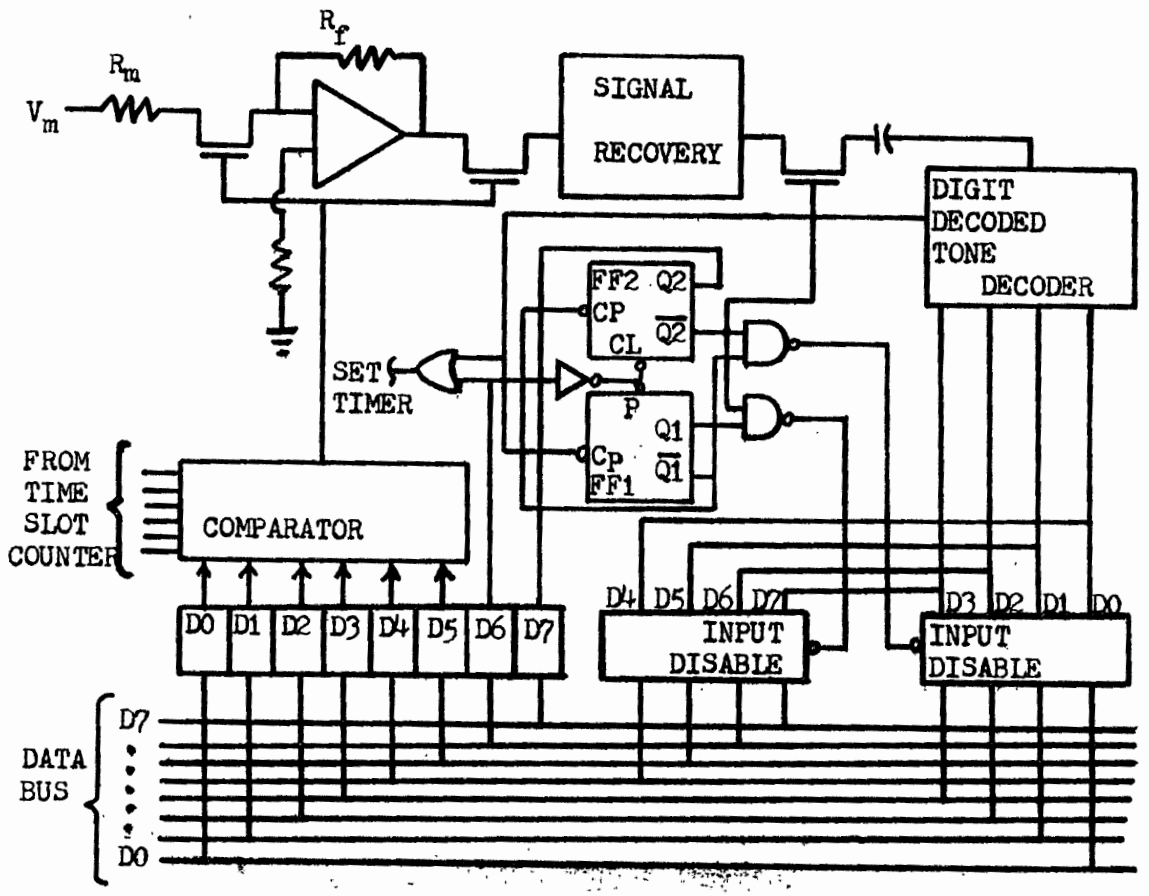


Figure 16. Tone Decoder control.

a description of the component elements of the circuit must be given. The analog gate at the input of the Tone Decoder is used to gate the multifrequency tones to the Decoder. When the appropriate number of digits has been dialed, this gate is turned off. The tone decoder puts out a four bit binary number in response to a multifrequency tone, which is in turn generated at the Subscriber's Set in response to a hexadecimal input.

In this design, the system can handle a maximum of 256 subscribers. For the sake of simplicity of design, no effort is made to design the system so that the dialing can be done in the decimal system. Instead the dialing is done in the hexadecimal system.

Since the Data Bus is 8 bits wide and the Tone Decoder is designed to produce a four bit binary output in response to a hexadecimal input, the output of the decoder is gated so as to steer the bits in such a manner that when both digits of the called subscriber's number have been dialed, the bits are stored in the correct order in a three-state buffer register which is on the microprocessor Data Bus. The buffer register is made up of two National Semiconductor MM74C173 "three-state" registers. These registers have an Input Disable input. When this input goes low, data can be transferred into the register. Since the buffer register is made of two four-bit registers, each with its own Input Disable input, the two four-bit segments of the register can be gated sequentially to receive the two four-bit bytes in the correct order, so that when dialing has been completed, the bits D0-D7 can be applied to the Data Bus in the correct order, as shown in fig. 16.

The steering of the Tone Decoder output, the control of the analog gate at the input of the Tone Decoder, and the control of the Dial Tone,

are effected by the two flip-flops, FF1 and FF2, fig. 17. These are National Semiconductor MM74C76, J-K flip-flops. The J and K inputs are connected to the positive supply which means that they are in their toggling mode. At the negative going edge of a pulse applied to their clock input they change state.

The Tone Decoder's Status Register is 8 bits wide. The bits are assigned as follows: D0-D5 contain the time slot number assigned the Tone Decoder during a call. D6 is used in a manner similar to bit D7 of the Subscriber Status Register. When the microprocessor writes a 1 into bit D6, this bit is used to start the Dial Decoding process for a particular call. On the other hand, when bit D6 is read by the microprocessor, it contains information regarding the Dial Timer. When the Dial Decoding process is initiated a timer is activated which allows a certain amount of time, as much as 20 seconds, for the subscriber to dial the first digit. After the first digit has been dialed, the timer is reactivated allowing the same time for the dialing of the second digit. The output of the timer is read as bit D6 by the microprocessor. If the timer lapses and the dialing is not completed, the microprocessor will drop the subscriber and continue with the polling of the other subscribers and return to the subscriber that was dropped earlier in the proper sequence. The subscriber will then be treated as a new request for service.

Bit D7, when read by the microprocessor provides information as to whether the dialing has been completed. A 1 on D7 means dialing has been completed, a 0 means that a complete number has not been dialed.

The tone decoding occurs as follows: When a 1 is entered into bit #D6 of the Tone Decoder Status Register, it is inverted and applied

to the Preset input of FF1 and the Clear input of FF2. This sets Q1=1, $\overline{Q1}$=0, $\overline{Q2}$=0, Q2=1. $\overline{Q2}$=1 enables the analog gate at the input of the Tone Decoder. $\overline{Q2}$, Q1 and $\overline{Q1}$ are logically combined, as shown in fig. 17, to steer the output of the decoder. Since the higher order digits are dialed first, Q1 and $\overline{Q2}$ are combined in a logical NAND function to enable the first half of the register that will receive the high order four bit byte first. The Tone Decoder is designed with a "Digit Decoded" output. This linegoes negative when a multifrequency tone has been decoded and the four-bit number is at the output of the decoder.

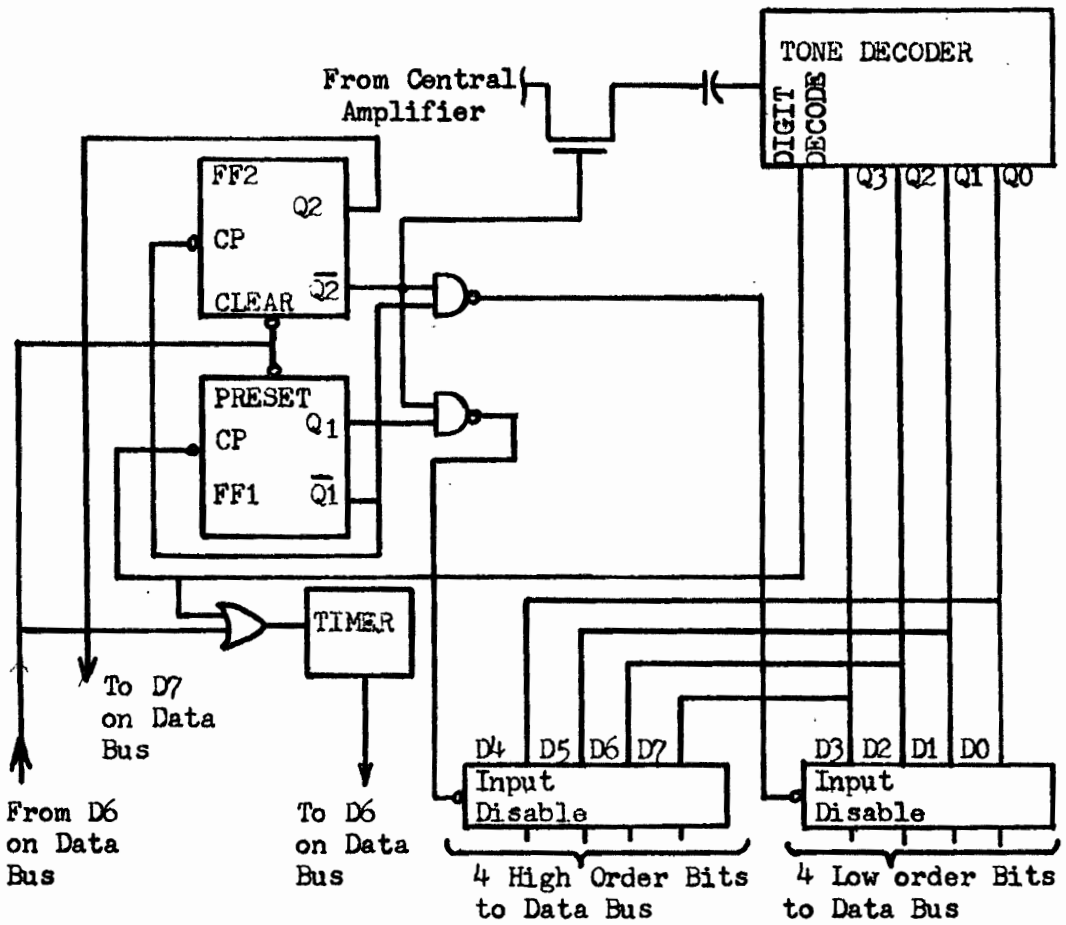


Figure 17. Steering of Tone Decoder Output.

This negative going pulse applied to the Clock input of FF1 causes it to change state. Now Q1=0, $\overline{Q1}$=1 and $\overline{Q2}$=1. $\overline{Q2}$ is combined in a logical NAND function with $\overline{Q1}$ to enable the second half of the buffer register that will receive the low order four bit byte. When the second digit has been decoded, the clock pulse output of the Tone Decoder causes FF1 to return to its original state, where Q1=1, $\overline{Q1}$=0. The Q1 output is connected to the clock pulse input of FF2, so that when Q1 changes state from 1 to 0 the negative-going edge causes FF2 to change state, Q2=1 and $\overline{Q2}$=0. Since $\overline{Q2}$=0, the analog gate at the input of the decoder is disabled so that no more tones can be applied to the decoder. The Q2 output is connected to bit #D7 on the Data Bus, and signifies to the microprocessor that the called subscriber's number is found in the buffer register at the output of the Tone Decoder.

The Dial Tone must be mixed with the calling subscriber's Receive Audio signal, and it must be removed when the first digit has been dialed. Fig. 18 shows the interconnection details of the Dial Tone Control circuit. The output of the comparator associated with the Tone Decoder is combined with the Q1 output of FF1 and the $\overline{Q2}$ output of FF2 to gate the Dial Tone ON during the time slot assigned to the calling subscriber. Each Tone Decoder has a Dial Tone Generator associated with it. When an available Tone Decoder has been identified and assigned the same time slot as the calling subscriber, the Dial Tone is gated on to the Mixing Amplifier by an analog gate controlled by the output of a three-input AND gate, whose inputs are: the output of the Tone Decoder's time slot Comparator, Q1 of FF1 and $\overline{Q2}$ of FF2. When the first digit has been dialed and decoded FF1 changes state and Q1=0. Therefore, the analog gate that controls the Dial Tone is disabled and

the Dial Tone is removed from the calling subscriber's Receive Audio line.

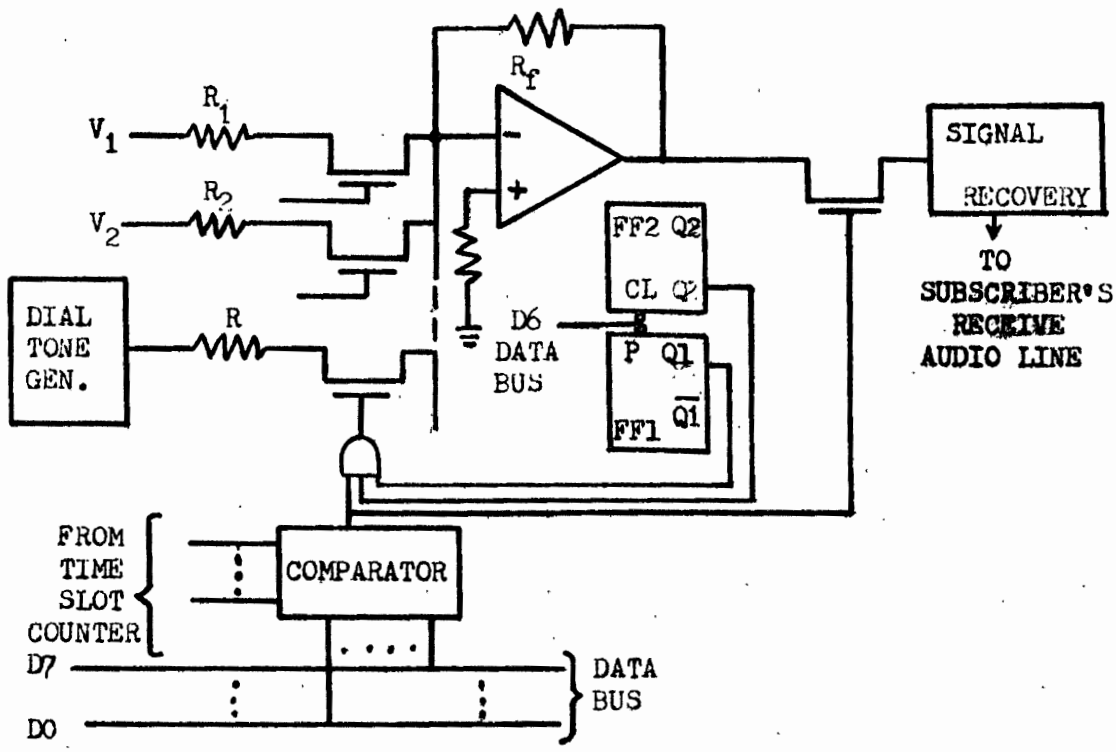


Figure 18. Dial Tone Control.

Memory. The microprocessor is organized as shown in fig. 19. The Read Only Memory, the Random Access Memory and the "peripherals", in this case the Subscriber Status Registers are all on the Memory, Data, and Control Buses.

The concept of "Page" in Memory is very important in 8-bit microprocessor systems. The internal organization of an 8-bit processor is around 8-bit registers, 8-bit parallel data paths, etc. A "Page" of memory contains 256 8-bit words. Each of these words is individually addressable.

The Read Only Memory (ROM) is a nonvolatile storage device. The data stored in ROM is contained in the physical configuration of

the device and is not altered after the manufacturing process. Furthermore, information is not lost during interruptions of power. As a result, ROM provides a desirable storage medium for the program that directs the microprocessor through the steps required to control the system. In this application the total number of program instructions is not more than 150. Consequently, the program and all the constants required in the execution of the program can be stored in less than two pages of ROM.

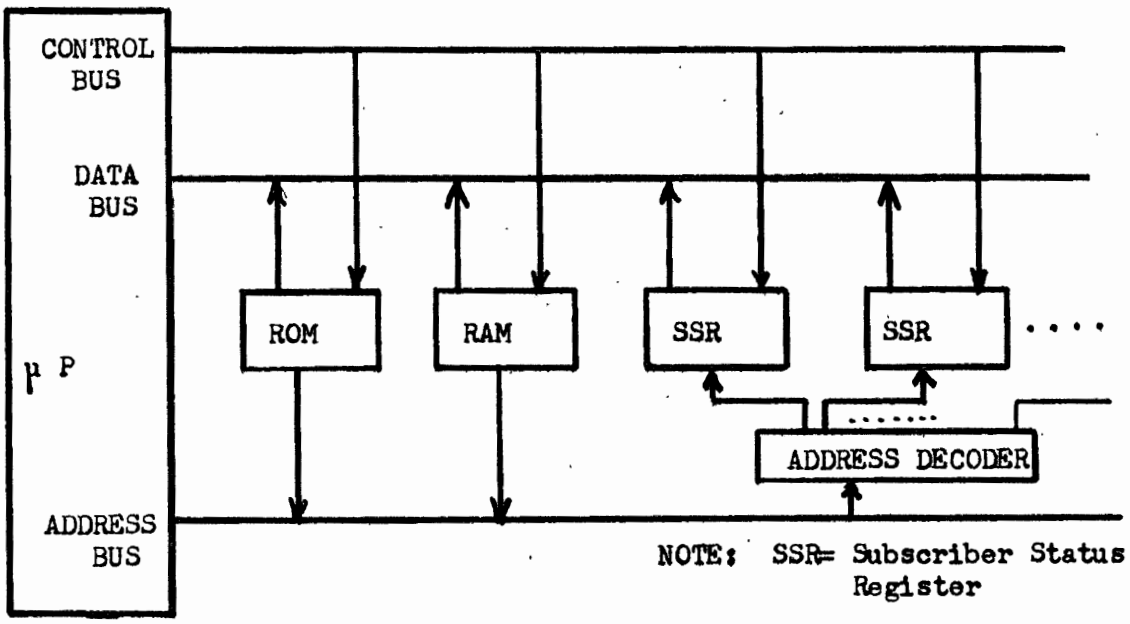


Figure 19. Organization of Microprocessor Memory Space.

The Random Access Memory is used to store information that is obtained during the execution of the program, eg. the numbers of available time slots, Tone Decoders, the results of arithmetic operations, etc. Whereas the microprocessor cannot write into ROM but only read information out of it, data can be transferred both into as well as out of RAM.

The addressing of each ROM or RAM location is effected by placing the 16-bit address of the location on the Address Bus. Reading information out of memory or writing information into it requires, in addition to the address information, the utilization of the R/W (Read/Write) control line. The R/W goes high when reading information out of memory and it goes low when writing information into it. Fig. 21 shows the timing diagram for reading information from Memory. Fig. 20 shows the timing diagram for writing data into Memory. The timing of all data transfers is controlled by the system clock. The clock is a two-phase square wave. It can be thought of as two non-overlapping, positive-going pulse trains. The two phases are referred to as Phase One and Phase Two. Phase One clock pulse, as shown in fig. 20 is the positive pulse during which the address lines change and the Phase Two clock pulse is the positive pulse during which the data is transferred.

The Subscriber's Status Registers, although peripheral devices, for the MCS6502 are in the "Memory space" and therefore addressable like any other memory location.

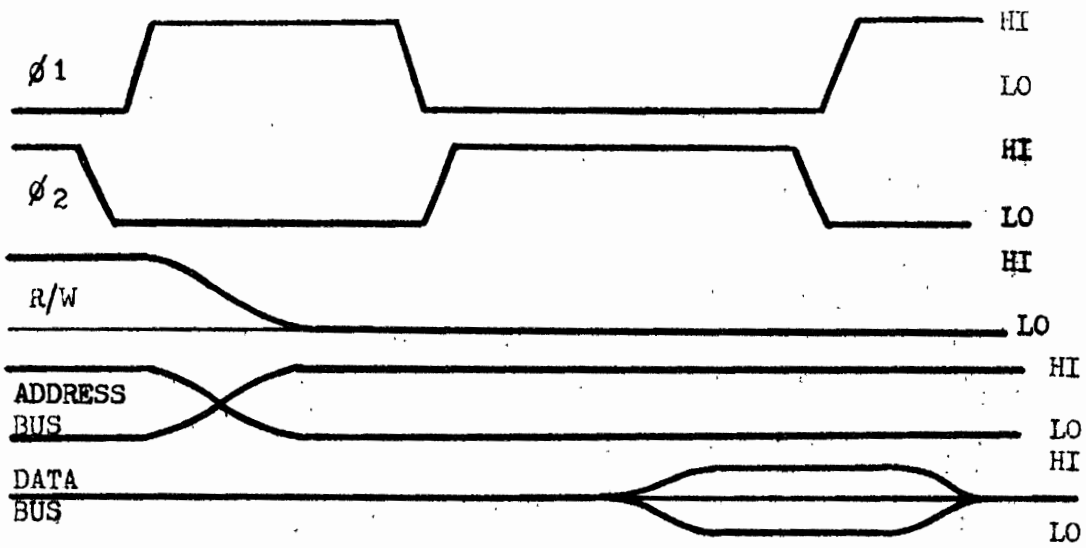


Figure 20. Timing for writing data into Memory.[5]

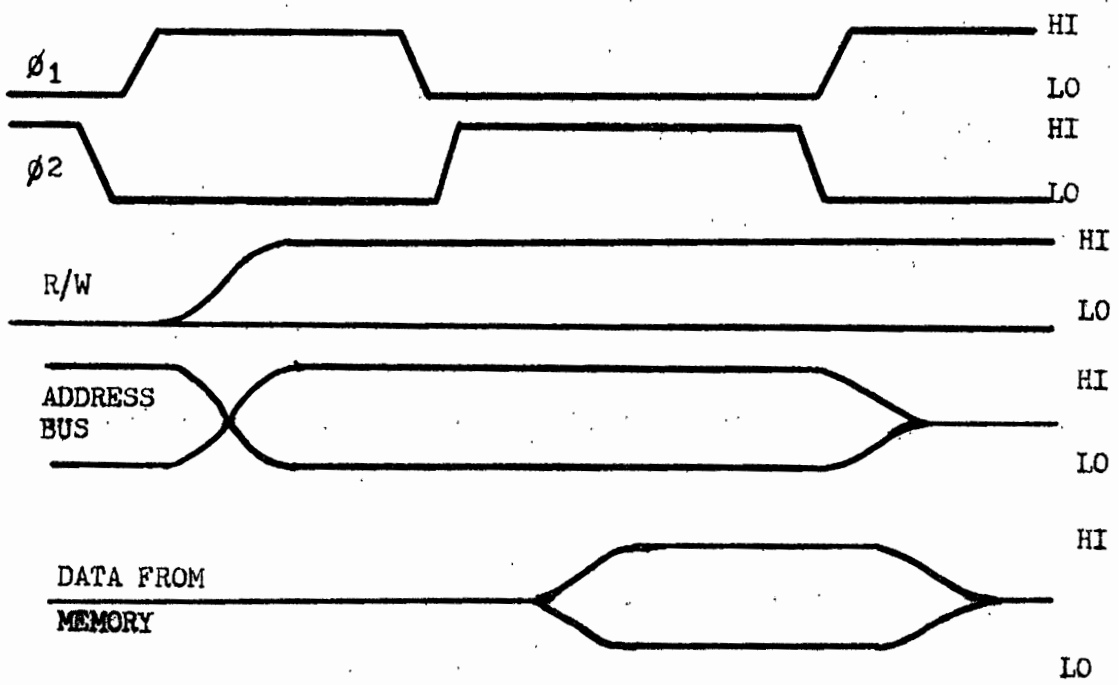


Figure 21. Timing for reading data into Memory.[5]

[5]Author unknown, MCS 6500 Microcomputer Hardware Manual (Norristown: MOS Technology, Inc., 1975), Pp. 18-19.

Central Audio Mixer-Audio Mixing Scheme. As shown in fig. 2, page 5, each Subscriber's Line is terminated in the Subscriber Interface, inside the Central Switching Unit. The Audio signal, superimposed on the DC signalling levels is AC coupled to the Central Audio Mixing Amplifier, shown in fig. 22, below.

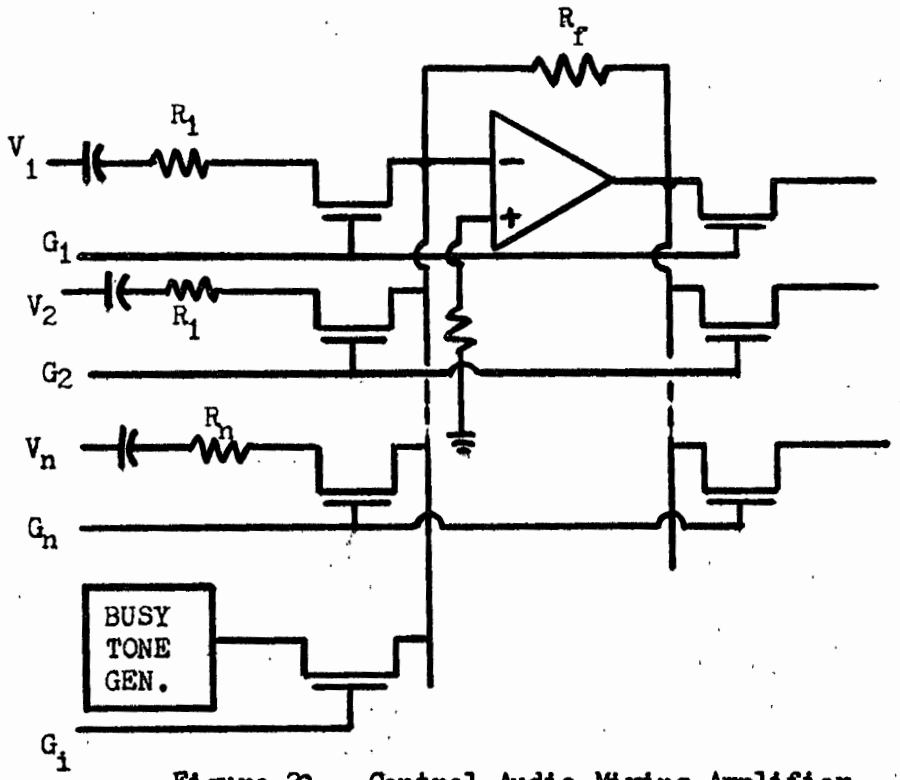


Figure 22. Central Audio Mixing Amplifier.

The Audio signal is time-division multiplexed and demultiplexed by the Central Audio Mixing Amplifier. The input signals are gated onto the amplifier by analog gates. Other analog gates gate the Receive Audio line of the subscribers onto the output of the amplifier during the appropriate time slot. Two or more subscribers programmed to occupy the same time slot can conduct a conversation.

The programming of subscribers on to a time slot is done as follows: Associated with each subscriber is a 6-bit comparator. The comparators

are Motorola MC14585CP magnitude comparators. Each MC14585CP has two sets of four-bit inputs. These two sets of inputs are compared to each other, bit for bit, and according to the outcome of the comparison one of three outputs goes high, A>B, A=B, or A<B. Since in this application the words to be compared against each other are six bits wide, two MC14585CP will be cascaded, as shown in fig. 23 below.

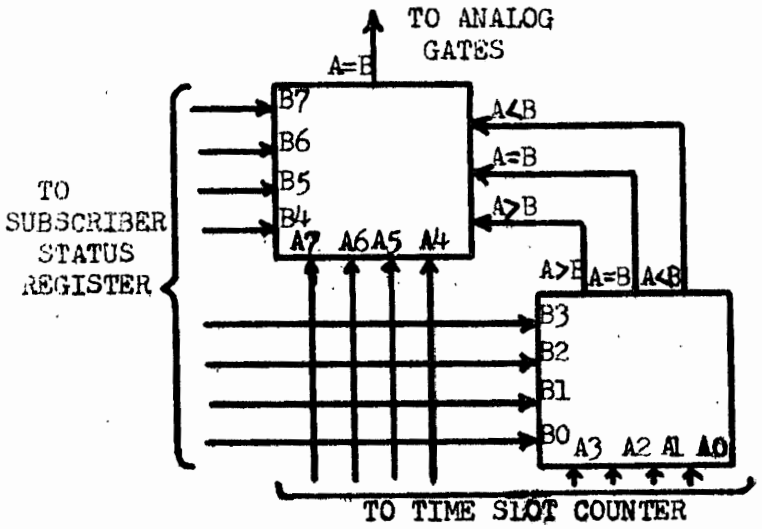


Figure 23. Two Cascaded Four-Bit Comparators.

One set of inputs to the magnitude comparator is the output of the Time Slot Counter. The Time Slot Counter counts the output pulses of the clock that controls the time-division multiplexing of the signals. In this application 63 time slots will be counted, and the Counter will return to 1 and start over again.

The other set of inputs to the comparator are the lowest six bits of the Subscriber Status Register. These bits contain the time slot number assigned by the microprocessor to the subscriber. When the two inputs are identical the A=B output of the comparator goes high. This activates the analog gates that connect the Audio Transmit and Audio

Receive lines to the Amplifier. If the two inputs are not identical the output of the comparator remains low and the analog gate is not activated. If no time slot has been assigned, that is, if the lower six bits of the subscriber's status register are zeroes, the output of the comparator remains low, since the other set of inputs will never be 000000.

This scheme provides the system with the feature that a comparatively small number of trunks, time slots, can be shared on a time-division basis by a much larger number of subscribers, to allow each subscriber to access every other subscriber as required. That is efficiency can be designed into the system.

Another feature that this scheme provides is that the microprocessor, Control function, and Multiplexing-Demultiplexing, Audio Mixing function, are performed independent from each other. That is the microprocessor can go about the business of determining the kind of service each subscriber requires, while the Multiplexer independently mixes the audio signals as previously programmed by the microprocessor.

Analog Gates[6]

The subscriber's Audio Transmit and Audio Receive signals are controlled by MOS analog switches. These are devices that when gated ON present low channel resistance to the analog signal, and when gated OFF, present very high channel resistance. Relays are electromechanical devices with these characteristics but they do not perform in high speed multiplexing applications. The parameters determining the desirability of an analog gate for a multiplexing-demultiplexing application are:

[6]Author unknown, Application Note 53, High Speed Analog Switches, (Santa Clara: National Semiconductor Corp., 1971), Pp. 1-6.

1. ON resistance.
2. OFF resistance.
3. ON resistance modulation by the analog signal.
4. **Switching speed** - Commutation Rate.

The switching speed at which an analog gate can be operated is a limiting factor in determining the number of subscribers that can be accommodated in an application such as this. The ON resistance of an analog gate attenuates the signal through it, therefore it is preferred to be as low as possible. The OFF resistance is one of the factors determining the amount of cross-talk between channels, therefore it is desirable that it be as high as possible. The ON resistance modulation by the amplitude of the analog signal is a very important characteristic. It introduces nonlinearities, intermodulation distortion, that are very disturbing when present in the audio signal.

J-FET and MOS-FET devices are the most popular for multiplexing-demultiplexing applications. J-FET analog gates have lower ON resistance, 20-30 ohms, and no ON resistance modulation, characteristics that are very important in applications requiring a high degree of precision. MOS-FET analog gates have higher ON resistance, 150-400 ohms and they exhibit ON resistance modulation. However, these characteristics can be minimized by appropriate design. Since the analog gate is in series with the Ri resistors, fig. 22, page 33, and these resistors are chosen to be 10k ohms, the attenuation introduced by the gate ON resistance is negligible. The ON resistance modulation is a function of the amplitude of the analog signal. Consequently, if the amplitude of the signal is low, the ON resistance will be minimized. On the positive side, MOS-FET gates demonstrate higher switching speeds and considerably lower costs.

Therefore, for applications such as this, where precision is not required, MOS-FET analog gates are chosen.

Central Multiplexing Amplifier-Bandwidth, Slewing Rate, Settling Time. A summing amplifier is used in the Audio mixer, because more than two subscribers can be gated ON at the input during the same time slot without loading each other down. Also, since the output impedance of the amplifier is very low, many subscribers can be gated ON to the output.

An amplifier for this kind of application must have very high bandwidth. Since adjacent time slots pertain to different subscribers, the input signal to the amplifier is a signal composed of the interleaved time samples of the various subscribers' inputs. Since there is no correlation between the audio signals of adjacent subscribers, the mixing amplifier must be capable to "follow" the composite signal whose amplitude may vary from the positive extreme to the negative during the transition from one time slot to the next. Consequently, the bandwidth of the amplifier is the most important factor determining the maximum number of time slots that can be obtained. Since however, only one amplifier of this kind is used in each system, the high cost of such an amplifier is not a large part of the total cost of the system.

Fig. 24 shows three audio channels, the Pulse Amplitude modulated waveform of each, and the time division multiplexed, composite signal of the three channels.

In a telecommunication system, each audio channel has a bandwidth of 3,500 HZ. In order to be able to accurately reproduce the original audio during demultiplexing, each channel must be sampled at a minimum rate of 7,000 times per second. Since there are 63 channels or time

slots in this system, the amplifier must have a bandwidth of at least 63 x 7,000 HZ = 0.44 MHZ. For operational amplifiers the small signal bandwidth characteristic is given by the unity gain frequency, Fc. This is usable, however, when the input signal is very small, typically below 100 mv. For larger signals, the full-power bandwidth is given by Fp, the highest frequency at which full power can be developed with low distortion. Fp is much smaller than Fc, typically by a factor of 10 or more.

Other characteristics that determine the performance of an amplifier in a multiplexing application such as this are its Slewing Rate and its Settling Time. The ability of an amplifier to reproduce at its output a rapidly changing input signal cannot be measured only in terms of frequency. The ability of an amplifier to "follow" nonsinusoidal signals with high rates of change is measured by its "Slewing Rate".

In this application where the input to the amplifier is a series of pulses of short duration, and varying amplitude, the amplifier must be capable of reproducing at its output the same pulses without distorting their shape. Even though an amplifier may display a high slewing rate, the amplitude of a pulse may not be reliably determined until the amplifier "settles". Fig. 25 shows the amplifier response to a step input. The "Settling Time" is the amount of time required by the output signal to reach its final value to within some error $\pm\epsilon$.

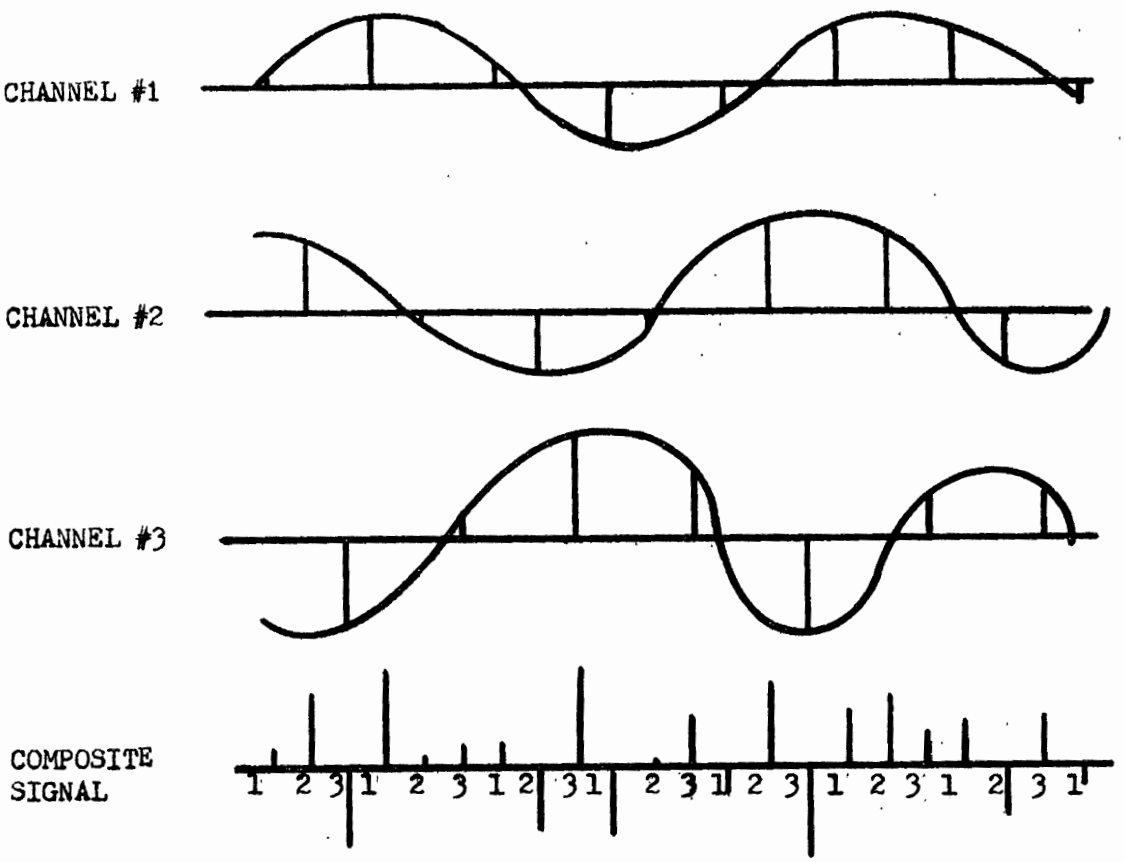


Figure 24. Three Analog Channels, Pulse Amplitude Modulated, Time Division Multiplexed.

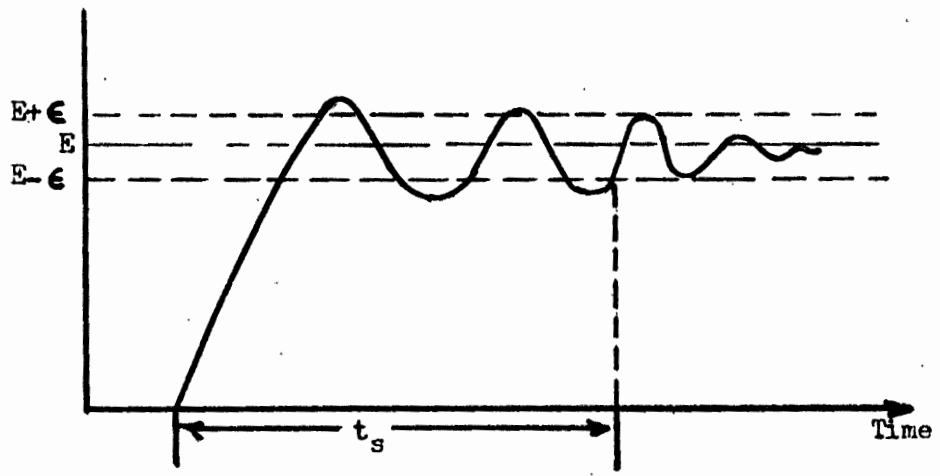


Figure 25. Settling Time.

Cross-talk. Cross-talk is defined as the disturbance created in one channel by the signal of an adjacent channel. The actual mechanism of coupling of the signal from one channel to the other can be inductive, capacitive, or resistive. In an application such as this, with high commutation rates and short sampling times, stray capacitances of the input and output of the amplifier become very important. Consequently, a "guard time" must be allowed between adjacent pulses of the composite signal so that all capacitances are discharged and the input to the amplifier returns to the reference potential. This insures that there will be no residual signal from one sample added to the adjacent sample.

Voice Signal and Sampling Rate. The spectrum of frequencies contained in human speech is shown in fig. 26 below.

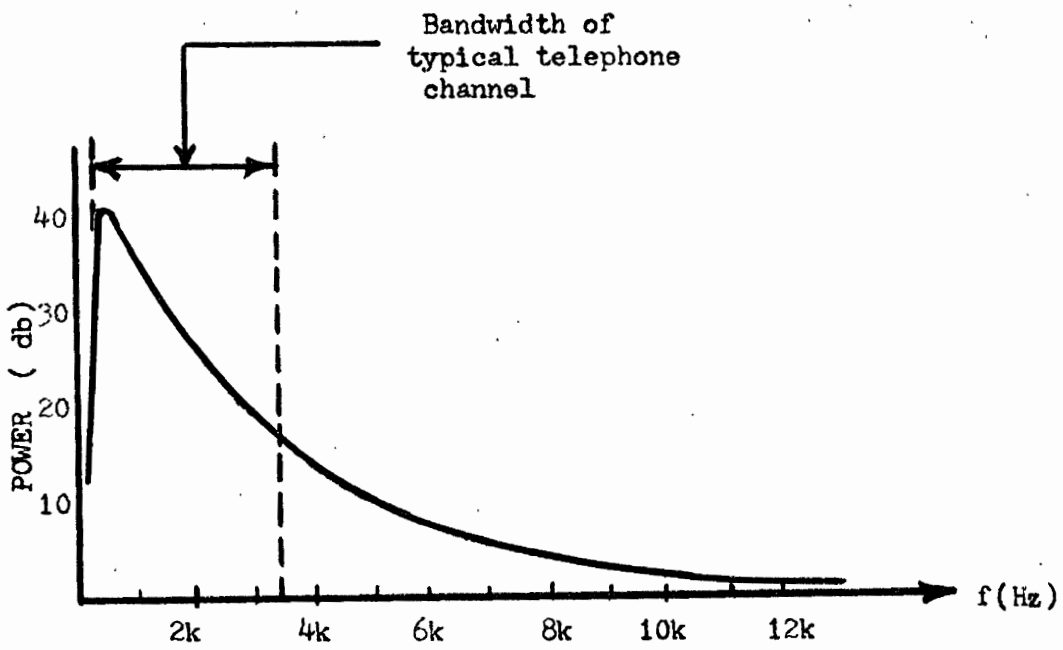


Figure 26. Power Spectrum of Human Voice Signal.[7]

[7] James Martin, Telecommunications and the Computer (Englewood Cliffs: Prentice-Hall, Inc., 1969), P. 186.

Frequencies between 100 HZ and 12 KHZ are present in the human voice, but as seen in fig. 27, most of the significant energy is contained in the band 200 HZ-5000 HZ. Intelligibility studies have shown that the optimum compromise between economics and quality of signal transmitted occurs when the signal transmitted is limited to 3.5 KHZ. Transmitting higher frequencies on a telephone channel would make the Receive Audio signal more "life-like" but would not increase significantly the amount of "information" transmitted. At the same time, the bandwidth required to multiplex a number of such channels would increase, thus increasing costs.

The basic principle that determines the frequency at which a signal must be sampled, in order that it may be reconstructed, as in the case of a demultiplexed Pulse Amplitude Modulated signal, is called the Sampling Theorem. In a restricted sense it states that if a message is a magnitude-time function which is instantaneously sampled at regular intervals and at a rate at least twice the highest significant frequency present in the signal, the samples contain all the information of the original message. The significance of this is that it determines the minimum rate at which the channel may be sampled by the multiplexer if the signal is to be reconstituted by the demultiplexer. That is, if the signal in the audio channel has a bandwidth of 3.5 KHZ it must be sampled at least 7,000 times per second if the original information is to be recovered. This dictates the minimum clock rate required, given the number of channels and the bandwidth of each, in a multiplexing application. Since in this application there are 63 channels to be sequentially sampled and each must be sampled 7,000 times per second, the minimum clock rate is $63 \times 7000 = 0.441$ MHZ.

Subscriber's Set. The Subscriber's Set contains a Transmit and Receive amplifier that amplify the Transmit and Receive Audio signals, respectively. It contains a Ringing Tone Generator that when activated generates a tone that notifies the subscriber that he is being called. It also contains a Multifrequency Tone Generator which generates the combinations of tones that are used to transmit to the Central Switching Unit the digits of the called subscriber's number. Fig. 28 shows a block diagram of the Subscriber's Set. Resistor R4 provides the Ring-back tone. That is, when the called Subscriber's Ringing Tone Generator is activated, its output is coupled to the subscriber's Transmit line through resistor R4 and transmitted to the Central Switching Unit where it is mixed into the Receive audio of the calling subscriber.

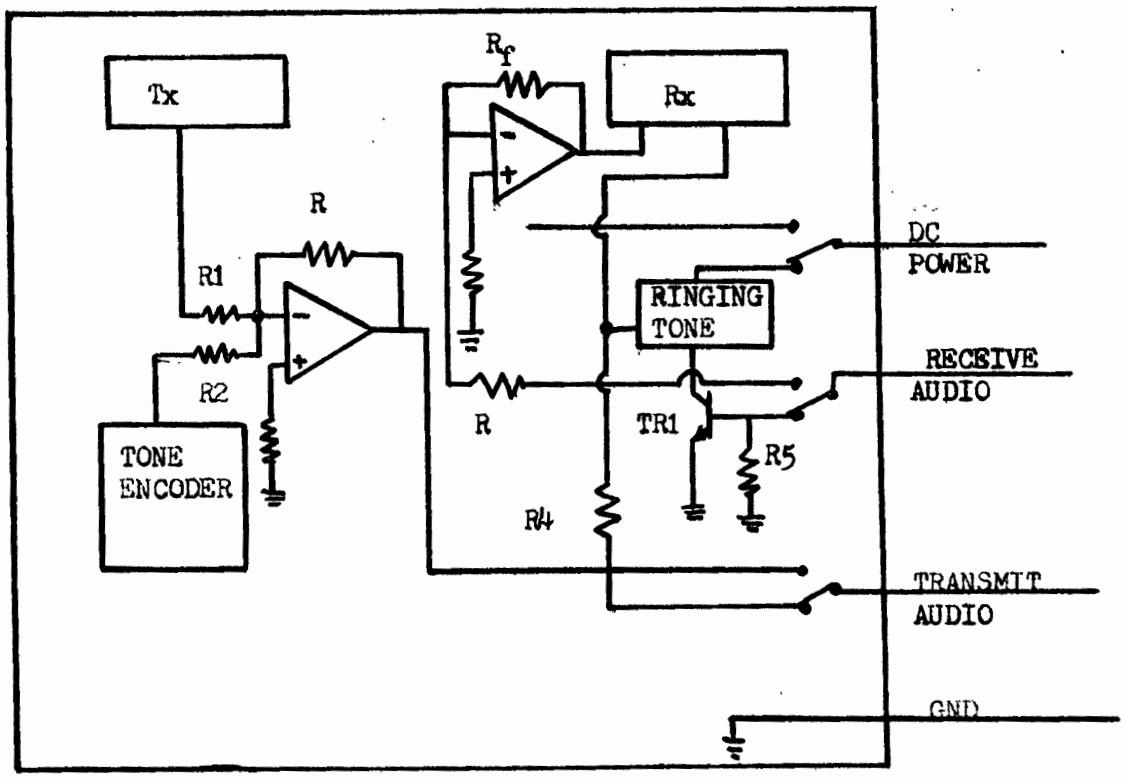


Figure 27. Subscriber's Set.

CHAPTER III

CONTROL PROGRAM

A flow chart outline of the sequence of tasks that the microprocessor has to perform is shown on pages 48 and 49. The sequence of instructions that must be carried out in order to control the system are shown on pages 58 through 64. Comments relevant to each instruction are found on pages 65 through 72.

The zeroth page of memory, locations 0000 - 00FF, is used for storage of data as required during the operation of the program. Locations 0001 - 0040 constitute the Time Slot-Subscriber Assignment Stack, 0041 - 0080 the Time Slot Available Stack, 0081 - 0085 the Tone Decoder Available Stack. Locations 0081 and 0085 are the Time Slot Available and the Tone Decoder Available Pointers, respectively. The remainder of the zeroth page is used for storage of various constants required for the operation of the program. Details are shown on Table I, page 55.

Page 1 of memory is not used in this application. On page 2, locations 0200 - 02F7 are the addresses if the Subscriber's Status Registers, 02F8 - 02FB are the addresses of the Tone Decoder's Status Registers and locations 02FC - 02FF are the addresses of the Output Registers of the Tone Decoders. Pages 3 and 4 are used for the storage of the program and are of the Read Only type.

Upon activation of the system, the Initialization Subroutine will store all the required constants into the zeroth page of Memory, as

shown in Table I. Locations 0001 - 0040 will be cleared. This is the Time Slot-Subscriber Assignment Stack. Each location pertains to the time slot of the same number and its contents are the number of the subscriber last determined to be in the time slot. If the microprocessor determines, as it goes through the polling process, that a subscriber has been assigned a time slot, it proceeds to determine the time slot number, and it stores the subscriber's number in the Time Slot-Subscriber Assignment Stack location pertaining to that time slot. As the polling continues, and a second subscriber is determined to be on the same time slot as the previous subscriber, the previous subscriber's number is compared with the current subscriber's number. If the two are not the same, the new subscriber's number is entered in the Time Slot-Subscriber Assignment Stack location pertaining to the time slot. If the two numbers are identical, it means that only one subscriber is assigned the time slot. The microprocessor uses this method to determine when to discontinue a call and make the time slot available for a subsequent call. So long as there are two subscribers assigned the same time slot the call can continue. When only one subscriber is left, the microprocessor will drop him from the time slot by entering 0000 0000 in his Subscriber's Status Register and at the same time will make the time slot available by adding it to the Time Slot Available Stack, locations 41 - 80.

Since upon initialization, no subscriber is assigned to any time slot, the contents of all locations of this stack are zeroes. The numbers 0000 0001 - 0100 0000 will be stored in increasing order in locations 41 - 80. These are the numbers of the time slots, and

locations 41 - 80 constitute the Time Slot Available Stack.

Upon initialization, all the time slots are unoccupied, and therefore are included in the Time Slot Available Stack. When a time slot is assigned to a subscriber it is removed from the Stack and zeroes are stored in its location. Since the duration of each conversation is a random characteristic, time slots become available in random order. When a time slot becomes available, at the end of a call, its number is stored in a location in the Time Slot Available Stack. A Time Slot Available Pointer is associated with the Time Slot Available Stack. The contents of this pointer is the address of the location in the Time Slot Available Stack where the number of the next available time slot is to be found. When a time slot is assigned to a subscriber, the Time Slot Available Pointer is incremented by 1 so that it points to the next location where the number of the next available time slot is stored. When a time slot becomes available at the end of a call, the Time Slot Available Pointer is decremented by 1 and the number of the newly available time slot is stored in the location to which the pointer points.

Locations 82 - 85 constitute the Tone Decoder Available Stack. There are four Tone Decoders in the system, and they are numbered 0 - 3. The numbers 0 - 3 correspond to the Tone Decoders whose Status Registers are located in locations 02F8 - 02FB respectively. Upon initialization the numbers 0, 1, 2 and 3 are stored, in increasing order, in locations 82 - 85. Location 86 is the Tone Decoder Pointer associated with the Tone Decoder Available Stack, and its contents are the address of the location where the number, 0, 1, 2 or 3, of the next available Tone Decoder is to be found. When the first call, after initialization is made, the Tone Decoder Pointer points to location 82. The contents of

this location are the number 0000 0000. After this Tone Decoder is assigned to the calling subscriber, the Tone Decoder Pointer is incremented by 1 so that it points to the next location where the number of the next available Tone Decoder, 0000 0001, is stored. The numbers 00 - 03, when added to the number 02F8 generate the address of the Tone Decoder Status Register for the appropriate Tone Decoder. Also when added to the number 02FC they generate the address of the Tone Decoder Output Register associated with the particular Tone Decoder.

Since Tone Decoders are released, following dialing, in random order, the order in which the numbers 0, 1, 2 and 3 appear in the Tone Decoder Available Stack is also random after the first few calls. Location 87 on the zeroth page of Memory is the Subscriber Pointer. The contents of this location are the number, 0 - F7, of the subscriber currently being serviced by the microprocessor. During initialization the number F7 is stored in location 87. Subscriber F7 is polled first. When the microprocessor finishes servicing this subscriber, it decrements the Subscriber Pointer and proceeds to poll subscriber F6, etc. After the Subscriber Pointer is decremented to 00, and service to this subscriber is completed, the Subscriber Pointer is reset to F7 and the process is repeated.

The microprocessor, by adding the contents of the Subscriber Pointer to the number 0200, addresses the Subscriber's Status Register and transfers its contents to the Accumulator. Checking flag Z in the Processor Status Register yields information about the status of the subscriber. If Z=1, the contents of the Subscriber Status Register are 0000 0000. This means that the subscriber is ON Hook, he is not being rung-up, and no time slot has been assigned to him. The subscriber

requires no further attention. The Subscriber Pointer is decremented by 1 and the same check is performed on the next subscriber. The most probable state in which a subscriber can be is the idle state. However, if Z=0, in instruction #4, the subscriber is not idle, because some bits in his Status Register are not zeroes. Depending on the contents of the Subscriber's Status Register conditional branches are made to provide the service required by the subscriber at each instance. The decisions as to the type of service required are shown as diamonds in the flow chart.

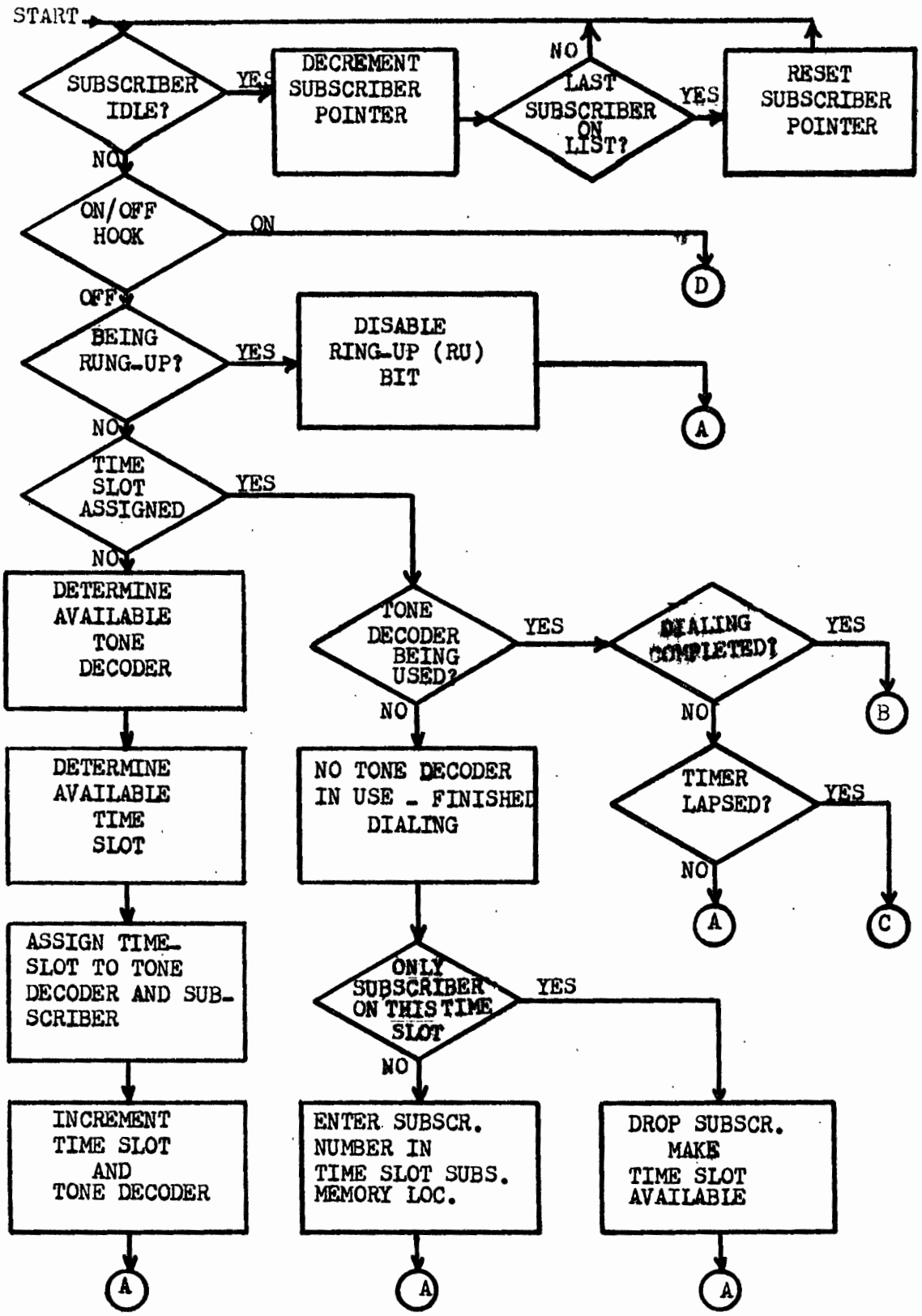


Figure 28. Flow-chart outline.

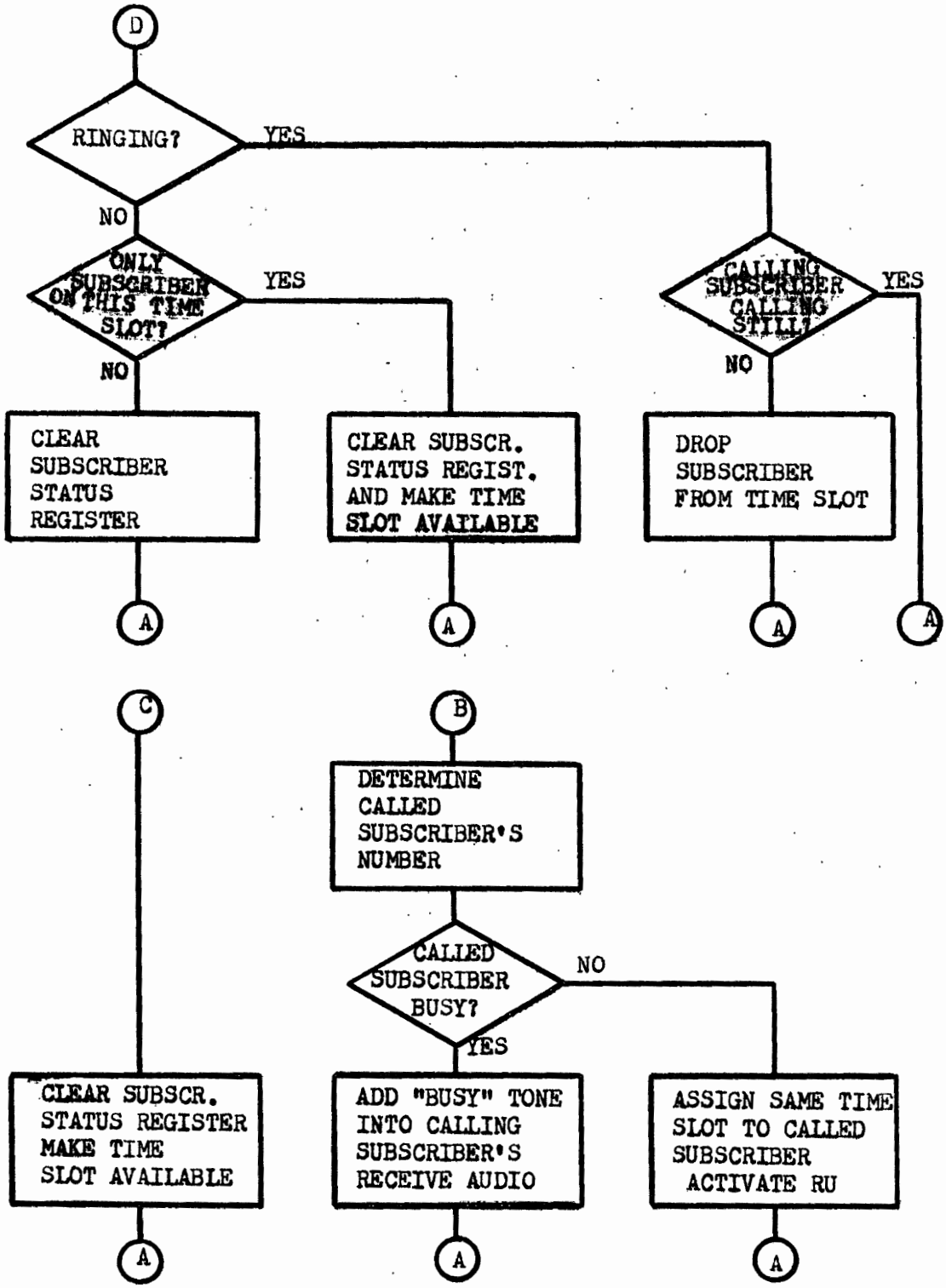


Figure 28. Flow-chart outline (cont'd).

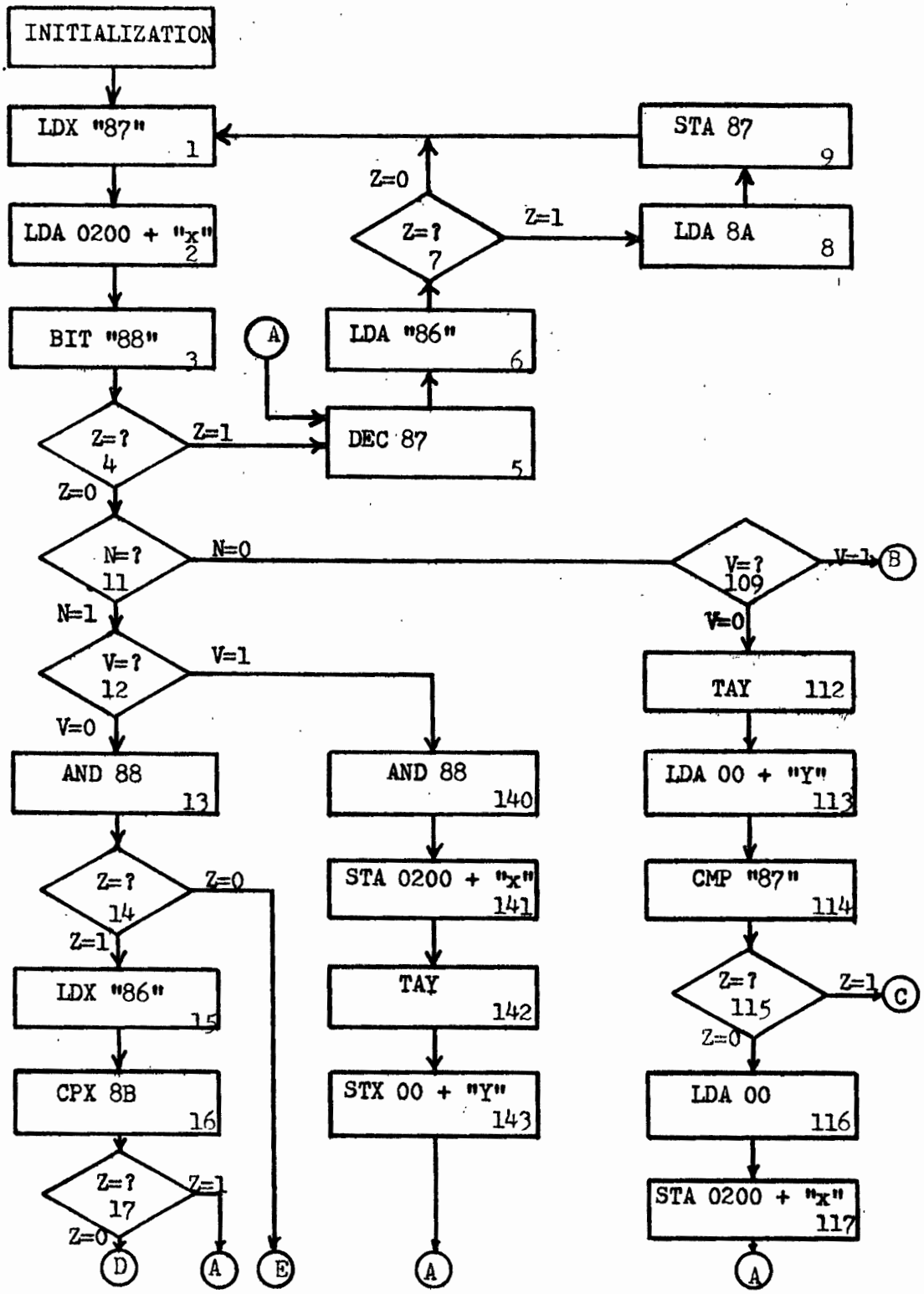


Figure 29. Flow-chart.

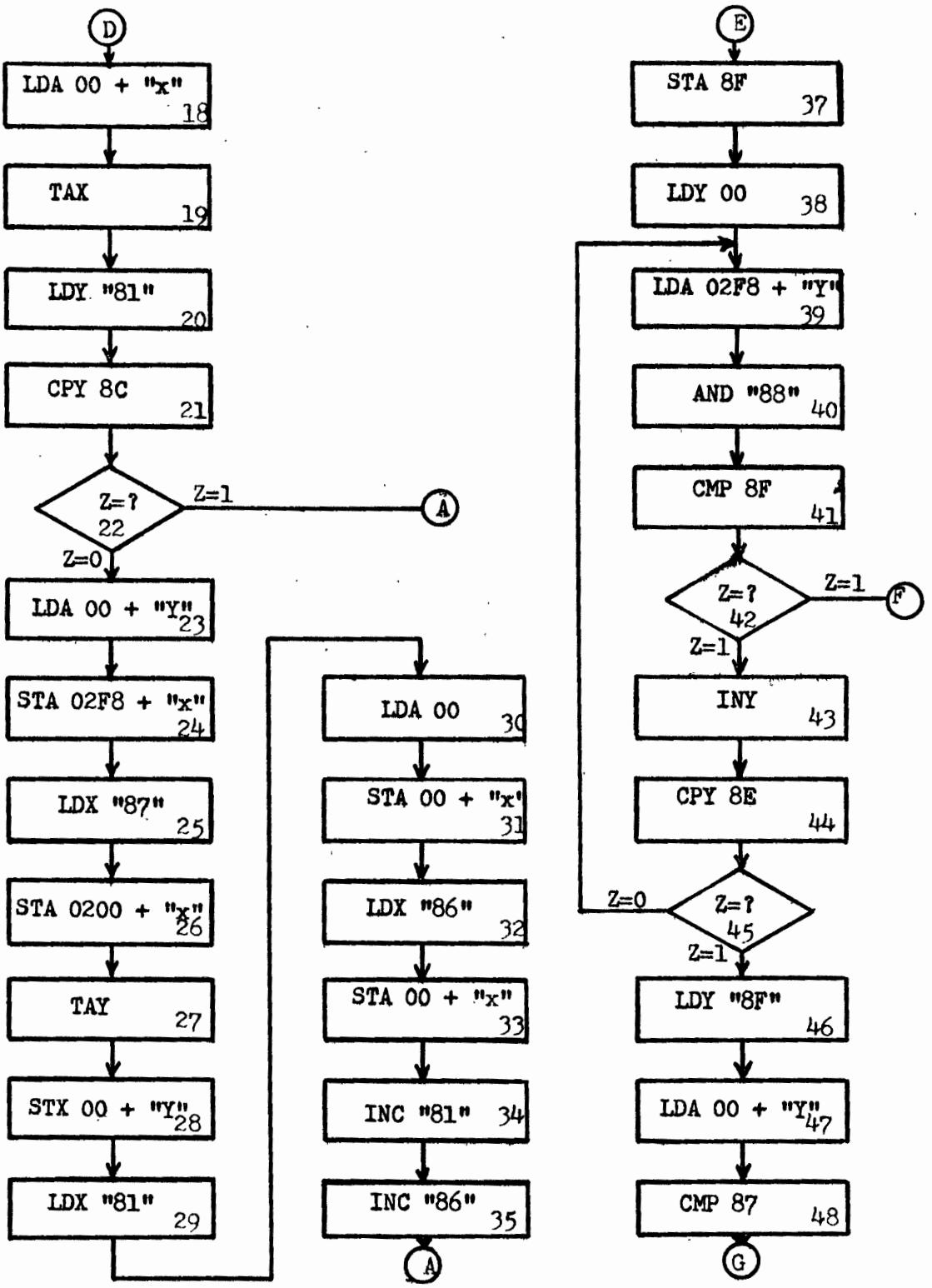


Figure 29. Flow-chart (cont'd.).

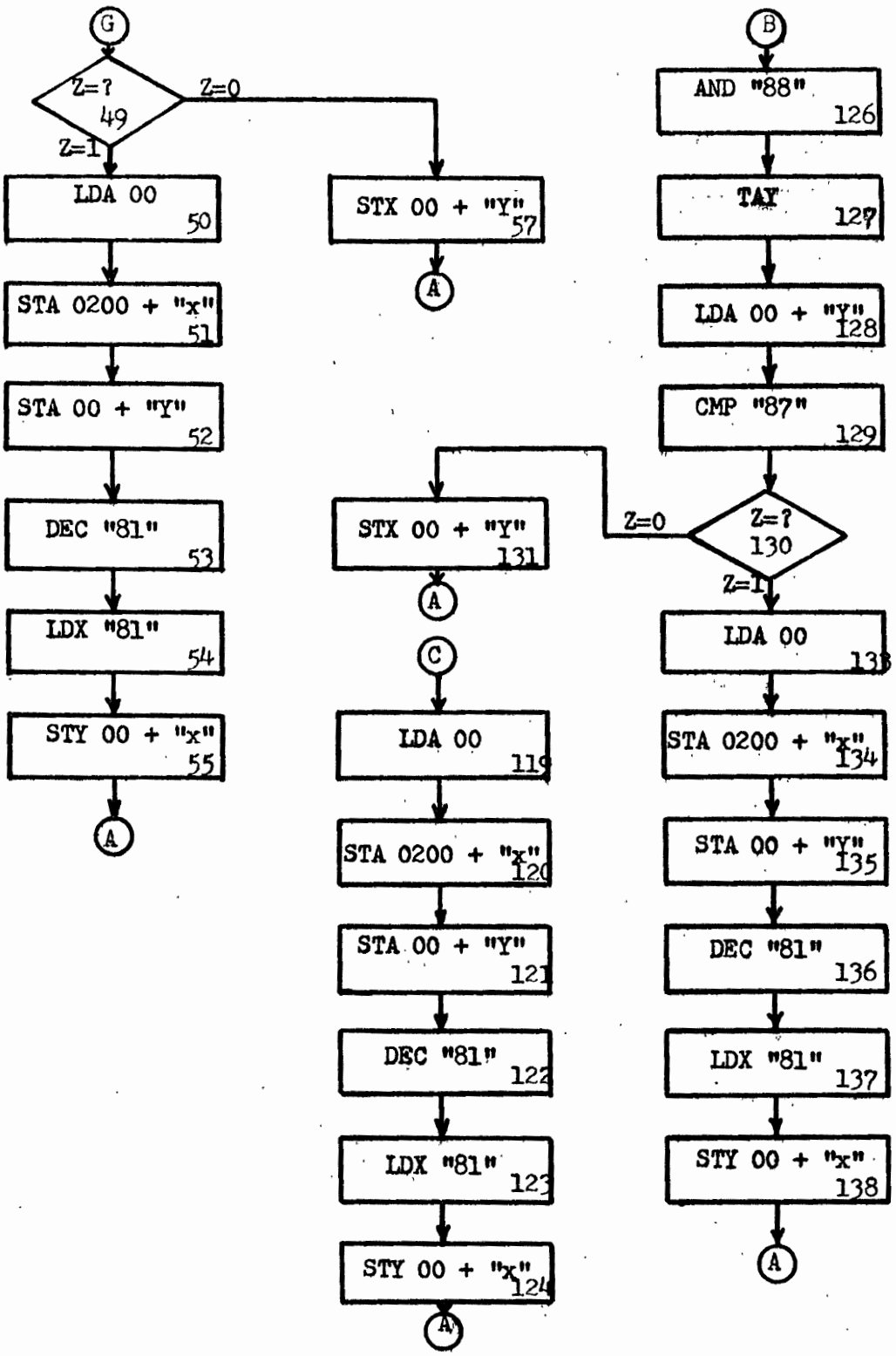


Figure 29. Flow-chart (cont'd.).

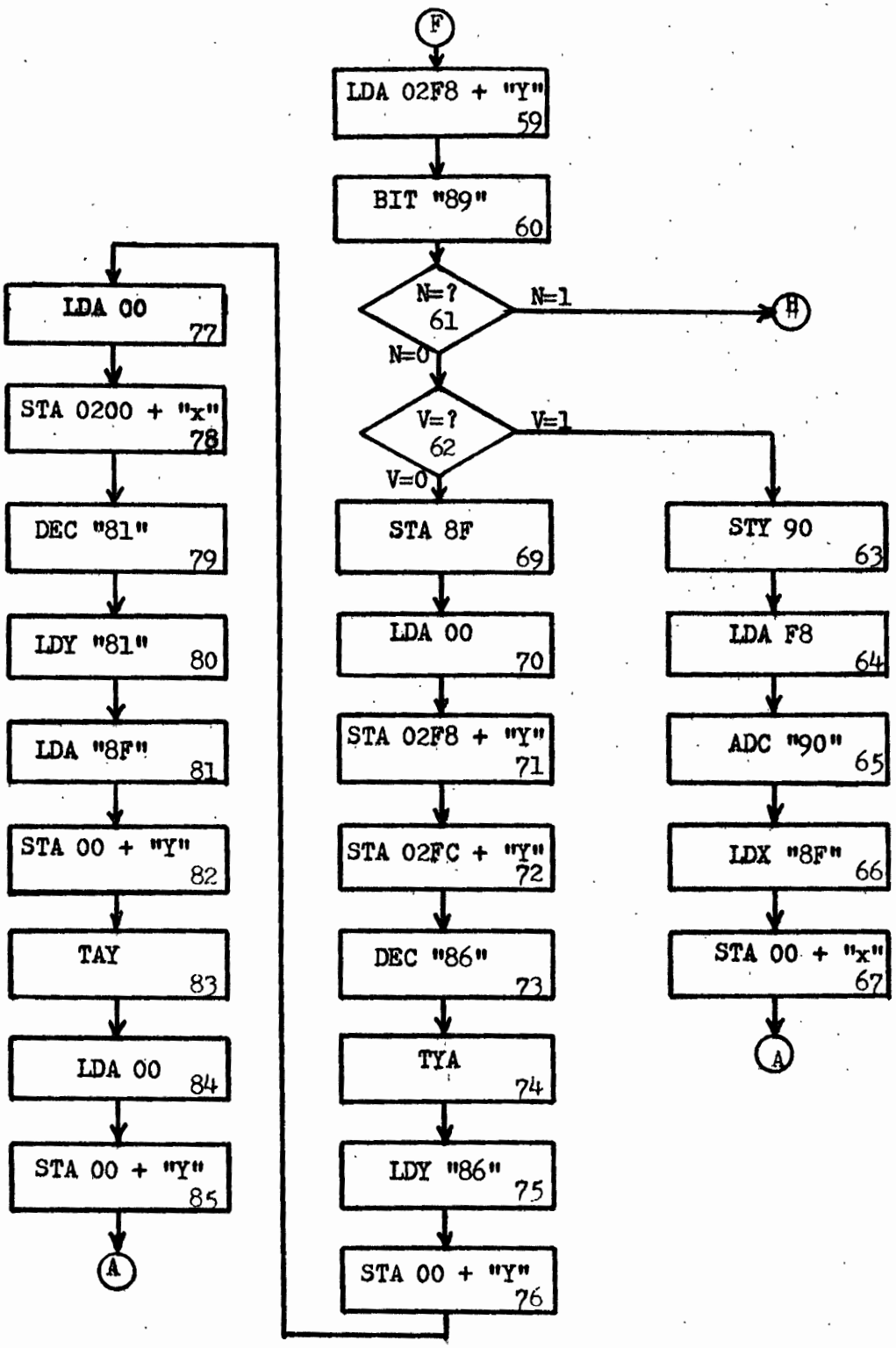


Figure 29. Flow-chart (cont'd.).

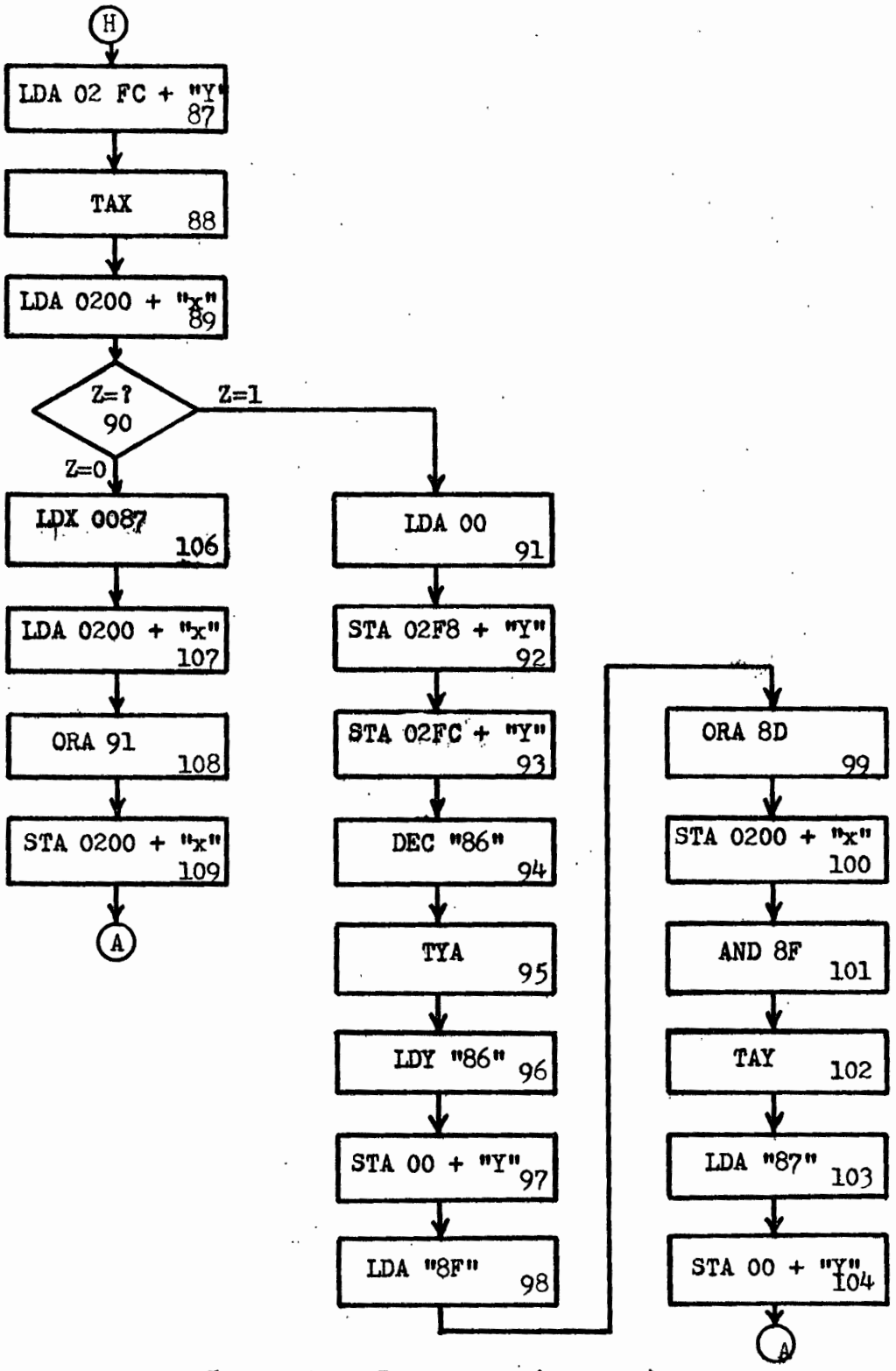


Figure 29. Flow-chart (cont'd.).

TABLE I

0TH PAGE OF MEMORY

Address Hexadecimal	Decimal	Contents	Comments
0000	0000	0000/0000	Contains zero as a constant.
0001	0001	xxxxxxxx	These 63 locations pertain to the 63 time slots. The numbers contained herein are the address (in page two) of the last subscriber assigned to this particular time slot. 63 time slots used. Time slot 0000 is not used.
0040	0064		
0041	0065	xxxxxxxx	These 63 locations constitute a stack of variable length. The contents of location 0081 point to the location where the number of the next available time slot is located. If the pointer points to itself, all the time slots are "Busy". The contents of these locations are 8-bit numbers 0000 0001 - 0100 0000.
0080	0128	xxxxxxxx	
0081	0129	xxxxxxxx	Time Slot Available Pointer. Contains the location where the number of the next available time slot is located.
0082 0083 0084 0085	0130 0131 0132 0133	xxxxxxxx xxxxxxxx	These 4 locations constitute the Tone Decoder Available Stack.
0086	0134	xxxxxxxx	Tone Decoder Pointer. (Location of next available Tone Decoder.)
0087	0135	xxxxxxxx	Subscriber Pointer. (Subscriber currently being serviced.)

TABLE I (COND'D.)

0TH PAGE OF MEMORY

Address Hexadecimal	Decimal	Contents	Comments
0088	0136	0011 1111	Mask needed to mask out the six bits that constitute the time slot number to which the subscriber has been programmed.
0089	0137	1111 1111	1's, required for the BIT Instruction.
008A	0138	1111 1000	The number of subscribers, (248)D, (F8)H in the system.
008B	0139	1000 0110	86. Address of Tone Decoder pointer.
008C	0140	1000 0001	81. Address of Time Slot Available Pointer.
008D	0141	0100 0000	In order to set the RU bit with the ORA instruction, Instruction #98.
008E	0142	0000 0011	3-The number is needed in step 44 to determine if all tone decoders have been tested for assignment to subscriber currently serviced.
008F	0143	xxxxxxxx	This location used for temporary storage of Accumulator in Instruction #37.
0090	0144	0000 00xx	Temporary storage of the contents of Y register in instruction #63.
0091	0145	1000 0000	Used to activate Busy Tone.

TABLE II

2ND PAGE OF MEMORY (SUBSCRIBER STATUS REGISTER)

Memory Location - Address	Contents/Comments
0000/0010/0000/0000 (0) 0000/0010/0000/0001 (1) 0000/0010/1111/0111 (247)	These 248 locations contain the "Subscriber's Status Registers". The bits of these registers are assigned as follows: /LS RU #5 #4 #3 #2 #1 #0/ #0-#5, 6 bits, number of time slot to which subscriber has been assigned. LS - Line Status/Busy Tone RU - Ring Up
0000/0010/1111/1000 (248) (0) (2) (F) (8) 0000/0010/1111/1100 (252) (0) (2) (F) (B)	These 4 locations contain the number of the time slot to which the Tone Decoder has been assigned. /#7 #6 #5 #4 #3 #2 #1 #0/ #0-#5 number of the time slot Bit #7: 1-Dialing Completed 0-Dialing not Completed Bit #6: 1-Timer not lapsed } output 0-Timer lapsed Timer: 20 seconds
0000/0010/1111/1100 (253) (0) (2) (F) (C) 0000/0010/1111/1111 (256) (0) (2) (F) (F)	These 4 locations contain the Decoded output of the Tone Decoders. Each location is permanently associated with a tone decoder.

TABLE III

CODED PROGRAM INSTRUCTIONS

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
1	LDX 87	A6 87	
2	LDA 0200 + "X"	BD 0200	
3	BIT 89	24 89	
4	BNE xx	D0 xx	xx - Loc. where instr. #11 is stored.
5	DEC 87	C6 87	
6	LDA 87	A5 87	
7	BNE xx	D0 xx	xx - Loc. where instr. #1 is stored.
8	LDA 8A	A5 8A	
9	STA 87	85 87	
10	JMP xx	4C xx	xx - Loc. where instr. #1 is stored.
11	BPL xx	10 xx	xx - Loc. where instr. #111 is stored.
12	BVS xx	70 xx	xx - Loc. where instr. #140 is stored.
13	AND 88	25 88	
14	BNE xx	D0 xx	xx - Loc. where instr. #37 is stored.
15	LDX 86	A6 86	
16	CPX 8B	E4 8B	
17	BEQ xx	F0 xx	xx - Loc. where instr. #5 is stored.
18	LDA 00 + "X"	B5 00	
19	TAX	AA	
20	LDY "81"	A4 81	

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
21	CPY 86	C4 8C	
22	BEQ xx	F0 xx	xx - Loc. where instr. #5 is stored.
23	LDA 0000 + "Y"	B9 0000	
24	STA 02F8 + "X"	9D 02F8	
25	LDX "87"	A6 87	
26	STA 0200 + "X"	9D 0200	
27	TAY	A8	
28	STX 00 + "Y"	96 00	
29	LDX "81"	A6 81	
30	LDA 00	A9 00	
31	STA 00 + "X"	95 00	
32	LDX "86"	A6 86	
33	STA 00 + "X"	95 00	
34	INC 81	E6 81	
35	INC 86	E6 86	
36	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
37	STA 8F	85 8F	
38	LDY 00	A0 00	
39	LDA 02F8 + "Y"	B9 02F8	
40	AND "88"	25 "88"	

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
41	CMP 8F	C5 8F	
42	BEQ xx	F0 xx	xx - Loc. where instr. #59 is stored.
43	INY	C8	
44	CPY 8E	C4 8E	
45	BNE xx	D0 xx	xx - Loc. where instr. #39 is stored.
46	LDY 8F	A4 8F	
47	LDA 00 + "Y"	B9 0000	
48	CMP "87"	C5 87	
49	BNE xx	D0 xx	xx - Loc. where instr. #57 is stored.
50	LDA 00	A9 00	
51	STA 0200 + "X"	9D 0200	
52	STA 0000 + "Y"	99 0000	
53	DEC "81"	C6 81	
54	LDX "81"	A6 81	
55	STY 00 + "X"	94 00	
56	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
57	STX 00 + "Y"	96 00	
58	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
59	LDA 02F8 + "Y"	B9 02F8	
60	BIT "89"	24 89	
61	BMI "xx"	30 xx	xx - Loc. where instr. #87 is stored.

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
62	BVC xx	50 xx	xx - Loc. where instr. #69 is stored.
63	STY 90	84 90	
64	LDA F8	A9 F8	
65	ADC 90	65 90	
66	LDX "8F"	A6 8F	
67	STA 00 + "X"	95 00	
68	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
69	STA 8F	85 8F	
70	LDA 00	A9 00	
71	STA 02F8 + "Y"	99 02F8	
72	STA 02FC + "Y"	99 02FC	
73	DEC "86"	C6 86	
74	TYA	98	
75	LDY "86"	A4 86	
76	STA 00 + "Y"	99 00	
77	LDA 00	A9 00	
78	STA 0200 + "X"	9D 0200	
79	DEC "81"	C6 81	
80	LDY "81"	A4 81	
81	LDA "8F"	A5 8F	
82	STA 00 + "Y"	99 00	
83	TAY	A8	
84	LDA 00	A9 00	

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
85	STA 0000 + "Y"	99 0000	
86	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
87	LDA 02FC + "Y"	B9 02FC	
88	TAX	AA	
89	LDA 0200 + "X"	BD 0200	
90	BNE xx	D0 xx	xx - Loc. where instr. #106 is stored.
91	LDA 00	A9 00	
92	STA 02F8 + "Y"	99 02F8	
93	STA 02FC + "Y"	99 02FC	
94	DEC "86"	C6 86	
95	TYA	98	
96	LDY 86	A4 86	
97	STA 0000 + "Y"	99 0000	
98	LDA "8F"	A5 8F	
99	ORA "8D"	05 8D	
100	STA 0200 + "X"	9D 0200	
101	AND 8F	25 8F	
102	TAY	A8	
103	LDA "87"	A5 87	
104	STA 0000 + "Y"	99 0000	
105	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
106	LDX "87"	A6 87	

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
107	LDA 0200 + "X"	BD 0200	
108	ORA "8B"	05 8B	
109	STA 0200 + "X"	9D 0200	
110	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
111	BVS xx	70 xx	xx - Loc. where instr. #126 is stored.
112	TAY	A8	
113	LDA 00 + "Y"	B9 0000	
114	CMP "87"	C5 "87"	
115	BEQ xx	F0 xx	xx - Loc. where instr. 119 is stored.
116	LDA 00	A9 00	
117	STA 0200 + "X"	9D 0200	
118	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
119	LDA 00	A9 00	
120	STA 0200 + "X"	9D 0200	
121	STA 0000 + "Y"	99 0000	
122	DEC "81"	C6 81	
123	LDX "81"	A6 81	
124	STY 00 + "X"	94 00	
125	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
126	AND "88"	25 88	
127	TAY	A8	

TABLE III (CON'D.)

INSTR. NO.	MNEM. CODE	HEXADECIMAL CODE	
128	LDA 0000 + "Y"	B9 0000	
129	CMP "87"	C5 87	
130	BEQ xx	F0 xx	xx - Loc. where instr. #133 is stored.
131	STX 00 + "Y"	96 00	
132	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
133	LDA 00	A9 00	
134	STA 0200 + "X"	9D 0200	
135	STA 00 + "Y"	99 00	
136	DEC "81"	C6 81	
137	LDX "81"	A6 81	
138	STY 00 + "X"	94 00	
139	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.
140	AND 88	25 88	
141	STA 0200 + "X"	9D 0200	
142	TAY	A8	
143	STX 00 + "Y"	96 00	
144	JMP xx	4C xx	xx - Loc. where instr. #5 is stored.

COMMENTS RELEVANT TO PROGRAM COMMANDS

The process identified by the INITIALIZATION command includes a series of steps required to transfer the various constants to RAM in order to make the program operative. The numbers used below refer to the commands as numbered on the flow chart. Numbers within quotation marks signify "the contents of", eg. "86" means the contents of location 86.

1. Location "87" is the Subscriber Pointer. The number contained in location 87 is the number of the subscriber currently being serviced.

2. Locations 0200-02F7 contain the Subscriber Status Registers. The addressing mode used here is the Indexed Absolute; the contents of the "X" Index register are added to the second and third bytes of the instruction.

4. Is subscriber idle? If Z=1 the subscriber is idle requiring no service. Z=0 signifies that some bits in the Subscriber's Status Register are 1's.

7. A counter with the number of subscribers is decremented, instruction #5, when service to a subscriber has been completed. When the counter is decremented to zero, instruction #7, it is reset to the maximum count, contained in memory location 8A, and the process starts again.

11. N=0 signifies that the subscriber is ON Hook.

12. V=0 signifies that the subscriber is not being rung-up.

13. The subscriber is Off-Hook. He is not being rung-up. The next task is to determine whether this is a new request for service or whether the subscriber has completed dialing. In order to determine whether this is a new request for service, the lowest six bits of the Subscriber's Status Register will be examined. If they are zeroes, no time slot has been assigned. Consequently, since he is Off-Hook, the subscriber wishes to initiate a call. To isolate the six lowest bits, the contents of the Subscriber Register are logically AND'ed with the word 0011 1111, stored in location 88 of memory.

14. If the contents of the accumulator, following instruction 13, are zeroes, the subscriber has not been assigned a time slot. This is a new request for service.

15. Location 86 contains the Tone Decoder Pointer. This pointer contains the location, 82-85, where the number of the next available Tone Decoder is to be found. So, if location 86 contains the number 82, the number of the next Tone Decoder will be stored in location 82. Locations 82-85 will contain the numbers 0, 1, 2, or 3. These numbers, when added to number 02F8, generate the address of the Status Register pertaining to the Tone Decoder that will be available next.

16. Location 8B contains the number 86. When the contents of location 86 is 86, the pointer is pointing to itself. Consequently there is no Tone Decoder available. The call cannot be completed. The polling will continue to the next subscriber.

18. The Accumulator will be loaded with the contents of the location to which the Tone Decoder Pointer points. These contents will be either a 0, 1, 2 or 3. This number will be used in instruction #24 below to generate the address of the Tone Decoder Status Register that will be used in the completion of this call.

20. Location 81 contains the Time Slot Available Pointer. This pointer points to the location, 41-80, where the number of the next available time slot is to be found. When the pointer points to itself all the time slots are being used and none is available.

21. Location 8C contains the number 81. This is used in instruction 22.

22. When the contents of location 81 is the number 81, there are no time slots available.

23. Load Accumulator with the contents of 00+"Y". The Accumulator now contains the number of the time slot which will be assigned to the subscriber now being serviced, as well as the Tone Decoder assigned to this call.

24. Store the time slot number in the Status Register of the Tone Decoder. The number of the Tone Decoder is stored in the X Index register.

25. Location 87 contains the number of the subscriber currently being serviced. In order to assign the time slot to the calling subssriber, load X with "87".

26. Store the Accumulator, time slot number, in location 0200+"X", where "X" is the number of the subscriber being serviced. Location 0200+"X" is the address of the Status Register of the subscriber being serviced.

Remaining tasks:
1. Clear register to which Tone Dec. Pointer points.
2. Clear register to which T.S.A. Pointer points.
3. Increment Tone Decoder Available Pointer (86).
4. Increment Time Slot Available Pointer (81).
5. Store subscriber number in "Time Slot-Subscriber" memory location.

26. (con'd.) "Accumulator" --- Time slot number
"Y register" --- T.S.A. pointer
"X register" --- "Subscriber Pointer"

28. Memory locations 1-64 are associated with time slots 1-64, on a one to one basis. That is, location 5 is associated with time slot #5, location 37 is associated with time slot #37, etc. The contents of each of these locations is the number of the subscriber last determined to be on the time slot associated with the location. This segment of memory will frequently be referred to as the Time Slot-Subscriber segment of memory. With this command the subscriber number, contained in the X Index register, is stored in the appropriate Time Slot-Subscriber memory location.

29. The contents of the Time Slot Available Pointer are loaded into the X Index register in order to be used to generate the address, in instruction #31.

30. The Accumulator is loaded with zeroes. Immediate Addressing mode is used.

31. Zeroes are stored in the location where the time slot number used to be. Thus, this time slot has been removed from the list of available time slots.

33. The contents of the Tone Decoder Pointer are used to generate the address in order to remove the Tone Decoder from the availability list.

34. The Time Slot Available Pointer, location 81, is incremented by 1, in order to point to the next available time slot.

35. The Tone Decoder Pointer, location 86, is incremented by 1, to point to the next available Tone Decoder.

37. If Z=0, after the execution of instruction #4, the subscriber is Off-Hook, not being rung up, and has been previously assigned a time slot. The microprocessor must determine whether the subscriber is in the process of dialing or whether he has completed the dialing and is only conducting his conversation. If it is determined that he is dialing, that is, he has been assigned a Tone Decoder, it must be determined whether he has finished dialing. If not, whether the timer has lapsed or not. The number of the time slot assigned the subscriber is stored in location 8F for use in the future.

39. The loop between instructions 39-45 is used to compare the Status Registers of each of the four Tone Decoders to determine whether any of them has been assigned the same time slot as the subscriber currently being serviced.

42. If Z=1, a Tone Decoder has been found which has been assigned the same time slot as the subscriber now being serviced by the microprocessor.

45. If Z=0, continue around the loop to instruction #39. If Z=1, all the Tone Decoder Status Registers have been examined and none was found to be on the same time slot.

46. The time slot number, temporarily stored in location 8F during instruction #37, is loaded into the Y Index register.
Since it has been determined that the subscriber is not dialing, it must be determined whether the called subscriber is still on the line. The Time Slot-Subscriber part of memory is used for this purpose. When a subscriber is determined to be on a time slot, his number is stored in the location pertaining to that time slot. As the polling continues, the microprocessor comes up to the other subscriber taking part in this call. The previous subscriber's number is erased and the new subscriber's number is entered in the location in the Time Slot-Subscriber part of memory corresponding to the time slot. Consequently, if there is more than one subscriber on a time slot, the number of the subscriber currently being serviced will be different than the number stored in the Time Slot-Subscriber memory location. When these two numbers are identical, there is only one subscriber left on the time slot. Everyone else has dropped out.

49. If Z=0, the two numbers are not identical. The number of the subscriber currently being serviced is stored in the Time-Slot Subscriber location in memory.
If Z=1, only the subscriber currently being serviced is on this time slot. Therefore, he must be dropped and the time slot made available for a subsequent call.

51. The X Index register contains the subscriber's number. This is used to generate the address to clear the Subscriber Status Register and thus remove this subscriber from the time slot.

52. The Y Index register contains the time slot number, after instruction #46. It is used to generate the address to clear the Time Slot-Subscriber location in memory.

53. The Time Slot Available Pointer is decremented by 1, since an additional time slot is becoming available.

55. The contents of the Time Slot Available Pointer are used to generate the address to store the number of the newly available time slot in the Time Slot Available Stack.

59. If it is determined that a Tone Decoder has been assigned to the subscriber currently being serviced, it must be determined whether the dialing has been completed and if it has not, whether the timer has lapsed. The Tone Decoder Status Register is transferred to the Accumulator.

61. Bit #7 is checked. If N=0, the dialing has not been completed. If N=1, dialing is complete.

62. Following the BIT instruction, #60, the V-flag is set equal to bit #6 of the Accumulator. If V=1, the timer has not lapsed. If V=0, the timer lapsed before the completion of dialing.

63. V=1. Timer has not lapsed. The Tone Decoder's number must be stored in the Subscriber-Time Slot Assignment Stack, to prevent the microprocessor from dropping the subscriber from the time slot during the next polling. The Tone Decoder number, 0, 1, 2 or 3 is temporarily stored in location 0090.

64. Load Accumulator with the number F8. Immediate Addressing Mode.

65. Add the Tone Decoder number to the number F8, in order to generate the number of the Tone Decoder's Status Register.

66. Location 8F is used in instruction #37 to temporarily store the time slot number assigned to the subscriber currently being serviced. This number is transferred to the X register in order to be used to generate the address of the location in the Subscriber-Time Slot Assignment Stack pertaining to the time slot.

67. The Tone Decoder Status Register number is stored in the Subscriber-Time Slot Assignment Stack.

71. V=0, instruction #62 means that the timer has lapsed before the completion of dialing. Both the subscriber and the Tone Decoder will be dropped from the time slot, the time slot will become available for a subsequent call and the polling will continue to the next subscriber. Tone Decoder is dropped from time slot with this command.

72. The Tone Decoder Output Register is cleared.

76. The Tone Decoder becomes available for future calls and its number is stored in the Tone Decoder Available Stack.

78. Zeroes are stored in the Status Register of the subscriber currently being serviced by microprocessor. He is, thus, dropped from time slot.

79. The Time Slot Available pointer is decremented and, in instruction #82, the time slot number is added to the stack of available time slots.

85. Clear the subscriber's number from the Time Slot-Subscriber Assignment Stack.

87. If, after instruction #62, it is determined that dialing has been completed, the microprocessor must proceed to determine the called number and add the called subscriber to the time slot. Transfer to the Accumulator the contents of the Output Register associated with the Tone Decoder.

89. The microprocessor must determine whether the called subscriber is busy, before ringing him up. The contents of the output Register are used to generate the address of the called subscriber.

90. If Z=0, the subscriber is busy, since some bits are 1's in his Status Register. If Z=1, the subscriber is idle and, therefore, may be rung up.

92. Clear the Tone Decoder Status Register.

93. Clear the Tone Decoder Output Register.

97. Make Tone Decoder available for a subsequent call. The Tone Decoder number is transferred from the Y Index Register to the Accumulator in instruction #95.

98. The Tone Decoder is added to the available list. The time slot number used in this call has temporarily been stored in location 8F, instruction #37.

99. The contents of location 8D are the binary word 0100 0000. The time slot number to be assigned to the called subscriber is 00xx xxxx. If number 0100 0000 is logically OR'd with number 00xx xxxx, number 01xx xxxx will be obtained, where xx xxxx is the number of the time slot. The 6th bit is used to activate the Ringing Tone Generator, so that when the word 01xx xxxx is stored in the called Subscriber's Status Register, the time slot assignment is effected and the Subscriber's Ringing Tone Generator is activated.

100. The time slot number is transferred to the Y Index register.

104. The Calling subscriber's number is stored in the Time Slot-Subscriber Assignment Stack.

108. Z=0 after instruction #90 means that the subscriber is busy. Consequently, the call cannot be completed, and a "Busy" tone must be added to the subscriber's Receive Audio line. Bit #7 of the Subscriber Status Register controls the Busy Tone. Therefore, in order to activate the Busy Tone for the calling subscriber, the contents of memory location 91 (1000 0000) are logically OR'd with the contents of the Subscriber Status Register. This adds the Busy Tone.

111. N=0 in instruction #11 means that the subscriber is ON Hook. However, in instruction #4 some of the bits of the Subscriber Status Register were determined to be 1's. Consequently the subscriber is either being called by somebody else and has not answered yet or he has hung-up after conducting a call and is now being detected. V=0 means that the subscriber is not being rung-up. After the BIT instruction, #3, the V-flag is set equal to bit #6, the Ring-Up bit.

113. Load the Accumulator with the contents of the Time Slot-Subscriber memory location associated with the time slot used during this call.

114. Compare the number of the subscriber currently being serviced, "87" with the number of the subscriber last determined to be assigned this time slot. If the two numbers are identical, the subscriber currently being serviced is also the last subscriber on this time slot. Since he has hung up, he must be dropped from the time slot and the time slot must become available to a subsequent call. If the two numbers are not identical at least one other subscriber is on the time slot. Since the currently serviced subscriber has hung up he will be dropped from the time slot, but the time slot will not be made available.

117. Since Z=0, only the currently serviced subscriber will be dropped from the time slot.

120. Since Z=1, the currently serviced subscriber is dropped from the time slot, and also the time slot must become available.

121. The Time Slot-Subscriber location in memory is cleared.

122. The Time Slot Available Pointer is decremented by 1.

124. The time slot number is stored in the availability stack.

126. Since in instruction #106 V=1, the subscriber is being rung-up. The microprocessor must determine whether the calling subscriber is still calling or whether he has hung up since the last polling. The Accumulator is loaded with the contents of the Subscriber's Status Register. Performing a logical AND with the word 00xx xxxx the time slot number is extracted from the register.

128. The number of the subscriber determined during the last polling to be in the Time Slot-Subscriber Assignment Stack is stored in the Accumulator.

130. Z=0 means that the subscriber currently being serviced is not the only one in the time slot.

131. The subscriber's number is stored in the appropriate Time Slot-Subscriber location.

134. Z=1 in instruction #130 means the subscriber currently being serviced is the only subscriber on the time slot. The calling subscriber has already hung up. Clear the Subscriber's Status Register.

135. Clear the Time Slot-Subscriber Assignment Stack location pertaining to the time slot used during this call.

138. Make the time slot available for a subsequent call.

140. V=1 in instruction #12 means that the subscriber is Off-Hook and being rung at the same time. This condition arises immediately after going Off-Hook to answer a call. Logical AND of 01xx xxxx with 0011 1111 results in 00xx xxxx.

141. 00xx xxxx is stored in the Subscriber Status Register. This resets the Ring Up bit in the register. The ringing itself is disabled as soon as the receiver goes Off Hook.

143. The subscriber's number is stored in the Time Slot-Subscriber Assignment Stack.

CHAPTER IV

CONCLUSIONS

The capability of the microprocessor to perform efficiently the control function as it pertains to the routing of audio signals, in order to conduct selective telecommunication, is demonstrated in this project. The microprocessor determines the required action on the basis of software rather than hardware, as would be the case with wired logic. Since the microprocessor is a relatively inexpensive elctronic component, systems of small size, up to a few hundred subscribers, can be implemented at low cost. Prior to the development of the microprocessor, Minicomputers would be required to provide any degree of flexibility to the system at a reasonable cost. Since minicomputers cost several thousands of dollars by themselves, a system would have to have several hundreds of subscribers before a minicomputer could be considered economically feasible. As a result, flexibility was the domain of large, computer controlled, systems only. The microprocessor allows flexibility at a reasonable cost for systems servicing only a few subscribers.

By "flexibility" is meant the ability of the system to adapt its response to a request for service according to the needs of different subscribers, or the same subscriber at different times. That is, the system could be programmed to reroute calls automatically to another subscriber when the first subscriber so desires. It could be programmed to route all calls to one extension at night, it could allow conference

calls with more than two subscribers, with the capability to add to or drop subscribers from the conference. It must have built-in self-test subroutines that determine faults in the system and direct the microprocessor to take corrective action, either to substitute redundant circuits for the faulty ones, or lock circuits out in order to eliminate interference.

The microprocessor could be programmed to perform other tasks, in addition to the control of the audio switching. Some of these could be the monitoring of environmental conditions in every room of large buildings, with the appropriate action taken if conditions were not optimum. Arithmetic operations could be performed, as well as the monitoring of fire, smoke and burglary alarms. The possibilities are many and the cliche that they are limited by the designer's imagination comes closer to the truth since the development of the microprocessor.

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