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Early Layout Design Exploration in TSV-based 3D Integrated Circuits

by

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Abstract

Through silicon via (TSV) based 3D integrated circuits have inspired a novel design paradigm which explores the vertical dimension, in order to alleviate the performance and power limitations associated with long interconnects in 2D circuits. TSVs enable vertical interconnects across stacked and thinned dies in 3D-IC designs, resulting in reduced wirelength, footprint, faster speed, improved bandwidth, and lesser routing congestion. However, the usage of TSVs itself gives rise to many critical design challenges towards the minimization of chip delay and power consumption. Therefore, realization of the benefits of 3D ICs necessitates an early and realistic prediction of circuit performance during the early layout design stage.

The goal of this thesis is to meet the design challenges of 3D ICs by providing new capabilities to the existing floorplanning framework [87]. The additional capabilities included in the existing floorplanning tool is the co-placement of TSV islands with circuit blocks and performing non-deterministic assignment of signals to TSVs. We also replace the wirelength and number of TSVs in the floorplanning cost function with the total delay in the nets. The delay-aware cost function accounts for RC delay impact of TSVs on the delay of individual signal connection, and obviates the efforts required to balance the weight contributions of wirelength and TSVs in the wirelength-aware floorplanning. Our floorplanning tool results in 5% shorter wirelength and 21% lesser TSVs compared to recent approaches. The delay in the cost function improves total delay in the interconnects by 10% - 12% compared to wirelength-aware cost function.

The influence of large coupling capacitance between TSVs on the delay, power and coupling noise in 3D interconnects also offers serious challenges to the performance of 3D-IC. Due to the degree of design complexity introduced by TSVs in 3D ICs, the importance of early stage evaluation and optimization of delay, power and signal integrity of 3D circuits cannot be ignored. The unique contribution of this work is to develop methods for accurate analysis of timing, power and coupling noise across multiple stacked device layers during the floorplanning stage. Incorporating the impact of TSV and the stacking of multiple device layers within floorplanning framework will help to achieve 3D layouts with superior performance.

Therefore, we proposed an efficient TSV coupling noise model to evaluate the coupling noise in the 3D interconnects during floorplanning. The total coupling noise in 3D interconnects is included in the cost function to optimize positions of TSVs and blocks, as well as nets-to-TSVs assignment to obtain floorplans with minimized coupling noise. We also suggested diagonal TSV arrangement for larger TSV pitch and nonuniform pitch arrangement for reducing worst TSV-to-TSV coupling, thereby minimizing the coupling noise in the interconnects.

This thesis also focuses on more realistic evaluation and optimization of delay and power in TSV based 3D integrated circuits considering the interconnect density on individual device layers. The floorplanning tool uses TSV locations and delay, non-uniform interconnect density across multiple stacked device layers to assess and optimize the buffer count, delay, and interconnect power dissipation in a design. It is shown that

the impact of non-uniform interconnect density, across the stacked device layers, should not be ignored, as its contribution to the performance of the 3D interconnects is consequential.

A wire capacitance-aware buffer insertion scheme is presented that determines the optimal distance between adjacent buffers on the individual device layers for nonuniform wire density between stacked device layers. The proposed approach also considers TSV location on a 3D wire to optimize the buffer insertion around TSVs. For 3D designs with uniform wire density across stacked device layers, we propose a TSV-aware buffer insertion approach that appropriately models the TSV RC delay impact on interconnect delay to determine the optimum interval between adjacent buffers for individual 3D nets. Moreover, our floorplanning tool help achieve 3D layouts with superior performance by incorporating the impact of nonuniform density on the delay, power and coupling noise in the interconnects during floorplanning.

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Table of Contents

List of Tables

List of Figures

Glossary

3D-IC:	3D Integrated Circuits
3D-P:	3D Packaging
3D-SIC:	3D Silicon Integrated Circuits
3D-SOC:	3D System on Chip
3D-WLP:	3D Wafer Level Packaging
B2B:	Back to Back
BEOL:	Back end of line
BIL:	Buffer Insertion Length
CMP:	Chemical Mechanical Polishing
D2D:	Die to Die
D2W:	Die to Wafer
DRIE:	Deep Reactive-Ion Etching
F2B:	Face to Back
F2F:	Face to Face
FEOL:	Front end of Line
GSRC:	Giga Scale Research Center
HCG:	Horizontal Constraint Graph
KOZ:	Keep Out Zone
MCNC:	Microelectronics Center of North Carolina
TSV:	Through Silicon Vias
VCG:	Vertical constraint graph
W2W:	Wafer to Wafer

List of Symbols

A_{TSV}	Area of TSVs
C_{avg_wire}	Average wire capacitance of multiple device layers
C_{buf}	Capacitance of unit size (1x) buffer
C_{top1}	Coupling capacitance between top surface of TSV and wires on top
C_{top2}	Coupling capacitance between TSV sidewall and outside wires on top
C_{side1}	Coupling capacitance between TSV sidewall and side wires
C_{side2}	Coupling capacitance between TSV sidewall and non-overlapped wires
C_{c1}	TSV coupling with adjacent vertical and horizontal TSVs
C_{c2}	TSV coupling with adjacent diagonal TSVs
$C_{a(w-g)}$	Area capacitance between wires and ground plane
$C_{f(w-g)}$	Fringe capacitance between sidewall of wires and ground plane
$C_{a(w-w)}$	Wire to wire coupling
C_{sw_top}	Capacitance per unit length between sidewall of upper wire and top surface of lower wire
C_{top_top}	Capacitance per unit length between top surface of upper and lower wire
C_{corner}	Capacitance per unit length between two corners of the wires
C_{tot_wire}	Total Capacitance of a wire
C_{TT}	TSV-to-TSV coupling
C_{TSV}	TSV Capacitance
C_{TW}	TSV-to-wire coupling
C_{wire}	Capacitance per unit length of wire
D	TSV diameter
D_{min}	Minimum spacing between TSVs and metal wire
D_i^{nom}	Delay in a buffered segment on i^{th} device layer
D_i^{rem}	Delay in a remaining segment on i^{th} device layer
D_{wire}	Delay in wire
H	Height of wires or thickness of dielectric
H_{TSV}	Height or Length of TSVs
ID_i	Interconnect density on i^{th} device layer
k_{horiz}	Dielectric constant between same metal layers
k_{vert}	Dielectric constant between two different metal layers
L_{rem}	Length of wire segment between receiver and closest buffer before TSV
L_{rem_TSV}	Length of wire segment between TSV and closest buffer before TSV
L_{wire}^{TSV}	TSV equivalent wirelength
L_{wire}	Length of wire

N_i^{buf}	Number of buffer for a wire on i^{th} device layer
n_layer	Number of device layers
npin	Number of pins in a net
N_{TSV_tot}	Total TSVs in the design
N_{TSV}	Number of TSVs in a 3D net
R_c	TSV Contact Resistance
R_{TSV}	TSV Resistance
R_{wire}	Resistance per unit length of wire
P(n_TSV)	Probability for *n* number of TSVs in a 3D wire
p_{inv}	Parasitic capacitance of inverter
R_{buf}	Resistance of unit size (1x) buffer
S	Spacing between wires
S_i	Spacing between wires on i^{th} device layer
S_{min}	Minimum spacing between wires defined by process parameters
S_{TSV}	Spacing between TSVs
T	Thickness of wires
TWL_{3D}	Total wirelength of 3D design on all device layers
TWL_i	Total wirelength on i^{th} device layer
V_{noise}	Magnitude of noise voltage at victim net
V_{signal}	Magnitude of signal voltage at aggressor net
W	Width of wires
WS_i	Length of wire segment on each device layer
W_{TSV}	TSV width
W_{buf}	Buffer size

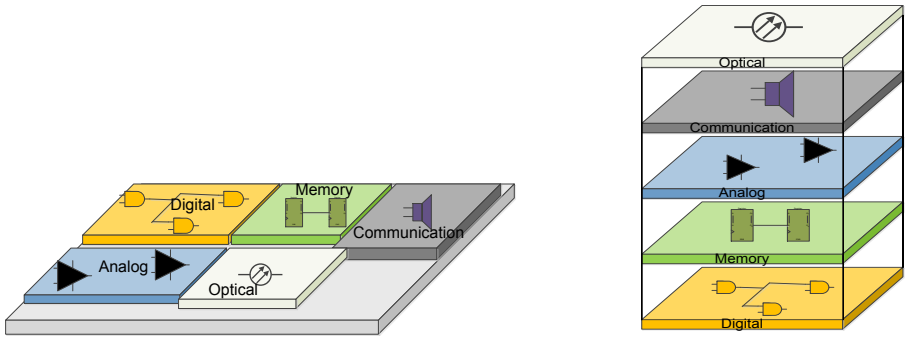
1. Introduction

The unprecedented demands for higher performance and on-chip functionality at minimum cost and power, has resulted in aggressive scaling of devices. However, the interconnect performance has not been able to keep up with the dramatic improvement of the device performance. Therefore, the delay, power and reliability in the interconnects has become a major concern in 2D system-on-chip. With continued scaling of CMOS technology into the nanometer range, 3D integration using through-silicon via (TSV) has gained tremendous momentum as it offers attractive and viable alternatives for improving density, performance, energy efficiency and cost. Moreover, TSV-based 3D-ICs do not require a revolutionary new 3D design and process technology. However, new capabilities are needed in various design stages, like system-level design exploration, physical design stages; timing, signal integrity and thermal analysis, IC testing and packaging.

The goal of this thesis is to meet the design challenges of 3D ICs by providing additional capabilities to the existing 3D floorplanning framework [87]. These TSV-aware capabilities include the impact of TSV area, location and its RC parasitics in the early stage of physical design. The developed floorplanning tool will facilitate in the early stage evaluation and optimization of timing, power, signal integrity of 3D circuits. Early design exploration will enable better design decisions for later stages in the 3D IC design flow, so that the overall timing closure and design convergence can be better achieved.

1.1 Three-Dimensional Integrated Circuits

Three-dimensional (3D) integrated circuits are fast emerging as a viable design paradigm, which explores the vertical dimension; in order to alleviate the performance and power limitations associated with long interconnects in 2D circuits [1-4]. Shorter interconnects due to smaller footprint results in faster performance and improved power efficiency. 3D design architecture enables vertical stacking of device layers (Si), which can be achieved by wire-bond or flip chip packaging methods or interlayer interconnects also known as through-silicon-via (TSV). Each device layer in 3D structures can have its own dedicated metal stack. Furthermore, 3D structures may accommodate multiple heterogeneous functionalities such as logic, memory, analog/RF circuits, micro-electrical mechanical systems (MEMS), biomedical, optical I/Os at different process nodes as shown in Figure 1 (b). Most computational systems have rapidly growing memory bandwidth demands that can be achieved by stacking memory top of logic or processor block. A memory bus I/O circuit delivering 100 GB/s memory bandwidth would consume only 2W in 3D integration technology as compared to 20W in 2D-IC technology [5]. The technique for 3D integration pertinent to this work is TSV-based 3D IC.



(a) **(b)**

Figure 1: Implementation of heterogeneous functionality using (a) 2D ICs, (b) 3D ICs

1.2 Through-Silicon Via Technology

A Through-Silicon-Via connection, shown in Figure 2, is a galvanic connection between the two sides of a Si wafer that is electrically insulated from the substrate and from other TSV connections [1][2][3]. The insulation layer surrounding the TSV conductor is called the TSV liner. The function of this layer is to electrically isolate the TSVs from the substrate and from each other. This layer also determines the TSV parasitic capacitance. In order to avoid diffusion of metal from the TSV into the Si-substrate, a barrier layer is used between the liner and the TSV metal. TSVs are used as interconnect between packages, as an alternative to wire-bond and flip chip methods, allowing for faster performance and better power profile. TSV connecting consecutive device layers occupies silicon area only on the upper device layer. The take-off metal for TSVs is the top metal layer (M_{top}) of the bottom substrate. Whereas, the landing metal for TSVs depends is either M_1 or M_{top} of the top substrate, and defined by TSV processing. The diameter of fabricated TSVs are typically in the range 2-10μm, and the aspect ratio

ranges from 10:1 to 20:1. The basic physical and electrical characteristics of TSVs will be defined by the 3D process flow.

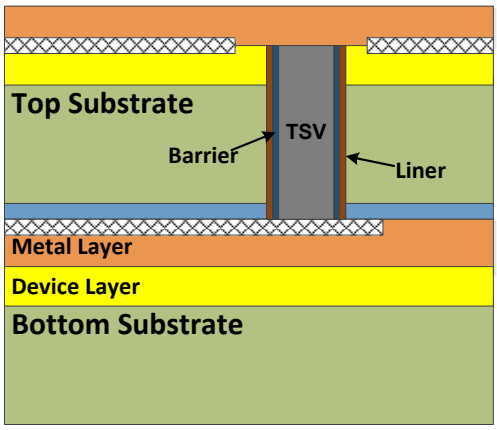


Figure 2: TSV Structure connecting two vertically stacked device layers

1.2.1 TSV-based 3D Process Flow

The process technology for TSV fabrication is well established and is being manufactured in high volume [3]. The steps for TSV-based 3D process are (i) TSV formation, (ii) IC wafer thinning, and (iii) alignment and bonding. The processing steps for TSV formation such as via etching (DRIE), insulator deposition, via filling and barrier deposition are well established. The known techniques for IC wafer thinning are grinding, CMP, wet and plasma etching. Additional techniques require for wafer or die bonding are adhesive bonding, fusion oxide bonding or metal-to-metal bonding. The different process flows for TSV-based 3D IC may be characterized by following key characteristics (i) order of TSV processing, (ii) method of 3D bonding and (iii) stacking method.

TSVs are classified based on the order of its processing with respect to the device wafer fabrication process as via-first, via-middle and via-last (Figure 3). Via-first TSVs are fabricated before Si front-end of line (FEOL) device fabrication processing. Via-middle TSVs are fabricated of TSVs after the Si FEOL device fabrication processing but before the back-end of line (BEOL) interconnect process, and via-last TSVs are fabricated after or in the middle of the Si BEOL interconnect process from back side or front side. The manufacturing of via-first TSV is the most challenging as it suffers from issues with temperature compatibility of subsequent CMOS steps. Hence, polysilicon is the preferred material for via-first TSVs due to its compatibility with CMOS devices, but has poor electrical properties. Via-last TSVs occupy significantly larger silicon area resulting in lower via density. Moreover, via-last TSVs offer obstacles for the interconnect layers causing higher routing congestion than via-first TSVs. Via-last TSVs are preferred for power/ground or clock connects and their location must be considered during the physical design phase to achieve better performance.

Via-middle TSVs are processed after device fabrication, but before metal layers are deposited. Via-middle TSVs also offer higher via-density compared to via-last TSVs due to their smaller sizes, and preferred for inter-block connections. The material used for via-middle TSVs is either copper (Cu) or Tungsten (W). The thermo-mechanical stress induced by W-TSVs is negligible as coefficient of thermal expansion (CTE) of tungsten is very similar to silicon [14][15]. But, due to high resistivity of W-TSVs are not so much popular for high performance applications. Cu-TSVs on the other hand suffer from large

thermo-mechanical stress, but provide better electrical performance. In this thesis, we focus on the Cu-based via-middle TSVs due to their superior performance and established manufacturing.

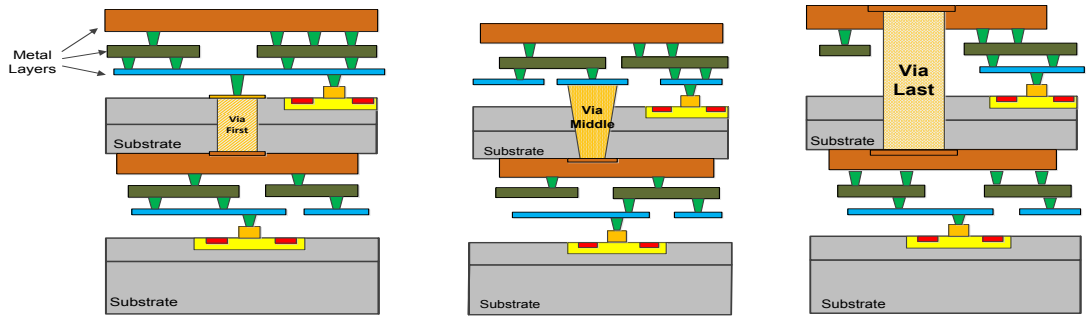


Figure 3: Classification of TSVs based on the order of its processing with respect to the device wafer fabrication process. a) via-first, b) via-middle and, c) via-last technology

The existing bonding methods for 3D ICs are wafer-to-wafer (W2W), die-to-wafer (D2W), and die-to-die (D2D) bonding. The W2W bonding shown in Figure 4(a) offers low cost, higher via density and better alignment. However, W2W suffers from low yield, as a bad die can be stacked on top of a good die resulting in chip failure. D2W and D2D result in higher yield as the dies are tested prior to 3D stacking. The additional testing cost and lower throughput can increase the overall cost of the chip.

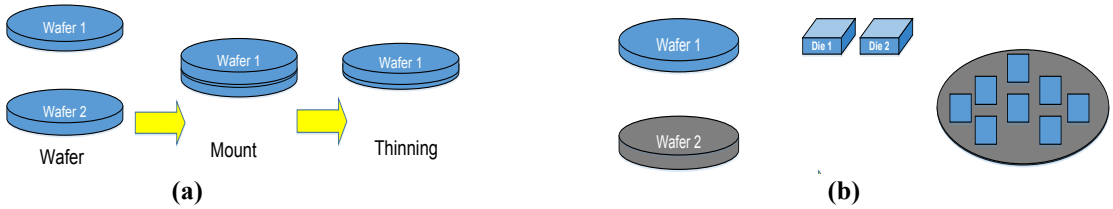


Figure 4: 3D bonding method using (a) wafer-to-wafer, (b) die-to-wafer

In addition to these primary characteristics, three secondary characteristics are identified, as Face-to-Back (F2B), Face-to-Face (F2F) and Back-to-Back (B2B) as shown in Figure 5. This work is based on F2B die-stacking strategy, as it does not limit the number of device layers that can be stacked.

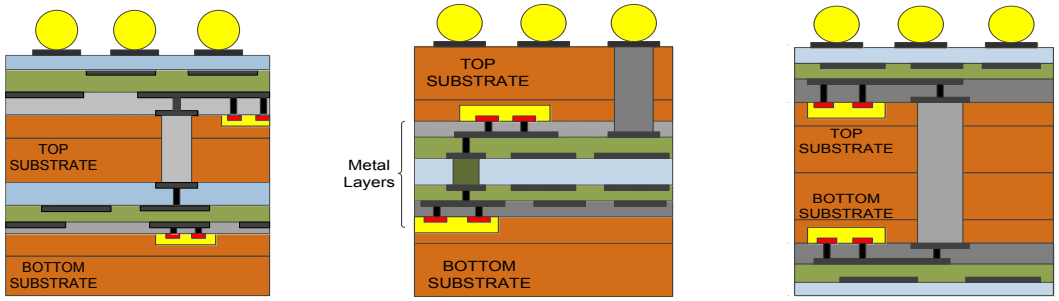


Figure 5: Comparison of different stacking techniques, (a) Face-to-Back, (b) Face-to-Face, and (c) Back-to-Back.

1.3 Benefits of TSV-based 3D-IC

3D integration is fast emerging as a viable design paradigm to resolve the existing interconnect bottleneck [1] encountered in 2D ICs, because of the continued device scaling. Recent advancements in through-silicon via (TSV) technology hold excellent opportunities for future generations. The advantages of 3D ICs with TSVs compared to traditional packaging techniques and two-dimensional SoC can be summarized as follows:

1. Shorter Interconnects: Due to smaller footprint [1-4], the length of interconnects between packages decreases. It allows for faster performance and a better power profile.

2. Lower Costs: Functionalities like analog and memory don't necessarily need to move to advanced process nodes [4][5].
3. Higher I/O Bandwidth: It allows for high interconnect speeds and bandwidth requirements up to 100 Gbits/second [5]. Multiple TSVs between functional blocks will allow high interconnect speeds and better power efficiency.
4. Reduce Power Consumption: Due to shorter interconnects, big drivers are no longer required. A 3D stack can use small I/O drivers with lower power [5].
5. Heterogeneous Integration: Developing technologies such as MEMS, photonics, carbon nanotubes, spintronic devices manufactured on different technological nodes, can be integrated into 3D stacks [5].

1.4 Challenges with TSV-based 3D IC

Despite all the advantages mentioned in the previous section, 3D IC technology faces several critical challenges due to the fact that this technology is relatively new. The stacking of multiple device layers and usage of TSVs itself gives rise to many critical design challenges towards minimization of chip delay and power consumption. The major challenges associated with TSV-based 3D ICs are:

- **Early Design Exploration in 3D IC**: Due to the degree of design complexity introduced by TSVs in 3D ICs, an early stage evaluation and optimization of performance, power and signal integrity of 3D circuits will facilitate better design decisions for later stages in the 3D IC design flow. Existing methods for early design exploration use pre-layout methods like Rents rule to estimate wirelength distribution

in a 3D circuit for timing, power and signal integrity analysis. However, these methods need to account for the impact of TSVs and stacked die implementation for more accurate and realistic representation of 3D designs.

- **3D Floorplanning:** The non-trivial size of TSVs, the need for keep-out-zones (KOZ) around individual TSVs and the required pitch between adjacent TSVs, results in increased silicon area. KOZ is required to mitigate the impact of TSV-induce thermo-mechanical stress on adjacent devices and TSVs. KOZ is also critical to reduce the impact of TSV-to-TSV coupling on the performance of 3D interconnects. However, the KOZ will increase the chip area significantly. The number and position of TSVs is crucial and will impact the wirelength. The wirelength goes up with too many TSVs in the circuit. Given these considerations, a TSV-aware 3D floorplanning to minimize the chip area, wirelength and TSV count becomes quite challenging.

- **Extraction and Analysis:** Existing extraction and analysis tools need to be extended for 3D ICs. The extraction tools must model the TSV capacitance including all its components, which will depend on the TSV parameters and the spatial distribution of TSVs and the wires on the layout. The interconnect RC performance depends on the available routing resources, wire technology and the density of the wires. The interconnect density in 3D ICs will depend on the placement of blocks and TSVs, and may not be the same across multiple stacked device layers. Therefore, the extraction tools should have the visibility into the top and bottom of each die. Further, analysis

tools will require TSV-aware capability, and therefore, timing, power and signal integrity must be analyzed across multiple die considering the interaction of dies.

- **Power/Ground and Clock Planning:** With 3D stacking, power planning gets more complex. Designers need to provide enough power to drive all of the device layers. Therefore, via-last TSVs are preferred for P/G/CLK signals due to superior electrical properties. However, via-last TSVs occupy large space on silicon resulting in low via density. Moreover, via-last TSVs causes routing obstacles increasing the problem complexity of routing stages. Managing clocks across multiple die without incurring skew is another challenge wit TSV-based 3D ICs. If separate clocks are used for individual stacked device layers, the synchronization of different clocks is also critical.

- **Thermal Issues:** Due to increased power density in stacked device layers and insufficient heat removal source can result in hotspots and chip failure [1][3][5]. Thermo-mechanical stress caused by the different coefficient of thermal expansion (CTE) of TSV material induces stress in the silicon. Thermal TSVs are inserted in the hotspots to mitigate the thermal issues. However, the thermal TSVs will require sufficient whitespace in the hotspots impacting the area and manufacturability. Thermal-aware 3D floorplanning [6][7] can be very effective in minimizing hotspot and peak chip temperature by optimizing the placement of blocks. The other cooling techniques insert micro-scale fluidic channels into 3D ICs to alleviate thermal problems [75].

- **Compound Yield**: Design and test strategies are required to improve the yield of IC design [3]. The wafer testing methods need to account for die stacking and TSV bonding. The primary challenges associated with wafer testing also include access to die inside stack and proper handling of thinned wafers. 3D ICs also introduce new intra-die defects as a result of new manufacturing steps such as wafer thinning, or TSV bonding.

Hence, the mainstream acceptance of 3D IC will require an effective and successful 3D IC design framework. An effective 3D IC design framework will provide a higher level of abstraction through early estimation and floorplanning, and achieve timely design closure by including physical, electrical, thermal, and process information. The higher level of abstraction is critical for better automation of subsequent stages and streamlining the design process.

1.5 Contributions

This dissertation focuses on two aspects of early design analysis: *a)* TSV-induced coupling noise in 3D interconnects, and *b)* the impact of interconnect densities on the performance of multiple stacked device layers.

1.5.1 Coupling Noise in 3D integrated circuits

We proposed an empirical model for fast estimation of coupling noise introduced by TSVs in 3D wires, given by Eq. 28. The developed model is used during floorplanning to estimate coupling noise in individual 3D interconnects. The model is derived by curve

fitting to HSpice simulations of 3D nets with the different length of the wires and TSV dimensions. The model is validated for a typical range for wires from 10μm to 2500μm, and typical diameters for TSVs from 1μm to 3μm, as shown in Figure 30. We incorporated an additional term in the cost function to account for the coupling noise introduced by TSVs, which is a summation of coupling noise in 3D nets. The direct inclusion of coupling noise in the cost function helps in reducing the total and worst coupling noise by 23% and 21% respectively, as compared to the coupling-unaware cost function, which can be seen in Table 13. Although, the introduction of coupling noise in the cost function increases the delay and power in the interconnects by 6% and 8% respectively (Table 14), the mean delay is better than the typical cost function consisting of area, wirelength and number of TSVs, as shown in Figure 33. In addition, we have also investigated the possible benefits of diagonal form of TSV arrangement to minimize the coupling noise in the interconnects. The extrapolation equations from the regular arrangement were used to compute TSV-to-TSV coupling between diagonal TSVs, which need to be verified using simulation methods. The results for larger and less practical TSV pitch for diagonal arrangement looks promising, where the total and worst coupling noise in the circuits reduces by 30% and 21% (Table 16) respectively, as compared to regular TSV arrangement. However, the TSV-to-TSV coupling between diagonal TSVs for TSV pitch equal to twice of its diameter needs to be developed. Moreover, further floorplanning experiments have to be conducted to find out if the diagonal arrangement will reduce TSV coupling noise for practical cases. Finally, we use nonuniform pitch to

minimize coupling noise with the lesser rise in chip area and delay, instead of widely used larger TSV pitch method, as shown in Figure 37.

1.5.2 Interconnect Density-aware Performance Evaluation/Optimization

In this thesis, we estimated the actual wire capacitance (Table 20) on each device layer considering the nonuniform interconnect densities across multiple stacked device layers. This is because, we observed that the wirelength distribution on individual device layers is not the same, and its impact on the performance of 3D interconnects is consequential. We also included the estimated delay and coupling noise, considering different wire capacitance, across multiple stacked device layers in the cost function. This optimizes the position of blocks and TSV islands on the layout, and helps achieving better floorplans as compared to the floorplanning done using the same wire capacitance on all device layers. The power-delay product reduces by up to 17% (Figure 51) and total coupling noise by up to 43% (Table 24), as compared to the floorplanning assuming the wire capacitance on all device layers is the same.

We also observed that due to nonuniform wire density, the performance and power in the interconnects reduces, while the coupling noise due to TSVs increases. We present a trade-off between the delay and coupling noise for different weight values of these parameters in Figure 52.

We suggest interconnect synthesis and optimization techniques such as wire capacitance-aware buffer insertion, optimizing the width of the wires on the individual

device layers separately, increasing the wire spacing and the number of semi-global metal layers on the device layers with higher interconnect density.

1.5.3 Significance of the work

The work presented in this thesis is built on a floorplanning tool that was previously developed by R.K. Nain, and is based on an evolutionary algorithm (EA) using sequence pair (SP) representation [37][84][87]. The additional capabilities to the original tool provide the possibility of early evaluating the design choices for different TSV's parameters, and their placement topologies providing 3D layouts that can offer better performance. This tool can be deployed at the system-level stage, as the information related to macros/blocks such as area, aspect ratio, gate/pin count, power consumption is available. 3D floorplanning offers early possibility of evaluating the design with different TSV technologies, dimensions and placement topology providing more reliable solutions with better performance. Moreover, the optimization of the circuit performance during the floorplanning will facilitate in reducing the problem complexity in the placement and routing stages. The optimization of circuit performance during floorplanning will require an accurate evaluation of the performance parameters like delay, power and coupling noise on the floorplan, which is the focus of this thesis.

1.6 Dissertation Organization

The dissertation is divided into following sections: The floorplanning stage and its challenges are summarized in Chapter 2. Chapter 3 gives more details on proposed TSV and delay- aware 3D floorplanning, and presents a comparison with existing works. The focus of chapter 4 is on the modeling of TSV RC and wires RC values during the floorplaning. Chapter 5 discusses the buffer planning and its impact on the delay and power in buffered 3D interconnects. It also highlights the advantage of optimizing the placement of blocks and TSVs to achieve layouts with optimal delay and power. Chapter 6 addresses the issue of coupling noise in 3D interconnects using proposed floorplanning framework. The study of non-uniform interconnects density between different device layers and its influence on wire capacitances is presented in chapter 7. The analysis of influence of varying wire capacitances on the performance metrics, such as delay, power and coupling noise, and their optimization is also discussed in chapter 7. Finally, chapter 8 presents the conclusions and future works.

2. IC Floorplan Design

In today's world, there is an ever-increasing demand for SOC speed, performance, and features. To cater to all those needs, the industry is moving toward lower technology nodes. The current market has become more and more demanding, in turn forcing complex architectures and reduced time to market. The complex integrations and smaller design cycle emphasize the importance of floorplanning, i.e., the first step in Netlist-to-GDSII design flow. A typical SOC can include many hard- and soft-IP macros, memories, analog blocks, and multiple power domains. Because of the increases in gate count, power domains, power modes, and special architectural requirements, most SOCs these days are hierarchical designs. The SOC interacts with the outside world through sensors, antennas, displays, and other elements, which introduce a lot of analog component in the chip. All of these limitations directly result in various challenges in floorplanning.

Floorplanning includes macro/block placement, design partitioning, pin placement, power planning, and power grid design. What makes the job more important is that the decisions taken for macro/block placement, partitioning, I/O-pad placement, and power planning directly or indirectly impact the overall implementation cycle. The designer takes care of the design parameters, such as power, area, timing, and performance during floorplanning. In hierarchical designs, the quality of the floorplan is analyzed after the blocks are integrated at the top level.

Floorplanning involves positioning of these macro/blocks on the chip to improve the performance of the design. Since most of the information regarding these blocks like area, aspect ratio, gate/pin count, power consumption; the floorplanning stage can move to early design phase. Hence, floorplanning can provide early feedback that evaluates architectural decisions, estimate footprints, wire congestion, delay and power consumption. Figure 6 (a) shows an example of the original design phase, while Figure 6 (b) shows the design flow where floorplanning is done in an early stage of the design cycle.

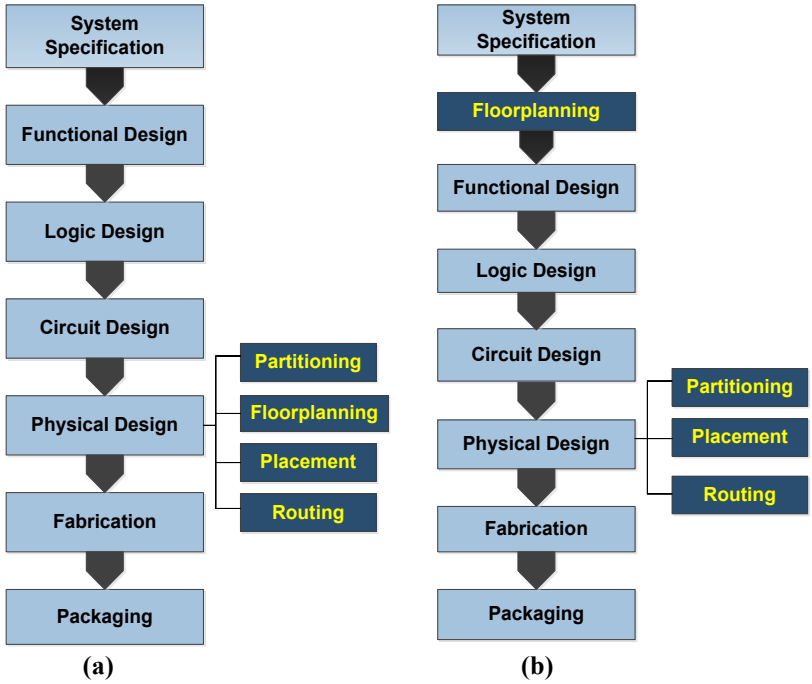


Figure 6: (a) original design phases and (b) using floorplanning in the early design phase.

2.1 Floorplanning Problem

The floorplanning problem can be stated as follows: Let B = {b_1, b_2…, b_n} be a set of rectangular blocks with given aspect ratio (h_1/w_1, h_2/w_2……, h_n/w_n). N = {n_1, n_2…., n_m} represents the list of nets connecting pins located at the center of each block. Classical 2D floorplanning aims to optimize the area of the chip and total inter-block wirelength. In addition to chip area minimization, modern VLSI floorplanning also needs to handle some important issues such as *soft modules* and *fixed-outline* constraints. Unlike a hard module that has a fixed dimension (width and height), the shape of a soft module needs to be determined during floorplanning for a given fixed area. It is required from a floorplanner to find a desired aspect ratio for each soft module to optimize the floorplanning cost. However, in our floorplanning problem we only consider hard macro/blocks. Let (x_i, y_i) denote the coordinate of the bottom-left corner of each block. A floorplan F is an assignment of (x_i, y_i) for each block on 2D layout such that there are no overlaps of the blocks.

In 3D floorplanning, the blocks are distributed to *L* device layers such that there is no overlap of the blocks on any device layer. The goal of the floorplanning is to optimize a predefined cost metric such as maximum footprint of all layer, wirelength, which is the sum of interconnect lengths, and number of TSVs, vertical connection between adjacent layers.

2.2 Floorplan Structure

The two types of layout structures in floorplan are slicing and non-slicing floorplan. A slicing floorplan is attained by repetitively slicing the floorplan region horizontally or vertically. A slicing floorplan is represented using a binary tree, known as slicing tree, with modules at the leaves and type of cut at the internal nodes. The two types of cuts are H (horizontal), for dividing the floorplan left or right, and V (vertical), for dividing the floorplan in top or bottom region. The non-slicing floorplan is represented using horizontal constraint graph (HCG) and vertical constraint graph (VCG), and defines the horizontal and vertical relationship between blocks or modules.

2.3 Representations for Non-slicing floorplans

The topological representation used for floorplan can be critical due to NP-hard complexity of floorplanning problems. The representation should be able to traverse large search space in least computational time. The existing representations for non-slicing floorplans are Bounded Slicing Grid Structure (BSG) [19] [20], Corner Block List (CBL) [21], Corner Sequence (CS) [22], Sequence Pair (SP) [23] [24], B* Tree [25] [26], Transitive Closure Graph (TCG) [27] [28], Integer Coding [29], O Tree [30]. These representations can be compared based on solution space search and computational complexity as shown in Table 1.

Table 1: Comparison of search spaces and computational complexity in non-slicing floorplan representations

Floorplan Representations	Search Space	Computational Complexity
B* Tree	$O[(n!2^{2n-1})/n^{1.5}]$	O(n)
O-Tree	$O[(n!2^{2n-1})/n^{1.5}]$	O(n)
TCG-S	$O((n!)^2)$	O(n. logn)
Fast-SP	$O((n!)^2)$	O(n.log(logn))
CBL	$O[(n!2^{3n-3})/n^{1.5}]$	O(n)
CS	$O((n!)^2)$	O(n)

2.4 Floorplanning Algorithm

Floorplanning problem is NP-hard, and the multi-variable optimization increases the solution search space significantly. Migrating from 2D to 3D designs will further increase the solution space due to increase in device layers and the number of parameters to be optimized. A typical 3D floorplanning problem includes area, wirelength and number of TSVs in the optimization phase. With the increase in the number of parameters, modules and device layers in 3D floorplanning, the size of the solution space will exponentially grow and deterministic algorithms may not be able to find an acceptable solution. Therefore, stochastic search based algorithms with smaller runtime overhead are more suitable for 3D floorplanning design. These non-deterministic algorithms perturb the solution space at each iteration to improve the quality of final solution.

Simulated annealing is a commonly used probabilistic technique for finding globally optimized solution during floorplanning [31] [32] [33] [34]. It is based on the technique involving heating and controlled cooling of a material to minimize defects in the crystal. The algorithm initiates with a randomly generated initial solution, and searches for a better solution based on set of perturbations. The approach accepts the worse solutions

after the perturbation as it allows for more extensive search for the optimal solution. However, as the temperature of the material cools down, the probability of accepting worse solutions decreases.

An evolutionary algorithm is another stochastic search method and begins with an initial set of solutions. It allows for parallel search reducing the computational time for searching solution space. The flow of evolutionary algorithm used in the floorplan design is discussed in [35] [36]. This work is based on the 3D floorplanning software developed by R.K. Nain [37] [84] [87], which is based on evolutionary algorithm and uses sequence pair representation. Some of the moves used to perturb the floorplan are:

1) Swap: Positions of two randomly chosen blocks are exchanged.
2) Invert: The order of a sequence between two randomly chosen points is reversed.
3) Rotate: Swap a module's width and height
4) Exchange: Positions of two randomly chosen modules on two different device layers are exchanged.

2.5 Basic 3D Floorplanning tool

The work presented in this thesis is built on a floorplanning tool that was previously developed. The initial version of 3D floorplanning tool is based on an evolutionary algorithm (EA) using sequence pair (SP) representation [37] [84]. This initial version placed circuit blocks across multiple devices ignoring TSV area and its position to determine total wirelength. The parameters optimized during floorplanning are: 3D area,

wirelength and TSV count. Since, TSVs are not physically placed, the final area and wirelength are underestimated.

2.6 General Assumptions

Throughout the course of this research certain assumptions were made to facilitate the development of the floorplanning tool. These assumptions are based on the technology requirements for 3D ICs suggested by ITRS.

These assumptions involve:

1) The device layers are stacked using face-to-back (F2B) die-stacking strategy because it is the most commonly used configuration, and also doesn't limit the number of device layers that can be stacked
2) The number of stacked device layers assumed in our analysis is limited to four. This is because with the increasing device layers beyond four, the total wirelength saturates or increases slightly [83].
3) Each device layer has its own dedicated metal stack. The number of metal layers and its properties are the same for individual device layers [3].
4) The wires spanning to multiple consecutive device layers have one TSV between consecutive device layers.
5) We used Cu-based via-middle TSVs that occupy silicon area only on the upper device layer for connections between consecutive device layers. Cu-based via-

middle TSVs were used because of their superior performance and established manufacturing.

6) Modern ASIC designs are arranged in the fixed-outline context, where the layout area, routing area and tracks are fixed before floorplanning begins. Hence, during floorplanning, the blocks and TSV islands are packed within a fixed-outline region [77], with the maximum allowed whitespace of 15% and aspect ratio of 1.0. The fixed area is defined by total area of the blocks and allowable whitespace. The optimum chip area (*chip_optiarea*) is the summation of area of blocks and TSVs. The packing area (*chip_packarea*) is calculated by the *chip_w*chip_h*nlayer,* where *chip_w* and *chip_h* represents the width and height of the minimum rectangle that encloses the blocks and TSVs. The *chip_w* and *chip_h* is the maximum value of all the device layers represented as *nlayer*. The packing efficiency of a floorplan is represented as the ratio of *chip_optiarea* and *chip_packarea*.

7) The specifications of original and expanded GSRC benchmark circuits used in our experiments are reported in Table 2. The table shows the different test cases used for analysis, the total block area and the total nets for the original and expanded benchmark circuits. We have chosen n100, n200 and n300 circuits for comparison with the existing approaches for floorplanning. The other floorplanning benchmarks like MCNC circuits are old and outdated. As VLSI chips grow in size and complexity, large-scale placement is becoming essential to achieve multiple

design objectives. Hence, we expanded the benchmark circuits by increasing the size of each block by 100 times and included additional multi-pin nets.

Table 2: Specification of Modified GSRC Benchmark Circuit

Test Case		Total Block Area		Total Nets	
Original	Expanded	Original	Expanded	Original	Expanded
n100	n100_exp	0.176 mm^2	17.64 mm^2	885	885
n200	n200_exp	0.187 mm^2	18.67mm^2	1585	2136
n300	n300_exp	0.273 mm^2	27.32 mm^2	1892	2914

2.7 Strategy for data generation

In this section, we will describe the steps for evaluation and optimization of area, wirelength, delay, power and coupling noise using the developed floorplanning tool. The data reported in the results sections are obtained on the final best fit floorplan. In order to obtain the optimized floorplan, the flow diagram of evolutionary algorithm illustrated in Figure 7 is described below.

- **Inputs:** In addition to the typical floorplanning inputs such as list of blocks and nets, we also include TSV, wire and buffer specifications. TSV dimensions are needed to allocate sufficient space on the layouts for TSV islands, and to give a more accurate estimation of the chip area. Whereas, the RC parameters of the wires, TSV and buffers are required during the floorplanning iterations only when the delay, power or coupling noise are included in the cost function.
- **Random floorplan generation:** The floorplanning begins with an initial set (population) of randomly generated floorplans. Our experiments are then

performed with the population size of 20. The number of floorplans generated at every iteration is twice of the initial population. Then, the best 20 floorplans are selected after evaluating the cost function.

- **Floorplan Perturbation:** At every iteration, each floorplan is perturbed by randomly selecting one move from a set of pre-defined moves like *swap, invert, rotate, exchange*, and *change group*. These moves were included in the initial software inherited from [37]. In addition, move involving the random swapping of nets between TSV islands have been introduced. The probabilities of all the moves changes dynamically during different stages of floorplanning based on the quality of generated floorplans as it proceeds toward convergence.
- **Evaluating Cost Function:** In every generation of evolutionary algorithm, the cost function for each floorplan is evaluated. The set of floorplans with minimized weighted cost function are selected at each iteration. The cost function will also help to rank the layouts in the order of better fitness or performance. The order of layouts may change depending on the parameters minimized in the cost function. An in-depth comparison between three different floorplanning cost functions is presented in this thesis. Designers often require during early design exploration, to identify and estimate the trade-offs between the various performance parameters such us delay, power, and coupling noise. Choosing an appropriate cost function, which can guide the 3D floorplanner in a way that the targeted objectives are minimized, facilitates this decision. Consequently, the value of the weights

assigned to each objective in the cost function can result in a major influence on the quality or the "goodness" of the floorplan. As there is no definitive way to determine the weights, they are usually chosen based on experimental results on different types of floorplanning problems.

As shown in Table 3, we have used three different cost functions – *CF1, CF2* and *CF3*. For the cost function CF3, we have assigned different weights to the parameters, and classified the cost function as *CF3a, CF3b, CF3c and CF3d*. The existing studies [16-18] use various functions to minimize area, wirelength and TSV count during floorplanning stage. These studies have not included the delay or coupling noise in the cost function in their approaches, which results in floorplans with inferior performance. We replaced the wirelength and number of TSVs with the total delay in the cost function named *CF2*. Lastly, in cost function *CF3*, we included the coupling noise parameter to explore the influence of the combined interaction between delay and coupling noise parameters on optimizing the delay and coupling noise of the final floorplan. This interaction is important because both the parameters are dependent on the large capacitive effects of TSVs assigned to a wire, which is performed simultaneously with the nets-to-TSVs assignment during floorplanning. We experimented with the following range of weights - *a)* α between *0.05* to *1.0*, *b)* β between *1* to *50*, *c)* ρ between *10* to *100*, and *d)* δ between *10* to *100*. However, for the purpose of comparison, Table 3 shows the cost functions used in this thesis and the

associated weights values, which have minimized the average value of the parameters.

Table 3: Cost functions used and associated weight values

Cost Function	Expression	Best Weights			
		α	β	ρ	δ
CF1	Area + α*WL + β*TSV	0.2	10	-	-
CF2	Area + ρ*Delay	-	-	100	-
CF3a	Area + ρ*Delay + δ*Coup	-	-	80	20
CF3b	Area + ρ*Delay + δ*Coup	-	-	50	50
CF3c	Area + ρ*Delay + δ*Coup	-	-	20	80
CF3d	Area + ρ*Delay + δ*Coup	-	-	0	100

- **Termination Criteria:** The evolutionary algorithm terminates if the number of iterations exceeds the maximum number of iterations defined as the input to floorplanning algorithm. Also, the algorithm terminates if the chip area meets the fixed-outline constraint and the fitness (cost) function remains constant for certain number of iterations. In our experiments, the maximum number of iterations for a floorplanning run is 50000.

After termination of floorplanning algorithm, the best fit floorplan is selected from a set of floorplans, as the final 3D layout. The chip area, total wirelength, number of TSVs, delay, power and coupling noise are estimated based on the arrangement of blocks and TSV islands, and nets-to-TSVs assignment on the final floorplan, as shown in Figure 8. The 3D chip area is the maximum area of all the device layers, which is defined by the minimum rectangular region enclosing all the blocks on each device layer. During

floorplanning, the wirelength is estimated using the widely-used net-splitting method by Li et al [17]. Each 3D net is split into subnets based on the pin location on device layers and assigned TSVs within islands. The total wirelength is the summation of HPWL of all subnets. Total number of TSVs in the design are computed by the summation of TSVs required for each net. Since, the total wirelength and total number of TSVs will depend on the arrangement of blocks and TSVs, we execute 25 runs of floorplanning algorithm. The total wirelength and total number of TSVs estimated on the final floorplan of each run are reported in chapter 3.

Prior to performing buffer insertion on the final floorplan, TSVs' and wire RC parasitics are computed. However, RC values of the wires will depend on the interconnect density on each device layers, and will be influenced by the position of blocks and TSV islands on the floorplan. Therefore, we evaluate the interconnect density across stacked device layers on the final 3D layout. A TSV-aware buffer insertion scheme is utilized for the 3D layouts which have uniform wire density on all the device layers, and the resulting buffer count, delay and power estimated on the final floorplan is reported in chapter 5. For 3D floorplans with nonuniform wire density across stacked device layers, a wire capacitance-aware buffer insertion scheme is applied on the final floorplan to minimize power and performance.

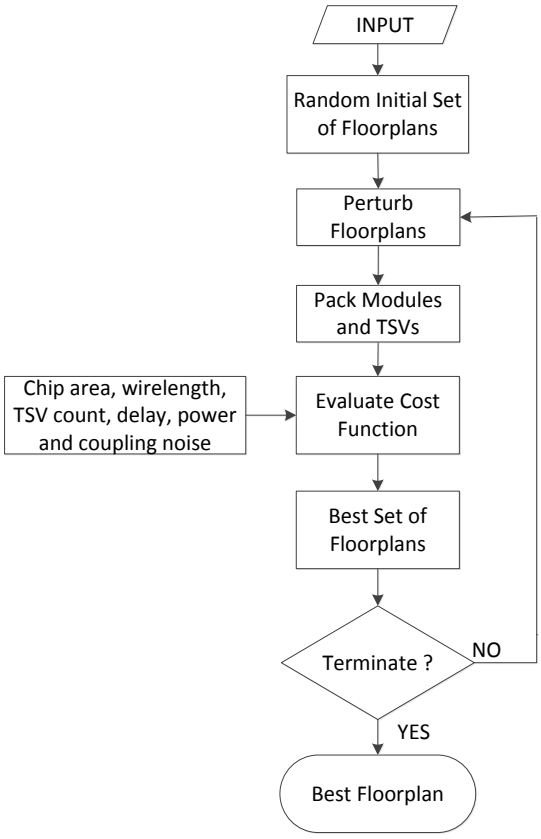


Figure 7: General flow diagram for achieving optimized 3D floorplan with minimized weighted cost function

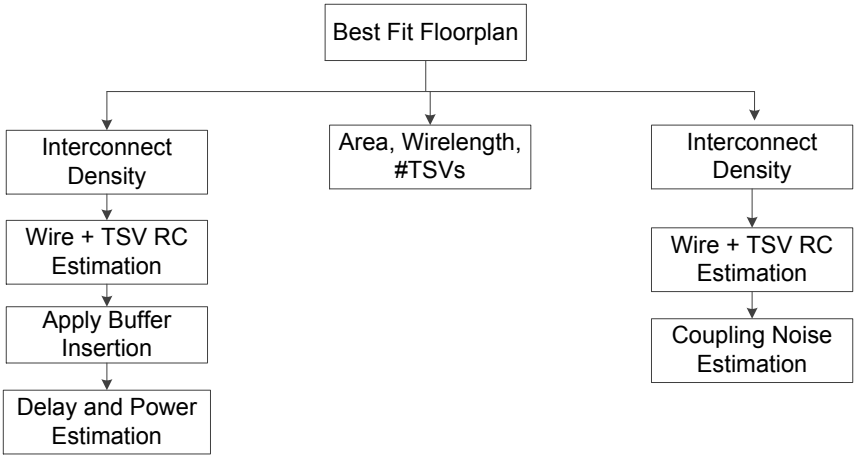


Figure 8: Steps of evolutionary algorithm with different cost functions

3. TSV- and delay-aware 3D Floorplanning

The size of TSV is very large compared to logic gates and other circuit components at 45nm. Therefore, to eliminate the impact of TSV thermo-mechanical stress on the devices, some space needs to be reserved around TSVs, this space is known as Keep-Out-Zone (KOZ). The thermo-mechanical stress induced by TSVs impacts the carrier mobility and threshold voltage in nearby devices [14][15] as well as in the TSV. The TSVs may also impact in the performance and reliability of 3D ICs. The size of KOZ is different for analog and digital circuit, and depends on the TSV dimensions. The stress interaction due to multiple TSVs increases the size of KOZ. The KOZ is also essential to minimize TSV-to-TSV coupling capacitance that may greatly impact the performance of 3D interconnects [3]. Hence, TSV count is crucial to minimize area overhead, which will also help optimize the wirelength. Also, it is important to accurately estimate the size of the KOZ to be able to better evaluate and optimize the performance in 3D circuits.

Moreover, TSV introduces placement and routing obstacles. The nets-to-TSVs assignment is also critical to achieve short wirelength. The wirelength in 3D circuits also depends on TSVs arrangement on the layout. TSVs also introduce delay in the nets. The delay due to TSV also depends on the length of the wire. It is not advisable to use too many TSVs for a small circuit, as it may increase the total delay in a 3D circuit. Hence, the balancing of weight functions between TSVs and wirelength is critical to be able to achieve an optimized delay in the interconnects. The separate minimization of wirelength

and TSVs may not result in lowest delay values. Given these considerations, a TSV-aware 3D floorplanning is quite challenging and needs considerable attention.

In this chapter, we present a TSV and delay-aware 3D non-deterministic floorplanning tool, TSV-DAF, with co-placement of circuit blocks with TSV islands. Through iterations, 3D nets are assigned to TSVs, and delay of interconnects, which is one of the components of the cost function, is evaluated using RC parameters of wires and TSVs. The proposed delay-aware approach effectively models the TSV RC delay impact on the delay of a net and hence, helps to guide the nets-to-TSV assignment during floorplanning. To counter the effect of TSV-induced stress and TSV-to-TSV coupling, we include appropriate TSV pitch and KOZ.

3.1 Previous Works

Several prior 3D floorplanning tools had completely ignored the impact of TSV size and position on chip area and wirelength [6-9]. However, further studies have confirmed that not including physical sizes of TSVs during 3D floorplanning results in significant errors in estimating area, and ignoring TSVs position will result in underestimation of wirelength [17-18]. In this section, we briefly describe the methodology of TSV aware floorplanning algorithm used in some recent publications [16-18] [37]. The results of these specific studies have been used in comparison with our proposed approach. In [37], the experiments were done on gate-level netlists to optimize gate positions and included

intra-block wirelength. Since, no floorplanning benchmarks were used. There is no way to compare our results with theirs.

In [16], Knechtel et al. considered TSV placement after 3D floorplanning of blocks. They use a uniform grid structure to facilitate TSV island insertion by computing available deadspace. A grid tile is selected for island insertion only if unobstructed i.e., has a certain minimum available deadspace. Next, cluster of nets spanning all unobstructed tile are identified for island insertion, depending on the available deadspace to each cluster and the number of nets linked to the cluster. However, this limits the solution as the grid tiles with less deadspace than the minimum criteria are ignored for island insertion. Also, in case a net cluster spans an obstructed tile, deadspace needs to be shared by clusters, which may affect solution quality. They also propose deadspace-channel insertion for additional space for TSV island insertion, which would be problematic with fixed outline constraints. They considered arranging TSVs in islands, but did not account for delay contribution of TSV in the formulation of their TSV assignment problem during 3D floorplanning.

Tsai et al. [17] proposed a two-stage simulated annealing based floorplanning and used available whitespace to place TSV blocks. First, TSV blocks are created within available whitespaces and then nets are assigned to TSVs for wirelength minimization. To further reduce wirelength in the second stage, the algorithm deterministically reassigns TSVs among the TSV blocks on the final floorplan. Although this results in a compact area

floorplan, the nets-to-TSVs assignment done for fixed final floorplan does not effectively minimize the wirelength.

Li et al. [18] proposed co-placement of TSVs with circuit blocks and fulfilling fixed outline constraints. To reduce the complexity of the problem and the runtime of the algorithm they use a partitioning algorithm to permanently assign blocks to device layers and to minimize the number of TSVs.

3.2 3D Floorplanning Flow

The 3D floorplanning is a critical phase during which the positions of blocks and placement topology of TSVs need to be performed simultaneously as it influences the overall system performance. 3D floorplanning offers an early possibility of evaluating the design with different TSV technologies, dimensions and placement topology, providing more reliable solutions with better performance. This section will describe the key components included in the floorplanning tool developed by R.K. Nain [37][84][87] that are essential for accurate prediction and better optimization of performance in 3D circuits. These components are (i) co-placement of blocks and TSVs, (ii) nets-to-TSVs assignment, (iii) delay-aware cost function.

3.2.1 Co-placement of Blocks and TSVs

The primary concern during co-placement of blocks and TSVs is to obtain a good estimation of the area occupied by TSVs defined by TSV arrangement. Physical

arrangement of TSVs during layout design may have significant impact on the circuit performance, power, yield and reliability. Spreading isolated TSVs throughout the layout may be effective in reducing wirelength as TSVs can be placed closed to blocks. However, the thermo-mechanical stress associated with TSVs influences the carrier mobility and threshold voltage in the adjacent devices. Hence, placing TSVs very close to the blocks should be avoided. The arrangement of TSVs inside the islands offers more reliable solutions as the devices are not adjacent to TSVs. Also, the islands allow redundancy by shifting the connection from failed TSV to neighboring good TSV without increasing the wirelength. However, additional multiplexers required to shift the signal will increase the area. Moreover, for heterogeneous integration, TSVs inside the islands can be assigned different values of pitch on individual device layer.

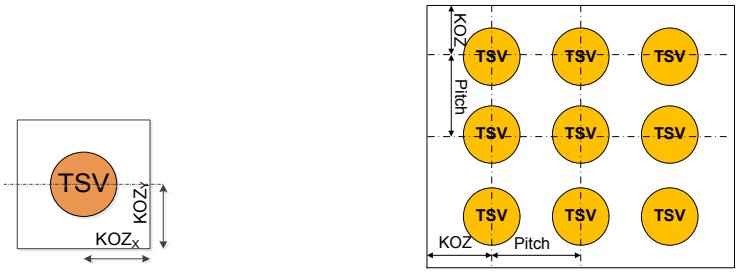


Figure 9: Layout and space occupied by (a) isolated-TSV (b) 3x3 TSV Island

Furthermore, TSVs are separated by desired pitch also result in smaller average footprint per TSV compared to isolated TSVs. The area of an island with TSV array of *mxn* is given by $[(m-1)*Pitch+2KOZ_x]\left[(n-1)*Pitch+2KOZ_y\right]$, where $KOZ_x$and KOZ_y will depend on *m* and *n* respectively. The footprint per TSV is computed by dividing the total area of the islands by the number of TSVs inside the islands. As the

dimension of the TSV array increases, the footprint per TSV reduces greatly as shown in Table 4. For this analysis, we have used TSV diameter as 3µm[1] to show the impact of TSV pitch and KOZ on the area, which was ignored in [17] [18]. This is primarily due to sharing of KOZ between TSVs. The KOZ around TSVs in islands is 20%-27% larger than the isolated TSV due to cumulative interaction of TSV stress. But, still the TSV arranged in islands result in smaller footprint per TSV. However, for small number of TSVs in the design, the individual TSVs may be preferable. It can be observed that the area occupied by each island on the layout increases on the other hand, which may introduce routing obstacles. In order to ensure better packing efficiency, the size of the island must be of the order of average size of circuit block. For the designs, where the size of the blocks varies significantly, the TSV count will determine the optimized size of the islands.

Table 4: KOZ, area per TSV and TSV island area for different TSV array inside islands (TSV diameter=3µm and pitch=6µm)

TSV array inside Islands	Desired KOZ	Area per TSV	Area of TSV Island
1x1	4.8µm	92.16µm^2	92.16µm^2
2x2	5.3µm	49.44µm^2	213.16µm^2
3x3	5.7µm	38.44µm^2	345.96µm^2
4x4	6.1µm	34.31µm^2	547.56µm^2
5x5	6.3µm	30.03µm^2	750.76µm^2
6x6	6.4µm	26.35µm^2	948.64µm^2
7x7	6.5µm	23.87µm^2	1169.64µm^2
8x8	6.5µm	22.09µm^2	1413.76µm^2
9x9	6.5µm	20.55µm^2	1664.64µm^2
10x10	6.5µm	19.36µm^2	1936.4µm^2

[1] The floorplanning approaches discussed in [17][18] used TSV diameter as 3µm and TSV pitch and KOZ was not included for estimation of TSV area

Due to significantly smaller footprint per TSV, we arranged TSVs in islands for the proper separation and desired KOZ. We have assumed 8 islands on each device layer, so that the typical array size of islands is between 7x7 to 10x10 or the set of three GSRC benchmarks used in this analysis. This range of TSV island sizes results in a smaller average area per TSV and the total island area is of the order of average block area in the tested benchmark circuits, resulting in better packing efficiency. The total area of each TSV island will depend on the number of TSVs in each island and the size of desired KOZ. The estimation of the number of TSVs in a 3D circuit is achieved by using a probabilistic method. After TSV count is estimated, TSVs are uniformly distributed to each island. The desired KOZ is estimated for all the islands based on the given TSV dimensions and TSV array size.

3.2.1.1 Probabilistic Estimation of TSV count

The estimation of TSV count in a 3D circuit is require for computing TSV array size inside each island. The probabilistic method is based on the assumption that each net might require from zero to n-number of device-layers minus one TSVs and compute the number of TSVs required for the net based on a probabilistic model using locations of net pins. The model considers each multi-pin net and the probability of TSVs contributed by each net. The number of TSVs required by a particular net depends on the number of pins in the net and the number of device layers considered.

Let's assume that there are N_{nets} nets, and each net has *npin* number of pins. The blocks are placed on *n_layer* device layers, and there could be only one TSV for a multi-pin net spanning two consecutive layers. The probability of zero TSV needed for N_{nets} is given by Eq. (1).

$$P(0\_TSV) = {}^{1}/_{(n\_layer)^{(npin-1)}} \quad (1)$$

Hence, the probability of a net requiring at least one TSV, *P (n_TSV)*, is given by the following equation (Eq. (2)).

$$P(n\_TSV) = 1 - P(0\_TSV) \quad (2)$$

The probability of one TSV, *P (1_TSV)*, and two TSVs, *P (2_TSV)* depending on the number of pins for the net is estimated using Eq. (3) and Eq. (4) respectively.

$$P(1\_TSV) = P(n\_TSV) * {}^{1}/_{(n\_layer-1)^{(npin-1)}} \quad (3)$$

$$P(2\_TSV) = P(n\_TSV) * \left(1 - {}^{1}/_{(n\_layer-1)^{(npin-1)}}\right) \quad (4)$$

Similarly, the probability of n-TSVs required by each net may be estimated. The maximum number of TSVs required by a net will also depend on the number of layers in the design. The total number of TSVs (N_{TSV_tot}) in the design is estimated using Eq. (5), where N_{2pin}, N_{3pin},…. N_{npin} represents the number of nets with 2 pins, 3pins and so on.

$$N_{TSV\_tot} = N_{2pin} * P(n\_TSV) + N_{3pin} * P(n\_TSV) + \cdots N_{npin} * P(n\_TSV) \quad (5)$$

3.2.1.2 Area of TSV Island

After estimating the capacity of TSV islands, the area occupied by an island on the layout is computed. We have assumed that the TSVs inside the islands are separated by constant pitch as shown in Figure 9. The minimum TSV pitch assumed in our experiments is twice of TSV diameter as per ITRS [3] guidelines. Next, we estimate the required KOZ around TSV islands to avoid placement of blocks and other TSV islands in close proximity. Hence, an accurate estimate of the required KOZ is essential to minimize the impact of TSV stress as well as area overhead due to TSVs. We use look-up-table for obtaining KOZ for given TSV array size and TSV dimensions, computed using analytical model [14] [15].

3.2.2 Nets-to-TSVs Assignment

We incorporated a novel nets-to-TSVs assignment procedure within the 3D floorplanning flow. The net assignment procedure begins only after the benchmark area reaches a desired percentage of the minimum size. In the beginning of the floorplan run, the netlist is divided into '*k*' subgroups. The number of net sub-groups is equal to the number of islands on each device layer, and is fixed at the beginning of the floorplanning process. Next, for each net sub-group, a TSV island is reserved on each but zero device layers.

During net-movement, two net subgroups are randomly selected for swapping of nets. Next, a fixed-size window is used to randomly select subsets of nets in both net subgroups. The randomly selected subsets of nets are swapped between the two sub-

groups, which means that now these swapped nets will be assigned to opposite TSV islands. It has to be noted that during the net movement, the position of the circuit blocks does not change during the iteration.

Figure 10 illustrates the impact of random net moves in wirelength estimation. An example of a two-pin net n (p1, p2) is shown in the figure. For the net to span between Layer #1 and Layer #0 requires a single TSV. Figure 10 (b) shows that after the random move, the net gets assigned to a TSV island situated on the same device layer but allocated to net subgroup 2 (GR2). As can be observed, the movement of nets impacts the wirelength of the net and hence the delay estimation for the net, whereas the number of TSV assigned to the net remains unchanged as the net pin-locations do not change

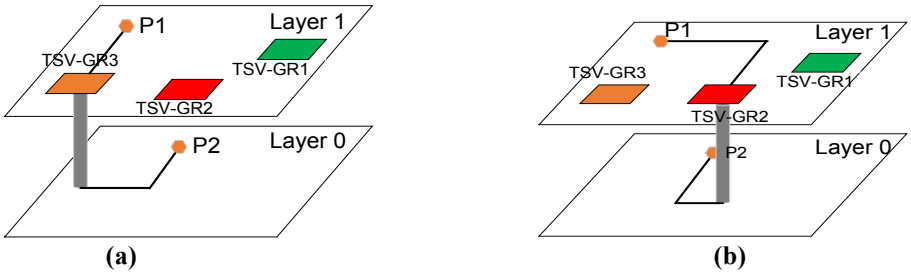


Figure 10: Example of impact of random net moves while estimating the wirelength. The net requires a single TSV to span between Layer #1 and Layer #0, (a) Before Net Movement—n (p1, p2) belongs to net subgroup 3 (GR3), and (b) After Net Movement n (p1, p2) belongs to net subgroup 2 (GR2)

The inclusion of random net movements during floorplanning helps significantly increase the sample search space and improves the solution quality as compared to fixed nets-to-TSVs assignment. The probability of net-movements decreases with increasing number of iterations during floorplanning. The non-deterministic nets-to-TSVs assignment significantly reduces the wirelength compared to the approach where net-to-

TSVs assignment is fixed through all the floorplanning iterations. The co-placement of TSVs and islands and non-deterministic nets-to-TSVs assignment results in better delay in the 3D circuits compared to exact approach like max-flow min-cost algorithm [17][18] and greedy grid-based approach [16] used on the final floorplan.

3.2.3 Delay-aware 3D Floorplanning

The conventional floorplanning focuses on optimizing the wirelength and the number of TSVs separately. However, the separate minimization of wirelength and TSVs does not account for the variable impact of TSVs on the delay of a wire as shown in Figure 11. It can be observed that the impact of TSVs on the overall delay of a wire is much larger on shorter nets, increasing the delay by three times. However, as the length of the wire increases, the impact of TSV on the wire delay saturates. Therefore, it is essential to model the impact of TSV on the delay in the individual nets during floorplanning to optimize the position of blocks and TSVs on the layout and guide the nets-to-TSVs assignment. The delay modeling in individual nets is described in the following section.

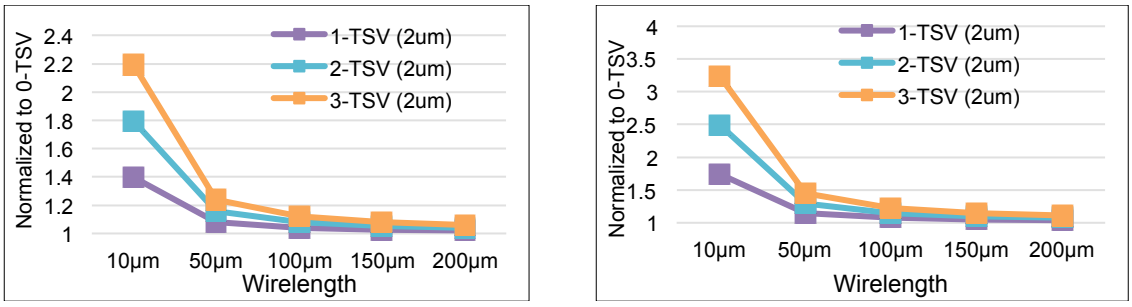


Figure 11: The delay in the wire of given length with the 1 TSV, 2 TSVs or 3 TSVs with diameter of 2µm normalized to the delay in the net without TSV (a) TSV aspect ratio 10:1, (b) TSV aspect ratio 20:1

3.2.3.1 Net Delay Model

In this section, a fast and computationally efficient Elmore net delay model is presented, which is used to guide our delay aware 3D floorplanning. The equivalent Elmore delay model for 3D wires is shown in Figure 12. The figure illustrates the TSV delay contribution on net delay. The RC parameters of a TSV and wire are represented as R_{TSV}, C_{TSV}, R_{wire} and C_{wire} respectively. The number of layers in the design may greatly impact the influence of TSVs on the delay. As the number of layer increase, shorter wirelength and more TSVs may cause TSV delay to dominate.

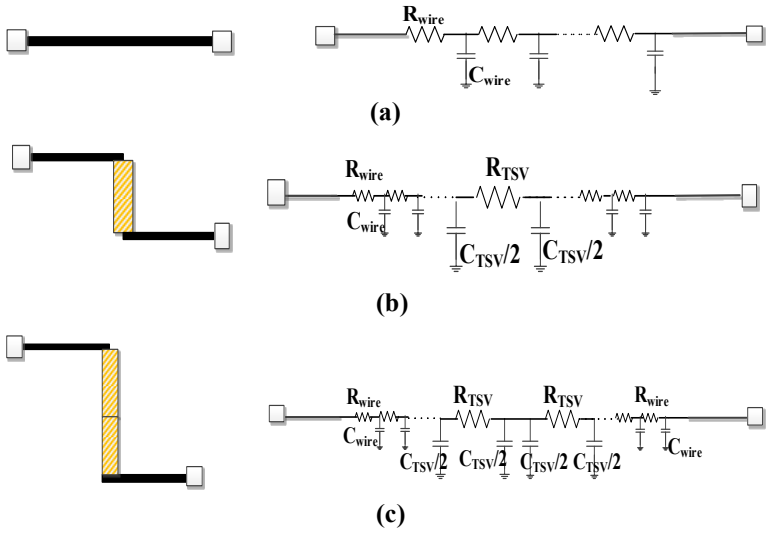


Figure 12: Elmore Delay net model (a) wire without TSV, (b) with 1-TSV, (c) with 2-TSV

The delay in individual nets is computed using Eq. (6), which is obtained by replacing the TSV with its equivalent wirelength. The delay in each net is computed after nets-to-TSVs assignment and evaluated at each iteration by using delay-aware cost function.

$$Net\ Delay = \frac{1}{2} R_{wire} C_{wire} L_{wire}^2 + \frac{1}{2} R_{TSV} C_{TSV} N_{TSV}^2 \quad (6)$$

3.2.3.2 Delay-aware Cost Function

The cost function guides the floorplanning algorithm to achieve layouts with optimized desired parameters. In the proposed approach, we introduce a total delay term, which is the summation of delay in each net, in the cost function (*CF2)* as shown in Eq. (8). The delay in individual nets is computed after performing the buffer insertion, which will be discussed in chapter 5. The delay term assists the floorplanning algorithm in monitoring the influence of TSVs on the delay in the wire. This ensures that the placement of blocks and TSV islands, as well as nets-to-TSVs assignment minimizes the overall delay in the circuit.

CF1 is a wirelength-aware cost function that has two separate components to optimize delay performance: wirelength (*WL*) and the total number of TSVs (N_{TSV}), hence, it does not optimize delay directly. *CF2* is a delay-aware cost function that optimizes directly the total delay of the design. Parameters α, β, and ρ are weights assigned to the given cost metrics in each function. The delay of each net is calculated based on its wirelength and the number of included TSVs. Both parameters are optimized simultaneously through the delay objective. There is no need for a trial-and-error process to find good weight values for the wirelength and the number of TSVs components (α, and β respectively) as it is necessary in cost function *CF1*.

$$CF1 = Area + \alpha * WL + \beta * N_{TSV} \quad (7)$$

$$CF2 = Area + \rho * Total\ Delay \quad (8)$$

3.3 Experimental Results

Our experiments were performed on a 4xDual Core Sun SPARC IV CPUs at 1.35 GHz and total 32 GB RAM. The general assumption and strategy for data generation is described in section 2.6 and 2.7. The input specifications like TSV diameter, pitch and KOZ are kept similar for the comparison with the existing approaches in [16], [17] and [18].

3.3.1 Statistical Analysis of CF1

In this section, we present statistical analysis of the wirelength and number of TSVs estimated on the final floorplan obtained using CF1 as the cost function during floorplanning. The primary objective of this cost function is to minimize chip area, wirelength, and number of TSVs in the design. The weight functions assigned to wirelength and number of TSVs are $\alpha = 0.2$, and $\beta = 10$ respectively. We consider the average of 25 floorplanning runs for the estimation of the total wirelength and number of TSVs on the final floorplan.

Figure 13(a)-(d) show the histogram plots for wirelength and number of TSVs computed on the final floorplan of n100 and n200 circuits. It can be observed that the mean wirelength for n100 and n200 is 127.93 mm and 248.38 mm respectively. We computed the coefficient of variation (CV) to measure the dispersion in the wirelength that represents the amount of variability relative to the mean. The CV ranges between 2% to 3% for the wirelength and 3% to 4% for the number of TSVs in the benchmark

circuits. From this analysis, we can conclude that the average value of the wirelength and number of TSVs are good approximations to use for comparison with existing floorplanning approaches discussed in [16][17][18]. This is because of the small coefficients of variation in the distribution of wirelength and the number of TSVs.

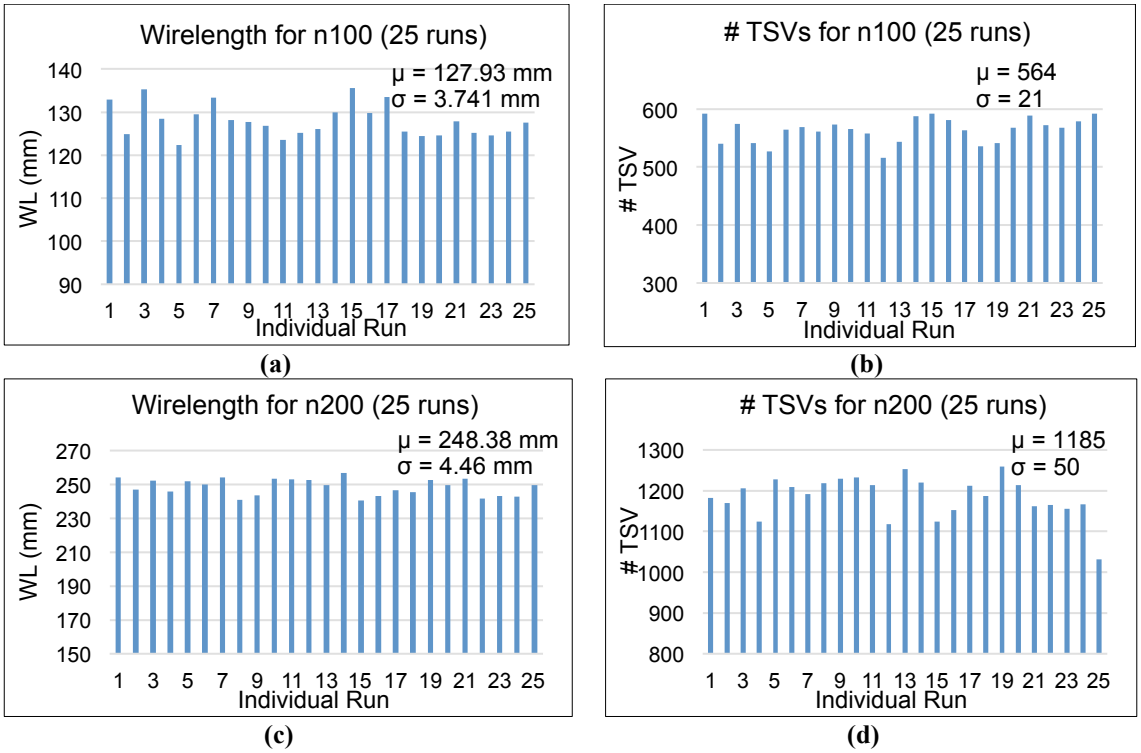


Figure 13: Parameters estimated on the final floorplan after 25 runs with TSV diameter 2μm (a) Total wirelength for n100, (b) Number of TSVs in n100, (c) total wirelength of n200, (d) number of TSVs in n200

3.3.2 Comparison with Existing Approaches

Table 5 compares our floorplanning results using *CF1* with Knechtel *et al* [16]. We consider best results generated by their algorithm using dead spaces for TSV insertion. They concluded that their other methods do not have enough whitespace at the desired

places for placing TSVs. It resulted in longer wirelength compared to deadspace insertion method. For fair comparison, we introduce the same TSV pitch (10μm) in TSV islands, for each case of TSV footprint. As shown in Table 5, compared to [16] we achieve on an average 5% reduction in wirelength and 21% lesser TSVs.

Table 6 compares our results generated using *CF1* with Tsai *et al* [17] and Li *et al* [18]. For fair comparison with both the cases, we do not include pitch nor KOZ in islands. In [17] the wirelength is a summation of width, height and depth of a 3D bounding box of all pins and center of TSV islands. The depth is the sum of height (20 μm) of all tiers within the 3D bounding box. For fair comparison with our wirelength model, wirelength for [17] is estimated considering tier height as zero. The wirelength for Tsai *et al*. reported in Table 6 is estimated by subtracting depth of each TSV from total wirelength reported in [17]. Our non-deterministic approach for nets-to-TSVs assignment results in 3% to 9% average reduction in wirelength compared to deterministic (max-flow min-cost) approach used in [17] [18].

As discussed earlier, the coefficient of variance for wirelength ranges between 2%-3%, and hence, the longest wirelength generated by floorplanning tool will still be slightly better than the existing approaches. Our floorplanning tool uses significantly lesser TSVs and 3%-4% variation in TSV count will not impact the quality of generated solution.

Table 5: Comparison of wirelength, TSV with Knechtel et. al. [16]

TSV Footprint	Layers	Circuit	Knechtel [2]		TSV-DAF	
			TSV	*WL (mm)*	*TSV*	*WL (mm)*
$2\mu m^2$	3-layer	n100	534	125.26	407	122.49
		n200	1034	254.76	855	237.42
		n300	1480	349.77	1026	348.89
			1.0	1.0	0.76	0.97
	4-layer	n100	654	113.88	464	112.90
		n200	1182	235.54	1152	232.64
		n300	1597	312.76	1512	321.09
			1.0	1.0	0.88	1.001
$4\mu m^2$	3-layer	n100	539	130.36	378	128.20
		n200	1038	288.97	825	267.49
		n300	1425	361.89	1045	359.44
			1.0	1.0	0.74	0.97
	4-layer	n100	652	116.96	532	116.91
		n200	2257	407.53	1158	248.57
		n300	1569	341.54	1515	330.12
			1.0	1.0	0.76	0.86
Normalized			1.0	1.0	0.79	0.95

Table 6: Comparison of wirelength, TSVs with Tsai et al. [17] and Li et al. [18]

Layers		Tsai [17]		Li [18]		TSV-DAF	
		TSV	*WL (mm)*	*TSV*	*WL (mm)*	*TSV*	*WL (mm)*
3	n100	833	144.1	505	146.1	412	132.41
	n200	1509	280.7	1043	266.4	798	245.77
	n300	1899	386.6	1244	380.6	1162	368.07
Normalized		1.0	1.0	0.65	0.98	0.54	0.91
4	n100	1171	125.3	677	133.9	523	123.71
	n200	2179	247.5	1572	250.8	1144	234.39
	n300	2730	337	1758	350.9	1544	332.72
Normalized		1.0	1.0	0.64	1.04	0.51	0.97
Avg. Normalized		1.0	1.0	0.65	1.01	0.53	0.94

We compared the runtime of each benchmark circuit using our floorplanning algorithm with the existing approaches in Figure 14. The deterministic algorithm by Li [18] results in least runtime and is independent of the size of benchmark circuits. With the increase in problem size, the runtime of non-deterministic algorithms by Knechtel [16] and Tsai [17]

increases by 5x compared to our (TSV-DAF) approach. Please note that the runtime of existing approaches is taken from [16] [17] [18] and absolute comparison is not possible as the algorithms are implemented on CPU with different hardware configurations.

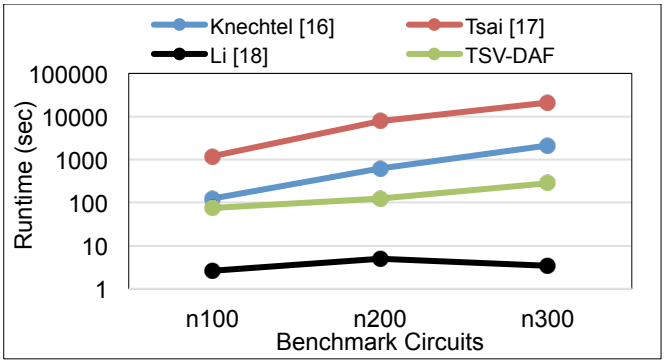


Figure 14: Runtime comparison of different floorplanning approaches

We did not compare our delay results with previous floorplanning approaches [16-18], because they do not include the electrical characteristics of wires and TSVs. Our delay values are the sum of individual net delay based on wirelength and TSVs used for each net. Hence, it is difficult to predict the total delay in absence of wirelength distribution and TSVs used for each net in these works.

The total delay obtained on the final floorplan using our approach was compared using *CF1* and *CF2,* and is shown in Table 7. To compute the delay in the nets, we have used the Elmore model, which consists of wire and TSV delay, as shown in Figure 12. In Table 7, we reported only the best delay values obtained on the final floorplan, and respective wirelength and number of TSVs for each circuit. We have used three values for each weight function, $\alpha = (0.1, 0.5, 1.0)$, $\beta = (5, 20, 50)$, and $\gamma = (10, 50, 100)$. It can

be observed that *CF2* obviates the need to balance the weights between wirelength and TSVs, resulting in reduced delay in the circuits on an average by 13%. In case of n100 circuits, despite longer wirelength with CF2, the total interconnect delay is much smaller compared to *CF1*. This is because of better distribution of TSVs to wires of shorter length to minimize the impact of TSV on the delay in the wires.

Table 7: Comparison of the total delay obtained on the final floorplan of benchmark circuits with CF1 and CF2 for TSV diameter 2µm and contact resistance 10Ω

Test Case	Wirelength-Aware (CF1)				Delay-Aware FP (CF2)			
	# TSV	WL (mm)	Delay (ps)	Runtime (s)	# TSV	WL (µm)	Delay (ps)	Runtime (s)
n100	404	118.89	912	75.85	400	120.28	833	72.15
n200	807	238.45	1739	122.5	906	230.98	1648	123.75
n300	929	351.73	3287	278.6	1104	329.58	2492	275.5

3.4 Summary

Based on the results from the proposed TSV- and delay aware floorplanning tool, which co-places TSV islands with circuit blocks and uses delay as one of the optimization objectives, it can be observed that total delay of systems can be better optimized than when wirelength and the number of TSVs are optimized as separate components of the cost function in wirelength-aware tools. It obviates the efforts required to balance the weight contributions of wirelength and TSVs in the wirelength aware floorplanning. The wirelength-aware floorplanning requires careful selection of appropriate weights in cost function to achieve good delay value.

The delay-aware floorplanning also allows capturing variable impact of TSVs on wires of the different length. It was observed that the total delay depends on the wirelength distribution and the number of TSVs assigned to individual nets. In our experiments, with a given range of physical dimensions and electrical parameters of wires and TSVs, the total delay is largely influenced by wirelength, whereas TSVs contribute only 2–3% to the reduction in total delay. The better distribution of TSVs to wires of different length is achieved by incorporating delay in the cost function CF2. The cost function CF1 with separate TSV and wirelength terms requires a balance cost function to achieve smaller delay. However, the delay in cost function CF2 combines both the term reducing the trade-off. Since, the number of TSVs have quadratic impact on the delay, the delay optimization reduces TSVs greatly. The statistical analysis shows that the coefficient of variance in the wirelength and TSV distributions after 25 runs is 3% and 4% respectively.

4. Electrical Characteristics of TSV

The main challenge with TSV parasitics is to achieve a low TSV capacitance. TSV capacitance is typically of the order of tens of femto (F) [43-46]. The existing extraction and analysis tools need to be extended for 3D ICs. These tools must include RLC parasitics for TSVs in the analysis. TSV capacitance consists of two coupling components, 1) TSV-to-TSV, and 2) TSV-to-wire. These components depend on TSV pitch, TSV and wire dimensions and spatial distribution of surrounding TSVs and wires. The use of field solvers and simulations may not be advisable for estimating TSV capacitance during floorplanning due to timing overhead of these methods. The look-up tables will need many variables to compute TSV capacitance resulting in complexity issues. Moreover, the impact of TSV on the delay in interconnects also depend on the wire delay. For a shorter wire, TSV delay will constitute a larger percentage of interconnect delay. Hence, it is critical to accurately model the delay in the wires to predict the performance of the 3D circuits. In this chapter, we modified the TSV-to-wire coupling component of the analytical model for TSV capacitance developed by Kim et. al [46].

The basic electrical characteristics of TSVs such as resistance, capacitance and inductance have been discussed earlier in the literature [43] [44] [45]. These simulations based approaches are accurate, but the computation intensive, making them unsuitable for full chip analysis and design optimization. Moreover, they ignored the critical impact of depletion capacitance surrounding the TSV dielectrics. Kim et al. [46] proposed an

analytical model for fast computation of TSV capacitance. But, the analytical model used for computation of TSV-to-wire capacitance is not suitable for smaller wire and TSV dimensions. Therefore, the model does not provide good results as TSV dimensions scale down. The compact AC models proposed in [78][79] computes TSV capacitance considering 2-TSV model. A Poisson equation based model [80] takes into account the depletion capacitance, but assumes coupling between two TSVs only. In [60] [61][62], a new multi-TSV model for TSV capacitance is proposed that considers the effects of silicon depletion region, silicon substrate and E-field distribution with neighboring wires and TSVs.

4.1 TSV Capacitance

In this section, we will present the modified TSV capacitance model based on the existing work by Kim et al [46]. In the improved TSV capacitance model, we modified coupling TSV-to-wire (C_{TW}) component from Kim's model, while TSV-to-TSV (C_{TT}) and fringe capacitance are kept the same. As discussed previously, the existing model [46] is not scalable to smaller TSV and wire dimensions. The scaling of TSV and wire dimensions primarily impacts the TSV-to-wire coupling capacitance. Therefore, we focus on improving the scalability of TSV-to-wire coupling component. The magnitude of TSV-to-wire coupling depends on the TSV technology. The via-middle TSVs have coupling with adjacent TSVs and wires on the top and bottom of TSVs. While, via-last TSVs have coupling with adjacent TSVs and wires on the top, bottom and also sides of

TSVs. TSV-to-TSV coupling capacitance includes the effects of silicon substrate and depletion region. TSVs in the islands are separated by sufficient pitch, and hence we ignore the impact of coupling with the non-neighboring TSVs. We ignored the impact of TSV liner in our analysis. The two components of coupling capacitance and RC model [46] for via-middle technology are shown in Figure 15.

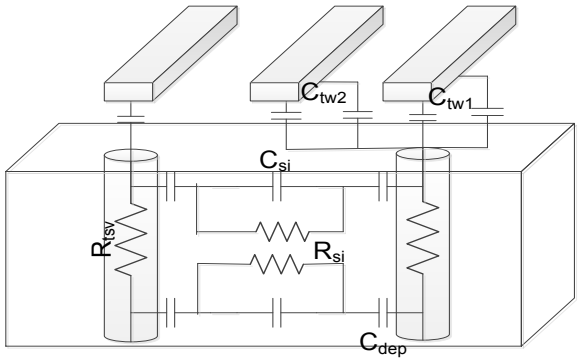


Figure 15: Simplified TSV RC model for via-middle TSVs [46]

4.1.1 Overview of Capacitive Components for Via-Middle TSV [46]

The different components of TSV coupling with wire (C_{TW}) are shown in Figure 16 (a). They are categorized based on the different surfaces exposed to TSV.

1. C_{top1} is the capacitance between the top surface of a TSV and wires on top of the TSV represented by $C_{area\ 1}$ in Figure 16 (a).
2. C_{top2} is the capacitance between a sidewall of the TSV and outside wires connected to wires on top of TSV, represented by $C_{fri\ 1}$ in Figure 16 (a).
3. C_{side1} is the capacitance between sidewall of TSVs and side wires, represented by $C_{fri\ 2}$ in Figure 16 (a).

4. C_{side2} is the capacitance between a sidewall of the TSV and side wires in non-overlapped regions, represented as $C_{fri\ 3}$ in Figure 16 (a).

The component of TSV-to-TSV coupling (C_{TT}) capacitance has two components as shown in Figure 16 (b).

a) C_{c1} is between TSV and adjacent horizontal and vertical TSVs.

b) C_{c2} is between TSV and adjacent diagonal TSVs.

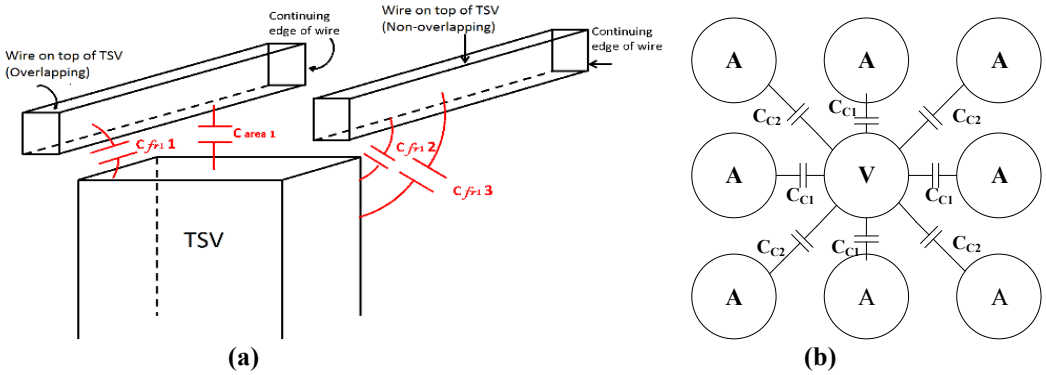


Figure 16: Coupling capacitance between (a) TSV-to-wire (C_{TW}) (b) TSV-to-TSV (C_{TT}) [46]

4.1.2 Multiple Wires on Ground Plane

3D-IC has multiple wires over the TSV cross-section, where TSV is considered as ground planes. The capacitance consists of area-capacitance between the bottom surface of wire and top surface of ground plane; fringe-capacitance between a sidewall of the wire and top surface of ground plane as shown in Figure 17.

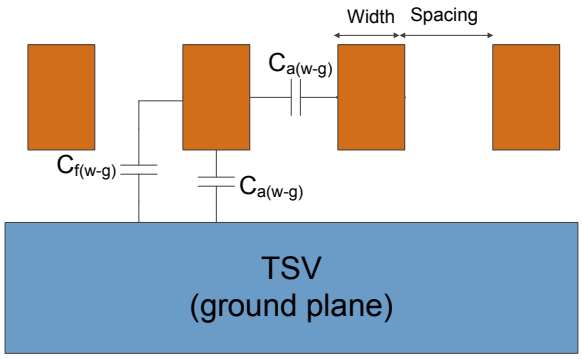


Figure 17: Capacitance of multiple wires on TSV (ground plane) [46]

Kim et al. have used Sakurai-Tamaru model [47], shown in Eq. (9), for estimation of C_{TW} capacitive component, which exist between TSV and adjacent wires. Where, C represents the capacitance per unit length, W is the width of the wire, S is spacing between wires, T represents the thickness of the wire, and H is the height of the wire or thickness of dielectric layer.

$$C_{a(w-g)} = \varepsilon\left\{1.15\left(\frac{W}{H}\right)\right\}, C_{f(w-g)} = \varepsilon\left\{2.80\left(\frac{T}{H}\right)^{0.222}\right\},$$

$$C_{a(w-w)} = \varepsilon\left\{2\left[0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{H}{S}\right)^{1.34}\right\}$$

$$C_{w-g} = C_{a(w-g)} + 2 * C_{f(w-g)} - C_{a(w-w)} \quad (9)$$

Sakurai's model has been widely used due to its simplicity and accuracy, but is only applicable for metal lines on one plane and does not generate good results for multi-level interconnect architectures. The other existing methods are not suitable, either due to large computational time or limited to single line on the ground plane. Wu at el. [48]

proposed an empirical model, shown in Eq. (10) for multilevel interconnect architectures, suitable for smaller width and spacing. A description of various components of TSV capacitance can be found in Appendix B.2.

$$C_{a(w-g)} = \varepsilon\left\{\left(\frac{W}{H}\right)\right\},\ C_{f(w-g)} = \varepsilon\left\{2.977\left(\frac{T}{H}\right)^{0.232}\right\},$$

$$C_{a(w-w)} = \varepsilon\left[0.229\left(\frac{W}{S}\right) + 1.227\left(\frac{T}{S}\right)^{1.384}\right]\left(\frac{S}{H}\right)^{-0.0398}$$

$$C_{w-g} = C_{a(w-g)} + 2 * C_{f(w-g)} - C_{a(w-w)} \quad (10)$$

The empirical model proposed by Wu et al. is based on the process dimensional parameters. It provides capacitance variation based on process parameters with high computational efficiency for circuit simulations. The empirical model shows close correlation with simulation results from RAPHAEL as shown in Figure 18, for wide range of wire width and spacing [48].

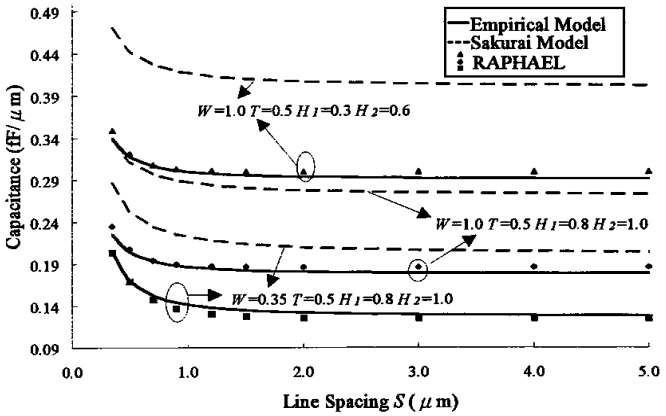


Figure 18: Capacitance of wires with given dimensions computed using of Empirical Model [48], Sakurai Model [47] and Synopsys RAPHAEL simulator (figure taken from [48])

4.1.3 Fringe Capacitance [46]

The formula for fringe capacitance between two wires is taken from [46]. C_{sw_top} is the capacitance per unit length between the sidewall of the upper wire and the top surface of the lower wire given by Eq. (11). C_{top_top} is the capacitance per unit length between the top surfaces of the upper and lower wires, and computed using Eq. (12). C_{corner} the capacitance per unit length between the two corners of the wire given by Eq. (13).

$$C_{sw\_top} = \frac{\varepsilon_{di}}{\pi/_2} ln\left[\frac{H+\rho T+\sqrt{S^2+(\rho T)^2+2H\rho T}}{S+H}\right] \quad (11)$$

$$C_{top\_top} = \frac{\varepsilon_{di} W\alpha\left(ln\left[1+{}^{W}/_{S}\right]+e^{-\frac{S+T}{3s}}\right)}{W\pi\alpha+(H+T)\left(ln\left[1+{}^{W}/_{S}\right]+e^{-\frac{S+T}{3s}}\right)} \quad (12)$$

$$C_{corner} = \frac{\varepsilon_{di}}{\pi}\sqrt{{}^{HS}/_{(H^2+S^2)}} \quad (13)$$

4.2 Via-Middle TSV Capacitance Modeling

In this section, we will present the modeling of TSV coupling with top and bottom wires, and neighboring TSVs. The variable settings for each component of the capacitance are described in Appendix B.2 (Table B.2.1).

4.2.1 Modeling C_{top1}

C_{top1} is the capacitance between the top surface of TSV and the wires overlapping with the top surface of a TSV. C_{top1} is computed using Eq. (14), where N_w represents the number of wires routed on the top of TSV [46].

$$C_{top1} = N_w(C_{a(w-g)} + 2C_{f(w-g)}) \quad (14)$$

4.2.2 Modeling C_{top2}

C_{top2} is the capacitance between the sidewall of TSV and the non-overlapping wires with the TSV top surface. C_{top2} is computed using Eq. (15), where N_w represents the number of wires routed on the top of TSV [46].

$$C_{fr\_2} = C_{f(w-g)} * W$$

$$C_{s1} = C_{sw\_top} * {S_{TSV}}/{2}, \quad C_{s2} = C_{sw\_top} * {S_w}/{2}, \; C_{fr\_3} = C_{s1} || C_{s2}$$

$$C_{top1} = N_w(C_{fr\_2} + 2C_{fr\_3}) \quad (15)$$

4.2.3 Modeling C_{side1}

C_{side1} is the capacitance between TSV sidewall and wires in the side of TSV. C_{side1} is computed using Eq. (16), where $M_w$represents the number of wires routed in the side of TSV [46].

$$C_{side1} = \sum_{m=1}^{M_w}\left(C_{sw\_top} * W_{TSV} + C_{sw\_top} * W_{TSV}\right) \quad (16)$$

4.2.4 Modeling C_{side2}

C_{side2} [46] is the capacitance between TSV sidewall and wires in the side of TSV, which are in non-overlapped regions. C_{side2} is computed using Eq. (17), where M_w represents the number of wires routed on the side of TSV. $C_{fr\_6}(m)$ is the coupling capacitance between the bottom side of the wire and the facing sidewall of the TSV, $C_{fr\_7}(m)$ and is the coupling capacitance between sidewalls of the wire and the facing sidewall of the TSV.

$$C_{s3} = C_{sw\_top} * W,\ C_{s4}(m) = C_{sw_{top}}(m) * {}^{S_{TSV}}/_{2},\ C_{fr\_6}(m) = C_{s3}||C_{s4}(m)$$

$$C_{s5} = C_{sw\_top} * {}^{S_{TSV}}/_{2}\ ,\ C_{s6} = C_{sw\_top} * S_w,\ C_{s7}(m) = C_{sw_{top}}(m) * {}^{S_{TSV}}/_{2}$$

$$C_{fr\_7}(m) = C_{s5}||C_{s6}||C_{s7}(m)$$

$$C_{side2} = \sum_{m=1}^{M_w}\left(C_{fr_6}(m) + C_{fr\_7}(m)\right) \quad (17)$$

4.2.4 Modeling C_{TT}

As discussed previous, TSV-to-TSV coupling [46] consists of two components. The coupling with sidewall of the TSVs is represented by C_{c1}, and computed using Eq. (18), where L_{fr_1} is the effective length impacting fringe capacitance of a TSV. The coupling with the corner of the TSVs is represented by C_{c2}, and given by Eq. (19). The constant K_{corner} is computed empirically given by Eq. (20).

$$C_{c1} = \varepsilon_{di}\,{}^{(H_{TSV} - 2L_{fr_1})}\Big/_{S_{TSV}} \quad (18)$$

$$C_{c2} = {}^{\varepsilon_{di}}/_{\pi\sqrt{2}} H_{TSV} K_{corner} \quad (19)$$

$$K_{corner} = \frac{1}{2}\frac{H_{TSV}}{S_{TSV}} \qquad (\text{If } {}^{H_{TSV}}/_{S_{TSV}} \leq 4.0)$$

$$= 2.0 \qquad (\text{If } {}^{H_{TSV}}/_{S_{TSV}} \geq 4.0) \quad (20)$$

Hence, TSV-to-TSV coupling for a TSV in the middle of array as shown in Figure 16 (b) is given by Eq. (21).

$$C_{TT} = 4(C_{c1} + C_{c2}) \quad (21)$$

4.3 TSV Resistance

The TSV resistance includes two components - (i) material resistance (R_{mat}) (ii) TSV contact resistance (R_{con}) between the TSV and the landing pad at both ends of TSV. The material resistance is dependent on resistivity of the TSV filling material and TSV dimensions (height and width). The typical TSV resistance ranges from tens of milliohms to hundreds of milliohms given by Eq. 22, where ρ represents the resistivity of the material, H_{TSV} is the length or height of TSV and A_{TSV} is the area of TSV. In this work, a cylindrical TSV is used, as it more reliable and easy to fabricate, therefore, TSV area is defined as $\pi(D/2)^2$, where D is the diameter of TSV.

$$R_{TSV} = {}^{\rho H_{TSV}}/_{A_{TSV}} \tag{22}$$

The TSV contact resistance is dependent on the TSV manufacturing and bonding technology. Okoro et al. [49] reported simulated mean resistance of defect-free 60 TSV daisy chain as 8.4 Ω. Kuo et al. [50] discussed that the coupling between TSV and the substrate contact is dominant due to direct connection through the bulk silicon substrate without any depletion region, resulting in TSV contact resistance around 38.5 Ω. Xu et. al [51] adopted four-point probe test to measure via resistance and contact resistance. Their test results show that a TSV with no defects has resistance of 4.74 Ω. Yang et. al [52] discussed that the effective contact resistance may reach 1600 Ω depending on substrate doping concentration. As the doping concentration of substrate decreases, the metal-silicon contact resistance increases. As the material resistance of TSV is significantly

smaller than contact resistance, we assume TSV resistance to be roughly equivalent to the value of contact resistance for our experiments. The range of TSV contact resistance used in this work is typically between 1Ω - 40Ω.

4.4 Experimental Results

The capacitance of via-last and via-middle TSV computed using Kim's and our model are presented in Table 8 and 9. TSV capacitance using Kim's model and Raphael simulations for given TSV dimensions are taken from [46]. Raphael simulator is a 2D and 3D field solver providing the most parasitic models in the industry. It considers the effect of electrical and thermal phenomena in multi-level interconnect structures. Its features two- and three-dimensional interconnect capacitance computation by the boundary element method. For via-last TSVs, there is an additional parameter (D_{min}), which defines the minimum spacing between a metal wire and a TSV. As via-last TSVs has more coupling with wire due to the presence of wires on the side of TSV, our model results in better accuracy. From the tables, can be seen that modified model estimates TSV capacitance more accurately especially for smaller TSV dimensions, reducing peak error from 6.03% to 2.6%.

Table 8: Comparison of via-last TSV capacitance with Kim et. al [46] and Synopsys Raphael simulations [46]

TSV dimension (μm)			D_{min}	TSV Capacitance (fF)		
Width	Spacing	Height		Raphael [46]	Kim's Model [46]	Modified Model
5	5	5	0.5	8.055	8.572 (6.03%)	8.232 (2.2%)
		20	1.0	16.280	15.570 (-4.36%)	16.367 (0.53%)
		50	2.0	33.751	35.115 (4.04%)	34.042 (-0.56%)
		100	2.0	64.799	67.581 (4.29%)	64.539 (-0.4%)

Table 9: Comparison of via-middle TSV capacitance with Kim et. al [46] and Synopsys Raphael simulations [46]

TSV dimension (μm)			TSV Capacitance (fF)		
Width	Spacing	Height	Raphael [46]	Kim's Model [46]	Modified Model
5	5	5	8.868	9.389 (5.88%)	8.629 (-2.6%)
		20	18.336	19.102 (4.18%)	18.524 (1.88%)
		50	37.033	37.129 (0.26%)	36.822 (-0.56%)
		100	68.227	67.174 (-1.54%)	67.319 (-1.33%)
	10	20	15.706	15.939 (1.48%)	15.833 (0.8%)
		50	27.984	29.615 (5.83%)	28.664 (2.4%)
		100	48.437	49.310 (1.78%)	48.807 (0.76%)
10	10	100	82.570	82.689(0.14%)	82.526(-0.05%)
		50	51.392	52.644(2.44%)	51.562(0.3%)
		20	32.645	32.752(0.33%)	32.798(0.46%)

4.5 Summary

TSV capacitance depends significantly on the spatial distribution of wire and TSVs on the layout. TSV coupling with the wires in lateral and vertical directions has significant impact on the TSV capacitance. TSV height greatly impacts the TSV-to-TSV coupling capacitance as shown in Table 8 and 9, and hence, wafer thinning is important to minimize TSV height. TSV pitch is also critical for minimizing TSV-to-TSV coupling,

reducing TSV capacitance by up to 24% when TSV pitch is increased 2x as shown in Table 9.

5. Delay and Power in buffered 3D Interconnects

Traditionally, buffer insertion in VLSI ICs has been the preferred technique to linearize the dependence of delay on interconnects' length, fix slew and noise violations while also reducing power in 2D ICs. However, unlike 2D ICs, buffer insertion during 3D floorplanning needs careful consideration of several constraints. Firstly, buffers occupy finite area and cannot interfere with TSV positions or circuit blocks on the layout. In addition, the buffers contribute non-negligible delay and capacitance, which unavoidably impacts the net delay and power. Instead of post-layout interconnect optimization, buffer planning should be done in early design phase, so that the optimized number and location of buffers is known upfront such that the timing constraint can be met [54]. Furthermore, for early design exploration it is essential to understand the impact of buffers on the power, performance and area of the chip.

In this chapter, we present methods for prediction of delay and power in buffered interconnects during floorplanning accounting for TSV area, position and its RC parasitics. The buffer insertion takes place on the final layout. A novel buffer insertion scheme is proposed, where the distance between adjacent buffers for individual nets vary depending on TSV delay and number of TSVs used. Our buffer scheme also incorporates buffer insertion around TSV considering TSV position on the wire to minimize signal degradation across TSVs. We also perform buffer insertion after nets-to-TSVs assignment at each iteration to improve the overall performance of 3D circuits.

5.1 Previous Work

Some of the recent works have considered the impact of TSV during buffer planning. Dong *et al* [53] proposed a simultaneous interlayer via and buffer planning algorithm at the floorplanning stage. The buffer insertion problem is reduced to a dynamic programming path problem. However, they ignore the significant impact of TSV RC parasitics on net delay. Therefore, the estimated delay in their approach is too optimistic and limited in accuracy. He *et al* [54] considered buffer insertion along with TSV insertion in available whitespaces. However, their whitespace re-distribution approach to improve the interlayer via allocation and buffer insertion rate could degrade total wirelength and overall packing. Also, they ignore the TSV RC delay impact on net delay. Lee *et al* [55] discussed an accurate model for estimating delay in buffered 3D interconnects.

Kim *et al* [38] considered the impact of TSV RC delay in 3D buffered interconnects. They applied a fixed-distance buffer insertion scheme for each 3D net which may not yield optimal results of buffer estimate. Although, they considered TSVs as obstacles during buffer insertion, they did not consider the actual TSV locations along the wire during buffer insertion. This may limit the accuracy of estimated buffers per net and therefore the delay of the net. The authors also ignore the significant capacitive coupling between adjacent TSVs in their TSV capacitance model, therefore, further limiting the accuracy of estimated interconnect delay. Their 3D wirelength prediction ignores the non-negligible TSV area. Hence their predicted wirelength and buffer count may be too

optimistic. In [56] the authors consider TSV-area aware wirelength distribution models and apply a buffer insertion algorithm based on dynamic programming. However, buffer insertion is not performed simultaneously with TSV assignment. This may lead to violation of TSV positions during buffer allocation and complications during the global/detailed routing stages.

5.2 Buffer Planning for 3D ICs

The buffer insertion for a 3D interconnect is performed on the final 3D layout in two phases. In the first phase, the buffers are inserted on the wire from driver side to receiver, at a fix distance defined by buffer insertion length *(BIL)*. BIL is optimized for individual nets considering the delay due to TSVs. In the second phase, optimal buffer planning around TSVs is performed in order to achieve minimized signal degradation.

5.2.1 Variable Buffer Insertion Length (BIL)

As discussed earlier, the simplistic method of inserting buffers at a fixed length interval in 2D wires, cannot be directly applied to 3D wires. This is because the presence of TSVs will impact the buffer insertion in 3D wires in two ways. First, for the purpose of buffer insertion a wire of equivalent length cannot replace a TSV as the buffer cannot be placed on a TSV. Second, larger RC delay component introduced by a TSV in a 3D wire will require buffer planning around TSVs to minimize the signal degradation across multiple device layers. Therefore, an optimal buffer insertion approach has to account for the non-

negligible TSV RC delay impact on wire delay. This will help to optimize the distance between consecutive buffers (*BIL*), improving the performance and power in 3D interconnects.

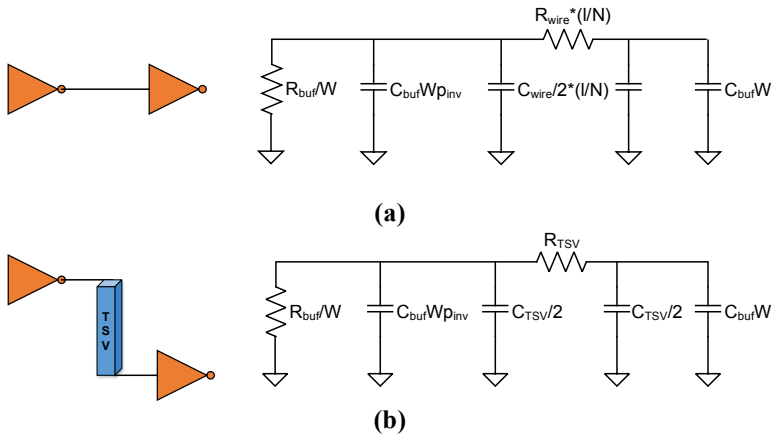


Figure 19: Elmore delay RC equivalent circuit of a single repeated wire segment: (a) 2D wire (b) 3D wire with single TSV

Figure 19 shows the equivalent distributed RC model for a single segment of repeated 2D wire and a 3D wire. For a 2D wire requiring no TSVs, the optimized buffer insertion length (*BIL*) is computed taking into account only the wire RC delay and buffer delay. However, for a 3D wire with TSVs, the presence of TSV parasitics will impact the delay of the buffered net as shown by Elmore delay in Eq. (23).

$$t_{pd} = N\left[\frac{R_{buf}}{W_{buf}}\left(C_{wire}\frac{L_{wire}}{N} + C_{buf} * W_{buf}(1 + p_{inv})\right) + R_{wire}\frac{L_{wire}}{N}\left(\frac{C_{wire}}{2}\frac{L_{wire}}{N} + C_{buf} * W_{buf}\right)\right] + N_{TSV}\left[\frac{R_{buf}}{W_{buf}}\left(C_{TSV} + C_{buf} * W_{buf}(1 + p_{inv})\right) + R_{TSV}\left(\frac{C_{TSV}}{2} + C_{buf} * W_{buf}\right)\right] \quad (23)$$

Where t_{pd} represents the delay of buffered 3D interconnect. 'N' represents the number of repeated segments post buffer insertion. W_{buf} represents the buffer size, 'L_{wire}' represents the length of the wire and N_{TSV} represents the number of TSVs in the wire. The optimized length of wire between buffers (*BIL*) is calculated by differentiating (23) wrt N and W, as shown in Eq. (24). The MATLAB code for obtaining optimized length of the wire between buffers is shown in Appendix.

$$BIL = \sqrt{2\left(C_{buf} * R_{buf} * (p_{inv} + 1) + C * N_{TSV} * R_{TSV}\right) \Big/ R_{wire} C_{wire}} \tag{24}$$

Parameters 'C_{buf}' and 'R_{buf}' represent the input buffer capacitance, and output buffer resistance respectively. R_{TSV} and C_{TSV} represent the TSV resistance, which is the summation of TSV material resistance and contact resistance, and TSV capacitance respectively. C_{wire} and R_{wire} represent the unit-length wire capacitance and resistance respectively. The specific values for all above parameters used in our approach are mentioned in Table 10.

Table 10: Wire, buffer and TSV parameters used for buffer insertion in this work [85] [86]

Parameter / Assumption		Value / Range
	Device Technology	45 nm
R_{wire}	Unit length wire resistance M4-M6	0.29-0.66 Ω/μm
C_{wire}	Unit length wire capacitance M4-M6	0.20-0.21 fF/μm
R_{buf}	Buffer output resistance (8x)	300 Ω
C_{buf}	Buffer input capacitance (8x)	6.585 fF
R_c	TSV Contact Resistance	10-40 Ω
V_{DD}	Supply Voltage	0.9 V
f	Frequency (GHz)	2.0
p_{inv}	Parasitic Capacitance Factor	0.5
P_{buf}	Dynamic Buffer Power (4x)	15.88 μW/GHz
	Dynamic Buffer Power (8x)	31.15 μW/GHz
	Dynamic Buffer Power (16x)	62.24 μW/GHz
	Dynamic Buffer Power (32x)	122.91 μW/GHz
	Buffer Load Capacitance	0.3656 fF
	Buffer Input Transition	0.0012 ns

As shown in Figure 20, the optimum buffer insertion length in presence of TSVs in a 3D net would be larger compared to a 2D wire with no TSVs, reducing required buffer count. Since the buffers inserted incur delay in the wire, the presence of additional delay element as TSV in Eq. (24) should reduce the buffers to minimize delay. For given buffer size and wire dimensions, the buffer insertion length for a net is independent of length of the wire and depends on the RC parasitics of TSV and required number of TSVs.

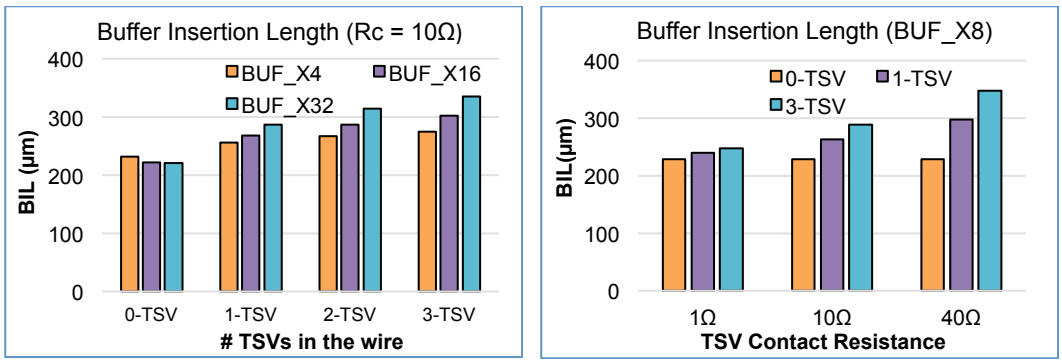


Figure 20: Influence of # TSV on the BIL (a) with buffer sizes, (b) with TSV contact resistance

5.3 Buffer Insertion around TSVs (TSV-BIS)

After Phase-I of buffer insertion at optimized BIL for individual nets, the goal of Phase-II is to achieve optimal buffer planning around TSV in order to minimize signal degradation across the TSV. Therefore, using the known TSV position (x, y coordinates) along the wire, we determine the ideal position of the buffer to minimize overall delay in the TSV segment. As shown in Figure 21 (a), after phase I, the remaining length of the wire segment before known TSV position is represented as L_{rem_TSV}, while the remaining length after TSV position is represented as $(BIL - L_{rem\_TSV})$. In order to account for TSV delay, we defined the equivalent wire due to TSV in Eq. (25). A buffer is inserted in front of TSV if condition in Eq. (26) is satisfied. Similarly, a buffer is inserted at the end of TSV if Eq. (27) is satisfied. For the scenarios where both the conditions are satisfied, a buffer is inserted on both the sides of TSV.

$$TSV_{wire} = N_{tsv}\sqrt{R_{tsv} * C_{tsv}/R_{wire} * C_{wire}} \quad (25)$$

$$L_{rem\_TSV} + TSV_{wire} \geq BIL \quad (26)$$

$$TSV_{wire} + \left(BIL - L_{rem_{TSV}}\right) \geq BIL \quad (27)$$

In Figure 21 (b), we present a scenario where the condition in Eq. (27) is satisfied, and hence a buffer is inserted at the end of TSV. The buffer in front of TSV is not needed and must be avoided, as it will further deteriorate the signal strength.

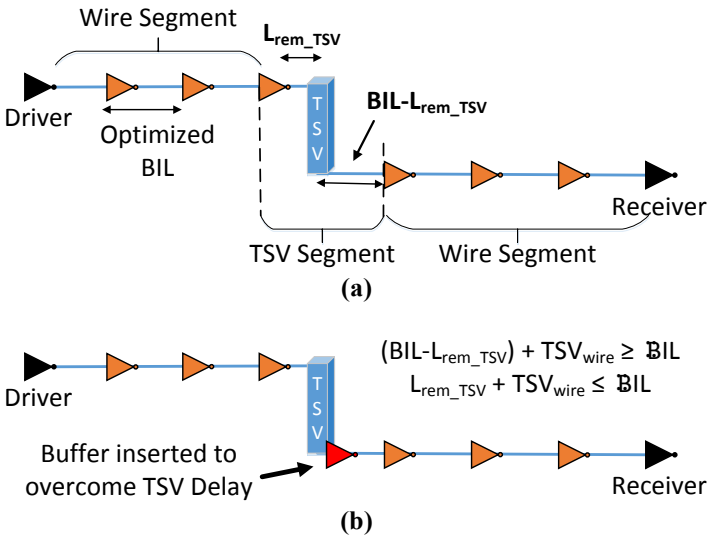


Figure 21 (a) 3D net after Phase-I of buffer insertion at optimized BIL (b) 3D nets after Phase-II of buffer insertion around TSVs (buffer in front of TSVs is not needed)

We demonstrate the importance of considering TSV position during buffer planning around TSVs, considering an example of a net with one TSV and *BIL* equal to 300µm. Figure 22 shows the delay in TSV segment for different positions of TSV on the wire using three buffer insertion techniques. BIS1 and BIS2 proposed by Kim et al. [38] refers to a scheme of buffer planning around TSV, where buffer is always inserted before TSV in BIS1; while a buffer is added both before and after the TSV in BIS2. TSV-BIS represents our TSV-position aware buffer insertion technique, where buffer is inserted

either in front or after TSVs. TSV has a diameter of 3µm (AR=10:1), and a contact resistance of 10Ω.

The horizontal axis defines the position of TSV on the wire represented as L_{rem_TSV}, and the vertical axis shows the delay in TSV segment. It can be seen that TSV-BIS technique results in least delay irrespective of position of TSV on the wire segment. The delay in TSV segment reduces by a maximum of 9%. It should also be noted the delay in TSV segment also changes with the position of TSV on the wire. The delay in a buffered segment with BIL of 300µm is around 27.98ps. If buffers are not inserted around TSVs, the delay in TSV segment may rise to about 41ps. BIS1 and BIS2 help to reduce the overall delay in TSV segment, but it largely depends on the position of TSV. For length of wire segment (L_{rem_TSV}) equal to 10µm, the reduction in delay achieved using BIS1 and BIS2 is around 8.7%. Whereas, TSV-BIS reduces the delay in TSV segment by 18% - 19% for given range $0 < L_{rem\_TSV} < BIL$.

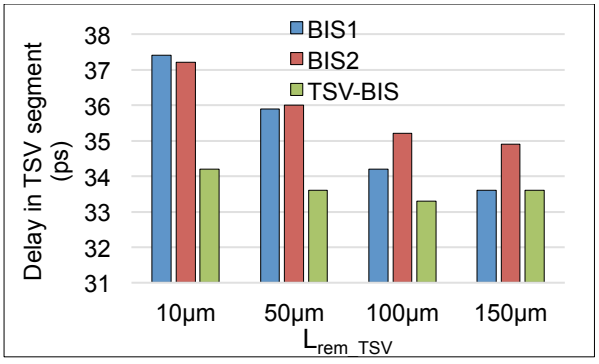


Figure 22: Comparison of delay in TSV segment using different buffer insertion techniques, BIS1 (in-front), BIS2 (both ends), TSV-BIS (Either in-front or end) for TSV contact resistance of 10Ω

5.4 Experimental Results

In this section, the proposed buffer insertion technique and its impact on the delay and power in interconnects of GSRC benchmark circuits is presented. The experiments related to variable buffer insertion length and buffer planning around TSVs are performed on the final floorplan. The final floorplan is achieved by minimizing chip area, wirelength and number of TSVs in the cost function. The weight function of these parameters is kept the same as in previous chapter. Whereas, for performance optimization during floorplanning, the total delay of buffered interconnect is included in the cost function. Hence, the buffer insertion is performed simultaneously with nets-to-TSVs assignment, and increases the floorplanning runtime by around 22%.

5.4.1 Variable Buffer Insertion Length

In this section, we will evaluate the effectiveness of using variable BIL on the final 3D floorplan in improving the evaluation of power and performance of 3D ICs. Table 11 compares the buffer count, total delay and power consumption in interconnects using *fixed-BIL* and *variable-BIL* for three different sizes of buffers. In the *fixed-BIL* method, 2D and 3D interconnects are treated the same and buffers are inserted at identical distance. It can be seen in Table 11 that the *variable-BIL* becomes really effective in minimizing buffers compared to *fixed-BIL*, as the buffer size increases. With increase in value of 'R_{buf}', *BIL* also increases. Although, the delay of each buffered segment increases, the number of buffered segments '*N*' reduces simultaneously, therefore

reducing the buffer count. Hence, the delay of interconnects remains largely unchanged. The capacitance of big-size buffers introduces significant power consumption in interconnects. The *variable-BIL* reduces power consumption by up to 12%, which may play critical role due to high power density in 3D circuits. Moreover, as the TSV contact resistance increases from 10Ω to 40Ω, the number of buffers using variable-BIL decreases further, keeping the total delay very similar.

Table 11: Buffer, Delay and Power comparison for fixed and variable BIL with TSV contact resistance of 10Ω & 40Ω and frequency of 2GHz

	Circuit	BUF_X8			BUF_X16			BUF_X32		
		Fix-BIL	Var-BIL (10Ω)	Var-BIL (40Ω)	Fix-BIL	Var-BIL (10Ω)	Var-BIL (40Ω)	Fix-BIL	Var-BIL (10Ω)	Var-BIL (40Ω)
Buffer Count	n100_exp	6740	6625	6557	7263	7185	7162	7257	7221	7206
	n200_exp	21896	21064	20696	22219	20886	19999	21321	19189	17988
	n300_exp	36293	34935	34319	37332	35029	33729	34453	31007	28927
	Avg.	1.0	0.965	0.954	1.0	0.944	0.929	1.0	0.911	0.892
Delay (ns)	n100_exp	118.1	111.6	118.12	80.59	80.15	80.34	80.26	79.57	79.99
	n200_exp	364.8	362.01	362.48	270.5	267.35	267.8	266.4	262.8	263.5
	n300_exp	651.2	648.82	649.35	460.4	457.8	458.67	460.4	457.5	458.67
	Avg.	1.0	0.995	0.996	1.0	0.990	0.994	1.0	0.986	0.994
Power (mW)	n100_exp	201.9	198.71	197.18	401.8	398.15	396.59	770.8	752.3	736.88
	n200_exp	653.4	631.88	622.27	1231	1167.7	1117.1	2270	2077.4	1928.7
	n300_exp	1082.7	1047.04	1031.4	2067	1959.7	1881.2	3627	3318.7	3105.4
	Avg.	1.0	0.970	0.960	1.0	0.949	0.934	1.0	0.916	0.887

The interconnect power consumption on each device layer (*DL*) for the benchmark circuits is shown in Figure 23. It can be observed that the total interconnect power is primarily due to the buffers, as the wire segment on each device layers are much smaller. The interconnect power due to buffers on each device layer is around 4x of the power consumption in the wires. The power contribution by TSVs is insignificant, but the additional buffers required around TSVs will considerably influence the total power. This

observation further validates the crucial need of optimal buffer planning around TSVs for optimizing the overall performance of 3D ICs.

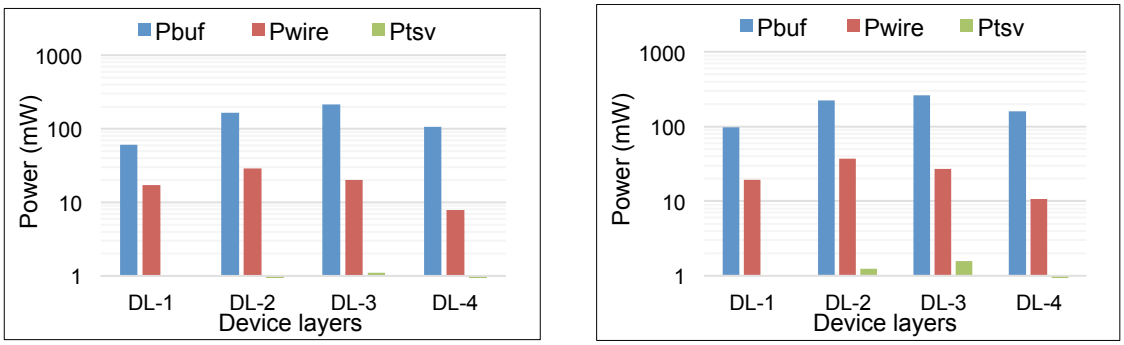


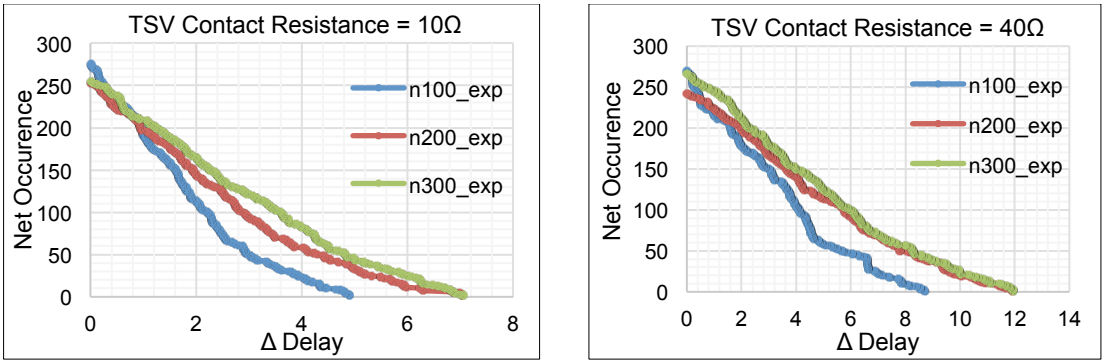
Figure 23: Power due to buffers, wires and TSVs on each device layer using variable BIL for (a) n200_exp (b) n300_exp (BUF_X8 & Rc = 40), and frequency of 2GHz

5.5.2 Buffer Planning around TSVs

The buffer planning around TSVs is critical to minimize signal degradation across between consecutive device layers. We perform the buffer insertion around TSVs after performing phase-I on the final 3D floorplan. We compare our buffer insertion scheme (*TSV-BIS*) with Kim et. al. [38] where a buffer is always inserted in front of TSVs (*BIS1*) on the final floorplan of GSRC benchmarks. We did not include the other buffer insertion technique proposed in [16] where buffers are inserted on both the sides of TSVs, as their assumption is that contact resistance of TSV is 100Ω. The studies [34-36] suggest that the maximum contact resistance of current TSV technology is around 40Ω, and therefore, the use of buffers on both sides of TSVs will be redundant, and further exacerbate the delay.

The distribution of delay in TSV segments with TSV-BIS and BIS1 for 3D nets and TSV contact resistance of 10Ω and 40Ω is shown in Figure 24. The percentage reduction

in delay using TSV-BIS is represented as *ΔDelay*. Our TSV-position aware buffer insertion technique reduces delay across TSV segments by 5%-12% as compared to BIS-1. As TSV contact resistance increases, the percentage reduction in delay using TSV-BIS also increases. TSV-BIS also avoids any violation of the nominal delay, which is defined by the delay in the buffered segment. This technique manages to reduce signal degradation around TSVs with minimal usage of buffers; therefore, also contributing to reducing power consumption in interconnects.



(a) **(b)**

Figure 24: Distribution of delay in TSV segments with TSV-BIS and BIS1 for 3D nets (a) TSV contact resistance 10Ω, (b) TSV contact resistance 40Ω

5.4.2 Delay-aware Cost Function

In this section, we demonstrate the effectiveness of the delay term in the cost function to obtain floorplans with the superior performance. First, we report the total delay in buffered interconnects estimated on the final floorplan of n200 using *CF1* (Eq. (7)) in Figure 25. The weight functions for each parameter are shown in Table 3. The mean and variance of the delay distribution is 97.42 ns and 10.13 ns. The coefficient of variance

(CV) of the delay distribution is around 11%, which is significantly larger than the CV of total wirelength shown in Figure 13 (chapter 3). This is due to the fact that the delay in an individual 3D interconnect is the combined effect of the length of the wire and the number of TSVs, shown in Figure 11 (chapter 3). Hence, although *CF1* is able to achieve minimization of wirelength and number of TSVs separately, it fails to address the combined effect of these parameters towards interconnect delay. It would require a lot of balancing of weights assigned to wirelength and TSV count, in order to achieve the desired delay. It can be concluded that the absence of the delay term in *CF1*, results in significantly larger variation in the delay distribution, hence, may not be suitable to be used for overall performance optimization.

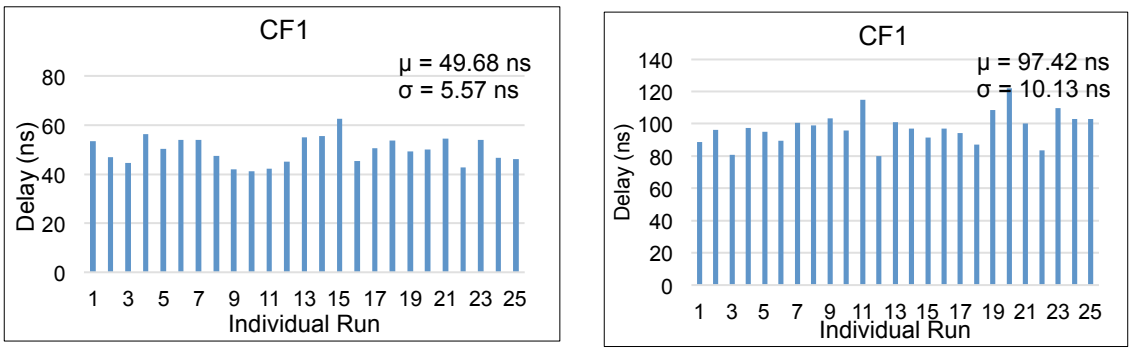


Figure 25: Delay estimated on the final floorplan of n200 circuit for 25 runs on (a) n100, (b) n200, where buffer size is 8x, TSV diameter is 2μm, and TSV contact resistance is 10Ω

In order to account for the crucial impact of TSVs on the wires of different lengths for delay minimization in buffered interconnects, the terms for wirelength and number of TSVs in *CF1* are replaced by the total delay term in *CF2*. The weight (ρ) assigned to the delay term in the *CF2* is 100. The estimated total delay distribution for n200 circuit on

the final floorplan after 25 runs is shown in Figure 26 (a). The dash-line in Figure 26 (a) represents the mean delay obtained with *CF1* after 25 runs, this is used for comparison. It can be observed that each layout achieved using *CF2* has total delay smaller than the mean delay value with *CF1*. The mean delay using *CF2* reduces by 12.3% as compared to *CF1*. The direct inclusion of the delay in the cost function also reduces the CV in the delay distribution to 4.6%. This proves that unlike *CF1*, the *CF2* better guides the assignment of TSVs to a wire, while considering the length of the wire, so that the delay contribution of the TSVs to wire is minimized. No effort is required for balancing the weights for wirelength and TSVs separately, for delay minimization. Also, the variable impact of TSVs on the wires of different length is taken in to account in CF2. The impact of TSVs on the delay of a 3D wire is significantly larger for shorter wires, as shown in Figure 11.

Figure 26 (b) shows the total delay estimated on the final floorplan using *CF1*. In the figure, we compare the total delay of each floorplan using *CF1* with the mean delay value using *CF2* after 25 runs. It can be seen that only 12% (3 out of 25) of the floorplan have better delay values compared to the mean delay using CF2. This means that the probability of achieving floorplan using CF1 with better delay values compared to CF2 is very small.

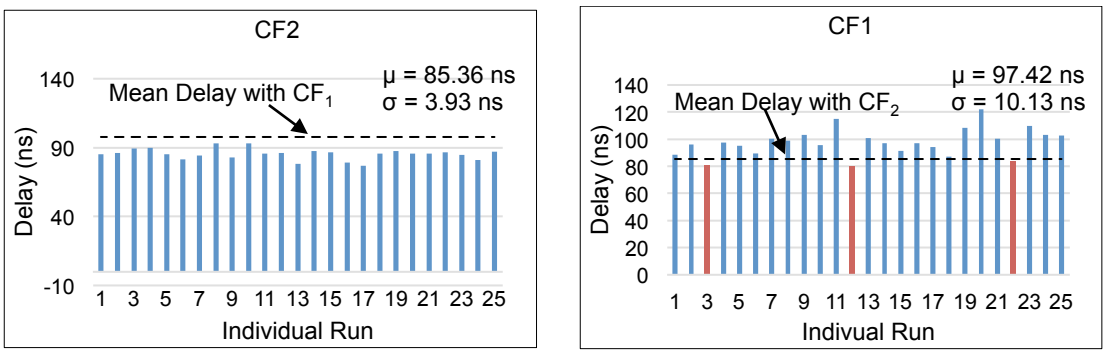


Figure 26: Delay estimated on the final floorplan for n200 circuit for 25 runs (a) using CF2, (b) using CF1, where buffer size is 8x, TSV diameter is 2μm, and TSV contact resistance is 10Ω

We also evaluated the power consumption in interconnects after 25 runs as shown in Figure 27. The total power is the sum of power consumption in wires, buffers and TSVs. The delay term in the cost function helps to optimize the number of buffers inserted in the individual nets to achieve lower delay in the wires. Since the total power depends largely on the power consumption in the buffers, reduction in the number of buffers reduces overall power. Hence, an additional term for power in the cost function may not be required. It can be seen that the mean of the total power of 25 runs with CF2 is 11% lower than with CF1. Moreover, the total power estimated on the final floorplan for each run with CF2 is better than the 25-run mean total power using CF1.

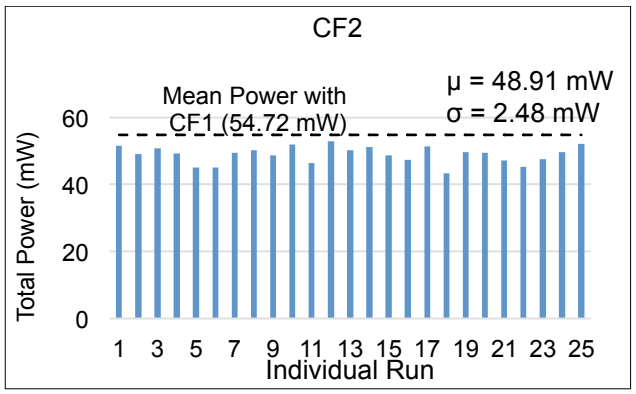


Figure 27: Power estimated on the final floorplan for n200 circuit after 25 runs using CF2, where buffer size is 8x and TSV contact resistance 10Ω

Figure 28 shows the runtime of different benchmark circuits using *CF1* and *CF2*. The buffer insertion performed at every iteration of the floorplanning using *CF2* increases the runtime on an average by 21%. The increase in the runtime due to buffer insertion in each net is independent of the circuit's size, as can be seen in Figure 28.

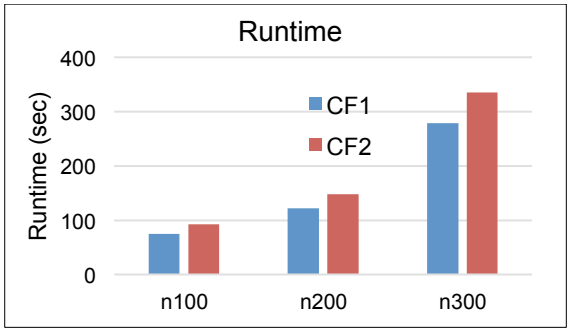


Figure 28: Runtime of different circuits using CF1 and CF2

5.5 Summary

In this work, we present methods for the evaluation of delay and power for buffered interconnects in 3D circuits considering TSV positions and nets-to-TSV assignment during floorplanning. Including the TSV area only, is not sufficient to account for TSV impact and results in underestimation of delay and power consumption in the 3D interconnects. The better estimation of the buffer count is also highly desirable when we consider its contribution to total interconnect power consumption. The contribution of the buffers to total interconnect power is around 4x larger than the power consumption in the wires. The total interconnect power is larger in intermediate device layers due to higher buffer count in these device layers. The contribution of TSVs to total interconnect power is negligible, but the power contributed by buffers required to overcome the impact of TSV delay, should not be ignored.

TSV can be considered as a wire segment contributing to the interconnect propagation delay, but the buffer cannot be inserted in the wire-segment representing a TSV. Hence, to optimize the propagation delay in nets with minimal usage of the buffers the impact of TSV delay on the buffer insertion length has to be considered in a specific way. The impact of TSV contact resistance on buffer insertion length is significantly higher for big-size buffers. The impact of TSV on delay in 3D interconnect can be ignored for contact resistance below 1 ohm. The dynamic buffer insertion length for each net results in reduction in the buffer count by up to 25%. The reduction in the buffer count also reduces

total interconnect power consumption on average by 16% to 21% for a single device layer.

The proposed scheme for buffer insertion around TSVs also minimizes the signal degradation with a minimal buffer usage. The technique considers the wire segment before and after a TSV as well as TSV delay to minimize delay in the TSV segments. Ignoring TSV location and its delay contribution may result in delay violation. The maximum reduction in the delay achieved in TSV segments using the proposed scheme is up to 5%-12% for TSV contact resistance ranging between 10Ω and 40Ω respectively.

6. Coupling Noise in 3D Integrated Circuits

The influence of large coupling capacitance between TSVs on the signal integrity (SI) in 3D interconnects offers serious challenges to the performance of 3D-ICs. It is shown in [57] that the average coupling noise in 3D nets is three times of noise in 2D nets. The large TSV coupling capacitance results in noise voltage at the victim net, affecting the performance and functionality of the 3D-IC. The unintentional switching of signal nets may also increase the power consumption in the nets. Due to the degree of design complexity introduced by TSVs in 3D ICs, the importance of early stage evaluation and optimization of signal integrity of 3D circuits cannot be ignored. To the best of our knowledge, this is the first work that addresses the early optimization of signal integrity during 3D floorplanning. The proposed work will facilitate reducing the problem complexity in the placement and routing stages.

In this work, we present methods for estimating coupling noise during floorplanning that allows for early stage evaluation and optimization of TSV induced coupling noise. To evaluate the coupling noise during floorplanning, a fast and accurate model for its computation is presented. Incorporating an efficient TSV coupling noise model within the 3D floorplanning framework facilitates better design decisions for later stages in the 3D IC design flow, so that the overall timing closure and design convergence can be better achieved. The coupling noise-aware cost function facilitates in optimizing the position of blocks and TSV islands, as well as nets-to-TSVs assignment to achieve 3D layout with minimized coupling noise.

We demonstrate the non-negligible impact of TSV position within an island on overall coupling noise. A diagonal form of TSV arrangement and nonuniform TSV pitch techniques are recommended for reducing coupling noise without incurring any significant increase in the area. The TSV-to-TSV coupling for diagonal arrangement of TSVs is deduced from the regular TSV arrangement. We have shown the effectiveness of diagonal TSV arrangement in reducing the coupling noise for TSV pitch equal to four-times its diameter. The effect of TSV islands' dimensions on the coupling noise in 3D circuits is also presented.

6.1 Previous Works

Several prior works [57-64] have analyzed coupling noise in 3D interconnects due to big-size TSVs. These studies focus on the placement stage, where the relative position of blocks and TSVs is fixed. Liu *et al.* [57] proposed a compact circuit model for full-chip SI analysis, which considers coupling between two-TSVs only. They proposed a buffer insertion and TSV shielding approach to reduce the signal integrity in the chip. Additionally, Liu *et al* in [58] proposed a force directed placement algorithm for SI refinement by TSV KOZ sizing. In their work, an additional force representing TSV coupling is introduced in the force-directed algorithm. However, their proposed technique increases the TSV pitch impacting design footprint.

Song *et al* [59] [63] proposed a compact TSV-to-TSV coupling model and extraction algorithm considering non-neighboring TSVs. Their approach offers a more accurate estimation of coupling noise. To address SI, they proposed a design methodology which

consisted of two techniques: 1) Spreading of victim and aggressive TSVs, and 2) Blocking of victim TSV with ground TSVs.

In [60-62], they proposed a multi-TSV coupling model that also considers the effects of silicon depletion region and silicon substrate. They perform an accurate full-chip coupling analysis on regular and irregular TSV arrangement, and also proposed a guard-ring model and its effectiveness in reducing coupling noise. In [64], they presented a TSV placement algorithm simultaneously performing coupling-aware placement and shield insertion.

In all the aforementioned studies, the techniques for alleviating the TSV-related coupling are deployed only during the placement stage. Therefore, efficacy of the proposed techniques is largely incumbent on the quality of the final 3D layout. More importantly, the relative positions of blocks and TSVs outside of blocks are fixed. The coupling noise introduced in a 3D wire will depend on (i) TSV-to-TSV coupling capacitance (ii) number of TSVs used and (iii) the wire capacitance, determined by the length of the wire. The abovementioned techniques like increasing distance between TSVs, use of ground TSVs or guard rings, focus solely on minimizing TSV-to-TSV coupling capacitance. None of these studies address the crucial impact of number of TSVs and the capacitance of the wire during nets-to-TSVs assignment. This objective is achieved in our floorplanning approach by optimizing the placement of blocks and TSVs through careful nets-to-TSVs assignment. After alleviating the worst coupling noise using the proposed approach during floorplanning, other post-layout planning techniques

of minimizing TSV-to-TSV coupling can be deployed to further eliminate noise from the circuit. In order to evaluate coupling noise in the nets during floorplanning, the developed empirical model is discussed in the next section.

6.2 Empirical Model for TSV Coupling Noise

The evaluation of coupling noise during 3D floorplanning requires a fast and efficient method to compute coupling noise based on known variables, such as, wirelength, the number of TSVs in a wire and electrical specifications of wire and TSVs. Prior works [57-63] developed a simulation-based approach for estimation and analysis of TSV induced coupling, using commercially available tools, like Synopsys HSPICE and Cadence Celtic. However, with increasing design complexity in 3D systems, simulation-based approaches can lead to large runtime, which may also increase the cost. Coupling noise evaluation not only depends on the physical parameters of the TSVs and wires, but is also influenced by the spatial locations of TSVs, during layout planning. Hence, it may not be practical to use pre-calculated look-up tables during 3D floorplanning for estimation of TSV-induced coupling. A 3-dimensional transmission line methods (3D-TLM) to model TSV signal propagation and TSV-to-TSV noise coupling is presented in [76]. However, the proposed model [76] ignores the influence of wire capacitance on the coupling noise in a 3D wire.

Therefore, we present a fast and simple closed-form empirical model for computation of coupling noise in the 3D wires during floorplanning. We obtained the empirical model

by simulating the simplified equivalent circuit shown in Figure 29 using HSpice, for different wirelength and TSV dimensions of the victim net.

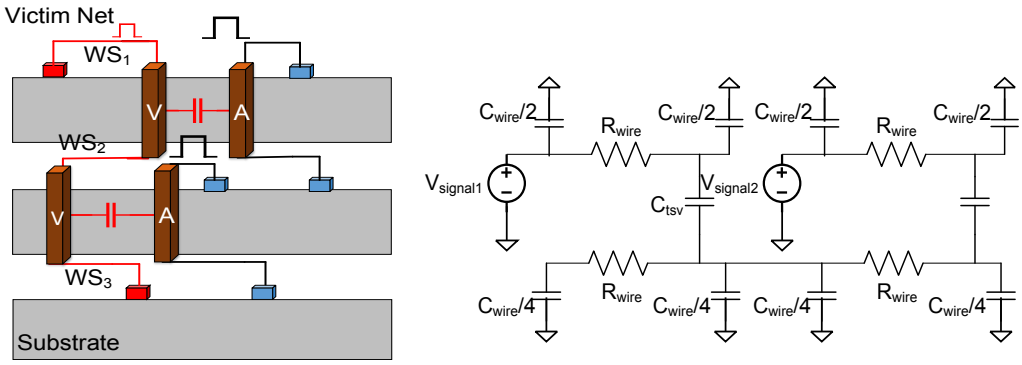


Figure 29: Simplified equivalent coupling noise model for 3D interconnects spanning to three device layers

The coupling noise at the victim net computed from HSpice simulations for wirelength ranging from 10µm to 500µm, and TSV diameters from 1µm to 3µm is shown in Figure 30. The fitted coupling noise model for 3D wires obtained from simulations is given by Eq. (28). The noise introduced by TSVs in a 3D wire will depend on the summation of TSV capacitances in the net and the total wire capacitance.

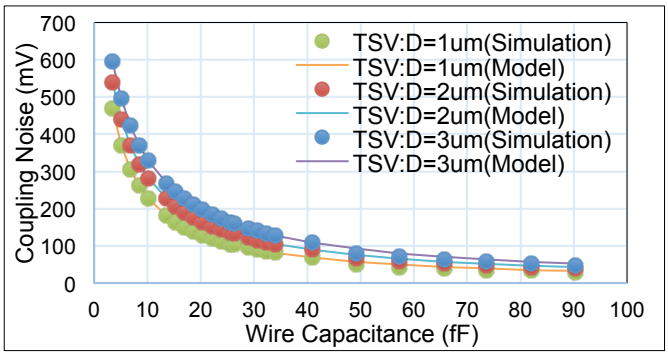


Figure 30: Coupling noise computed using empirical model and SPICE simulations for a 3D net with one TSV with diameter 1µm-3µm and varying length of the wire from 10µm-500µm

$$V_{noise} = \left[\sum_{i=1}^{N_{tsv}} C_{tsv_i} \Big/ (\sum_{i=1}^{N_{tsv}} C_{tsv_i} + C_{tot\_wire}) \right] V_{signal} \quad (28)$$

V_{noise}, represents the total coupling noise in the victim net due to V_{signal} on each aggressor net taken as 1V. C_{tot_wire} represents the total wire capacitance of victim 3D net, and is given by $C_{tot\_wire} = C_{wire} * \sum_{i=0}^{N} WS_i$. C_{wire} is the capacitance of wire per unit length (in μm), and WS_i is the length of wire segment on each device layer. The total wire capacitance of the victim net connected between three device layers (Figure 29) with the same wire capacitance on each device layer, is given by Eq. (29). N_{tsv}, represents the number of TSVs in a net. TSV capacitance (C_{tsv}) is computed using the empirical model described in chapter 4.

$$C_{tot\_wire} = C_{wire} * (WS_1 + WS_2 + WS_3) \quad (29)$$

We have not considered the parasitic resistance of TSVs (R_{tsv}), as it is less than 50mΩ, and will have negligible impact on the magnitude of noise introduced at the victim net. Our TSV-induced coupling model is based on the assumption that the capacitance of aggressor wire has no influence on the noise at the victim net. In this study, we focus on signal-TSVs, which are relatively smaller (TSV height ≤ 20μm), as compared to P/G TSVs. As the influence of inductance on coupling noise is negligible [73] for smaller TSVs, we ignore the TSV inductance as a variable in the coupling model. The impact of TSV liner on TSV capacitance is ignored, as the thickness of liner is negligible compared

to TSV pitch. Assuming an epitaxial layer with high resistivity, the effect of substrate resistance (R_{Si}) is ignored. Additionally, as the length of the wires exceeds 50μm and the operating frequency for digital applications exceeding 5GHz, the effect of inductive coupling between wires and TSVs is negligible [61], hence is ignored to simplify the model.

6.3 Non-uniform Wire Capacitance

The developed empirical model can also be extended for 3D integration, whereas, each tier is separately processed using different wire parameters. Accordingly, the properties of the metal layer stack on each device layer will be different depending on the process technology. In such cases, the wire segments of a net on each device layer will have different unit length capacitances. To incorporate this effect, the total wire capacitance is calculated by the summation of capacitance of the wire segment on each device layer using Eq. (30), where C_{wire_i} represents the wire capacitance per unit length on i^{th} device layer. The total wire capacitance of the victim net in Figure 29, which spans to three device layers and different wire capacitance per unit length on each device layer can be calculated using Eq. (31). The total wire capacitance is substituted in Eq. (28) to compute coupling noise in the victim net for heterogeneous 3D integration.

$$C_{tot\_wire} = \sum_{i=1}^{nlayers} C_{wire_i} WS_i \tag{30}$$

$$C_{tot\_wire} = C_{wire_1} * WS_1 + C_{wire_2} * WS_2 + C_{wire_3} * WS_3 \tag{31}$$

6.4 Validation of TSV Coupling Noise Model

In Table 12, the coupling noise computed by empirical model for a victim net of length 200μm and 2.5mm, spanning to consecutive layers is shown, where the metal stack parameters vary across multiple device layers. The proposed model is validated using three cases. Firstly, rows 1 and 2 show that the TSV position is critical, as it determines the length of the wire segment on each device layer and would affect the total capacitance. It can be observed that coupling noise increases by around 26% due to changing TSV position along the wire (change in the length of wire segments), keeping the same unit capacitance and total wirelength. Secondly, in rows 3 and 4, the effect of changing wire capacitance of each device layer is shown. Despite the same length of wire segment on each layer and total wirelength, the coupling noise in the wires could be different depending on the wire capacitance of each device layer across which the net spans. Hence, careful TSV positioning becomes even more crucial to minimize coupling, where wire parameters differ between device layers. Finally, rows 5 and 6 show that increasing the usage of TSVs in the designs, in addition to non-uniform wire capacitances across multiple device layers, can significantly impact coupling noise. Row 6 shows a 3D net with the same wirelength as row 1, but with only one extra TSV, which increases coupling noise by 78%.

Moreover, as the length of the wire increases to 2.5mm, the coupling noise introduced by TSVs reduces significantly to below 100mV. This is because; the large capacitance of

longer wires becomes a dominating factor, reducing the impact of TSV capacitance on the coupling noise.

Table 12: Validation of coupling noise model with Spice simulation for different length of segments of 200µm and 2.5mm length of wire, and unit length capacitance on each device layer, TSV cap = 10fF

Device layers	Unit Capacitance on each layer (fF)	Segment length on each layer WL = 200µm (µm)	Coupling Noise		Segment length on each layer WL = 2.5mm (mm)	Coupling Noise	
			SPICE (mV)	Model (mV)		SPICE (mV)	Model (mV)
2	0.12, 0.17	10, 190	229.88	229.899	1.0, 1.5	25.976	25.974
	0.12, 0.17	190, 10	289.85	289.875	1.5, 1.0	27.781	27.778
	0.12, 0.20	50, 150	217.39	217.421	0.5, 2.0	21.276	21.277
	0.17, 0.20	50, 150	206.19	206.194	0.5, 2.0	20.202	20.202
3	0.17, 0.2, 0.22	50, 50, 100	330.57	330.579	0.5, 0.5, 1.5	37.386	37.383
	0.12, 0.17,0.12	100, 95, 5	410.26	410.259	1.0, 1.0, 0.5	55.119	54.054
4	0,12, 0.17, 0.20, 0.22	50, 50, 50, 50	458.02	458.017	0.7, 0.6, 0.6, 0.6	65.122	64.103
	0,12, 0.17, 0.20, 0.22	100, 20, 40, 40	482.32	482.315	1.5, 0.5, 0.3, 0.2	77.028	75.188

The statistical validation of TSV coupling noise model is done to check the goodness of the developed model. During the validation, we compared the coupling noise predicted by the empirical model with the HSpice simulations. In Figure 31, we show an example of a victim 3D net and its equivalent circuit used for the statistical validation. We generated 10000 samples of the victim net routed between device layer #1 and #3. The length of the wire segments on each device layer, represented by WS_1, WS_2 and WS_3, are selected randomly from the defined range of wirelength. We took two different ranges for the wirelength (i) shorter wirelength range between [50µm-500µm] and, (ii) extended wirelength range between [50µm-2500µm]. These wirelength ranges were chosen because the wirelength distribution of GSRC and modified circuits lies within these ranges. Additionally, the TSV capacitance value on each device layer is selected

randomly between 5fF to 50fF. This is because the capacitance of TSVs with the diameter ranging between 1µm to 3µm lies within these values. However, the model would be acceptable for the wirelengths and TSV capacitance outside the mentioned range. The coupling noise in the individual nets is computed using the developed empirical model, and is implemented in MATLAB. We also created SPICE netlist of the equivalent circuit and performed the HSPICE simulations to obtain the coupling noise in the individual victim net.

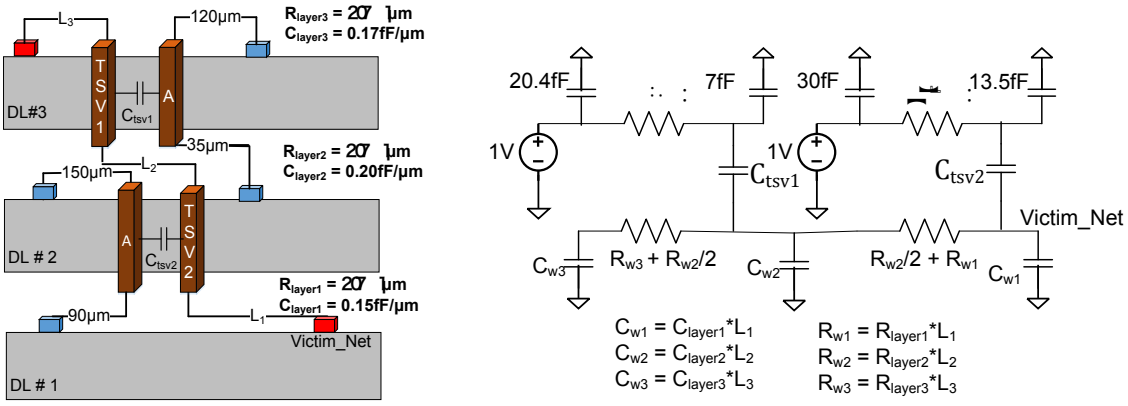
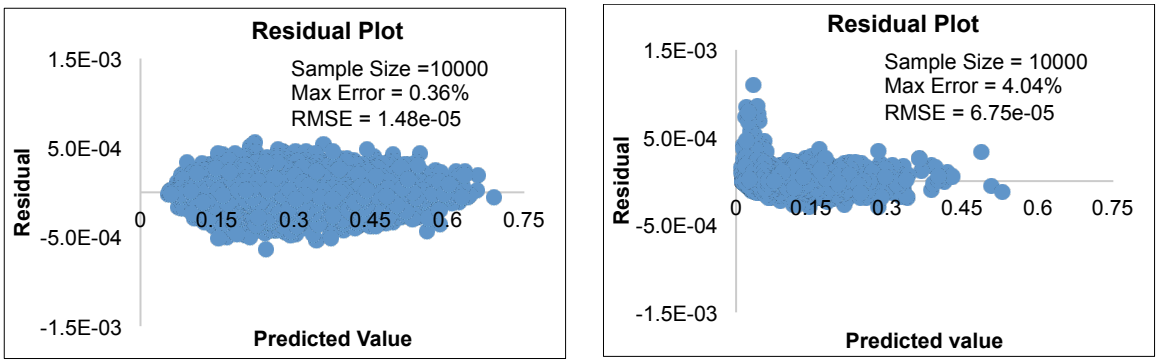


Figure 31: 3D victim net and its equivalent circuit representation used for statistical validation of the proposed model

Based on the coupling noise obtained for each net using the empirical model and HSpice simulations, we computed the residual values to show the correlation between model (predicted) and the simulation (observed). The residual plot for the two wirelength ranges is shown in Figure 32. Each point on the plot is the noise in a victim net, where x-axis represents the predicted (model) value and y-axis represents the residual value. The

residual value is the difference between the coupling noise computed using HSpice simulations and empirical model for individual nets. The small residual value shown in the Figure 32 suggests that the model is fairly accurate in predicting the coupling noise for variable wirelength and TSV coupling capacitance of the victim net spanning. The residual plot of the coupling noise for shorter wirelength range (Figure 32(a)) is shifted right as compared to extended wirelength range, suggesting that the coupling noise introduced by TSVs is significantly larger in shorter wires. The residual plot for the shorter wirelength range is also symmetrically distributed across zero-axis. On the other hand, the residual plot for the range (Figure 32(b)) of longer wirelength is not as symmetrical as short wirelength range. The residuals for the longer wirelength range predicted by the model are slightly higher compared to shorter wires. It is expected as the coupling noise for the longer wires is much lower, usually in the range of 15mV-20mV. Therefore, the percentage difference between simulated and predicted values is expected to be higher. Since, the coupling noise is below 50mV, slightly higher residuals are not much of a concern. By observing the residual plots, it can be concluded that the developed model can be effectively use for the computation of coupling noise in 3D wires with the specified range of wire and TSV capacitance (Figure 32).



(a) **(b)**

Figure 32: Residual plots for sample population of 10000 nets with C_{tsv1} and C_{tsv2} varying between [5fF-50fF], and length of wire segments in the range (a) Short wirelength range [50µm-500µm], (b) Extended wirelength range [50µm-2.5mm]

6.5 Coupling Noise-aware Cost Function

The observed impact of number of TSVs and TSV capacitance on the coupling noise in shorter wires further elucidate the critical impact of the 3D floorplanning stage, as not only it can determine the optimized position of TSVs during nets-to-TSVs assignment, but it can also be effectively used for design exploration in early stages of design. The nets-to-TSVs is a critical step in the floorplanning flow that can help in minimizing the impact of TSV on the coupling noise in 3D wires.

The cost function guides the floorplanning algorithm to achieve layouts with optimized desired parameters. The typical cost function (*CF1*) used during floorplanning separately minimizes the wirelength (*WL*) and number of TSVs (N_{TSV}). As discussed previously, the coupling noise introduced by TSVs in individual 3D nets will depend on the combined effect of TSVs and wirelength. Including the delay term in the cost function (*CF2*) accounts for variable impact of TSVs on the wires of different length. However, due to

small parasitic resistance of TSVs, RC delay product does not reflect the impact of large TSV capacitance. Since, the TSV-induced coupling noise in 3D wires is influenced by capacitive characteristics of TSV, the delay term is not sufficient to minimize the coupling noise in the individual victim nets.

In the proposed approach, we introduce a coupling noise term in the cost function (*CF3)*, which is the summation of noise voltage at each net, as shown in Eq. (38). The coupling noise term assists the floorplanning algorithm in monitoring the influence of TSVs on the coupling noise in the wire. This ensures that the placement of blocks and TSV islands, as well as nets-to-TSVs assignment minimizes the overall coupling noise in the circuit. Parameters α, β and γ represent the weights associated with the cost function parameters.

$$CF3 = Area + \rho * Delay + \delta * Noise \quad (32)$$

During 3D floorplanning, the direct optimization of coupling noise can play a decisive role in reducing coupling-related SI issues. This early optimization may not completely eliminate the noise, but will assist in reducing the magnitude of coupling noise and number of violating nets.

First, we demonstrate the effectiveness of coupling noise-aware cost function in reducing total coupling noise of the circuit. Table 13 shows the distribution of coupling noise in n200 circuit using coupling noise-unaware cost function (*CF1*) and coupling noise-aware cost function (*CF3*). We experimented with three different TSV diameters -

1µm, 2µm and 3µm. It can be observed that optimizing coupling noise during floorplanning by using *CF3*, reduces the worst coupling noise in the circuit by 16%-37% for specified TSV diameters. The number of nets with larger noise reduces, which decreases the total coupling noise in the circuit greatly. As shown in Table 13, *CF3* also reduces the total coupling noise in the circuit by 32%. It can also be seen that the coupling noise introduced by TSVs reduces significantly for 1µm TSV, decreasing the number of violating nets ($V_{noise} > 0.1V$) in the circuit greatly. Since, CF3 reduces the magnitude of coupling noise, the number of nets with $V_{noise} < 0.1V$ increases significantly. However, the typical threshold voltage of transistors at 45nm technology node is between 0.12V–0.3V [85], and hence noise voltage below 0.1V can be considered as non-violating.

Table 13: Distribution of coupling noise in n200 circuit using coupling noise-unaware cost function (CF1) and coupling noise-aware cost function (CF3) for TSV diameter = 1µm, 2µm, 3µm in n200 circuit, and TSV cap = 11.9fF

	TSV Dia = 3µm		TSV Dia = 2µm		TSV Dia = 1µm	
	Coupling Unware	Coupling Aware	Coupling Unware	Coupling Aware	Coupling Unware	Coupling Aware
$V_{noise} \geq 0.6$	71	12	8	0	0	0
$0.5 \leq V_{noise} < 0.6$	160	36	40	3	2	0
$0.4 \leq V_{noise} < 0.5$	292	171	188	52	4	1
$0.3 \leq V_{noise} < 0.4$	302	281	251	236	15	2
$0.2 \leq V_{noise} < 0.3$	-	236	167	235	112	10
$0.1 \leq V_{noise} < 0.2$	-	89	36	164	345	284
$V_{noise} \leq 0.1$	-	-	-	-	179	360
Total Noise (V)	363.61	278.92	247.02	189.15	132.45	83.38
Avg. Noise (V)	0.441	0.338	0.358	0.274	0.201	0.127
Worst Noise (V)	0.773	0.669	0.754	0.599	0.523	0.421

Next, we present a statistical analysis of overall performance of the circuit, after including the coupling noise term in the cost function. The mean values of area, delay,

power and coupling noise in n200 circuit with *CF2, CF3a, CF3b, CF3c, CF3d* are reported in Table 14. From the table, it can be observed that as the δ increases, the coupling noise initially shows significant reduction, but later achieves saturation. However, it is observed that the delay and power show only a slight increment for cost functions *CF3a* and *CF3b*, but substantial increase with *CF3c* and *CF3d*. It should be noted that assigning the same weight values to delay and coupling noise in *CF3b* reduces coupling noise in the circuit by 34%. However, the mean delay and power increases by 6.6% and 7.8% respectively. This increase in delay and power is due to fact that the coupling the noise introduced by TSVs only depends on the TSV capacitance, and hence increasing the weights of coupling noise term tries to minimize the number of TSVs to 3D wires with shorter length, in order to minimize the impact of TSV capacitance on the wire. However, the delay in the 3D wires is influence by both the resistance and capacitance of TSVs. This redistribution of TSVs to some of those shorter nets because of the coupling noise term, increases delay slightly in the 3D interconnects.

Table 14: Mean values of delay, power and coupling noise and area based on 25 runs with CF3 for specified weight parameters, TSV diameter = 2µm, TSV cap = 11.9fF, Buffer & wire parameters (Table 10), V_{signal} = 0.1V, frequency=2GHz

(ρ, δ)	Delay (ns)	Power (mW)	Coupling Noise (V)	Area (μm^2)
(100, 0)	85.36	48.91	246.09	0.284
(80, 20)	85.89 (+0.6%)	48.95 (+0.08%)	199.95 (-19%)	0.285 (+0.03%)
(50, 50)	90.77 (+6.3%)	52.75 (+7.8%)	162.85 (-34%)	0.287 (+1.1%)
(20, 80)	94.58 (+11%)	58.50 (+19%)	163.67 (-33.5%)	0.291 (+2.5%)
(0, 100)	101.46 (+19%)	64.71 (+32%)	164.44 (-33%)	0.295 (+3.9%)

As shown in Table 14, the cost function *CF3b* gives the least delay-coupling noise product of all the cost functions used in this thesis. Therefore, we present a statistical analysis of delay and coupling noise obtained for 25 runs with *CF3b*. In Figure 33 (a), we show the histogram plots of coupling noise estimated on the final floorplan when using *CF3b*. The mean and standard deviation computed from the distribution of total coupling noise are 163.51V and 5.82V respectively. The 25-run mean value of coupling noise evaluated on the final floorplans obtained using *CF2*, is shown by dashed-line, and is around 246V. Figure 33(b) shows the delay distribution of n200 circuit using *CF3b* cost function. The dash-line on the figure represents the 25-run mean delay value obtained using *CF2*. It can be seen that there are 28% (7 out of 25) floorplans using *CF3b* with the same or better delay compared to the mean delay value obtained using *CF2*. The coefficient of variation in the delay distribution using *CF3b* is 6.42%, which is slightly more than *CF2* (4.6%).

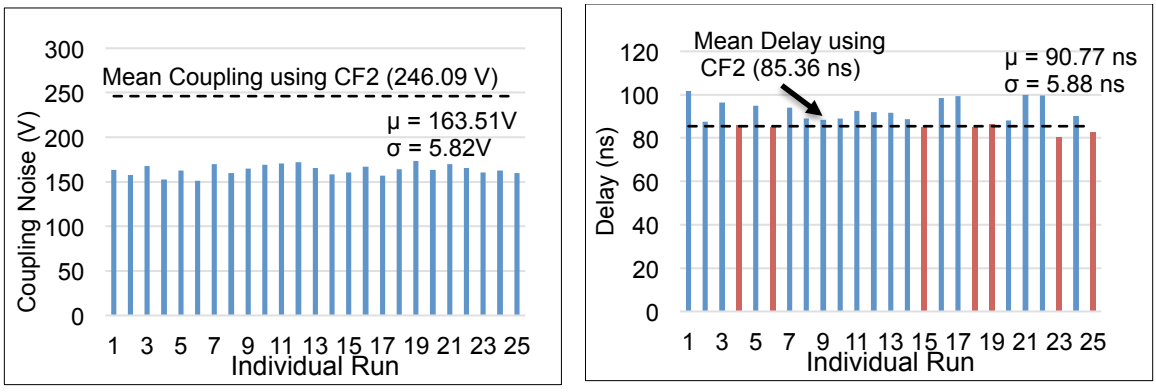
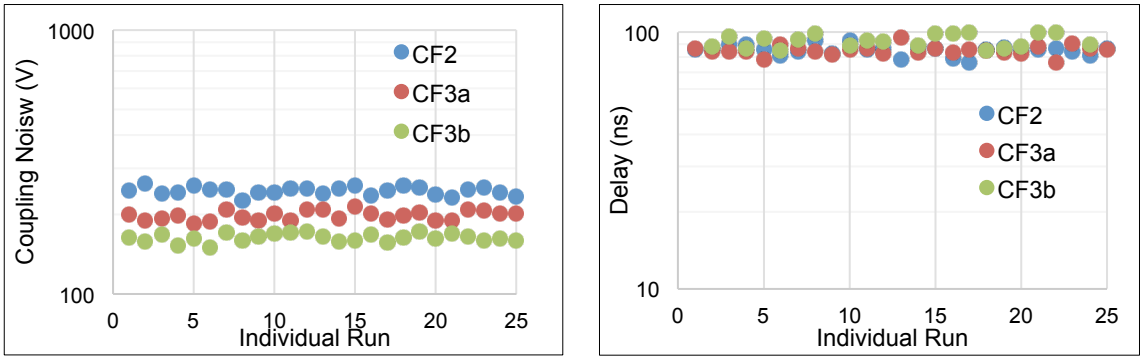


Figure 33: (a) Coupling noise, and (b) Delay estimated on the final floorplan of n200 circuit for 25 runs using CF3b, TSV diameter = 2μm, TSV cap = 11.9fF, Buffer & wire parameters (Table 10), V_{signal} = 0.1V

In Figure 34, we show the delay and coupling noise in n200 circuit after 25 runs using *CF2, CF3a* and *CF3b*. The coupling noise with *CF3b* is around 34% smaller than *CF2*, whereas the delay distribution with the three cost functions is very similar. The figure further demonstrates that the coupling noise term has a small impact on the delay in the circuit if appropriate weight functions are assigned to both delay and coupling noise terms in the cost functions. The coupling noise term in the cost function *CF3b* considers the impact of large TSV capacitance on the short wires to monitor the distribution of TSVs to the nets, reducing the coupling noise in the 3D wires significantly.



(a) **(b)**

Figure 34: Estimation of (a) coupling noise, and (b) delay, on the final floorplan using different weight functions in CF3 (for 25 runs), TSV diameter = 2µm, TSV cap = 11.9fF, Buffer & wire parameters (Table 10), V_{signal} = 0.1V

6.6 Proposed Techniques for Coupling Noise Reduction

In this section, we discuss specific techniques to minimize TSV-to-TSV coupling that can be deployed during 3D floorplanning. Past studies addressing the coupling issues due to multiple TSVs have focused on increasing the distance between TSVs, as the relative positions of TSVs are fixed during placement stage. Also, the movement of TSVs around

will depend on the distribution of whitespace. The insufficient whitespace on the layout will limit the quality of the final solution.

The coupling capacitance of a TSV inside an island will vary depending on whether it is located in the corner of the island or in the middle rows, surrounded by other TSVs. There are two coupling components of TSV-to-TSV coupling: a) C_{c1} represents the sidewall coupling with neighboring TSVs located along the horizontal or vertical lines, b) C_{c2} represents coupling with diagonal TSVs due to corner TSVs.

It has been discussed in [46] that the coupling capacitance due to sidewalls C_{c1} is almost 50% larger than the corner capacitance C_{c2}. Hence, arranging TSVs in a certain pattern to reduce C_{c1} can be effective in minimizing coupling noise. In the subsequent sections, we describe ways for further reduction of coupling noise by altering the arrangement of TSVs within islands.

6.6.1 Diagonal TSV Arrangement

In a TSV island, the position of a TSV with respect to other TSVs, plays a significant role in determining the overall coupling noise. In a regular array shown in Figure 35 (a), the TSVs in the middle of an island will have worse coupling due to eight neighboring TSVs, shown in red. The TSVs shown in yellow are surrounded by 5-TSVs, and will have sidewall coupling with 3-TSVs and diagonal coupling with 2-TSVs. The TSVs at the corner of the island, shown in green, will have the least coupling, with only three adjacent TSVs. The three different TSV capacitances, middle-TSV (C_{mid_TSV}), row-TSV (C_{row_TSV}) and corner-TSV (C_{cor_TSV}) in an island are given Eq. by (32-34).

$$C_{Mid\_TSV} = 4 * C_{c1} + 4 * C_{c2} \quad (32)$$

$$C_{Row\_TSV} = 3 * C_{c1} + 2 * C_{c2} \quad (33)$$

$$C_{Cor\_TSV} = 2 * C_{c1} + 1 * C_{c2} \quad (34)$$

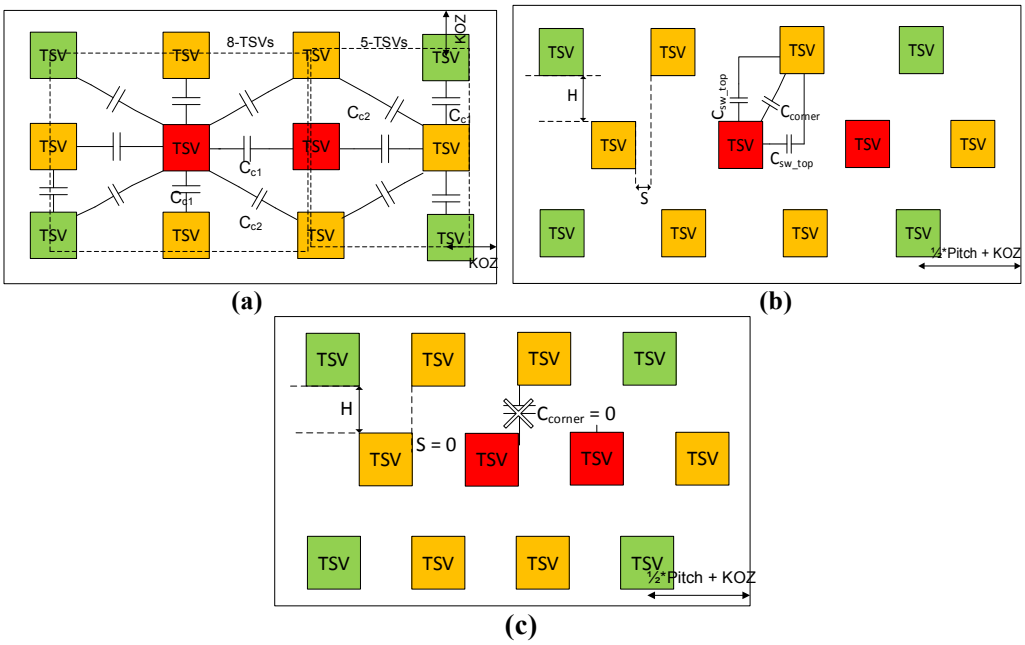


Figure 35: Different TSV-to-TSV coupling capacitance inside a TSV island consisting of middle-TSV (red), row-TSV (yellow), corner-TSV (green) for (a) Regular arrangement, (b) Diagonal arrangement (Pitch > 2*Diameter), (c) Diagonal arrangement (Pitch = 2*Diameter)

The above observations suggest that changing the TSV arrangement within the islands can reduce the coupling between TSVs. The form of arrangement of TSVs within islands needs to be chosen before the floorplanning run. Figure 35 (b) shows the diagonal arrangement, where alternate columns or rows of TSVs are shifted in vertical or horizontal direction respectively. The coupling between non-overlapping TSVs consist of fringe capacitance C_{sw_top} and C_{corner}, as shown in Figure 35 (b). These fringe capacitances

are computed using Eq. 11 and 13, where horizontal and vertical spacing between TSVs is represented by S and H respectively. The total coupling capacitance between non-overlapping TSVs is given by Eq. 35. However, the corner capacitance (C_{corner}) will become zero, as can be seen in Eq. (13), if either the horizontal (S) or vertical (H) spacing with the diagonal TSVs is zero. Therefore, for the diagonal arrangement shown in Figure 35(c), if the TSV pitch is equal to twice of its diameter, the horizontal spacing between the diagonal TSVs will be zero. This will result in the C_{corner} capacitance to be zero. Therefore, the applicability of Eq. 35 for the computation of capacitance between diagonal TSVs for the TSV pitch equal to twice of its diameter will require further investigation. This is because, the edge of diagonal TSVs will be vertically aligned, and other fringe capacitance components such as C_{top_top} may influence the coupling capacitance. Also, the fringe capacitance between non-aligned TSVs should increase with the decrease in TSV spacing. But, for TSV pitch equal to twice its diameter, the fringe capacitance would be lower compared to larger TSV pitch as C_{corner} goes to zero, which may not be true.

$$C_{fringe} = 2 * C_{sw\_top} + C_{corner} \tag{35}$$

$$C_{Mid\_TSV} = 2 * C_{c1} + 4 * C_{fringe} \tag{36}$$

$$C_{avg} = \left(N_{Mid\_TSV}C_{Mid\_TSV} + N_{Row\_TSV}C_{Row\_TSV} + N_{cor\_TSV}C_{Cor\_TSV}\right)\Big/_{N_{TSV}} \tag{37}$$

For the purpose of the analysis of diagonal TSV arrangement, it is assumed that the TSV pitch is equal to four times its diameter. By having larger TSV pitch, we ensure that C_{corner} is not equal to zero in the diagonal arrangement. The capacitance of TSVs inside the island decreases by 9%-14% for regular TSV arrangement. The capacitance of corner, row and middle TSVs for diameter 2µm and pitch 4µm is 7.23fF, 9.12fF and 11.93fF respectively. The TSV-to-TSV coupling component for corner, row and middle TSVs in the regular arrangement for 4µm TSV pitch is 3.03fF, 4.97fF and 7.87fF. As TSV pitch increases to 8µm, TSV-to-TSV coupling for corner, row and middle TSVs reduces to 1.62fF, 2.72fF and 4.40fF respectively. The C_{sw_top} capacitance in diagonal TSV arrangement decreases from 0.545fF to 0.279fF for the increase in TSV pitch from 4µm to 8µm. Whereas, C_{corner} capacitance increases from zero to 0.21fF as the TSV pitch changes from 4µm to 8µm. Additionally, we have used the worst and average coupling capacitance of TSVs inside the island. The TSVs in the middle have the worst coupling capacitance and is given by Eq. 36. The average coupling capacitance of TSVs in an island is estimated using Eq. 37. Table 15 shows the average and worst coupling capacitance of TSVs in an island for different array sizes with TSV diameter and pitch of 2µm and 8µm respectively. The worst coupling capacitance of TSVs remains constant for island sizes larger than 2x2. All the TSVs in a 2x2 island will be corner-TSVs with capacitance of 6.56fF and 5.94fF for regular and diagonal arrangement respectively. Therefore, the worst and average TSV capacitance is much lesser for smaller size of islands. As the TSV array size increases, the number of row and middle TSVs increases,

causing the average TSV capacitance of the island to rise. In the table, we can see a drastic increase in the average TSV capacitance when the TSV array size increases from 2x2 to 6x6. As the TSV array size increases beyond 6x6, we observed that the average capacitance nearly saturates. The worst capacitance of TSV islands for array size larger than 2x2 represents the capacitance of mid-TSVs, which is 10.87fF and 8.24fF for regular and diagonal arrangement respectively.

Table 15: Average and worst coupling capacitance for different TSV array dimensions inside island, TSV diameter = 2µm, height = 20µm and pitch = 8µm

TSV array	# TSVs			Regular Arrangement			Diagonal Arrangement		
	Cor	Row	Mid		Avg. Cap (fF)	Worst Cap (fF)		Avg. Cap (fF)	Worst Cap (fF)
2x2	4	0	0	Cor (6.56fF)	6.56	6.56	Cor (6.09fF)	6.09	6.09
4x4	4	8	4		8.30	10.87		7.02	8.47
6x6	4	16	16	Row (7.88f)	9.06	10.87	Row (6.76fF)	7.45	8.47
8x8	4	24	36		9.48	10.87		7.68	8.47
10x10	4	32	64	Mid (10.87fF)	9.74	10.87	Mid (8.47fF)	7.83	8.47
12x12	4	40	100		9.92	10.87		7.93	8.47

The coupling noise in n200 circuit with TSV diameter 1µm and 2µm using regular and diagonal TSV arrangement is shown in Table 16 (a) & (b). As discussed earlier, the TSV pitch for this experiment is kept four times of its diameter. This will increase the size of TSV islands, influencing the chip area and wirelength. But, for fair comparison between regular and diagonal TSV arrangement, we want to keep TSV pitch the same. We have used CF2 during the floorplanning and the coupling noise is evaluated on the final floorplan. The tables show the number of nets in the specified noise range, the total and worst coupling noise in the circuit. It can be seen that the number of nets with noise voltage exceeding 0.1V ($V_{noise} > 0.1$) reduces significantly for diagonal TSV

arrangement. This suggest that the diagonal TSV arrangement reduces the magnitude of coupling noise introduced by TSVs significantly by reducing TSV sidewall coupling capacitance. Although the number of nets with noise voltage below 0.1V increases for diagonal TSV arrangement, but their impact can be ignored as the threshold voltage of the CMOS transistors in 45nm technology is around 0.12V–0.3V [85]. The diagonal TSV arrangement reduces total and worst coupling noise by up to 30% and 21% respectively. The coupling noise due to worst TSV capacitance is higher than with the average TSV capacitance by up to 32% and 19% for TSV diameter 1μm and 2μm respectively. The coupling noise due to average TSV capacitance will be a better approximation of total coupling noise, as not all the TSVs would have coupling from all the sides. Since, the TSV-to-TSV coupling capacitance for diagonal arrangement has not been verified with the simulations, the presented results for the coupling noise in the interconnects are just an approximation. Therefore, the suggestions for improvements due to diagonal arrangements will require further validations using simulation methods.

Table 16: Number of nets with coupling noise in given ranges, total and worst coupling noise due to worst and average coupling capacitance for regular and diagonal TSV arrangements for TSVs inside island with (a) TSV diameter = 1µm, height = 10µm and pitch = 4µm, (b) TSV diameter = 2µm, height = 20µm and pitch = 8µm.

(a)

Noise Voltage	Average TSV cap		Worst TSV cap	
	Regular	Diagonal	Regular	Diagonal
$0.6 \leq V_{noise} < 0.7$	0	0	0	0
$0.5 \leq V_{noise} < 0.6$	1	0	1	1
$0.4 \leq V_{noise} < 0.5$	2	1	9	1
$0.3 \leq V_{noise} < 0.4$	14	5	47	9
$0.2 \leq V_{noise} < 0.3$	99	26	179	80
$0.1 \leq V_{noise} \leq 0.2$	539	351	603	446
$V_{noise} \leq 0.1$	304	576	120	422
Total Noise (V)	127.96	93.07	168.87	119.64
Worst Noise (V)	0.503	0.412	0.549	0.438

(b)

Noise Voltage	Average TSV cap		Worst TSV cap	
	Regular	Diagonal	Regular	Diagonal
$0.6 \leq V_{noise} < 0.7$	0	0	1	0
$0.5 \leq V_{noise} < 0.6$	2	0	11	1
$0.4 \leq V_{noise} < 0.5$	17	7	51	12
$0.3 \leq V_{noise} < 0.4$	82	42	191	65
$0.2 \leq V_{noise} < 0.3$	334	204	374	275
$0.1 \leq V_{noise} \leq 0.2$	544	594	376	521
$V_{noise} \leq 0.1$	92	224	35	165
Total Noise (V)	208.34	169.62	248.37	184.96
Worst Noise (V)	0.534	0.469	0.601	0.504

6.6.2 Nonuniform TSV Pitch

Increasing TSV pitch is a commonly used technique for minimizing coupling noise in 3D circuits [58-63]. Previous works have either used force-directed algorithm to increase the KOZ around TSVs [58], or spreading the TSVs apart [59-61] to minimize TSV-to-TSV coupling. Both of these techniques will depend on the whitespace distribution

around victim TSVs and therefore, offer limited solution quality. Moreover, as the relative position of blocks and TSVs cannot change during the placement stage, increasing TSV pitch may significantly increase the chip footprint violating the fixed outline region and influencing the circuit performance.

A non-uniform TSV pitch technique is proposed in order to minimize the area overhead. An example of this technique is shown in Figure 36, which shows a 4x4 TSV island with the reference, high and non-uniform pitch. Figure 36(b) shows that by doubling the pitch uniformly between each pair of TSVs in an island, the TSV area will increased by almost three times. Whereas, for non-uniform-pitch, the distance between the TSVs located in the middle rows/column of an island is increased, as they suffer from the worst coupling from adjacent TSVs. Additionally, the distance between TSVs in the corner rows remains unchanged in order to keep the increase in area small. From Figure 36(c) we observed that the TSVs highlighted in yellow have non-uniform spacing with neighboring TSVs. Hence, we have computed the coupling capacitance of the highlighted TSVs with neighboring TSVs individually. The horizontal and vertical spacing for one highlighted TSV with adjacent TSVs on its either side is shown in Figure 36 (c). As shown in the figure, due to different spacing, the coupling with diagonal TSVs will be different on either side, represented as C_{c2_1} and C_{c2_2}. K_{corner} value for C_{c2_1} and C_{c2_2} capacitive components calculated using Eq. 20, will be 1.25 and 2.0 respectively. The value of C_{c2_1} and C_{c2_2} capacitance is 0.583fF and 0.932fF respectively. Hence, for

nonuniform TSV pitch, the average capacitance of TSVs inside the island will decrease, keeping the increase in TSV island area below 50%.

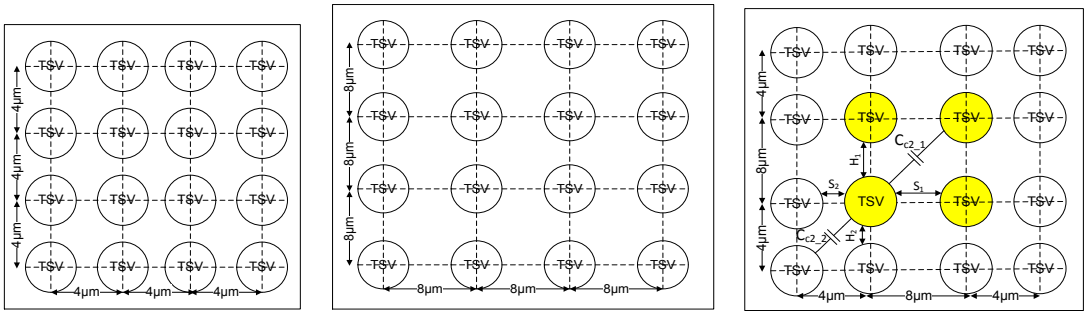


Figure 36: Trade-off between TSV island area and TSV pitch (a) with reference TSV pitch (area = 324µm^2), (b) doubling the TSV pitch to minimize coupling (area = 900µm^2), (c) non-uniform TSV pitch to minimize area overhead (area = 484µm^2)

Figure 37, compares the performance parameters such as footprint, wirelength, delay and coupling noise using high-pitch and non-uniform-pitch between TSVs within islands. A high-pitch island represents an island where TSV pitch is increased to 4 times of its diameter. A non-uniform-pitch island has TSV pitch equal to four times of the TSV diameter, only in the middle row of TSVs, while the TSVs on the periphery of the islands are at reference pitch from adjacent TSVs. The estimated parameters are normalized to their value with the reference pitch island, where pitch between each pair of adjacent TSVs is twice of TSV diameter.

The high-pitch TSV islands for 1µm diameter mitigates coupling noise in n200 circuit by 26% compared to TSV islands with reference-pitch, while the 3D footprint, total wirelength and delay rise by 5%. The non-uniform-pitch TSV islands are able to achieve 19% reduction in coupling noise compared to coupling noise with the reference-pitch islands, whereas, the increase in footprint, wirelength and delay is below 2%. Due to low

coupling capacitance with increasing pitch, the small TSV delay does not have a significant impact on the delay, as the total delay in 3D interconnects mainly depends on the buffers and wires. As the TSV diameter increases to 2µm, the high-pitch TSV island results in 24% reduction in coupling noise, but causes 30% area overhead and 17% increase in wirelength. This clearly suggests that if the TSV pitch were to be increased to reduce coupling noise during placement stage it would result in the violation of fixed-outline region, considering 15% total whitespace allowance. The increase in area and wirelength with non-uniform-pitch TSV island is 13% and 8% respectively, and satisfies the fixed-outline constraint, whereas, the coupling noise decreases by 19% as compared to reference-pitch TSVs. This experiment also suggests that as TSV diameter increases, using larger TSV pitch to minimize coupling noise will increase the area, wirelength and the delay in the circuit significantly.

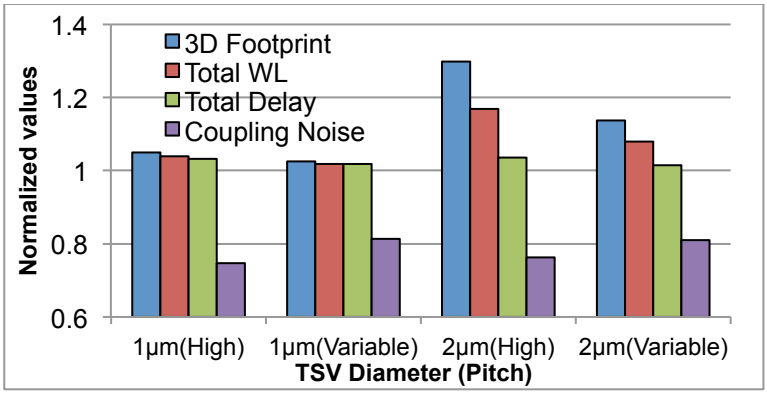


Figure 37: 3D footprint, total wirelength, total delay and total coupling noise in n200 with high pitch (4*Diameter) and non-uniform pitch TSV island normalized to normal-TSV pitch, where TSV diameters = 1µm and 2µm.

6.6.3 Detailed Nets-to-TSVs Assignment

The detailed assignment is a greedy approach to optimize coupling noise on the final floorplan by refining the assignment of nets to individual TSVs within each island. Although wirelength can change during the routing stage, but the detailed assignment will help in early evaluation of the goodness of final floorplan, and optimized the position of blocks and TSV islands to achieve desired performance. Performing the detailed assignment in routing stage and not meeting the desired performance will require repeating the physical design stage, impacting the signoff.

The random moves guide allocation of one TSV island for each group of nets. In the group of nets assigned to an island, the relatively shorter wires will have smaller wire capacitance. Assigning these short wires to TSVs with smaller coupling capacitance, further lowers the coupling noise in the wires. Therefore, TSVs at the corner of an island having least coupling are preferred for short wires. First, nets belonging to the same island are sorted in order of increasing wirelength. Next, the sorted nets in the list are assigned to corner TSVs first, then to row-TSVs and finally to middle-TSVs depending on the availability of TSVs.

We demonstrate, the efficiency of the detailed nets-to-TSVs assignment in minimizing coupling noise without incurring any significant runtime. Figure 38(a) shows the total coupling noise in n200 circuit after floorplanning run completes with global assignment, and total noise after the detail assignment on the final floorplan. Figure 38(b) shows the same experiment performed on n300 circuit. The experiment is performed for different

TSV dimensions, considering TSV aspect ratios (height/width) of 10 and 20. As can be observed from Figure 38(a) & (b), the proposed detail assignment further reduces coupling noise by 22% and 25% for n200 and n300 circuits respectively.

The significant reduction in coupling noise due to detail nets-to-TSVs assignment shows that early floorplanning and careful nets-to-TSVs assignment can be critical for overall design convergence and timely sign-off. This approach overcomes the limitations associated with the post-layout planning techniques focusing solely on the minimization of TSV-to-TSV coupling [57-64]. Performing detail assignment further fine-tunes the noise performance of the final floorplan, providing greater insight towards making better design decisions up front, so that overall design convergence and timing closure can be better achieved.

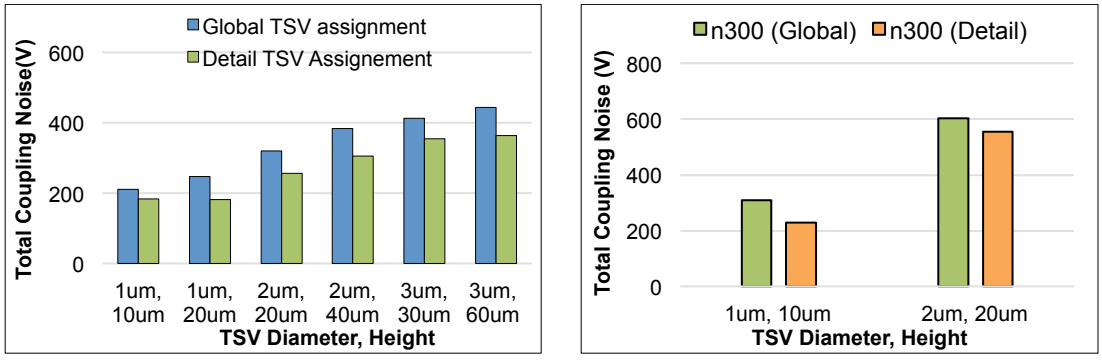


Figure 38: Total coupling noise using global and detail nets-to-TSVs assignment, (a) n200 circuit with different TSV diameters (aspect ratio 10:1, 20:1), (b) n300 circuit

6.6.4 TSV Island Size

The size of TSV islands has a significant impact on the packing efficiency during floorplanning, which affects both the chip area and wirelength. Big-size TSV islands reduce overall TSV area due to sharing of KOZ, but cause routing obstacles. Moreover, the average TSV coupling will be much larger, as compared to TSV coupling in smaller TSV islands. Small-size islands may result in reduced wire length, as they can be packed more efficiently closer to blocks. However, the average TSV area increases, therefore impacting the 3D footprint.

Table 17 shows the total coupling noise in the nets for n200 circuit with TSV diameter of 2μm and 3μm. The coupling noise is computed using average capacitance of TSVs in the islands, as it gives better estimation of total coupling noise introduced by TSVs. The average TSV capacitance for 6x6 TSV islands is around 8.6% higher than 4x4 as shown in Table 15, resulting in larger coupling noise in the victim nets. Area of 8x8 TSV islands matches closely with the block sizes in n200 circuit resulting in better packing and resulting in shortest wirelength. The better wirelength in the circuit with 8x8 TSV islands improves the total coupling noise in the circuit. The average coupling capacitance of 6x6 island is only 4% smaller than 8x8 islands, but due to overall larger area taken by TSVs, the coupling noise worsens. In spite of larger overall area occupied by TSVs with 4x4 island, the lowest average coupling capacitance keeps the total coupling noise in the circuit low.

Table 17: Total wirelength and coupling noise in n200 circuit with different size of TSV Islands

TSV Island Size	Total WL (mm)	Total Coupling Noise (V)	
		TSV (2μm)	TSV (3μm)
4x4	101.44	88.43	104.70
6x6	82.95	92.46	115.36
8x8	78.99	78.55	102.81
12x12	79.85	85.62	109.67

It can be concluded that the influence of TSVs on coupling noise is not just determined by TSV-to-TSV coupling alone, but also depends on the TSV packing, area and nets-to-TSVs assignment. Also, the appropriate choice for TSV island dimensions will depend on the circuit size and must be tested early in the design phase to achieve better performance in the circuit.

6.7 Estimation of ground TSVs

The strategy for estimation of ground TSVs is demonstrated in Figure 39. The figure shows an example of the number of ground TSVs required for coupling noise voltage at the victim net TSV. In the figure the middle TSV represents the victim TSV, which is surrounded by aggressor TSVs in all the sides.

The number of ground TSVs is obtained using SPICE simulations, which calculates the number of ground TSV required to reduce the coupling noise below 100mV. To achieve this, first we obtained the coupling noise from the final floorplan. Then, we performed SPICE simulations to obtain the required number of ground TSVs for certain magnitude of coupling noise. During the simulations, there are no ground TSVs additionally inserted, but instead we estimated the number of ground TSV needed by grounding the

aggressor TSVs around the victim TSV. The aggressor TSVs were grounded one at the time until the noise voltage in the victim net falls below 100mV.

Finally, we obtained a range of coupling noise that requires the same number of ground TSVs. The example presented in Figure 39, shows that two ground TSVs are required to reduce noise below 100mV for a victim TSV with coupling noise in the range of 0.15V-0.2V. As the coupling noise increases to 0.25V-0.3V, the number of ground TSVs required will be 4.

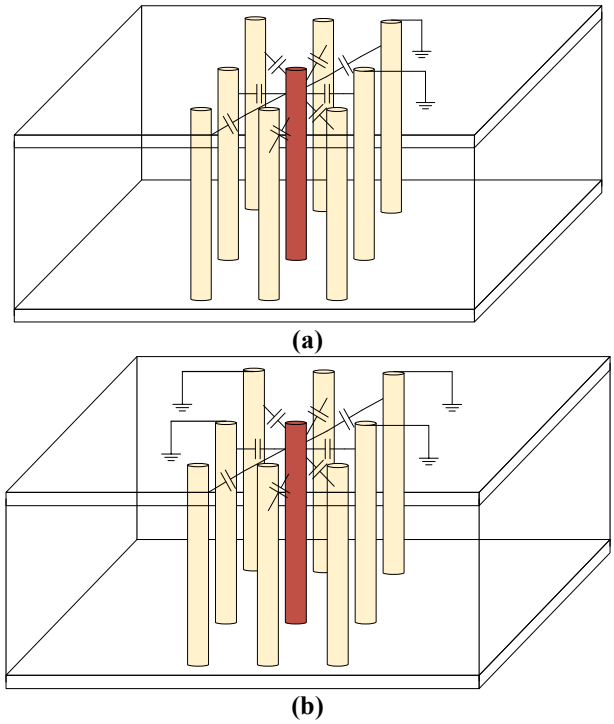


Figure 39: Number of ground TSVs (shielding TSVs) required for coupling noise voltage at the victim TSV is (a) between 0.15V to 0.2V, (b) between 0.25V to 0.3V

Based on the experiment discussed above, the number of required ground-TSVs for different ranges of coupling noise is shown in Table 18. As it can be seen, the range of coupling noise for ground-TSVs changes in step of 50mV for the noise at victim net

below 350mV. For the coupling noise on the victim net larger than 350mV, the increase in ground-TSVs is in step of 100mV. As the coupling noise increases beyond 550 mV, the reduction in coupling noise at victim net below 100mV will require 8 ground-TSVs. The number of ground-TSVs is estimated on the final floorplan with *CF2* and *CF3* where TSVs are arranged regularly inside the islands.

In the table, the numbers of nets in the given ranges of coupling noise are listed in columns 3rd & 4th. The required number of ground-TSVs obtained experimentally to reduce the coupling noise below 100 mV is shown in the 2nd column. The total number of ground-TSVs for each case is the summation of the ground-TSVs estimated for the specified ranges of coupling noise, and it is shown in column 5th & 6th. It can be seen that the coupling noise-aware cost function results in 39% reduction of ground-TSVs. We have also computed the total area required by ground-TSVs for each case in column 7th and 8th. For simpler computation, we have assumed that ground-TSVs are placed individually. The area required for single ground-TSV with diameter 2μm including desired KOZ is around 49μm^2. The increase in total area due to ground-TSVs with CF3 is around 40% smaller than the area occupied by TSVs using CF2 during floorplanning.

Table 18: Number of ground TSVs estimated on the final floorplan in n200 circuit with TSV diameter of 2µm and V_{sig}=1V for (i) using CF2 and regular TSV arrangement, and (ii) using CF3 and regular TSV arrangement

Coupling Noise range (V)	Ground TSVs required	Number of nets		# ground TSVs	
		CF2 + Regular	CF3 + Regular	CF2 + Regular	CF3 + Regular
$V_{noise} \geq 0.55$	8	18	0	144	0
$0.45 \leq V_{noise} < 0.55$	7	44	14	308	98
$0.35 \leq V_{noise} < 0.45$	6	171	65	1026	390
$0.3 \leq V_{noise} < 0.35$	5	88	27	440	135
$0.25 \leq V_{noise} < 0.3$	4	124	58	496	232
$0.2 \leq V_{noise} < 0.25$	3	100	92	300	276
$0.15 \leq V_{noise} < 0.2$	2	33	184	66	368
$0.1 \leq V_{noise} < 0.15$	1	12	197	12	197
Total Number of ground TSVs				2792	1696

In real design, the ground TSVs are inserted around victim TSVs to provide shielding from neighboring aggressors. As shown in Figure 40, ground TSVs with the grey color are inserted around the victim TSVs. If the TSV spacing between the victim and aggressor TSVs is not sufficient, then the aggressor TSVs will be shifted away from the victim TSVs to facilitate the insertion of ground TSVs. This may increase the overall chip area significantly.

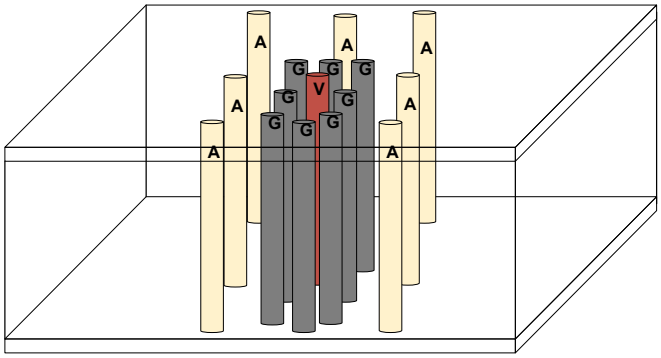


Figure 40: Victim TSV (brown) is surrounded by ground TSVs (grey) to provide shielding from aggressor TSVs (light brown)

6.8 Summary

In this chapter, a simple and efficient empirical model for fast evaluation of coupling noise during 3D floorplanning is proposed. We demonstrated that the coupling noise in a 3D wire is not just influenced by TSV-to-TSV coupling, but is also strongly impacted by wire capacitance and the number of TSVs in the wire. For designs with non-uniform wire capacitance across multiple device layers, locations of TSVs on a floorplan will play an important role in determining the total wire capacitance and hence, overall coupling noise in the wire. TSVs assigned to shorter wires have significantly larger impact on the coupling noise and therefore these wires should be connected to TSVs with smaller TSV-to-TSV coupling capacitances. The proposed coupling noise-aware cost function ensures that the placement of blocks and TSV islands, as well as nets-to-TSVs assignment minimizes the overall coupling noise in the circuit. The coupling noise-aware cost function reduces coupling noise by 32% compared to typical floorplanning cost function and helps minimizing the number of violating nets significantly. However, the delay and power in the interconnects increases by 6% and 8% respectively.

A detail nets-to-TSVs assignment on the final floorplan is presented, where the nets are assigned to specific TSVs inside the islands to further minimize coupling noise after the global assignment. The detail assignment will also provide an early assessment of coupling noise in the final layout and also help reducing the complexity of routing stage. The techniques to reduce TSV-to-TSV coupling using diagonal TSV arrangement and non-uniform TSV pitch offer promising solutions for minimizing coupling noise with

minimal increase in the overall area, wirelength and delay. The diagonal TSV arrangement reduces the total and worst coupling noise by 30% and 21% respectively for TSV pitch equal to 4-times of its diameter. However, the applicability of diagonal TSV arrangement for pitch equal to twice of its diameter needs to be investigated. This is because coupling capacitance between diagonal TSVs whose edges are aligned must be modeled accurately. Also, the TSV-to-TSV coupling capacitance for diagonal arrangement with the TSV pitch equal to four-times its diameter were deduced from the regular arrangement, and needs to be verified by simulation methods. Therefore, the suggested improvements in the coupling noise for diagonal TSV arrangement needs to be further investigated.

7. Interconnect Density in 3D Integrated Circuits

Interconnect delay and power are a dominant factor in determining the overall performance of 3D ICs, therefore an accurate benchmark of the interconnect RC performance is necessary. The interconnect capacitance is measured assuming that the metal layers are separated by a minimum-pitch. However, in a realistic 3D design, the actual separation between metal layers for a design, will be defined by the density of interconnects in the design. The computation of interconnect density for 2D is straightforward. However, in 3D circuits, the interconnect density needs to be evaluated for individual device layers, as each device layer has its own dedicated metal stack. Consequently, TSV positions are very critical for determining the accurate length of the segment on each device layer. None of the previous works have considered the interconnect density on individual device layers and its impact on the prediction and optimization of the performance of 3D circuits.

In this chapter, we focus on evaluating the influence of interconnect density on the performance of 3D ICs. The interconnect density and its influence on wire capacitances on the individual device layers is computed based on the wirelength distribution. We also analyze the impact of estimated wire capacitance on individual device layers on the performance and power in 3D ICs. A wire capacitance-aware buffer insertion scheme is presented to optimize BIL on the individual device layers and around TSVs, helps minimizing the buffer count, delay and power in 3D ICs. The estimated delay based on the different wire capacitances is included in the cost function to optimize the position of

blocks and TSV islands. It is shown that ignoring the impact of different wire capacitance during optimization can result in inferior solutions. We also study the impact of interconnect density on the evaluation and optimization of coupling noise.

7.1 Interconnect Density

7.1.1 Motivation

Interconnect planning is a trade-off between density, RC performance and cost. The narrow wires help achieve higher density, but have relatively larger RC delay. The wider wires have better RC performance but limited density. Either the density or RC performance can be improved by adding extra metal layers, but will increase the process cost. Hence, interconnect density play a critical role in determining the interconnect performance. Interconnect resistance and capacitance are defined by the technology parameters based on peak density considering the minimum separation between the metal lines. However, the separation between metal layers utilized for block-level connection will depend on the density of inter-block wires. Prior works [3][16][17] have completely ignored the influence of interconnect density on individual device layers on the wire capacitances, resulting in unrealistic estimation of delay and power in the interconnects. The estimation of wire density in 2D is straightforward. However, a 3D net spanning to multiple device layers may have different length of the wire segment on each device layer as shown in Figure 41 (a). The bottom device layer has significantly longer wire segment compared to upper layer for the net connecting blocks on consecutive device layers. This

example suggests that the length of the wires across multiple device is different, and interconnect density on all device layers will not be the same.

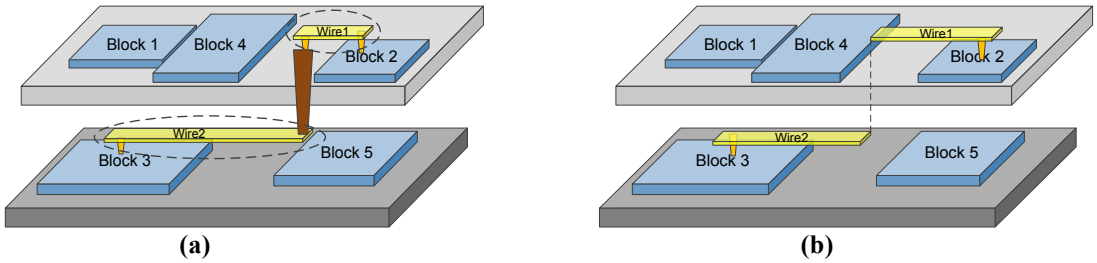
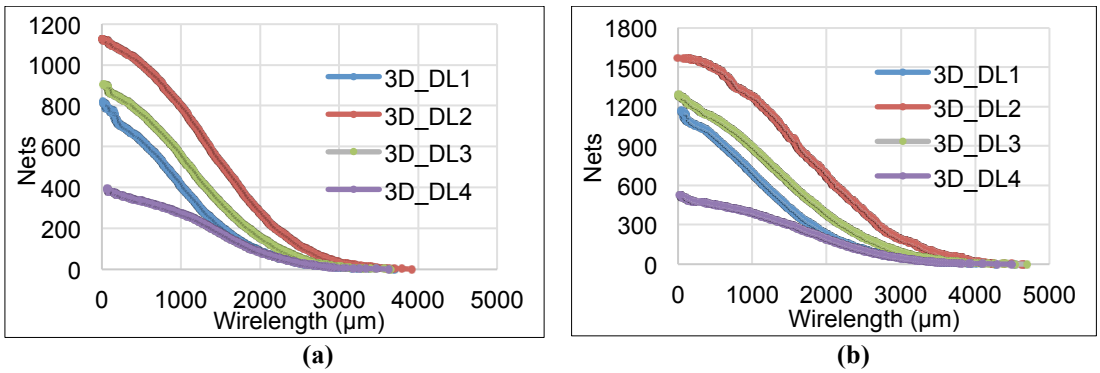


Figure 41: Wirelength of a 3D net connecting blocks on consecutive layers (a) with known TSV location (Wire1 ≠ Wire2), (b) Unknown TSV location (Wire1 = Wire2)

For accurate estimation of total wirelength on each device layer of 3D-IC, we used our floorplanning tool to obtain the wirelength distribution across stacked device layers. The wirelength distribution of modified GSRC circuits on individual device layers of 3D-IC is shown in Figure 42. The intermediate device layers in both the circuits have higher density as compared to bottom and top most device layers. It is primarily due to number of nets routed on intermediate device layers, which is represented by the vertical axis in Figure 42. This clearly suggests that due to different wire distribution on each device layer, the wire density will vary significantly across multiple device layers.



(a) **(b)**

Figure 42: Average wirelength distribution of 25 runs on each device layer of 3D-IC for (a) n200_exp, (b) n300_exp

The total wirelength on individual device layers need to be estimated accurately for calculating interconnect density. TSV position is necessary for determining the total wirelength on each device layer accurately. It is shown in Figure 41 (b), where TSV position is not identified, has same total wirelength as in Figure 41 (a), where TSV coordinates are known. However, the length of the wire segment on individual layers is very different form Figure 41 (a). Table 19 shows that the total wirelength on each device layer in modified GSRC circuits ignoring TSV location (TSV position-unaware) can be up to 25% different from the actual wirelength. The actual wirelength for each device layer is obtained on the final floorplan considering the TSV coordinates.

Table 19: Total wirelength with known TSV position (position-aware) and unknown TSV position (position-unaware) on each stacked device layer for the given circuits

Layer	Total Wirelength n200_exp			Total Wirelength n300_exp		
	TSV position aware (mm)	TSV position unaware (mm)	Diff (%)	TSV position aware (mm)	TSV position unaware (mm)	Diff (%)
# 1	588.02	737.00	+25.3	1632.6	2002.8	+22.6
# 2	1131.7	1056.2	-6.67	3188.3	2957.1	-7.25
# 3	890.62	868.44	-2.49	2234.2	2218.6	-0.70
# 4	367.01	315.75	-13.9	889.71	766.28	-13.8

7.1.2 Influence of interconnect density on the wire capacitance

Based on the observation in that the wirelength distribution on all the device layers is not the same, estimation of interconnect density and its influence on the wire capacitance for each device layer is discussed here. The interconnect density will depend on the placement of blocks and TSV islands on the 3D layout. Since, the position of blocks and TSV islands on the final floorplan may be different after each floorplanning run, we use average wirelength for the estimation of interconnect density on each device layer.

The total length of the wire segments assigned to i^{th} device layer is represented as TWL_i, and is obtained by summation the length of the wire segment (WS_j) on i^{th} device layer. The interconnect density on each device layer of modified GSRC circuits is shown in Figure 43. The average wirelength on each device layer from Table 18 is used as TWL_i. The estimated interconnect density (ID_i) on each device layer given by Eq. (41) is the ratio of total wirelength and 3D footprint (A_{3D}), which defines the maximum available routing area.

$$TWL_i = \sum_{j=1}^{Nnets} WS_j \, , where \; i = 1 \ldots N_{layers} \quad (39)$$

$$TWL_{3D} = \sum_{i=1}^{N_{layers}} TWL_i \quad (40)$$

$$ID_i = {}^{TWL_i}/_{A_{3D}} \quad (41)$$

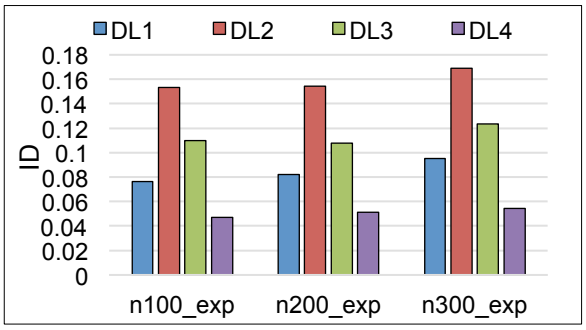


Figure 43: Average of interconnect density on individual device layers estimated based on 25 runs

In 3D-integrated circuits, every device layer has dedicated metal layer stack for routing intra and inter-die signal connections. Total capacitance of wire in multi-level interconnect stack is the sum of coupling with neighboring wires (intra-layer) and metal layers above and below (inter-layer), as shown in Figure 44. The coupling between neighboring wires is the dominant factor depends on the spacing between the wires defined by interconnect density. The coupling component with metal layers above and below also depends on the wire densities on those layers.

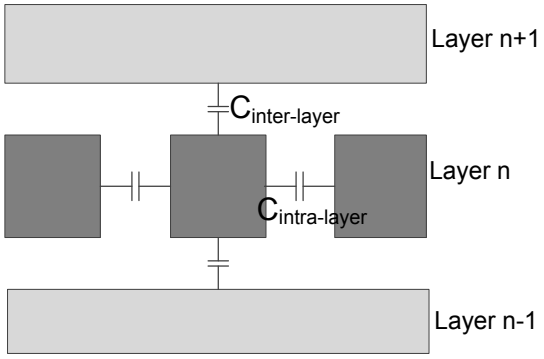


Figure 44: Components of wire coupling capacitance

Due to varying interconnect density across multiple device layers, spacing between wires on each device layer must be computed separately. The spacing between metal layers with maximum interconnect density is defined by technology, which is the minimum spacing. The device layer with the maximum wire density is assumed to have 0.12 nm wire spacing, which is the default spacing at 45nm. The wire spacing on other device layers is scaled accordingly, defined by the ratio of interconnect densities with respect to maximum density value, as shown in Eq. (42).

$$S_{DL2} = S_{min}, S_{DL1} = S_{min}\left({ID_{DL2}}/{ID_{DL1}}\right)$$

$$S_{DL3} = S_{min}\left({ID_{DL2}}/{ID_{DL3}}\right), S_{DL4} = S_{min}\left({ID_{DL2}}/{ID_{DL4}}\right) \quad (42)$$

Here, the capacitance per unit length on each device layer represented as C_{wire} is computed using Eq. (43). Where, ε_o is the air-permittivity, k_{vert} and k_{horiz} is the permittivity of dielectric material. In our analysis, we have taken SiO_2 as dielectric material with permittivity of 3.9. The width (*W*), height (*H*) and thickness (*T*) of the metal

layers remain same across multiple stacked device layers, whereas, the spacing between metal layers on a particular device layer is estimated using Eq. (42). The estimated values of spacing between metal layers and resultant wire capacitance per unit length are shown in Table 20. The device layer 2 will have the maximum density and therefore minimum spacing between the wires, resulting in maximum wire capacitance.

$$C_{wire} = \varepsilon_o \left[2k_{vert} {}^{W}/_{H} + 2k_{horiz} {}^{T}/_{S_{DL}} \right] \quad (43)$$

Table 20: Spacing between metal layers and wire capacitance on each device layer

Device Layer	Spacing (nm)	Capacitance (fF/μm)
#1	0.247	0.1175
#2	0.120	0.1797
#3	0.182	0.1382
#4	0.355	0.0967

7.1.3 Influence of interconnect density on the delay and power

In this section, we will analyze the influence of non-uniform interconnect density on the delay and power in buffered interconnect. We assume a 3D net spanning to consecutive device layers, which have different interconnect density. The length of the wire on both the device layers is the same and represented as L_{seg} in Figure 45. Here, we do not consider the different wire density on the individual device layers and perform buffer insertion using the method presented in chapter 5. TSV-aware buffer scheme inserts the same number of buffers on each device layer, represented as N_{seg}, assuming the same wire capacitance on both device layers. However, the delay in the wires on

these two device layers will be different and will depend on the unit length wire capacitance on particular layer. The delay in buffered segment on device layer #1 will be given by Eq. (44) and will depend on C_{w1}; while Eq. (45) gives the delay in buffered interconnect on device layer #2 and will depend on the wire capacitance C_{w2}.

$$D_{buf\_seg1} = \left[\frac{R_{buf}}{W}\left(C_{w1}\frac{l}{N} + C_{buf} * W(1 + p_{inv})\right) + R_w \frac{l}{N}\left(\frac{C_{w1}}{2}\frac{l}{N} + C_{buf} * W\right)\right] \quad (44)$$

$$D_{buf\_seg2} = \left[\frac{R_{buf}}{W}\left(C_{w2}\frac{l}{N} + C_{buf} * W(1 + p_{inv})\right) + R_w \frac{l}{N}\left(\frac{C_{w2}}{2}\frac{l}{N} + C_{buf} * W\right)\right] \quad (45)$$

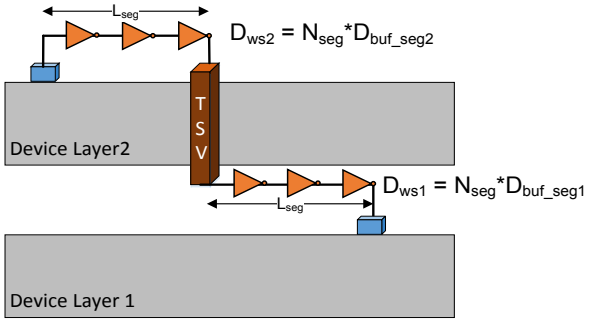


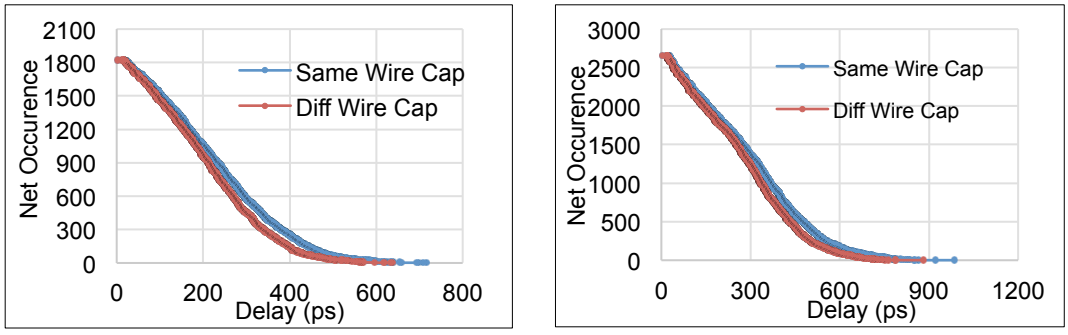
Figure 45: Buffer insertion performed on the two device layers assuming the same wire density and the estimated delay in buffered segments on each device layer assuming the different wire density

We conducted experiments to study the impact of non-uniform density on the delay in modified GSRC benchmark circuits. The TSV-aware buffer insertion technique is applied on the final floorplan assuming that the capacitance of wires is the same on all the device layers. Therefore, the *BIL* would be the same on each device layer. Then, the delay and power is estimated in the individual nets using the wire capacitance based on non-uniform interconnect density, and compared with the performance using the same wire capacitance on all the device layers.

The total delay estimated in the benchmark circuits reduces by 11%, while the estimated peak delay reduces by 12% due to nonuniform wire capacitance in 3D circuits, as shown in Table 21. The distribution of delay in individual nets of the benchmark circuits, shown in Figure 46, suggests a maximum reduction in delay of around 20%.

Table 21: Total delay, peak delay and total power in the benchmark circuits with the same wire capacitance on all device layers and different wire capacitance on individual device layers, TSV diameter 2µm, buffer and wire parameters from Table 10

Circuit	Total Delay (ns)		Peak Delay (ps)		Total Power (mW)	
	Same Wire Cap	Diff. Wire Cap	Same Wire Cap	Diff. Wire Cap	Same Wire Cap	Diff. Wire Cap
n200_exp	440.69	396.44	715.68	637.69	633.31	625.45
n300_exp	828.27	751.92	984.72	882.38	1133.08	1128.44



(a) **(b)**

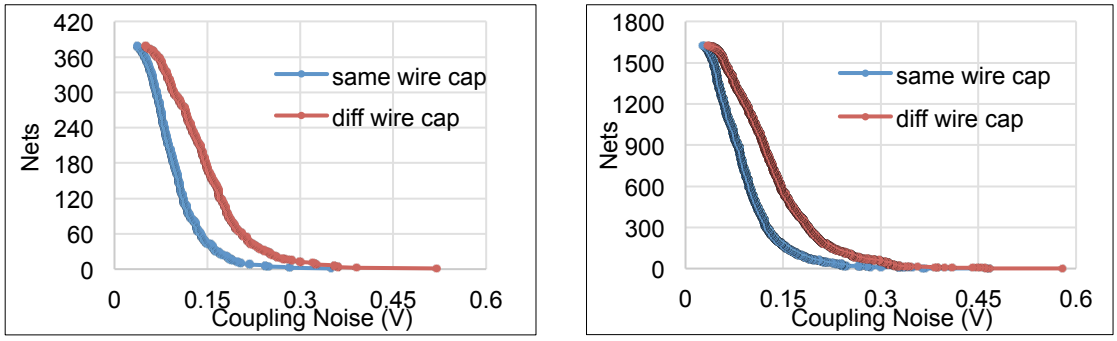
Figure 46: Delay distribution in individual nets using the same wire capacitance and different capacitances on all device layers of (a) n200_exp, (b) n300_exp

However, the total power in the interconnects does not change much with different wire capacitance across multiple stacked device layers. It is due to the fact that interconnect power consumption is primarily due to buffer power. As TSV-aware buffer insertion scheme is performed on the final floorplan, the number of buffers in the circuit with the same wire capacitance and different wire capacitance are identical. Hence, the total

power consumption in interconnects with the same and different wire capacitances is quite similar as shown in Table 20.

7.1.4 Influence on coupling noise

As discussed in the previous chapter that the wire capacitance has significant impact on the coupling noise in the 3D wires. Therefore, here we evaluate the impact of nonuniform wire density on the coupling noise. We used the empirical coupling noise model for heterogeneous integration proposed previous chapter to estimate coupling noise on the final floorplan. Figure 47 shows the distribution of coupling noise in individual nets of the circuits. The total coupling noise in the circuits increases on an average by 13% due to different wire capacitances across multiple stacked device layers. Also, we observed that the maximum increase in coupling noise in a victim nets is around 49%, suggesting that the impact of non-uniform interconnect density on the coupling noise is significant and should not be ignored.



(a) (b)

Figure 47 Distribution of coupling noise with the same wire cap or different wire cap on all device layers in (a) n100_exp, (b) n300_exp, for TSV diameter 2µm and Vsignal = 1V

7.2 Interconnect-Density Aware 3D Floorplanning

The previous section showed that the impact of non-uniform interconnect density across multiple stacked device layers on the performance of 3D circuits is significant, and should not be ignored. In this section, we present the improved 3D floorplanning approach to incorporate the effect of interconnect density during performance evaluation and optimization. First, we will present a wire capacitance-aware buffer insertion scheme to minimize delay and power on the final 3D floorplan. After final floorplan with nets-to-TSVs assignment is obtained, interconnect density and its impact on wire capacitance is evaluated. Then, the buffer insertion is performed, and the resulting delay and power is computed. Also, due to the substantial influence of different wire capacitances in individual device layers on the performance of 3D circuits, it is imperative to consider the effect of interconnect density during the floorplanning optimization. The estimated delay, power and coupling noise in the interconnects using wire capacitance-aware buffer insertion is included in the cost function and optimized at every iteration.

7.2.1 Wire Capacitance-aware Buffer Insertion

Due to different wire capacitances, the optimal buffer insertion length on the wire will not be the same. Hence, we insert buffers separately on each device layer at an optimized distance between adjacent buffers using Eq. (46). The steps of wire capacitance-aware buffer insertion technique are shown in Figure 48. First, the buffers are inserted on the wire segments starting from driver to receiver. The buffers insertion is done separately on

each device layer, where start and end buffer represents the first and last buffer inserted on each layer.

$$BIL = \sqrt{2\left(C_{buf} * R_{buf} * (p_{inv} + 1)\right) / R_w C_w} \quad (46)$$

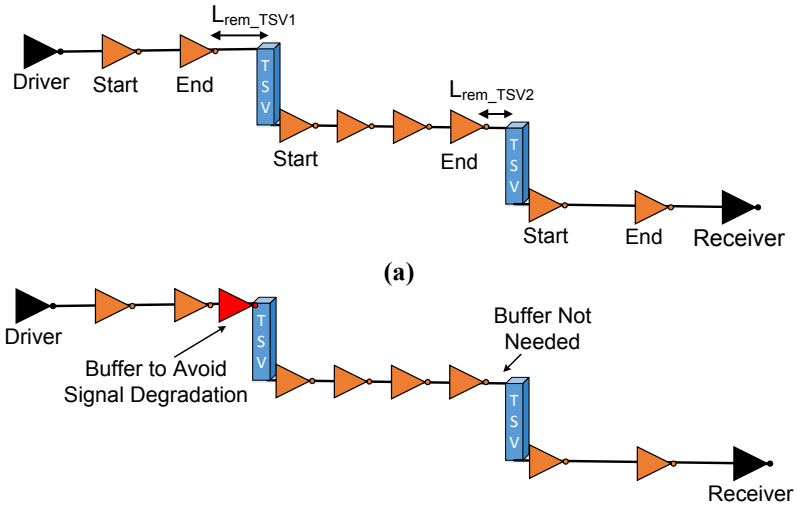


Figure 48: Buffer insertion approach for different wire capacitances on each device layer (a) Wire segment (b) TSV segment

Hence, the BIL will not be constant throughout the net for 3D nets spanning to multiple device layers. Also, there is a buffer always at the end of TSV and takes care of signal degradation across TSVs. However, we insert an additional buffer in-front of TSV if the condition in Eq. (47) is satisfied. As shown in Figure 48 (b), an extra buffer is inserted in-front of TSV on the top-device layer, whereas the buffer is not needed for TSV on intermediate device layer.

$$L_{rem\_TSV} + TSV_{wire} \geq BIL \quad (47)$$

7.2.2 Performance Optimization

We optimize the performance of 3D interconnects by using the delay-aware and coupling aware cost function and evaluating performance of the generated floorplans at each iteration. The interconnect density on each device layer is evaluated after a desired packing area is achieved to minimize the impact on the runtime. The accurate performance evaluation during the floorplanning helps achieving the true optimization of the circuit performance.

7.3 Results and Discussions

We implemented our 3D floorplanning algorithm with interconnect density-aware performance evaluation and optimization in C++/STL. The experiments were performed on a 4xDual Core Sun SPARC IV CPUs at 1.35 GHz and total 32 GB RAM.

7.3.1 Wire Capacitance-aware Buffer Insertion

In this section, we present a comparison of TSV-aware buffer insertion and wire capacitance-aware buffer insertion schemes. Both the techniques are applied on the final floorplan after evaluating the interconnect density on individual device layers. TSV-aware buffer insertion scheme presented in chapter 5, optimizes buffer insertion for individual nets, and only accounts for the number of TSVs and their RC parasitics. However, it ignores the different capacitance of segments of a 3D wire routed on different device layers.

7.3.1.1 Buffer Count

The total number of buffers in the wires are decided by the buffer insertion length. TSV-aware BIL does not take into account the nonuniform interconnect density, resulting in the same *BIL* on each device layer, as shown in Figure 49 (a). Whereas, the wire capacitance-aware BIL is optimized for individual device layers, and shows a difference of up to 60% compared to TSV-aware *BIL*. Since, the top device layer (*#4*) has lower wire capacitance, using the same *BIL* as on device layer *#2* will introduce large buffer delay, deteriorating the signal strength. Due to better optimization of *BIL* on each device layer, the wire capacitance-aware buffer insertion method reduces the total number of buffers in the tested benchmark circuits by 16%, as shown in Figure 49 (b).

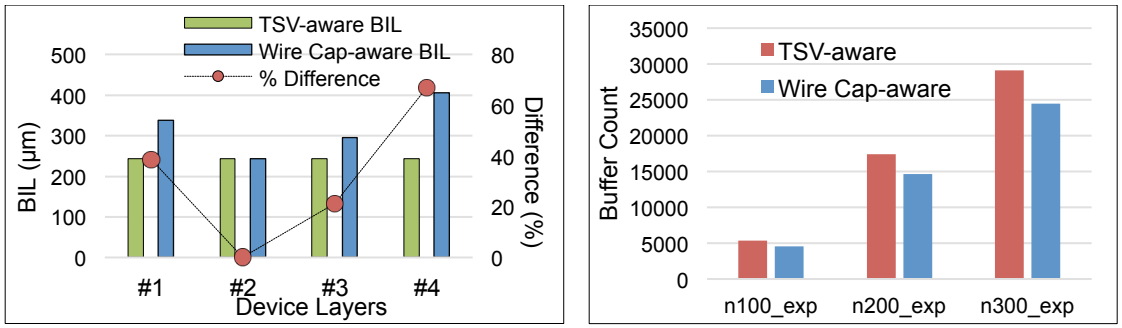


Figure 49: (a) Optimized buffer insertion length using TSV-aware and wire capacitance-aware buffer insertion length, (b) Total number of buffers in modified GSRC circuits using TSV-aware and wire capacitance-aware buffer insertion approach, TSV diameter 2µm, buffer and wire parameters are taken form Table 10

7.3.1.2 Delay and Power in Buffered Interconnects

The delay in the buffered interconnects using wire capacitance-aware buffer insertion approach is shown in Table 22, and compared with delay in wires using TSV-aware buffer insertion technique. The wire capacitance-aware buffer insertion method reduces total delay and peak delay in the circuits by 12% and 16%.

Table 22: Comparison of total and peak delay in the circuits using TSV-aware and wire capacitance-aware buffer insertion approach for TSV diameter 2µm, wire and buffer (BUF_X8) parameters are taken from Table 10

Circuit	Total Delay (ns)			Peak Delay (ps)		
	TSV aware	Wire Cap aware	% Diff	TSV aware	Wire Cap aware	% Diff
n200_exp	376.83	334.27	12.58	683.61	571.07	16.46
n300_exp	751.93	660.75	12.12	882.38	743.53	15.74

The significant reduction in delay in individual nets achieved using wire capacitance-aware buffer insertion is due to the reduction in delay of wire segments primarily on top most and bottom most device layers, as shown in Figure 50. The reduction in total delay on device layer #4 is 46%, on device layer #1 by 38%, and on device layer #3 by 22%.

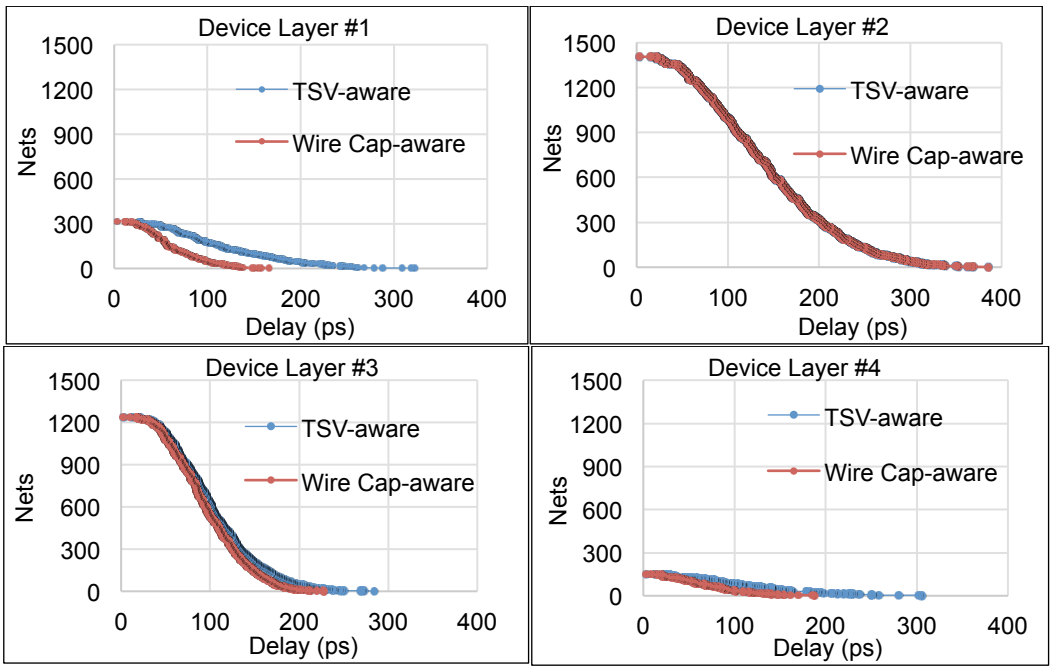


Figure 50: Delay on each device layer with TSV-aware and wire cap-aware buffer insertion in n300_exp circuit for TSV diameter 2µm, buffer and wire parameters are taken from Table 10

Total power consumption with different buffer sizes is shown in Table 23. It can be seen that wire capacitance-aware buffer insertion helps reducing total power consumption in the interconnects by 14% for different buffer specifications.

Table 23: Total power consumption in the interconnects with BUF_X4, BUF_X8 and BUF_X16 using TSV-aware and wire cap-aware buffer insertion using CF2, TSV diameter 2µm, buffer and wire parameters are taken from Table 10

Circuit	Total power (mW)					
	BUF_X4		BUF_X8		BUF_X16	
	TSV aware	Wire Cap aware	TSV aware	Wire Cap aware	TSV aware	Wire Cap aware
n100_exp	178.5	151.6	212	179.3	375.3	316.4
n200_exp	335.3	288.6	580.9	509.1	1172.6	1031
n300_exp	540.1	467.4	986	864.8	1933	1701.3
Norm.	1.0	0.858	1.0	0.866	1.0	0.86

7.3.2 Interconnect Density-aware Performance Optimization

7.3.2.1 Power-Delay Product

As the wire capacitance on each device layer is not the same, floorplanning with the assumption that wires have same RC delay on all device layers will result in suboptimal floorplans. In order to achieve true performance optimization during floorplanning, it is critical to model the performance of the layout accurately. Figure 51 shows the power-delay product obtained by optimizing performance and compared with the results when optimization is done assuming same wire capacitance on all the device layers. The results suggest that ignoring the different wire capacitance on individual device layers during optimization will result in the inferior quality of solutions, and up to 17% higher power-delay product.

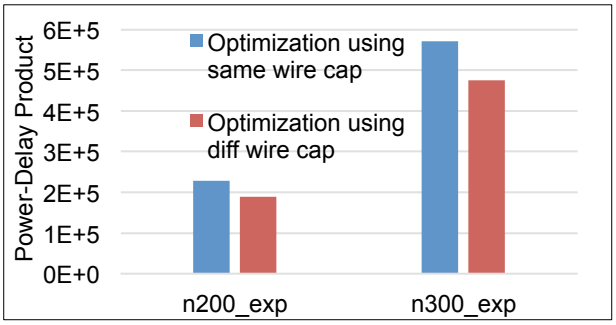


Figure 51: Power-delay product obtained after floorplanning optimization by including the delay and power in the cost function estimated based on same wire capacitance and different wire capacitance

7.3.2.2 Coupling Noise

In order to optimize the coupling noise during floorplanning, we included the coupling noise in the cost function. The coupling noise-aware cost function takes in to account the

different wire capacitance on each device layer to minimize the coupling noise and number of violating victim nets in the circuits. Table 24 shows that considering different wire capacitances during optimization helps in reducing the coupling noise by up to 44% and number of violating victim nets by 100%, as compared to optimizing coupling noise with the same wire capacitance. This reduction in coupling noise suggests that the optimized position of blocks and TSV islands would change for nonuniform wire capacitances across multiple stacked device layers.

Table 24: Total coupling noise, number of violating and non-violating nets with CF3 using same wire capacitance and different wire capacitance using TSV diameter 2µm and V_{signal} = 1.0V

Circuit	Total Noise (V)			# Violating Nets (V_{noise} > 0.1 V)			# Non-violating Nets (V_{noise} < 0.1 V)	
	coupling aware with same cap	coupling aware with diff cap	% Diff	coupling aware with same cap	coupling aware with diff cap	% Diff	coupling aware with same cap	coupling aware with diff cap
n100_exp	43.41	27.43	36.8	17	0	100	533	550
n200_exp	87.32	50.26	42.4	146	5	96.6	1054	1195
n300_exp	127.88	72.13	43.6	538	61	88.6	743	1220

7.3.2.3 Delay vs Coupling Noise Trade-off

As shown in previous experiments, the nonuniform interconnect density has conflicting impact on the delay and coupling noise. The total delay in the interconnects go down due to lesser impact of wire capacitance. However, as a result of smaller effect of wire capacitance, large TSV capacitance becomes critical, increasing the overall coupling noise in the wires. Hence, the adjustment of blocks and TSVs positions to minimize the total coupling noise will influence the delay in the circuit. The optimized position of

TSVs and blocks to achieve low coupling noise in the nets may not necessarily gives the best delay values. We use the cost function *CF3* to optimize the overall performance in the circuits. The weight (ρ) for delay in the circuit is kept constant, and the weight (δ) for coupling is varied as a factor of ρ. The effect of variation in γ on the delay and coupling noise in the circuit is shown in Figure 52. It can be seen that for $\rho/\delta \leq 1$, the percentage change in both delay and noise is below 10%. However, for $\rho/\delta > 1$, the coupling noise reduces by more than 50%. The maximum reduction achieved in coupling noise is around 66%, while compromising the delay in the circuit by 60%. Figure 52 shows that one has to be careful with the coupling noise term as the delay can increase drastically, for nonuniform capacitance across different device layers.

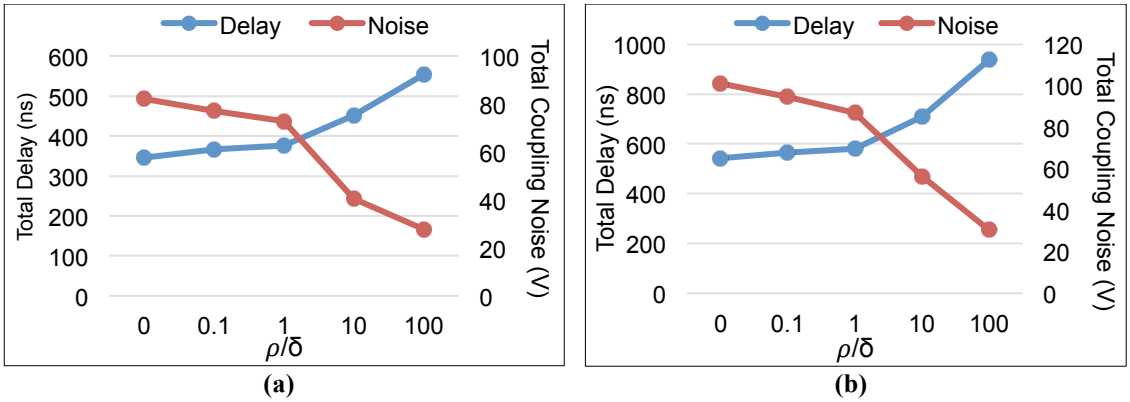


Figure 52: Delay and Noise trade-off with different weights for (a) n200_exp, (b) n300_exp, for TSV diameter 2µm and buffer parameters specified in Table 10

7.4 Interconnect Planning Techniques

The performance of semi-global interconnects can be greatly improved by using interconnect synthesis and optimization techniques such as buffer insertion, layer

assignment, wire sizing and wire spacing. The buffer insertion methodology to handle non-uniform interconnect density has been discussed in the previous sections. In this section, we provide a brief overview of other existing techniques for interconnect optimization for high-performance VLSI circuits. These techniques can be extended to multi-layer interconnect planning problem in 3D ICs, by appropriately incorporating the existent nonuniform interconnect density across multiple device layers. An interconnect-driven layout design flow can be critical in determining the overall performance, cost and routing requirements in 3D circuits. The interconnect planning techniques include the following methods to improve overall performance of interconnects.

7.4.1 Optimizing the width of the wires

Wire width on the individual device layers can be optimized using the wire width planning methodology proposed in [88]. Their method requires the length of the wires and buffer specifications to obtain optimum width of the wires. The estimated interconnect density can be used for predicting and optimizing the width of metal layers (semi-global) used for inter-block connections on individual device layers separately. We also suggest the use of narrow wires in the intermediate device layers to increase the interconnect density and keeping the overall cost low. Incorporating wire-sizing during early layout planning can also impact the allocation of buffering resources in the later stages of routing and hence, should be explored.

7.4.2 Increasing the wire spacing in the intermediate device layers

Another method to improve the interconnect performance in 3D ICs, would be increasing the spacing between semi-global metal layers in the intermediate device layers, which have higher wire density. However, to achieve similar spacing between the wires equivalent to maximum spacing of all the device layers, would result in chip footprint to increase by around 3 times. Despite the increase in routing area by 3 times, as shown in Figure 26, the 3D chip footprint will still be 25% smaller than 2D footprint.

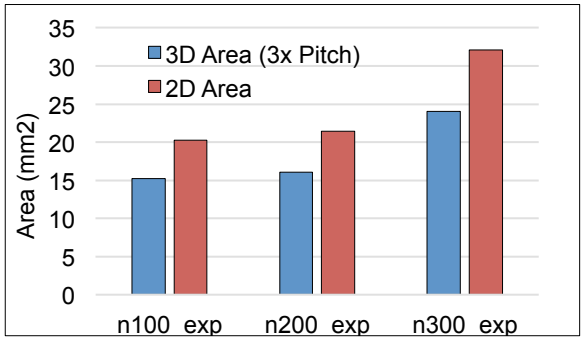


Figure 53: 3D footprint with wire spacing on all device layers equal to 3x the minimum spacing, and 2D with minimum wire spacing

7.4.3 Increasing the number of semi-global metal layers

The performance of interconnect presented in previous section is done assuming the same number of metal layer stack on each device layer. But, due to higher interconnect density in the intermediate device layers, we suggest the use of more number of semi-global metal layers in those device layers. This may increase the overall cost, however, it

will reduce the interconnect density in the intermediate device layers and help achieve optimal interconnect RC performance.

7.5 Summary

A 3D floorplanning approach is discussed that considers the influence of non-uniform interconnect density on the wire capacitances across multiple stacked device layers, for early and realistic estimation of the delay, power and coupling noise in the circuit. Buffer insertion approach is enhanced to optimize the buffer insertion length for individual device layers, improving the delay and power in 3D interconnects by up to 14%.

TSV position is critical for accurate estimation of interconnect density on individual device layers. Ignoring TSV position will cause interconnect density on a device layer to differ by up to 25%, impacting the estimation of wire capacitance and performance in 3D circuits. The interconnect density is highest in the intermediate layers, whereas the top layer has least density of interconnects.

The performance optimization during 3D floorplanning requires accurate modeling of wire capacitance on each device layer, and hence the impact of non-uniform interconnect density should not be ignored. Including the estimated coupling noise based on different wire capacitances in the cost function helps to minimize the total coupling noise in the circuits by 40%, which can be seen in Table 23. While, the count of violating victim nets in the test circuits reduce on an average by 95%, as compared to coupling noise with the same wire capacitance, as shown in Table 23. However, minimizing coupling noise will

influence the delay and power in the circuit and requires careful selection of weights of the parameters in the cost function. Introducing too many parameters in the cost function reduce the solution space, limiting the solution quality.

8. Conclusions and Future Work

Through silicon via (TSV) based 3D integrated circuits have inspired a novel design paradigm which explores the vertical dimension, in order to alleviate the performance and power limitations associated with long interconnects in 2D circuits. TSVs enable vertical interconnects across stacked and thinned dies in 3D-IC designs, resulting in reduced wirelength, footprint, faster speed, improved bandwidth and lesser routing congestion. However, the influence of TSV area, position and electrical characteristics on the 3D interconnects is not negligible, and must not be ignored. In this work, we presented an early design exploration approach using developed 3D floorplanning tool for more accurate and realistic evaluation of performance, power, and coupling noise in the 3D ICs. Moreover, solutions are presented which help to achieve 3D layouts with optimized timing, power and signal integrity considering the distribution of wires and TSVs on the layout. This thesis also presented methods to accurately model these performance parameters on the floorplan considering TSV position and area, as well as accurate TSVs and interconnect RC. An accurate benchmarking of TSV and wire RC parasitics within the 3D floorplanning framework facilitates better design decisions for later stages in the 3D IC design flow, so that the overall timing closure and design convergence can be better achieved.

8.1 Conclusions & Contributions

A TSV- and delay-aware floorplanning algorithm is presented resulting in 5% shorter wirelength and 21% reduction in TSV count compared to the recent works in [16-18]. The total delay reduced between 10% to 12% with a delay-aware cost function instead of a separate minimization of wirelength and TSVs. The non-deterministic nets-to-TSVs assignment improved delay on an average by 8% compared to fixed-assignment. The published papers related to this topic are as follows:

- M. Ali, M. A. Ahmed, M. Chrzanowska-Jeske, "TSV Stress Aware Performance and Reliability Analysis", *19th IEEE Intl. Conf. on Electronics, Circuits and Systems*, 19 February 2012.
- M. A. Ahmed, M. Chrzanowska-Jeske "Delay and Power Optimization with TSV Aware 3D Floorplanning", *15th Intl. Symposium on Quality Electronic Design*, 07 April 2014.
- M. A. Ahmed, M. Chrzanowska-Jeske, "TSVs in Early Layout Design Exploration for 3D ICs", *5th Latin American Symposium on Circuits and Systems*, 26 May 2014.
- M. A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske, "3D Floorplanning with Nets-to-TSVs Assignment", *21st IEEE Intl. Conf. on Electronics, Circuits and Systems,* 26 February 2015.
- M. A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske, "Dynamic Nets-to-TSVs Assignment in 3D Floorplanning", *Intl. Symposium on Circuits and Systems,* 30 July 2015

- M. A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske "TSV-and delay-aware 3D-IC floorplanning"**,** *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 2, pp. 235-248, March 2016.

In chapter 4, improvements to the analytical model [46] for computation of TSV capacitance is presented which models the TSV coupling with neighboring wires and TSVs. The component of TSV capacitance due to TSV-to-wire coupling is modified to incorporate the effect of multiple wires over TSV cross-section, and is better fitted for smaller TSVs and wire dimensions, reducing the peak error in the existing model [46] of 6% to around 2%. TSV capacitance is significantly influenced by spatial distribution of wire and TSVs, and hence, the presented model computes TSV capacitance with the average error below 1% compared to RAPHAEL simulations. The published paper related to the paper are as follows:

- M. A. Ahmed, M. Chrzanowska-Jeske, "TSV Capacitance Aware 3D Floorplanning", *IEEE 3D System Integration Conf.,* 9 January 2014.

Chapter 5 presented an approach for better estimation of delay and power on 3D floorplan considering TSV coordinates and nets-to-TSVs assignment. To minimize the propagation delay in 3D interconnects with minimal usage of buffers, the distance between buffers is optimized for each net considering the delay incurred by TSVs. The variable buffer insertion length strategy during 3D floorplanning minimizes delay with

25% lesser buffers, reducing evaluated power consumption in interconnects by 16% - 21%. The buffer planning around TSVs considering the position of TSVs on 3D wires reduced the estimated signal degradation across TSVs by 12%. The statistical analysis shows that using the typical cost function (CF1) during floorplanning does not account for the combined effect of TSVs and wirelength on the delay and coupling noise in the circuits, resulting in inferior solution. Inclusion of the delay term in the cost function accounts for the variable impact of TSV RC parameters on the wires of different length to minimize delay in the circuit. The published papers related to this topic are as follows:

- M. Chrzanowska-Jeske, M. A. Ahmed, "Power Efficiency of 3D vs 2D ICs". *19th IEEE Faible Tension Faible Consommation (FTFC),* 20-21 June 2013.
- M. A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske, *"*Performance Optimization and Power Efficiency in 3D IC with Buffer Insertion Scheme*",* 29th *IEEE Intl. System-on-Chip Conf. (SOCC)*, Sept. 6-9 2016.
- M. A. Ahmed, S. Mohapatra, M. Chrzanowska-Jeske, "Buffered Interconnects in 3D IC Layout Design", *Proc. of the 18th IEEE/ACM Intl. Workshop on System level Interconnect Prediction (SLIP),* 24 November 2016.

In Chapter 6, an empirical model based on curve fitting to simulated data is proposed for computing coupling noise introduced by TSVs in the wires spanning to multiple device layers. The coupling noise computed using the proposed model correlates well

with the HSpice simulations with an average error below 2%, for the range of wirelength on each device layer between 10μm to 2.5mm and TSV capacitance between 5 fF to 50 fF. The coupling noise on the floorplan minimized using detailed nets-to-TSVs assignment reduces the coupling noise on an average by 25%. The worst and total coupling noise in the victim nets using diagonal TSV arrangement reduces by 21% and 30% respectively, where the model for TSV-to-TSV coupling is derived from the regular TSV arrangement. This suggested improvement in coupling noise with the diagonal arrangement are shown for larger TSV pitch and need to be verified by the simulation methods. Further experiments need to be conducted to prove the effectiveness of diagonal TSV arrangement for more practical TSV pitch, which is equal to twice of its diameter.

Also, a nonuniform TSV pitch method is proposed to minimize coupling noise with smaller area overhead. The total area and wirelength reduction achieved using nonuniform TSV pitch is more than 50%, as compared to uniform increase of TSV by twice. The coupling noise term in the cost function CF3b considers the impact of large TSV capacitance on the short wires to monitor the distribution of TSVs to the nets, reducing the coupling noise by up to 34%. Although, the redistribution of TSVs to nets increases the delay and power in the interconnects by 6% and 8% respectively (Table 14), there are 28% floorplans obtained using CF3b that have the same or better delay compared to the mean delay value obtained using CF2. As the TSV diameter will go down, due to smaller TSV capacitance, the influence of increase weights of coupling noise term (CF3) on the delay will decrease. It is expected that the increase in the delay

with δ with 1µm TSV diameter would be much less than the delay rise for 2µm TSV. Also, the KOZ for TSVs with 1µm diameter would be much less. Therefore, increasing TSV pitch to reduce TSV-to-TSV coupling should have significantly lesser impact on the chip footprint and the wirelength. Finally, it is important to choose appropriate weight functions as they can noticeably change the quality of the floorplanning solutions.

In chapter 7, an interconnect density-aware approach during 3D floorplanning for performance evaluation and optimization in 3D circuits is presented. The developed floorplanning approach considers accurate TSV area, position and delay, and different wire capacitances based on non-uniform interconnect density across multiple stacked device layers to predict delay, power and coupling noise in the circuit. The interconnect density on each stacked device layer of 3D-IC needs to be computed separately. TSV position is critical to determine an accurate interconnect density on each device layer. The influence of the non-uniform interconnect density on the overall performance of the 3D circuits is significant, and should not be ignored.

A wire capacitance-aware buffer insertion method is discussed that takes in to account the interconnect density on individual device layers and TSV position on the wire to minimize the delay and power in the interconnects and across TSVs, avoiding excessive usage of buffers. Including the performance parameters such as delay and coupling noise estimated considering nonuniform wire density across multiple device layers helps achieve 3D floorplans with superior performance.

However, the weight functions of coupling noise and delay in the cost function should be carefully chosen in order to achieve an optimized overall performance in the 3D circuits. Interconnect planning needs to be done separately for each device layer due to nonuniform interconnect density in 3D circuits. It will help improving interconnect RC performance and density keeping the overall cost low.

In summary below is the list of specific contributions:

- A delay-aware 3D floorplanning approach is proposed that captures the variable impact of TSVs on the wires of different length to minimize overall delay in 3D ICs.
- Enhancing the floorplanning tool developed by R.K. Nain [87] with a novel approach to nets-to-TSVs assignment by incorporating random moves of nets between TSV islands during floorplanning helps in further increasing the solution search space for optimal nets-to-TSVs assignment procedure.
- A novel buffer insertion scheme integrated with nets-to-TSV assignment process that appropriately models the TSV RC delay impact on interconnect delay to determine the optimum interval between adjacent buffers. The approach is more suitable for 3D designs with the uniform wire density across stacked device layers.
- A simple empirical model for estimation of TSV induced coupling noise in 3D interconnects is proposed. The viability of the proposed model applied for heterogeneous 3D integration is shown, where the stacked layers are fabricated using different technology nodes.

- Coupling noise is directly included in cost function which guides the nets-to-TSVs assignment to simultaneously optimize the position of blocks and TSVs in order to achieve minimized coupling noise. A detailed nets-to-TSV assignment method is included to further minimize TSV coupling noise within each island.
- Diagonal TSV arrangement can be effective in reducing the coupling noise in interconnects for larger TSV pitch by reducing TSV-to-TSV coupling capacitance. The nonuniform TSV pitch methods help reducing TSV-to-TSV coupling capacitance specifically for TSVs which suffer from the worst coupling, thereby reducing coupling noise in 3D circuits without incurring any significant area overhead.
- The non-negligible impact of TSV position within an island on overall coupling noise is demonstrated. The effect of TSV islands' dimensions on the coupling noise in 3D circuits is also presented.
- A 3D floorplanning tool is presented that considers the interconnect density on the individual device layers for more accurate performance evaluation/optimization in TSV-based 3D ICs.
- For nonuniform wire density, a wire capacitance-aware buffer insertion approach is presented that determines optimal distance between adjacent buffers for the individual device layer. The proposed approach incorporates a scheme of buffer planning around TSVs in 3D wires, by considering the actual coordinates of TSVs along a 3D wire (TSV position-aware) ensuring minimization of signal degradation

across TSVs, but also helps to avoid excessive usage of buffers, which incurs additional area and power.

8.1.1 Conclusions

- TSV area and positions are critical for accurate estimation of performance in 3D circuits. Ignoring TSVs during early analysis will result in the underestimation of power and performance in 3D ICs.
- Impact of TSV delay on the overall performance of the 3D interconnects will depend on the length of the wire and wire RC parasitics. Hence, the delay-aware cost function obviates the efforts required to balance the weight contributions of wirelength and TSVs in the wirelength-aware floorplanning.
- TSV-aware buffer insertion length for individual nets helps to minimize delay and power in interconnects for contact resistance of TSVs exceeding 1Ω.
- The coupling noise in a 3D wire is not only influenced by TSV-to-TSV coupling, but is also strongly impacted by wire capacitance and number of TSVs in the wire.
- For designs with the non-uniform wire capacitance across multiple device layers, locations of TSVs on a floorplan will play an important role in determining the total wire capacitance and hence, overall coupling noise in the wire.

- TSVs assigned to shorter wires have significantly larger impact on the coupling noise and therefore should be assigned to TSVs with smaller TSV-to-TSV coupling capacitances.
- The non-uniform interconnect density in 3D circuits will significantly impact the performance of 3D circuits and should not be ignored in early design exploration.
- The wire capacitance of individual devices need to be carefully assessed prior to performing TSV-aware buffer insertion in the interconnects.
- The TSV-to-TSV coupling capacitance between diagonal TSVs should be verified by simulation methods.

The other publications not related to 3D-IC are:

- M. A. Ahmed, S. Pinge, M. Chrzanowska-Jeske, "Fast Floorplanning for Fixed-Outline and Nonrectangular Regions", *19th IEEE Intl. Conf. on Electronics, Circuits and Systems*, 2012.
- M. Ali, M. A. Ahmed, M. Chrzanowska-Jeske, "Stochastic Analysis of CNFET circuits using Enhanced Logical Effort Model in the presence of Metallic tubes", *21st IEEE Intl. Conf. on Electronics, Circuits and Systems*, 2014, 7-10 December 2014.
- M. Ali, M. A. Ahmed, M. Chrzanowska-Jeske, "Logical Effort Model for CNFET-based circuits", *IEEE 14th Intl. Conf. on Nanotechnology*, pp. 460-465, Aug. 2014.

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- M. Ali, M. A. Ahmed, M. Chrzanowska-Jeske, "Fast and Accurate Evaluation of delay in CNFET circuits", *IEEE 16th Intl. Conf. on Nanotechnology*, 22-25 August 2016.

8.2 Future Work

This thesis proposed the methods to evaluate and optimize the performance of 3D circuits during early design phase using expanded 3D floorplanning tool build on the original floorplanning code developed by Wang [35] and Nain [37] [84] [87]. Some of the possible future works that can be critical to overcome the major challenges preventing the usage of 3D integrated circuits, are as follows:

- Use of variable island sizes or isolated TSVs in 3D floorplanning tool can be critical in optimizing the 3D performance. Isolated TSVs can be placed close to the blocks and help improving the wirelength in the design. But, larger silicon area occupied by isolated TSVs will negatively impact the wirelength.
- The algorithms for nets-to-TSVs assignment are required that can be performed during floorplanning iterations considering the impact of TSV RC parameters, and also minimizing the runtime.
- For irregular TSV arrangements, TSV-to-TSV coupling will show a large variation depending on the number of neighboring TSVs and their distances. It

will be interesting to analyze the performance of 3D interconnects for irregular arrangement of TSVs.

- The noise introduced in the 3D wires due to inductive coupling between TSVs need to be included for power, ground and clock signals. As the big-size TSVs are used for these global signals, and the influence of inductive coupling cannot be ignored.

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Appendix: TSV Capacitance Components

1 Components of TSV Capacitance

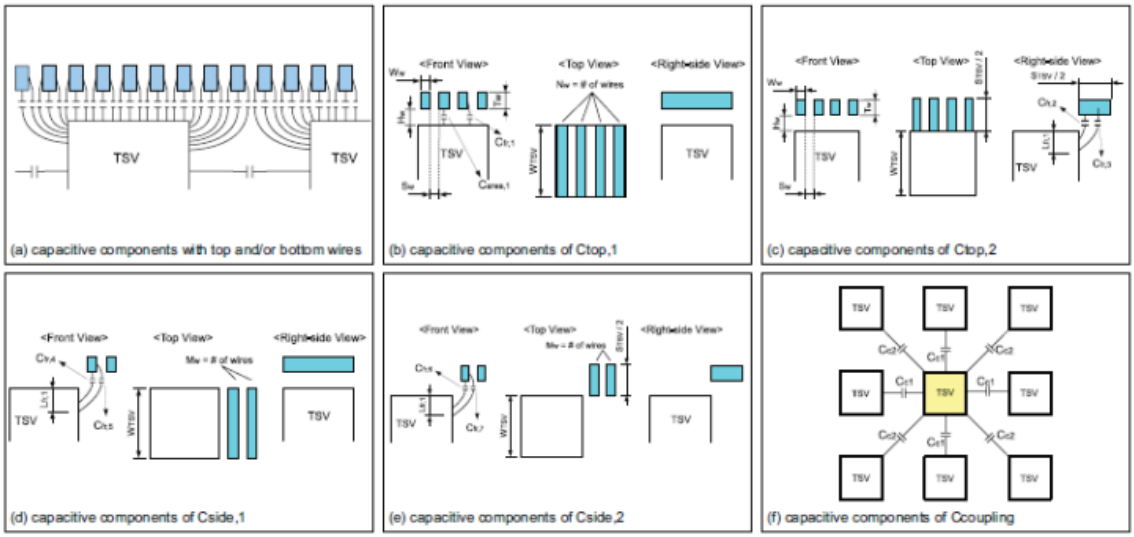

Figure 1.1: Capacitive components of TSVs for via-first TSV [46]

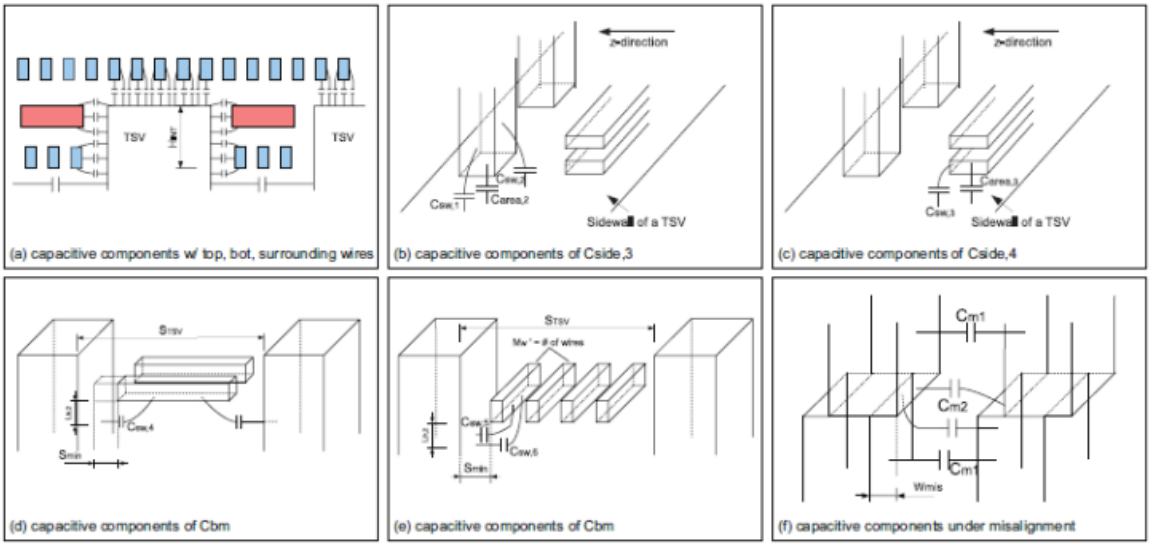

Figure 1.2: Capacitive components of TSVs for via-last TSV [46]

2 Modeling of TSV Capacitance

Table 2.1: Setting of variables used for TSV computation, CF (Capacitance Function) & Series means component in series [46]

		Series	C.F.	W	S	T	H	S_1	S_2
$C_{\text{top},1}$	$c_{\text{area},1}$		$c_{\text{a,w-g}}$	W_{w}	-	-	H_{w}	-	-
	$c_{\text{fr},1}$		$c_{\text{f,w-g}}$	-	-	T_{w}	H_{w}	-	-
$C_{\text{top},2}$	$c_{\text{fr},2}$		$c_{\text{sw,top}}$	$L_{\text{fr},1}$	H_{w}	$\frac{S_{\text{TSV}}}{2}$	0	-	-
	$c_{\text{fr},3}$	c_{s1}	$c_{\text{sw,top}}$	$\frac{S_{\text{w}}}{2}$	0	T_{w}	$\frac{H_{\text{w}}}{2}$	0	S_{w}
		c_{s2}	$c_{\text{sw,top}}$	$L_{\text{fr},1}$	$\frac{H_{\text{w}}}{2}$	$\frac{S_{\text{TSV}}}{2}$	0	-	-
$C_{\text{side},1}$	$c_{\text{fr},4}(m)$		$c_{\text{sw,top}}$	$\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	$H_{\text{w}} + (2m-1)\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	W_{w}	$m \cdot S_{\text{w}} + (m-1)W_{\text{w}}$	-	-
	$c_{\text{fr},5}(m)$		$c_{\text{top,top}}$	$\frac{L_{\text{fr},1}}{4 \cdot M_{\text{w}}}$	$H_{\text{w}} + m\frac{L_{\text{fr},1}}{M_{\text{w}}}$	W_{w}	$m \cdot S_{\text{w}} + (m-1)W_{\text{w}}$	-	-
$C_{\text{side},2}$	$c_{\text{fr},6}(m)$	c_{s3}	$c_{\text{sw,top}}$	$\frac{S_{\text{TSV}}}{2}$	H_{w}	$\frac{S_{\text{TSV}}}{2}$	0	-	-
		$c_{\text{s4}}(m)$	$c_{\text{sw,top}}$	$\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	$S_{\text{w}} + (2m-1)\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	W_{w}	$m \cdot S_{\text{w}} + (m-1)W_{\text{w}}$	-	-
	$c_{\text{fr},7}(m)$	c_{s5}	$c_{\text{sw,top}}$	$\frac{S_{\text{w}}}{2}$	0	T_{w}	H_{w}	0	S_{w}
		c_{s6}	$c_{\text{sw,top}}$	$\frac{S_{\text{TSV}}}{2}$	H_{w}	$\frac{S_{\text{TSV}}}{2}$	0	-	-
		c_{s7}	$c_{\text{sw,top}}$	$\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	$S_{\text{w}} + (2m-1)\frac{L_{\text{fr},1}}{2 \cdot M_{\text{w}}}$	S_{w}	$m \cdot S_{\text{w}} + (m-1)W_{\text{w}}$	-	-
$C_{\text{side},3}$	$c_{\text{area},2}$		$c_{\text{a,w-g}}$	W_{w}	-	-	S_{min}	-	-
	$c_{\text{sw},1}$		$c_{\text{sw,top}}$	$\frac{S_{\text{w}}}{2}$	0	$\frac{S_{\text{w}}}{2}$	S_{min}	0	S_{w}
	$c_{\text{sw},2}$		$c_{\text{sw,top}}$	$\frac{H_{\text{w}}}{2}$	0	W_{w}	S_{min}	0	H_{w}
$C_{\text{side},4}$	$c_{\text{area},3}$		$c_{\text{a,w-g}}$	T_{w}	-	-	S_{min}	-	-
	$c_{\text{sw},3}$		$c_{\text{sw,top}}$	$\frac{H_{\text{w}}}{2}$	0	W_{w}	S_{min}	0	H_{w}
$C_{\text{side},5}$	$c_{\text{sw},4}$		$c_{\text{sw,top}}$	$L_{\text{fr},2}$	0	$\frac{S_{\text{TSV}}-2S_{\text{min}}}{2}$	S_{min}	-	-
$C_{\text{side},6}$	$c_{\text{sw},5}(m)$		$c_{\text{sw,top}}$	$\frac{L_{\text{fr},2}}{2M'_{\text{w}}}$	$\frac{(2m-1)L_{\text{fr},2}}{2M'_{\text{w}}}$	W_{w}	$S_{\text{min}} + (m-1)W_{\text{w}} + (m-1)S_{\text{w}}$	-	-
	$c_{\text{sw},6}(m)$		$c_{\text{top,top}}$	$\frac{L_{\text{fr},2}}{4M'_{\text{w}}}$	$m\frac{L_{\text{fr},2}}{M'_{\text{w}}}$	W_{w}	$S_{\text{min}} + m \cdot W_{\text{w}} + (m-1)S_{\text{w}}$	-	-
C_{m2}			$c_{\text{sw,top}}$	W_{mis}	S_{TSV}-W_{mis}	W_{mis}	0	-	-

3 MATLAB code for Optimized BIL

$t_{pd} = N*[(R_{buf}/W_{buf})*(C_{wire}*(L_{wire}/N) + C_{buf}*W_{buf}(1+p_{inv})) + R_{wire}*(L_{wire}/N)*(C_{wire}/2*(L_{wire}/N)+ C_{buf} * W_{buf})] + N_{TSV}*[R_{buf}/W_{buf} *(C_{TSV} + C_{buf} *W(1+ p_{inv})) + R_{TSV}*(C_{TSV}/2 + C_{buf} * W_{buf})]$

$t_{pd1} = N*(R_{buf} /W_{buf})* C_{wire}*(L_{wire}/N);$
$t_{pd2} = R_{buf} * C_{buf} *N*(1+ p_{inv});$
$t_{pd3} = N* R_{wire} *(C_{wire}/2)*(L_{wire}/N)^2;$
$t_{pd4} = N* R_{wire} *(L_{wire}/N)*C_{buf} * W_{buf};$
$t_{pd5} = N_{TSV} *(R_{buf}/W_{buf})* C_{TSV};$
$t_{pd6} = R_{buf} * C_{buf} * N_{TSV} *(1+ p_{inv});$
$t_{pd7} = (N_{TSV}* R_{TSV} * C_{TSV})/2;$
$t_{pd8} = N_{TSV}* R_{TSV}* C_{buf} * W_{buf};$

$del\_pd1 = diff (t_{pd1}, N, W_{buf});$
$del\_pd2 = diff (t_{pd2}, N, W_{buf});$
$del\_pd3 = diff (t_{pd3}, N, W_{buf});$
$del\_pd4 = diff (t_{pd4}, N, W_{buf});$
$del\_pd5 = diff (t_{pd5}, N, W_{buf});$
$del\_pd6 = diff (t_{pd6}, N, W_{buf});$
$del\_pd7 = diff (t_{pd7}, N, W_{buf});$
$del\_pd8 = diff (t_{pd8}, N, W_{buf});$

$del\_pd1 = 0;$
$del\_pd2 = R_{buf} * C_{buf} *(1+ p_{inv});$
$del\_pd3 = - R_{wire}*(C_{wire}/2) *(L_{wire} /N)^2;$
$del\_pd4 = 0;$
$del\_pd5 = 0;$
$del\_pd6 = 0;$
$del\_pd7 = 0;$
$del\_pd8 = N_{TSV}* R_{TSV} *C_{buf};$

$R_{buf} * C_{buf} *(1+ p_{inv}) - R_{wire} *(C_{wire}/2) *(L_{wire} /N)^2 + N_{TSV}* R_{TSV}* C_{buf} = 0$
$R_{wire} *(C_{wire}/2)* (L_{wire} /N)^2 = R_{buf} * C_{buf} *(1+ p_{inv}) + N_{TSV}* R_{TSV}* C_{buf}$
$(L_{wire}/N)^2 = 2 * (R_{buf} * C_{buf} *(1+ p_{inv}) + N_{TSV}* R_{TSV}*C_{buf})/ (R_{wire} * C_{wire})$
$(L_{wire}/N) = sqrt (2 * (R_{buf} * C_{buf} *(1+ p_{inv}) + N_{TSV}* R_{TSV} * C_{buf})/ (R_{wire} * C_{wire}))$