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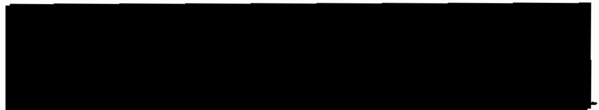
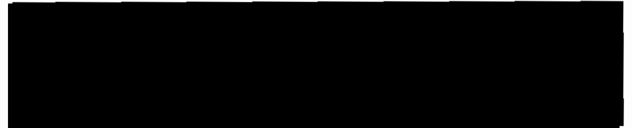
AN ABSTRACT OF THE THESIS OF Joachim Karl Wilhelm Duerr for the Master of Science in Mechanical Engineering presented September 4,1990.

Title: Finite Element Analysis of Thermal Stresses in Semiconductor Devices.

APPROVED BY THE MEMBERS OF THE THESIS COMMITTEE:



Hormoz Zarefar, Chair



Faryar Etesami

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Scott Wells

The failure of integrated circuit due to Silicon fracture is one of the problems associated with the production of a semiconductor device. The thermal stresses, which result in die cracking, are for the most part induced during the cooling process after attaching the die with

Gold-Silicon solder. Major factors for stress generation in material systems are commonly large temperature gradients and substantial difference in coefficients of thermal expansion.

This research covers the thermal stresses introduced upon cooling a composite Silicon device. A transient thermal analysis has been performed to determine the temperature gradients. The stress distribution has been investigated. For both analyses the Finite Element Method has been applied. Various parameters such as center and edge voids as well as varying thickness of the Eutectic layer have been taken into account.

The magnitude of the induced stresses was found to increase with increasing thickness of the eutectic layer. Center voids induce a new area of high stresses which can exceed the stresses at the edge of the device. Edge voids change the stress distribution and increase the tensile stresses in the top surface of the device. Thermal stresses due to nonuniform cooling of the device were found to be insignificant. The probability of die cracking depends mainly on the magnitude of the residual stresses and on the quality of the surfaces and edges of the die.

FINITE ELEMENT ANALYSIS OF THERMAL STRESSES IN SEMICONDUCTOR DEVICES

by

JOACHIM KARL WILHELM DUERR

A thesis submitted in partial fulfillment of the requirements for the degree of

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in
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Portland State University
1992

TO THE OFFICE OF GRADUATE STUDIES:

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TABLE OF SYMBOLS

Symbol	Name / unit
α	Coefficient of thermal expansion in $1/^{o}C$
k_x, k_y, k_z	heat conductivity coefficients
μm	micro meter 10^{-6} meter
mm	milli meter 10^{-3} meter
cm	centi meter 10^{-2} meter
m	meter
δ	Variation of
θ	Temperature
q^B	Rate of heat generated per unit volume
q^S	Rate of heat transfer per unit surface
q^i	concentrated heat flow inputs
^{o}C	Degree Celsius
K	Kelvin
Au	Gold
Si	Silicon
1-D	one dimensional
2-D	two dimensional
3-D	three dimensional
SX	Stress in x-direction
SY	Stress in y-direction
SZ	Stress in z-direction
UX	Displacement in x-direction

UY	Displacement in y-direction
UZ	Displacement in z-direction

CHAPTER I

INTRODUCTION

The structural design and the quality of fabrication have a great effect on the reliability of a semiconducting device. They are directly related to the number of thermal cycles, the amount of power dissipation, the intensity of mechanical impact and vibrations, as well as corrosion. Therefore, they dictate the time span in which the device will work properly.

One of the most serious reliability problems is the introduction of thermal stresses in virtually every step of the manufacturing process. In particular, large stresses are induced when the Silicon die is attached to a Ceramic leadframe. This connection is required for mechanical support, thermal and electrical reasons.

Commonly the attachment is a soldering process using Gold-Silicon Eutectic solder (Au-2%Si). In addition several types of adhesives are used for die attachment. The different attachment systems have been compared by other investigators [1] and the Eutectic system was found to be the most favorable because it results in the lowest thermal stresses.

The thermal stresses are induced during the cooling process, after the actual bonding process, due to nonuniform temperatures and difference in coefficients of thermal expansion. Most of the investigations so far have assumed that the highest stresses occur when the device has cooled to ambient temperature. The stresses induced due to the nonuniform temperatures during the cooling process have been neglected. A transient thermal analysis using the Finite Element Method is performed in this investigation to clarify if this assumption is valid.

Imperfect die attachment such as center and edge-voids can have a considerable influence on the stress distribution and magnitude or location of stress concentration. Voids in this context are the areas where the Silicon part of the device (thereafter referred to as die) is not covered by Eutectic. The induced stresses may also depend on the thickness of the Eutectic layer. The influence of these variables has also been investigated by applying the Finite Element Method.

However, for small chips the induced stresses and therefore the probability of die cracking is relatively small, but since chips of relatively big size, about 1cm and larger, have become practical on a larger scale, knowledge about the stress mechanisms becomes more and more important to ensure the quality and reliability of both, the production process and the product.

BONDING PROCESS AND CRACKING OBSERVATION

At the end of the integrated circuit production, the Silicon wafers are cut or separated into individual chips (die). Chip separation can be done by using a diamond impregnated saw blade, a pulsing laser or a diamond tipped scribing tool. Diamond sawing leads to straighter edges with less mechanical damage. The quality of the Silicon surface and edges influences the fracture stress of Silicon considerably (Table I) and therefore have a great effect on the probability of die cracking.

After separation the chips are sorted according to the results of an electrical inspection.

The die is then bonded to a metallized Ceramic substrate. The most common technique for die attachment uses Au-Si Eutectic alloy as solder.

The Au-Si solder consists of 97 wt% Gold and 3 wt% Si (82 atomic% Gold and 18 atomic% Silicon, Figure 1), the bonding temperature is usually around 400 ^{o}C, a temperature above the Au-Si freezing temperature of 363 ^{o}C. During bonding the unit is usually ultrasonic agitated or scrubbed to ensure uniform contact between solder and die (reducing void formation).

In addition to the Eutectic Au-Si system, several types of adhesives (e.g. Silver filled epoxies) are currently used for die-attachment. Due to the limited heat and electrical conduction these devices cannot be used in

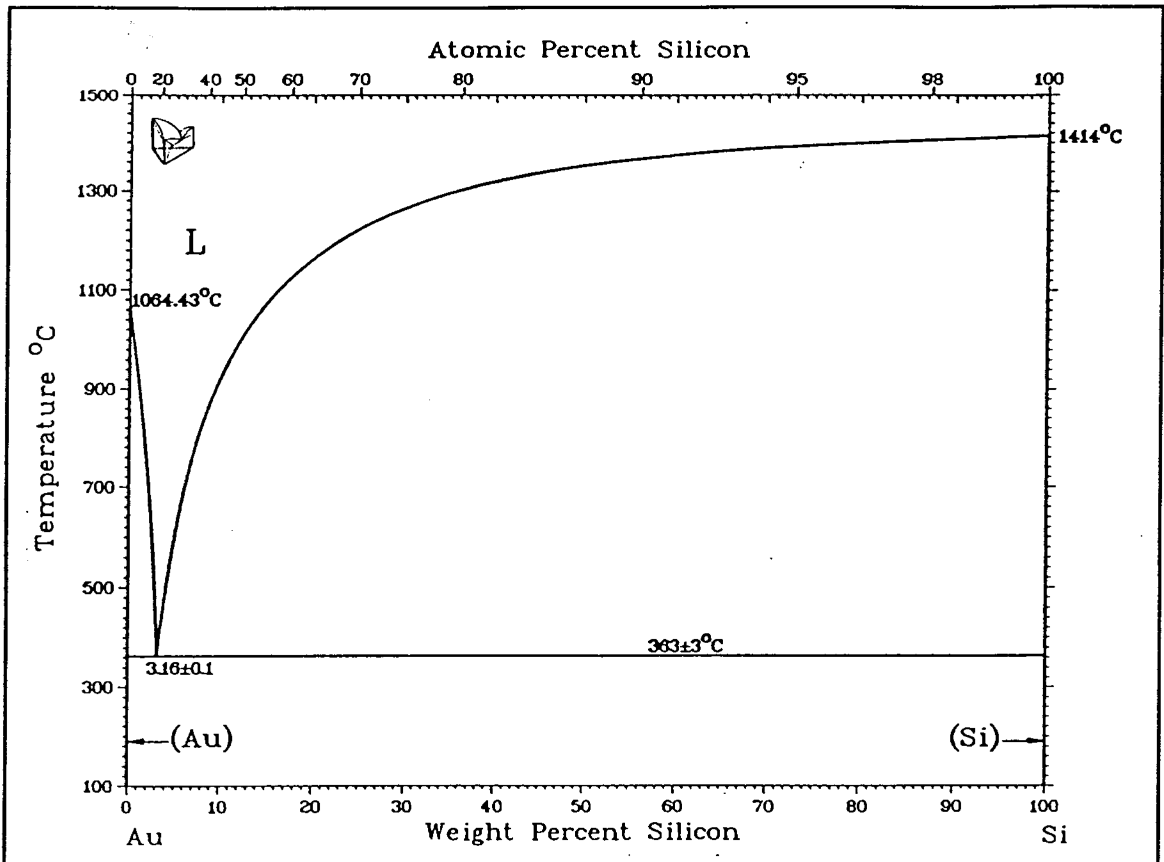

Figure 1. Au-Si phase diagram.

applications that require high temperatures or high currents through the chip-substrate bond.

After the Silicon die is bonded to the Ceramic substrate the wires and leads are attached and the whole device is encapsulated in plastic.

Two different fracture patterns are observed in Si-devices. Vertical die cracking due to bending of the device which induces tensile stresses in the surface of the die. Horizontal cracking mainly due to high stresses in the Silicon-Eutectic interface. Due to the properties of Silicon brittle fracture occurs. Horizontal cracks in the

surface of the die can be seen under an optical microscope with magnifications as low as 50x. By removing the Eutectic layer of a cracked device (remelting of the Eutectic) the relationship between die cracks and voids becomes apparent. Correlation between the location of the cracks and the voids has been reported [2]. The cracks originate from the backside of the die.

TABLE I

FRACTURE STRESS OF SILICON [1]

Si polished, surface flaws 0.5μm in depth	800 N/mm
Si polished, surface flaws 2.0μm in depth	400 N/mm
Si , microgrooves 5-10μm	175 N/mm

CHAPTER II

REVIEW OF LITERATURE

Since the late 1950's stresses in semiconductors have been studied by using elasticity method and photoelasticity techniques. In 1959 Taylor [3] employed the classical elasticity method to model semiconductors as axisymmetric rings. In the 1960's more investigations about the stress distribution after die attachment have been undertaken [4,5,6]. Riney [5] employed photoelasticity techniques to investigate the distribution of tensile stresses in the Silicon die. From the results he suggested that the region of the highest stress concentration is located at the bond-device interface, slightly inside the free edge of the die. Since then more intensive studies taking more parameters into account have been made. In 1979 Chen and Nelson [7] studied the stress distribution in bonded materials induced by the differential expansion or contraction of these materials. They presented several analytical models for different geometrical or material parameters. They concluded that the maximum shear stress always occurs at the edge of the joint and that unconstrained bending may induce significant tensile stresses whereas if bending is constrained the maximum shear stress will be increased. This

approach covers the basics of thermal stresses in bonded joints without any specific application. In 1982 Zarefar [8] investigated the thermal stresses in Single Crystal Silicon Devices by applying the Finite Element Method. To verify the computed stresses, a similar model was solved by using the Elasticity Method. He found that a thinner Eutectic layer and complete coverage of the Silicon by the Eutectic reduces the stresses. This investigation was used as a foundation for the work done in this thesis. In 1983 van Kessel, Gee and Murphy [1] compared the quality of different die-attachments (Eutectic Au-Si, Epoxy, Polyamide) and the relationship to stresses and vertical die cracking. They found that the adhesive die attachment leads to higher and more variable stresses than the Eutectic die attachment. No dependence of the thickness of the Eutectic layer was observed, which they explained by the small thickness of the Eutectic layer compared to the thickness of the die. They concluded that the contribution to the thermal stresses is mostly negligible. In 1984 Chian and Shukla [2] utilized experimental methods as well as finite element analysis to determine the mechanisms of die cracking. Their results show that edge voids along the die attachment interface change the local stress field and create a tensile stress field which increases the probability of die cracking. Furthermore, their results show that the thickness of the die is the most important variable that affects stress

distribution inside the die. In 1987 Kasem and Feinstein [9] investigated the fracture mechanism in packages with glass as die bonding material. They used a transient thermal analysis and a steady-state structural finite element analysis to determine the stress distribution inside the die. Due to the different bonding temperatures and mechanisms, most of their results cannot be applied to Au-Si bonded devices. Suhir [10] applied analytic methods to determine the thermally induced stresses in die and attachment. He studied the stresses in the die (normal stresses) as well as stresses at the interface between the different materials. Stresses have been calculated analytically for different die size and different thickness of the bonding material. The results show that for large die size (>1cm) the maximum stresses in the die are practically independent of its size. This approach uses the same analytical method, which is an extension of the Timoshenco (1925) theory of bi-metal thermostats, than an earlier investigation by E. Suhir [11] but is applied to thermal stresses in semiconductors.

Other bonding agents, such as plastic encapsulated electronic devices have also been subject to research [12-18] but are not subject of this thesis.

The preceding literature review reveals partly conflicting results. It is not absolutely clear how thickness of either the Eutectic layer or the die or both affect the induced stresses. Furthermore, most of the previous re-

searches are based on the assumption that the heat transfer through the whole device is equal and thus there are no thermal stresses due to a nonuniform temperature distribution during the cooling process. This is not true because of the obvious difference between the heat transfer properties of the different materials, which results in different cooling rates of these regions. The resulting transient heat conduction can result in a higher magnitude of thermal stresses due to the different temperature distribution.

CHAPTER III

THEORY

STRESS MECHANISMS

Large temperature gradients and substantial difference in coefficients of thermal expansion are major factors for thermal stress induction.

After the soldering process the device is cooled by convection. During the cooling process there is a non-uniform temperature distribution in the device which induces thermal stresses. The magnitude of these stresses depends on the difference between the highest and the lowest temperature in the device at any time during the cooling process. The lower the thermal conductivity of the material, the larger are the temperature gradients and therefore the induced thermal stresses.

The major contribution to the resulting stresses in the semiconductor device are thermal stresses due to the difference in thermal expansion of the bonded materials.

The semiconductor device consists of three different materials: The actual Silicon die, the Gold-Silicon Eutectic layer which is used as the solder and the Ceramic substrate where the chip is mounted (Figure 2).

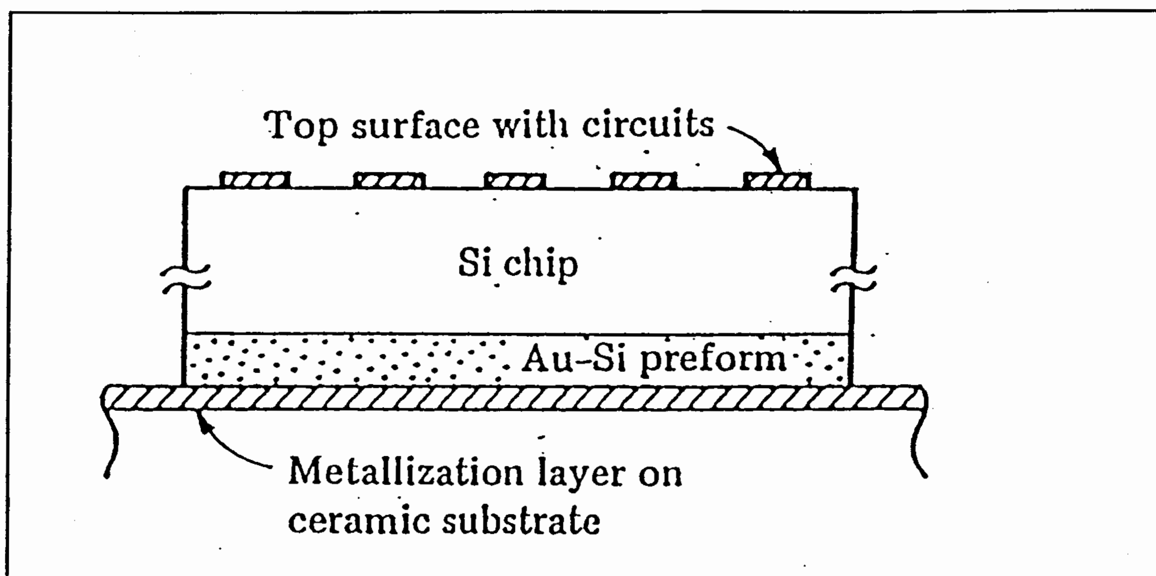

Figure 2. Silicon integrated-circuit chip attached to a metallized leadframe.

To determine the induced stresses the device can be seen as a beam consisting of three layers. Due to the higher coefficient of thermal expansion (Table II) the Ceramic (usually Alumina) contracts more than the Silicon die which means compressive stresses will be induced in the die during cooling. The thermal stresses will, to the most part, be a function of the difference in coefficients of thermal expansion, the temperature difference between freezing temperature of the Eutectic and the actual temperature of the device, Poissons Ratio, Youngs modulus of elasticity and the dimension of the device. With increasing size of the device the stresses will increase since the difference in contraction between the two layers increases. If bending of the die is allowed, a tensile stress component will be induced in the top surface of the die. Suppressed

bending reduces the tensile component and increases the principal stresses.

The influence of the Eutectic layer is hard to predict because there are two mechanisms to consider. First, its coefficient of thermal expansion is about three times higher than that of the Ceramic and more than seven times higher that of Silicon. Therefore, the induced stresses within the Silicon should increase with increasing Eutectic layer thickness. Second, the Eutectic is a "softer" (lower modulus of elasticity) material than Silicon and thus it may act as a buffer between the Ceramic and the Silicon layers, reducing the stresses resulting from their differing contraction.

Due to the high stiffness and dimension of the Ceramic leadframe compared to the Silicon, bending of the device is assumed to be negligible.

THE FINITE ELEMENT METHOD

Many complex systems in our surrounding cannot be understood in one operation. Subdividing these systems into individual components, whose behavior is readily understood and then rebuilding the original system from such components is a way in which not only scientists proceed. Systems can be modeled by using a finite number of well defined components. Such problems are called 'discrete'. If the subdivision is continued indefinitely, the problem can only be

defined by differential equations or equivalent statements. Such systems are called continuous.

The finite element method [19,20] is an analysis tool to solve continuum problems in a numerical way. The continuum problem is approximated, such that the continuum is divided into a finite number of parts (elements) whose behavior is specified by a finite number of parameters. The solution of the complete system as an assembly of its elements follows precisely the same rules as those applicable to standard discrete problems.

Structural Analysis

The finite element analysis can be used in a variety of different ways. The most important formulation is the displacement based finite element method. It can be regarded as an extension of the displacement method of analysis which has been used extensively in the analysis of beam and truss structures.

To obtain the solution of stress and strain distribution in elastic continua, a discetization of these problems has to be performed. This is done in the following manner:

- The continuum is separated by imaginary lines or surfaces into a number of 'finite elements'.
- The elements are assumed to be interconnected at a discrete number of nodal points situated on their

boundaries. The displacement of these nodal points will be the basic unknown parameters of the problem, just as in a simple, discrete, structural analysis.

- A set of functions is chosen to define uniquely the state of displacement within each 'finite element' in terms of its nodal displacements.
- The displacement functions now define uniquely the state of strain within an element in terms of the nodal displacements. These strains, together with any initial strains and constitutive properties of the material will define the state of stress throughout the element and, hence, also on its boundaries.
- A system of forces concentrated at the nodes and equilibrating the boundary stresses and any distributed loads is determined, resulting in a stiffness relationship of the form

$$\mathbf{q}_i = \mathbf{K}_i\ \mathbf{a} + \mathbf{f}_p + \mathbf{f}_{e0}$$

in which $\mathbf{q}$ represents the forces acting on the nodes, $\mathbf{a}$ the corresponding nodal displacement, $\mathbf{f}_p$ the nodal forces required to balance any distributed loads and $\mathbf{f}_{e0}$ the nodal forces required to balance any initial strain. The matrix $\mathbf{K}$ is known as the stiffness matrix.

The stiffness matrix of the complete element assemblage is effectively obtained from the stiffness matrixes of the individual elements using the 'direct stiffness method'. In

this procedure the stiffness matrmx **K** of the whole structure is calculated by direct addition of the element stiffness matrixes i.e.:

$$\mathbf{K} = \Sigma\ \mathbf{K}_i$$

where each element matrix $\mathbf{K}_i$ is written as a matrix of the same order as the structure stiffness matrix **K**. That means, that only the entries of $\mathbf{K}_i$ which correspond to the element degree of freedom can be nonzero. The equilibrium equation for the system is:

$$\mathbf{K}\ \mathbf{U} = \mathbf{R}$$

where **U** is the vector of the system global displacement and **R** the vector of forces acting into the direction of the structure global displacements.

After imposing the boundary conditions it is solved for the nodal displacements of the structure. The element nodal forces or stresses can now be obtained by multiplying the element stiffness matrix or the element stress matrix by the element displacements for each element. The forces or stresses at any section of the element can be interpolated between the nodal forces or stresses respectively.

The approach outlined here is known as the displacement formulation of the finite element method. It can be recognized that this approach is equivalent to the minimization of the total potential energy of the system in terms of the displacement field. If this displacement field is defined in a suitable way , then convergence to the correct

result must occur. The process is then equivalent to the Ritz procedure.

The equilibrium now leads to the statement that the 'total potential energy Π must be stationary' for variations of the displacements:

$$\delta\Pi = 0$$

This broader basis of the finite element analysis allows it to be extended to other continuum problems, where a variational formulation is possible.

Thermal Analysis

Once the functional for a specific problem is defined the finite element solution can be performed in an analogous manner to the stress analysis.

The functional governing heat conduction in three dimensions is :

$$\Pi=\int_V \tfrac{1}{2}\{k_x(\partial\theta/\partial x)^2+k_y(\partial\theta/\partial y)^2+k_z(\partial\theta/\partial z)^2\}dV$$

$$- \int_V \theta q^B dV - \int_S \theta^S q^S dS - \Sigma_i \theta^i Q^i$$

Where θ is the temperature; k_x, k_y, k_z are the heat conductivity coefficients; q^B is the rate of heat generated per unit volume; q^S is the rate of heat transfer per unit surface area of the body; and Q_i are concentrated heat flow inputs.

Defining the temperatures in a matrix $\mathbf{H}$ and the temperature gradients in a matrix $\mathbf{B}$ leads together with the condition of stationarity to:

$$\mathbf{K}\,\theta = \mathbf{Q}$$

where $\mathbf{K}$ is the conductivity matrix:

$$\mathbf{K} = \Sigma \int_V \mathbf{B}^T\, \mathbf{k}\, \mathbf{B}\, dV$$

and $\mathbf{Q}$ is the total nodal heat flow input:

$$\mathbf{Q} = \mathbf{Q}_B + \mathbf{Q}_S + \mathbf{Q}_c$$

where

$$\mathbf{Q}_B = \Sigma \int_V \mathbf{H}^T\, q^B\, dV$$

$$\mathbf{Q}_S = \Sigma \int_S \mathbf{H}^{sT}\, q^s\, dS$$

and $\mathbf{Q}_c$ is the vector of concentrated nodal point heat flow input.

The convective boundary condition is given by:

$$q^S = h(\theta_e - \theta^S)$$

where h is a convection constant and θ_e is the ambient temperature

FINITE ELEMENT PROGRAM

Finite element software packages are designed to be user orientated. They do not require special knowledge of system operations or computer programming in order to be used. Solving an engineering problem using finite element analyses requires three basic steps:

1) Preprocessing
2) Solution
3) Postprocessing

In the first phase, the following tasks have to be performed:

- geometry definition
- mesh generations
- material definitions
- constraint definition
- load definition
- analysis type definition

besides that preprocessors allow to display and easily alter the created model which allows a faster and more convenient programming.

In the solution phase the element matrix formulation and the calculations are performed.

The postprocessing phase is optional, since the results are already obtained in the solution phase. However it is very useful to reduce, reorganize, display and interpret the solution output.

Pre- and postprocessing using an interactive program with graphical presentation features reduce human effort in programming by providing an effective way to review the large quantity of data typically associated with finite element analyses.

The software package used initially was ANSYS [21]. To gain more plots and a more extensive solution elaboration the analysis was partially redone and continued with the finite element program MARC [22], where MENTAT [23] was used to perform the pre- and postprocessing.

Both software packages allow a variety of element and analysis types including a transient thermal analysis which is performed in this approach.

ANSYS works with integrated preprocessors and post-processors:

PREP7 (general mesh generation and model definition)

PREP6 (additional transient boundary condition generation)

POST1,29,30 (tabular printout, spatial displays)

POST26 (tabular printout, graph displays)

POST27 (solution combination)

The preprocessors output an ANSYS code which can be solved interactively or in batch mode. The solution output is read in by the postprocessors. Both, pre- and post-processors work interactively.

The MARC system consists of various programs where MARC is the actual solver. For pre- and postprocessing the interactive program MENTAT is used. Fortran subroutines can be used to input numerical data. The MENTAT preprocessor output can be formatted for different solvers. For some analyses types the output has to be altered or completed using the MARC codes, since some features of the MARC program are not supported by MENTAT.

CHAPTER IV

MODELING

The accuracy of a finite element analysis is mostly dependent on the type and number of elements used. However, the influence of parameters such as location, orientation, and aspect ratio of the elements must be taken into account. The result of an analysis obviously depends on the accuracy of the analysis itself as well as on the model with its initial and boundary conditions.

GEOMETRY

The investigated die is a block of very small dimensions. It consists of three layers, which are the ceramic leadframe, the actual silicon chip and a layer of solder which has been applied in a soldering process (Figure 2). This block can be modeled as a beam consisting of three layers (Figure 3).

A two-dimensional axisymmetric model, simulating a three-dimensional circular disc was constructed with eight node axisymmetric elements (Figure 4). Eight node quadratic elements were used, because these elements are more suitable for rapidly varying stresses. Furthermore, a comparison of strength of material, elasticity and finite element method

[24] showed that 8 node quadratic elements lead to the better results than 4 node linear elements, especially in case of curved beams. Since a curvature of the Silicon

Figure 3. Two-dimensional axisymmetric model.

layer in the area of the highest stresses is expected when edge voids are present, eight node elements were chosen to model the device.

The axisymmetric model was considered to be an efficient model because the number of calculations necessary to compute the result is only a fraction of the calculations necessary to solve a comparable three-dimensional model. Although the two-dimensional model is not as close to the actual die as a three-dimensional model, the accuracy of the computation itself will be higher since less computations induce less round-off errors. The temperature and stress distribution, as well as the influence of the above men-

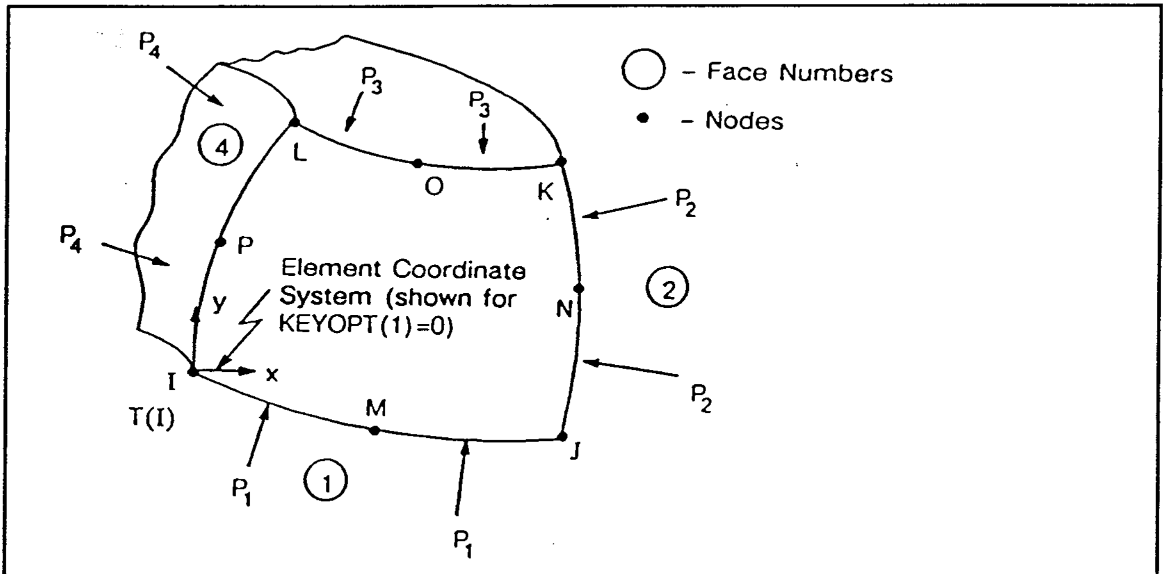

Figure 4. Axisymmetric element.

tioned parameters can be determined sufficiently with a two-dimensional model although the actual stresses occurring in the edges of the die will be higher than the ones computed by the two-dimensional model.

To perform the thermal and structural analysis the mesh described in Figure 3 was used.

MATERIAL PROPERTIES

The finite element software packages require a material property input with consistent units. The units used in this analysis are:

mm - millimeters

g - grams

s - seconds

N - Newton

J - Joule

The material properties may vary depending on the temperature.

The thermal analysis requires the material properties thermal conductivity, specific heat, density and poissons ratio. For the thermal analysis, density and poissons ratio are assumed to be temperature independent (Table II).

Thermal conductivity and the specific heat are input as a function of the temperature (Figure 5 and Figure 6).

TABLE II

TEMPERATURE INDEPENDENT MATERIAL PROPERTIES

	density in 10^{-3} g/mm^3	poissons ratio
Silicon	2.33	0.3
Eutectic	17.0	0.3
Ceramic	3.96	0.3

The structural analysis requires Youngs modulus and poissons ratio as material properties input. To perform an analysis of thermal stresses, the coefficient of thermal expansion is needed additionally. Yield stress and work hardening can be input optionally to describe the mechanical behavior more precisely. In this analysis the coefficient of thermal expansion is temperature dependent (Figure 7).

As in the thermal analysis the density and poissons ratio are assumed not to vary in the investigated temperature range (Table II). Furthermore the Youngs modulus of the silicon and the ceramic are temperature independent

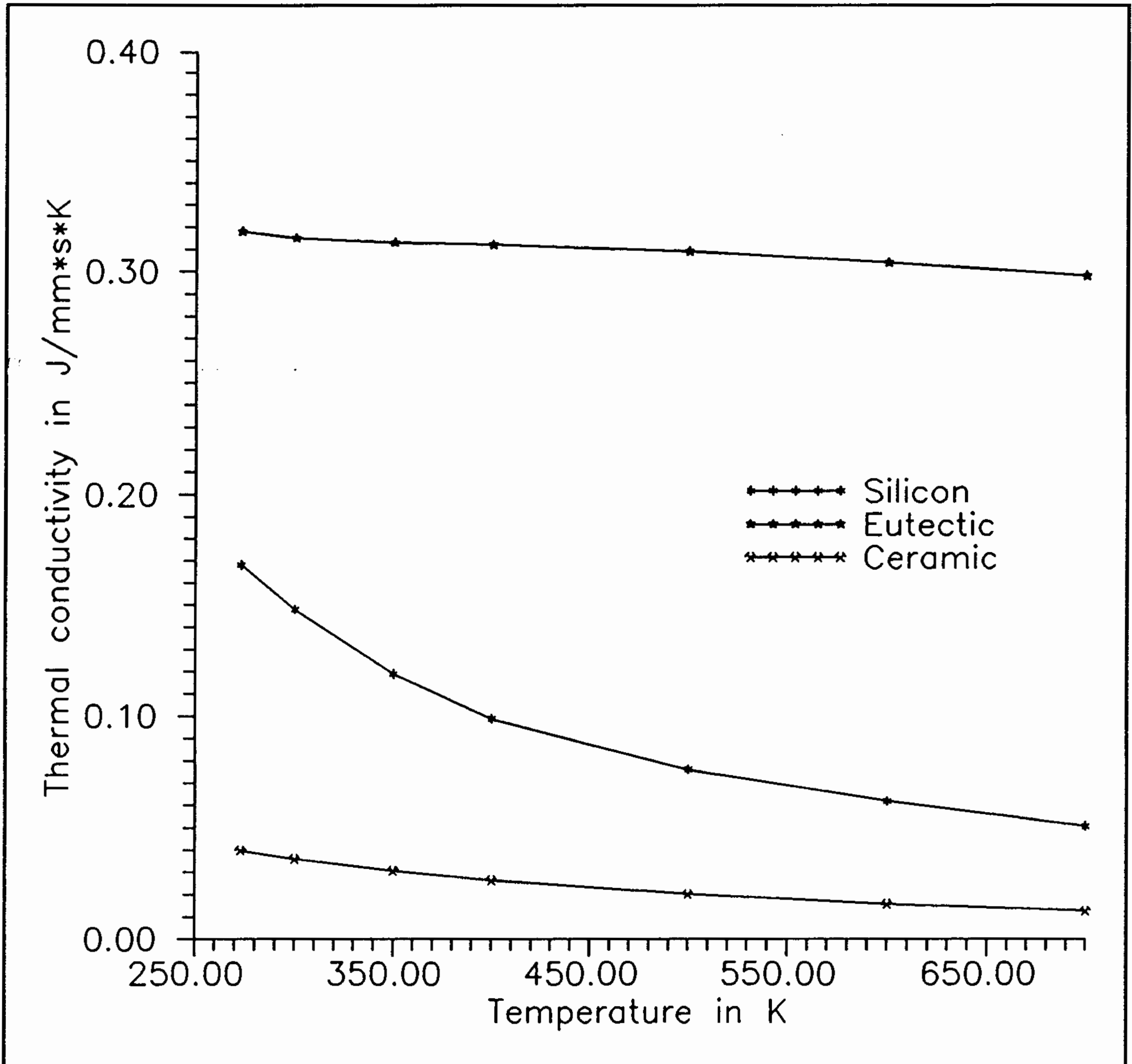

Figure 5. Thermal conductivity versus temperature.

(Table III). The Youngs modulus of the eutectic varies significantly, since the eutectic is liquid above 660 K. The idealized stress-strain curve of the eutectic is shown in Figure 8.

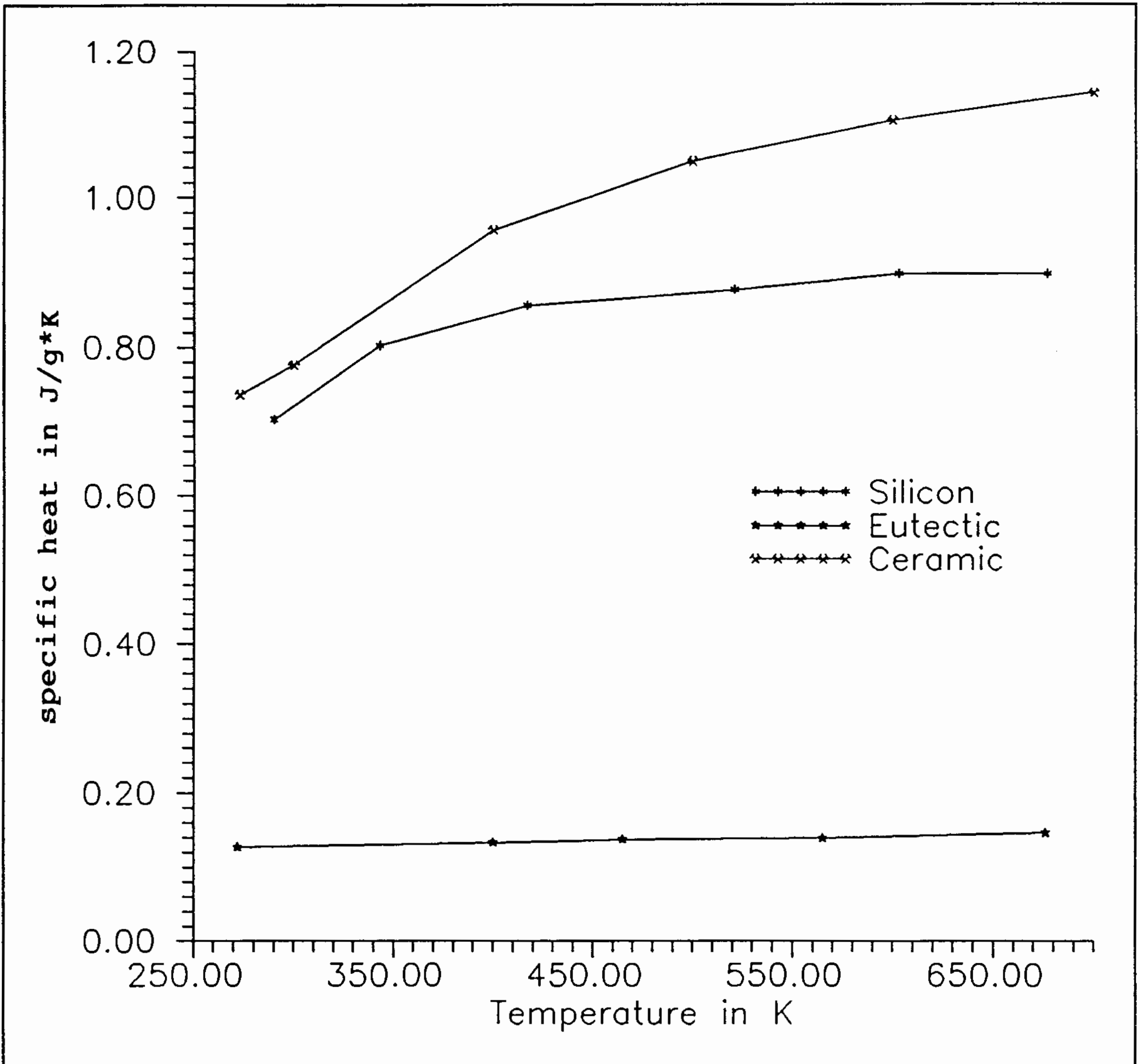

Figure 6. Specific heat versus temperature.

TABLE III

TEMPERATURE INDEPENDENT MATERIAL PROPERTIES IN STRUCTURAL ANALYSIS

	Youngs modulus in N/mm^3
Silicon	$106.8 * 10^3$
Ceramic	$344.7 * 10^3$

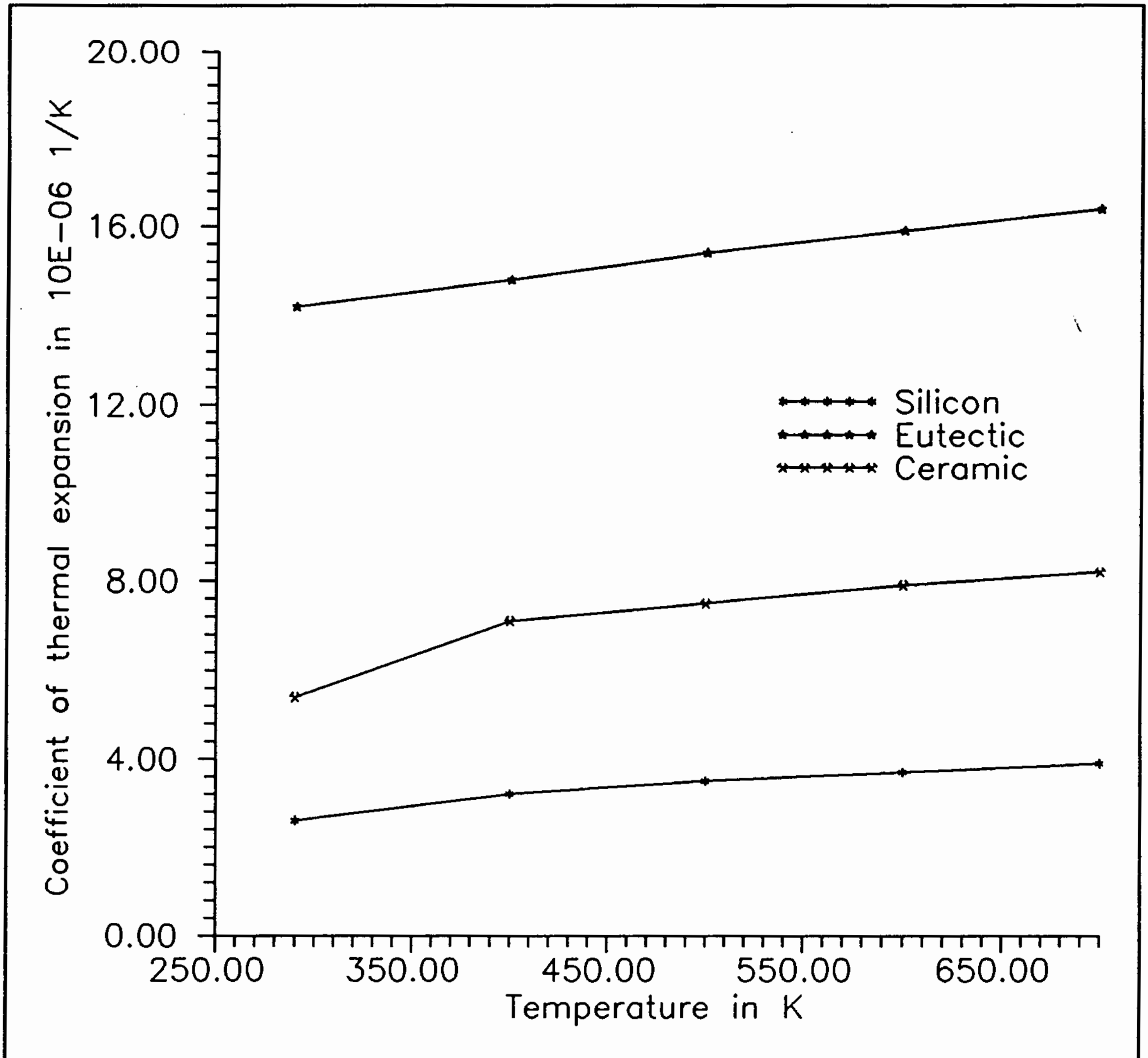

Figure 7. Coefficient of thermal expansion versus temperature

BOUNDARY CONDITIONS

Besides the geometry and the material properties a system is modeled by its boundary conditions. Prescribed force boundary conditions are often referred to as loads and prescribed displacement boundary conditions as boundary conditions. In addition to the prescribed displacement

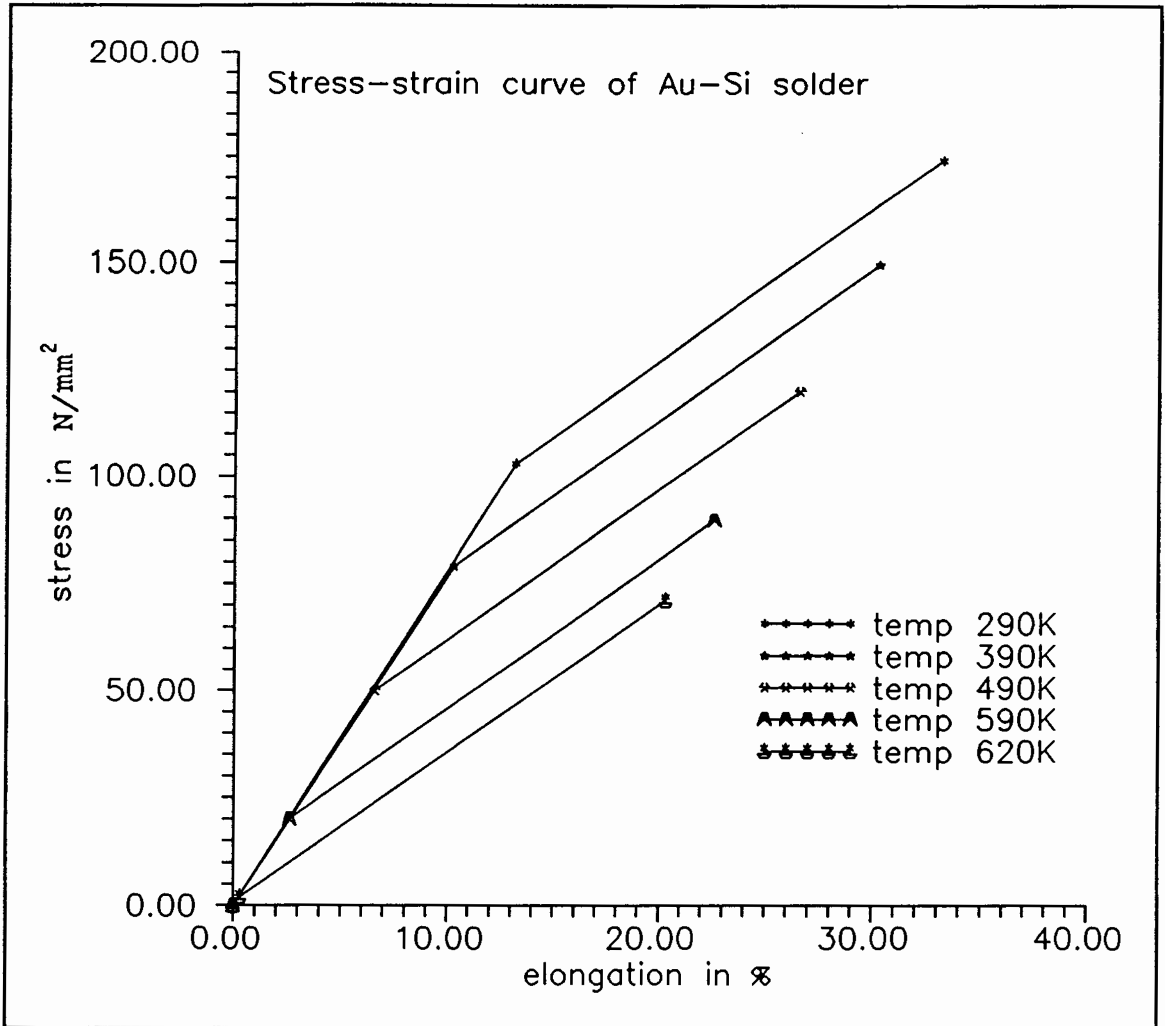

Figure 8. Idealized stress-strain curve of the eutectic.

boundary conditions, constraint relations may exist among the nodal displacements. Boundary conditions in a transient analysis which describe the initial state at t=0 are called initial conditions.

Different types of analyses require different kinds of loads and boundary conditions. The loads in stress analysis are forces, those in heat transfer analysis are fluxes. Since the temperature is the only degree of freedom in

thermal analysis the boundary conditions are temperatures.

The investigated problem is a die cooled by convection. The cooling can be modeled in two different ways:

- All the outside nodes (surface of the die) are constrained to ambient temperature θ_e (300 K) while all other nodes are initially set to soldering temperature (636 K). These conditions were applied in the ANSYS model.
- All the nodes of the die are set to soldering temperature and films are applied to the surface of the die. This was done in the MARC model.

The first way models a very fast cooling of the die. It can be seen as a convection process with an infinite convection coefficient h. Which means the ambient temperature is equal to the surface temperature θ^S of the die.

$$q^S = h(\theta_e - \theta^S)$$

Since the outside nodes are prescribed to ambient temperature, whereas all other nodes are set to soldering temperature at t=0, the temperature in the model varies considerably. This leads to problems when temperature dependent materials are used.

The second possibility allows a more precise description of the cooling process, since the film coefficient can be adapted to the type of the cooling process. The film coefficient depends on a variety of parameters, such as:

- dimensions
- flow velocity
- density of the cooling fluid
- viscosity
- specific heat
- thermal conductivity

The precise film coefficient for a specific cooling process is thus hard to determine without an experimental investigation. However, for the cooling by convection in air the following range of film coefficients is proposed [25]: 5.805 to 9.289 $* 10^{-6}$ J/s^2*mm^2

To model the fastest cooling process, which theoretically leads to the steepest temperature gradients and thus to the highest thermal stresses, a film coefficient of 9.26 $* 10^{-6}$ J/s^2*mm^2 and a sink temperature equal to the ambient temperature of 300 K is used.

The initial condition input is not supported by the MENTAT preprocessor and has to be done in MARC code in the MARC input file. All the nodes are set to soldering temperature (636K) initially.

Automatic time-stepping is used in the analysis. As initial timestep guess for the transient solution, 0.5 seconds is chosen since the dimensions are very small and fast cooling is expected. A maximum nodal temperature change of 80K is allowed. The maximum number of loadsteps is restricted to 20. The analysis stops if all nodal

temperatures are below 320K.

The nodal temperatures calculated for each increment are written into a post value tape which is read by the structural analysis.

The structural analysis is a thermally loaded stress analysis, which is bases on a set of temperatures defined throughout the mesh as a function of time. An initial stress free temperature of 636K is used in the structural analysis, since the temperatures at this point are uniform in the whole device and the solder is at its melting point. Thus there are no thermal stresses at this temperature.

The bottom node of the symmetry axis (node 256) is constrained in X and Y direction.

The thermal loads are read in from the post tape written by the thermal analysis. The maximum temperature change per step of the analysis is 50 and the maximum number of increments allowed is 50.

During the thermal analysis the influence of the thermal stresses induced by nonuniform temperature distribution turned out to be negligible. The residual stresses at the end of the cooling phase are the highest stresses occurring. Thus there is no need to use a transient analysis to investigate the influence of edge voids, center voids and varying eutectic layer thicknesses. With the ANSYS model a steady-state thermal stress analysis was performed. The same mesh as for the thermal model is used. Since the

ANSYS two dimensional structural elements have UZ as a degree of freedom, all nodes were constrained in z-direction (UZ=0). ANSYS assumes the y-axis to be the symmetry axis for the axisymmetric model. Therefore the nodes on the y-axis do not have to be constrained in x-direction. The stress at freezing temperature of the solder is considered to be zero, therefore the reference temperature (TREF) is set to 636K. The temperature (T) is set to ambient temperature (293K) for all nodes. ANSYS calculates the thermal stresses as a function of α*(TREF-T), where α is the coefficient of thermal expansion. Since no transient analysis is used, the material properties are temperature independent. The averaged values are used.

CHAPTER V

RESULTS AND DISCUSSION

THERMAL ANALYSIS

To solve the thermal MARC model according to the specified convergence and time-stepping parameters, 15 increments are needed to fulfill the stopping criteria (all nodal temperatures below 320K).

The results of the thermal analysis show that the device is cooled down below 320K in 246 seconds. During the cooling process the difference between the highest and the lowest nodal temperature in any increment is relatively small. Table IV shows the maximum and minimum nodal temperatures for each timestep. The according node numbers can be seen in Figure 9. No significant temperature gradients are detected in any area of the device. Figure 10 shows then temperature distribution in the device between node 99 and node 87 at increment number 5. At node number 94 and 91 a descendence temperature gradient is noted due to the change of material at these nodes.

The cooling process of the device is shown in Figure 11. The figure shows the nodal temperature of node number 256 and node number 6 versus time. Since the device cools down quasi-uniformly the two lines fall together.

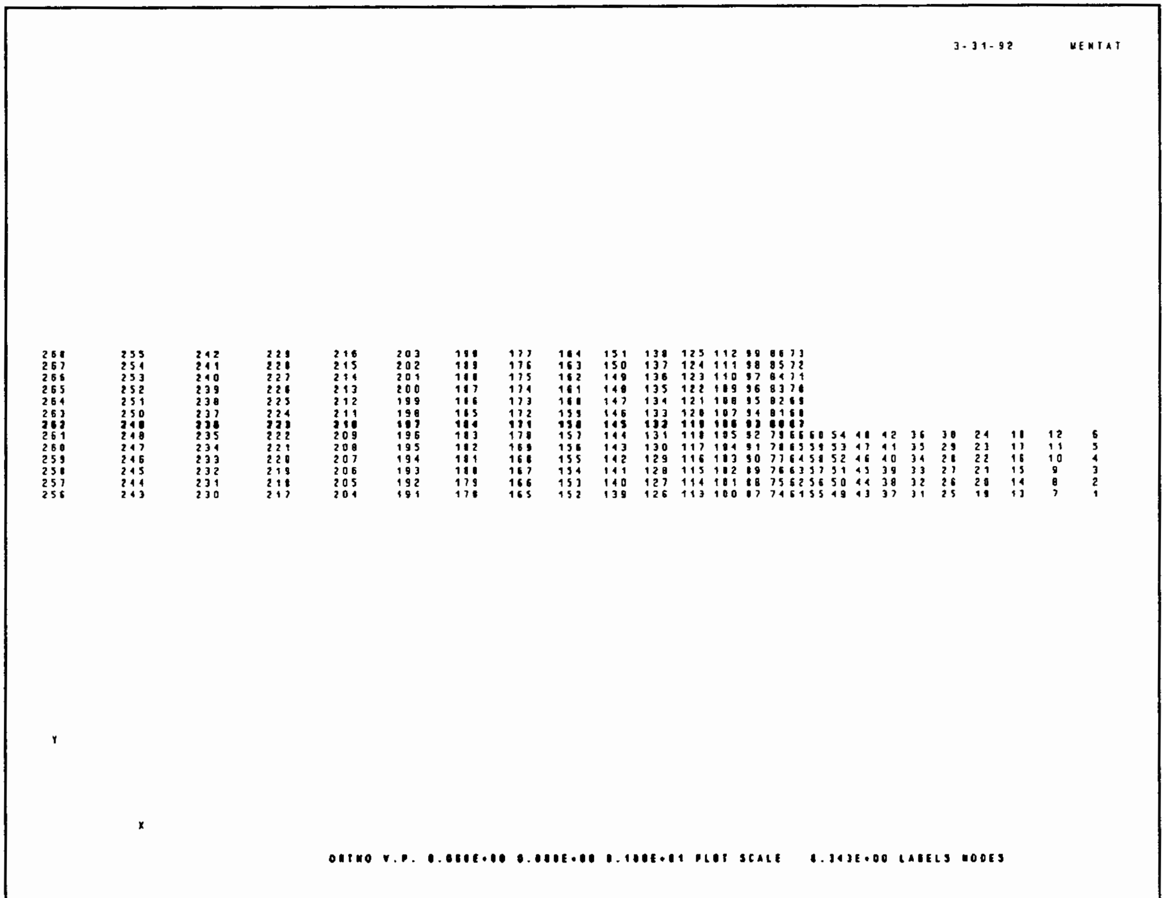

Figure 9. Node numbers

Corresponding results are obtained by the ANSYS model. Therefore it can be said, that the whole device cools down quasi-uniform. This might be anticipated, since the dimensions of the device are very small (Figure 3). To verify this assumption the ANSYS model is solved using 10 times and 100 times the dimensions of the actual die. All other parameters of the model are the same. The results show that the highest temperature difference during the cooling process increases considerably (Table V). Further verification is done by comparing the results to earlier thermal

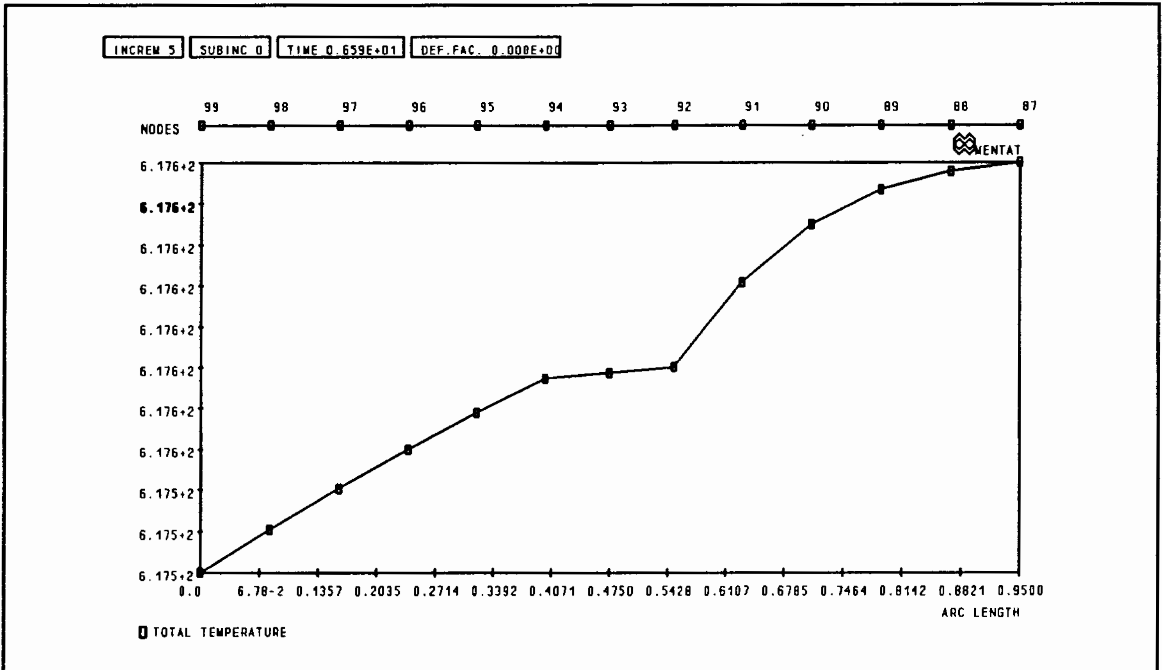

Figure 10. Temperature distribution through the device.

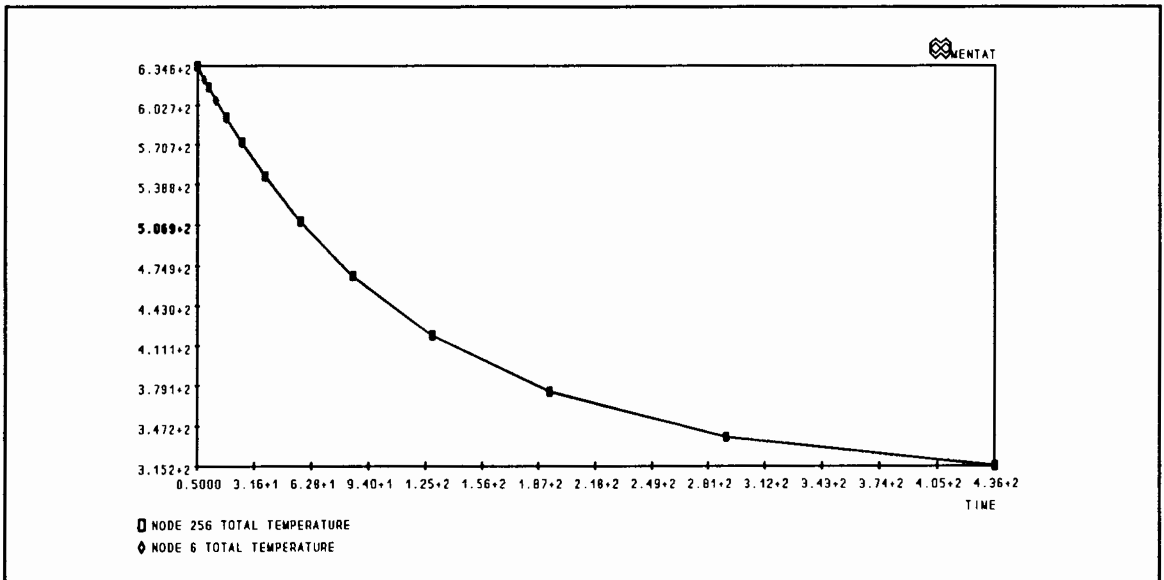

Figure 11. Cooling process.

analyses of similar models [9]. The results of these investigations showed temperature distributions similar to the ones resulting from the two dimensional thermal model.

TABLE IV

MAXIMUM AND MINIMUM TEMPERATURES IN TIMESTEP

Increment	Time in sec.	Max. temp. at node	Min. temp.	Temp. dif
1	0.5	634.65K at 256	634.09K at 6	0.56
2	1.25	632.54K at 256	631.71K at 6	0.83
3	2.37	629.36K at 256	628.43K at 6	0.93
4	4.06	624.66K at 256	623.70K at 6	0.96
5	6.59	617.73K at 256	616.80K at 6	0.93
6	10.39	607.67K at 256	606.77K at 6	0.90
7	16.08	593.24K at 256	592.40K at 6	0.84
8	24.62	573.01K at 256	572.25K at 6	0.76
9	37.44	545.51K at 256	544.85K at 6	0.66
10	56.65	509.88K at 256	509.36K at 6	0.52
11	85.49	466.87K at 256	466.48K at 6	0.39
12	128.87	419.72K at 256	419.46K at 6	0.26
13	193.62	374.59K at 256	374.44K at 6	0.15
14	290.92	338.25K at 256	338.17K at 6	0.08
15	436.89	315.32K at 243	315.29K at 6	0.03

TABLE V

HIGHEST TEMPERATURE DIFFERENCE FOR ANSYS MODELS

	Highest temp. difference during cooling process
original model	0.95 K
model with 10 times the actual dimensions	5.43 K
model with 100 times the actual dimensions	362 K

STRUCTURAL ANALYSIS

To solve the transient thermal stress model according to the specified parameters, 8 loadsteps are necessary. The results of the transient analysis show, that the thermal stresses induced due to nonuniform temperature distribution are negligible. Table VI shows the maximum compressive and tensile stresses in x direction and the maximum equal von mises stress in the whole device for each loadstep of the structural analysis. The highest stresses in the device are the residual stresses due to the difference in the coefficients of thermal expansion.

TABLE VI

MAXIMUM STRESSES FOR EACH LOADSTEP

loadstep	Sx tensile at node #	Sx compressive at node #	equal von mises at node #
1	30.89 at 171	11.56 at 202	32.43 at 68
2	54.02 at 223	22.39 at 199	58.05 at 69
3	69.27 at 197	32.91 at 199	81.98 at 69
4	89.23 at 223	45.08 at 201	91.48 at 264
5	106.01 at 223	59.11 at 202	91.04 at 265
6	119.41 at 223	71.41 at 202	91.36 at 72
7	130.77 at 223	79.75 at 203	91.69 at 267
8	139.52 at 132	79.91 at 203	90.40 at 124

The results of the steady state structural analysis shows a considerable dependance of the resulting stresses on the void size (coverage) and thickness of the eutectic layer. The investigation of the influence of edge voids shows that the compressive stress in x-direction (SX) decreases with decreasing coverage of the die with eutectic (increasing void size). This is to the most part due to the smaller distance of the attached area from the center of the die. The smaller the distance from the center of the die the smaller is the difference of contraction between the intersected materials and thus the stresses. Figure 12 shows the compressive stress in the die as a function of the coverage.

However, the tensile stresses increase considerable with decreasing coverage of the die. At a coverage of 80% (the coverage refers to the cross-section of the die which is modeled in the two-dimensional model, it is not the actual coverage of the three dimensional die) the magnitude of the tensile stresses increases about 50% compared to a coverage of 100% (Figure 13). The area where the highest tensile stresses occur changes depending on the coverage. Due to bending of the die an area of high tensile stresses is induced in the top surface of the die, whereas for perfect die attachment the highest tensile stresses occur on the outside of the die. Figure 14 shows the areas of highest stresses in the die for a coverage of 80% and 100%.

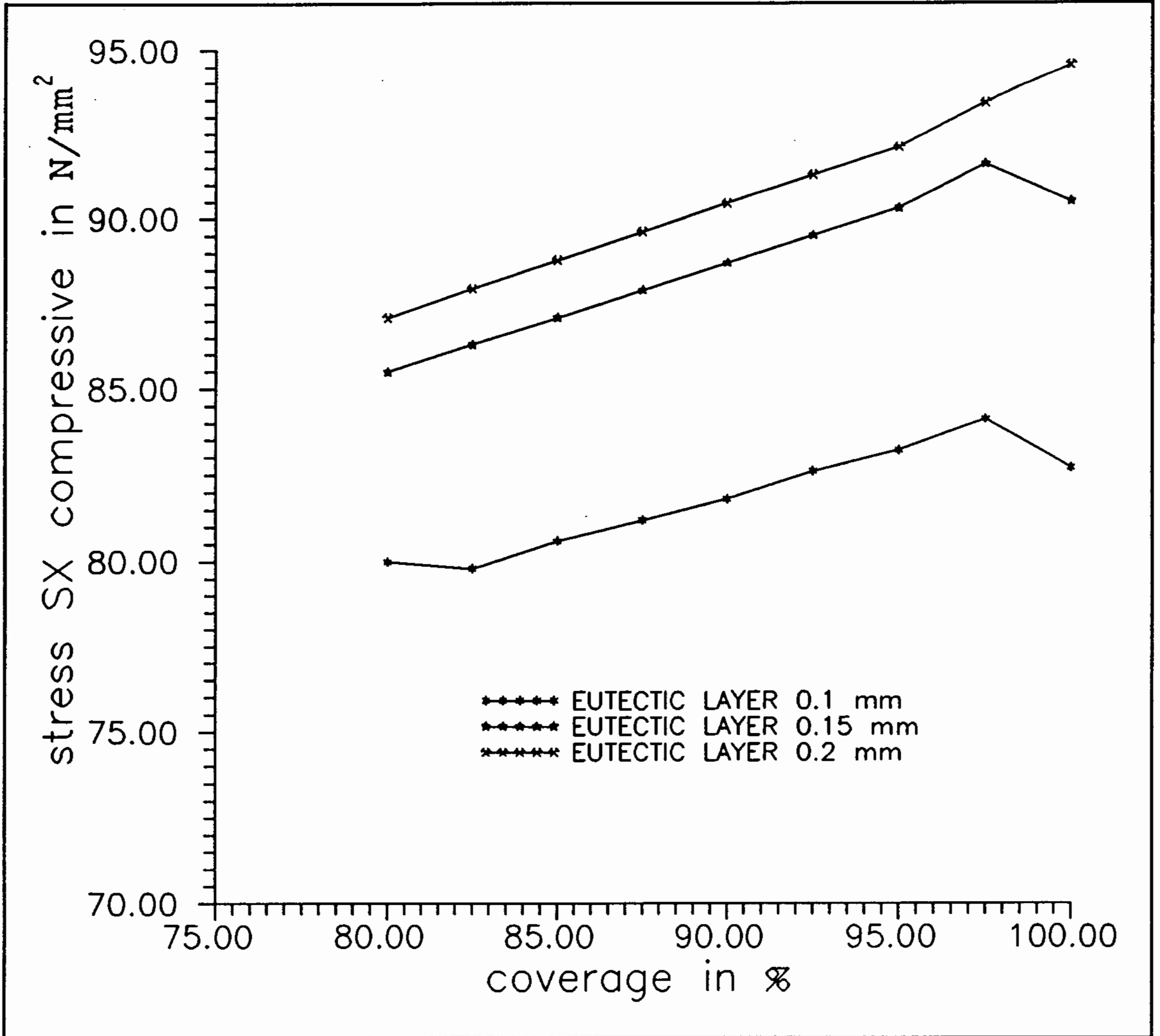

Figure 12. Sx compressive depending on coverage and eutectic layer thickness.

Investigation of the influence of center voids on the residual stresses show the stress distribution in the die changing considerably with increasing die size. For perfect die attachment the area of the highest stresses in obviously on the outside of the die. With increasing void size another area of high stresses in induced close to the center of the die (Figure 15). For a void radius of 0.25mm these stresses are still smaller than the ones on the outside of

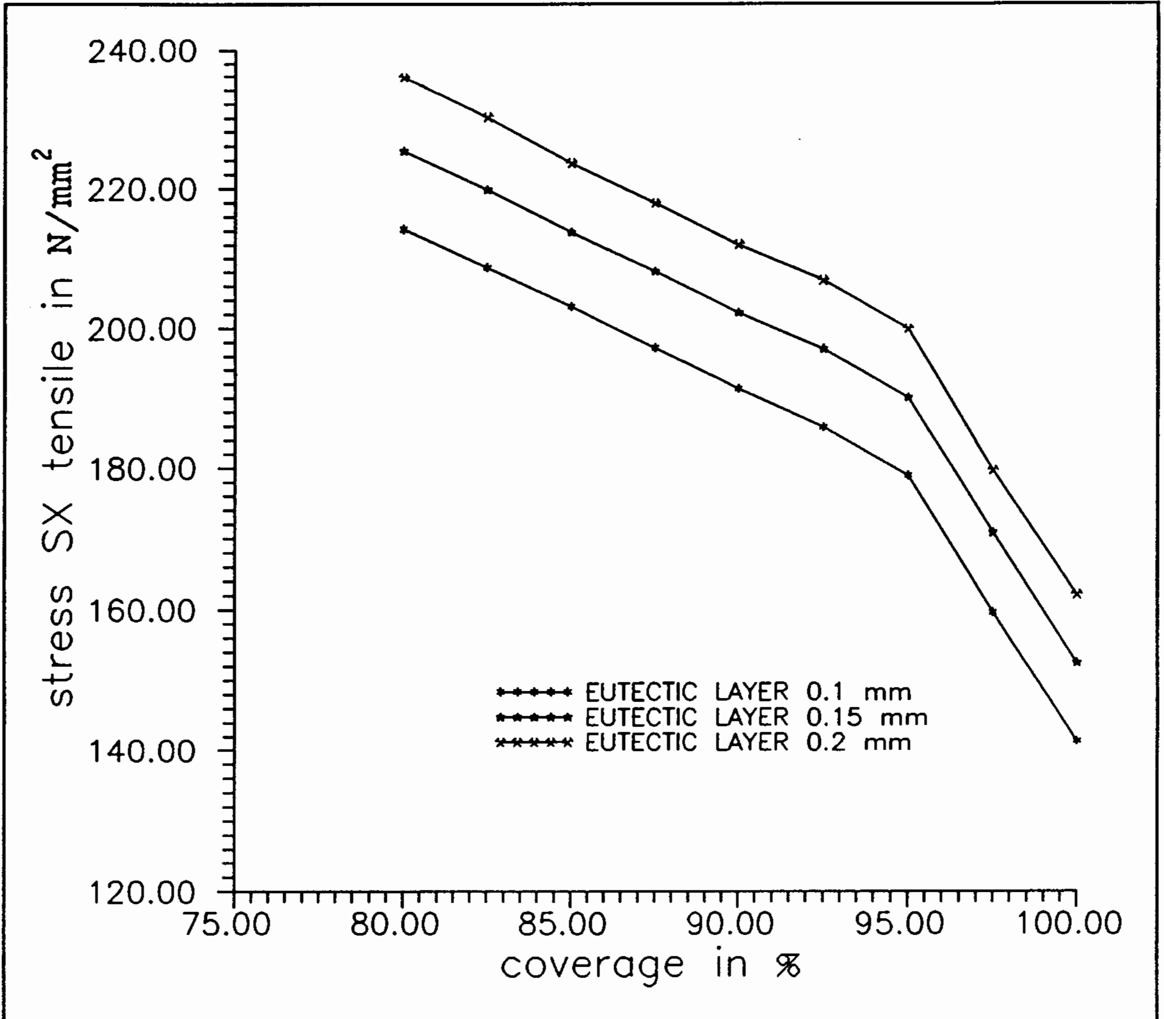

Figure 13. Tensile SX depending on coverage and eutectic layer thickness.

the die, but for radiuses larger than 0.5mm the stresses induced due to the center void exceed the stresses on the outside on the die.

A relationship between the thickness of the eutectic layer and the residual stresses is indicated by the results of the analysis (Figures 12 and 13). For all investigated stresses the magnitude increases with increasing thickness of the eutectic layer.

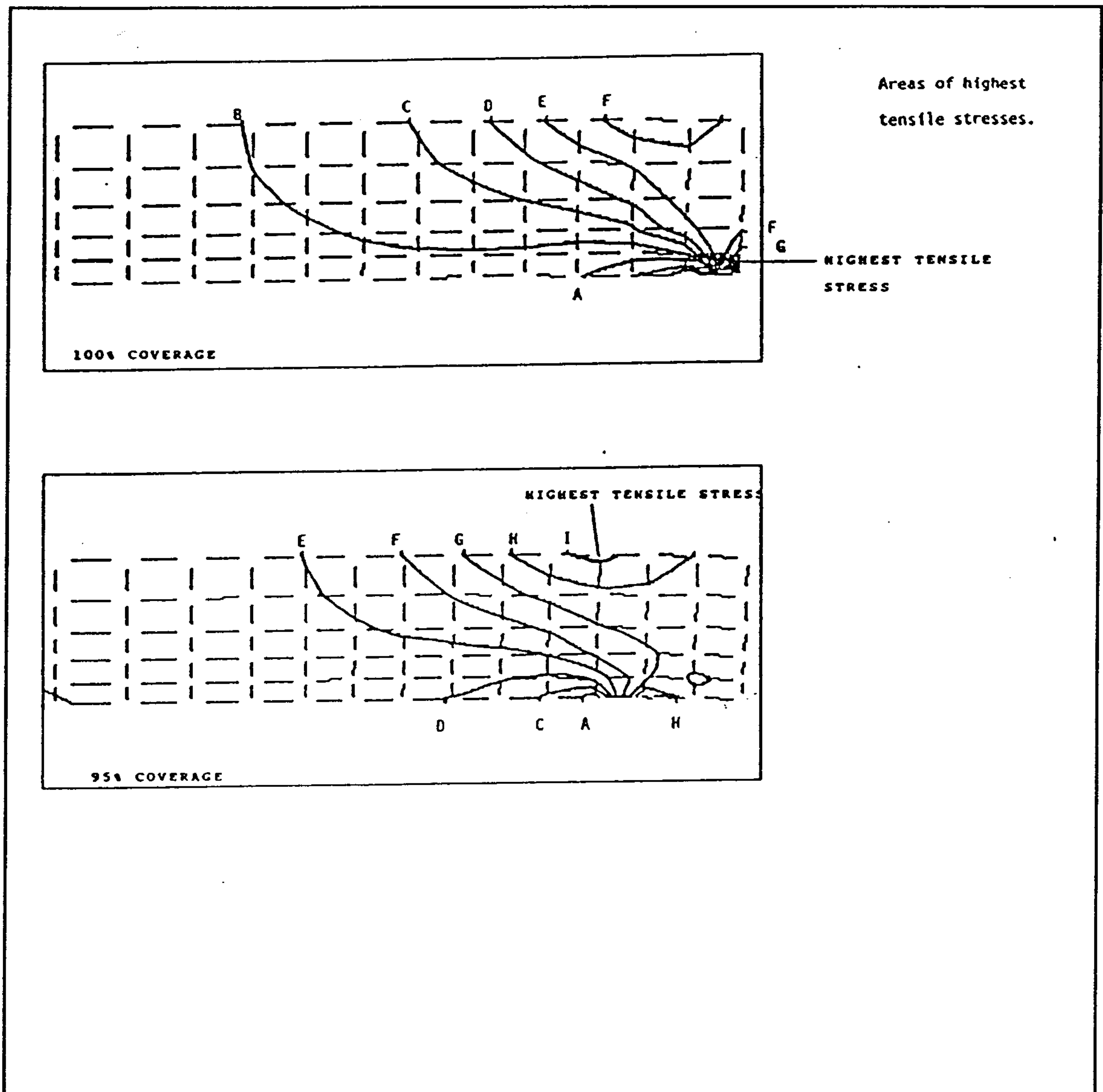

Figure 14. Areas of highest tensile stresses.

CONCLUSIONS

The thermal stresses induced due to nonuniform temperatures during the cooling process were found to be insignificant because of the small temperature gradients.

Center voids induce an area of high stresses in the

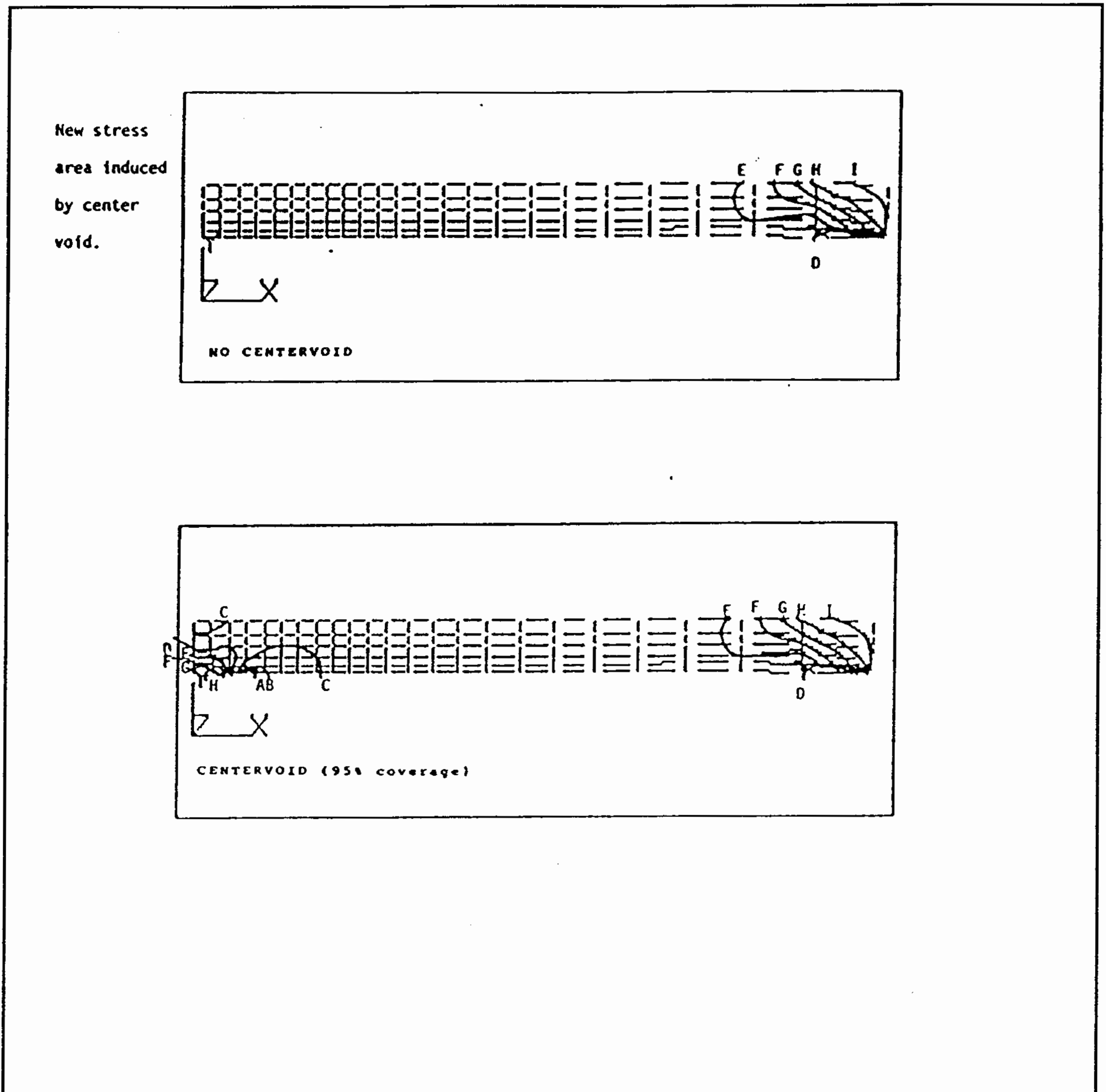

Figure 15. Stress areas induced by center void.

center of the die. The magnitude of these stresses can exceed the magnitude of the stresses at the edge of the device. Edge voids change the stress distribution. The tensile stresses in the top surface of the device increase considerably with increasing void size. The compressive stresses in the Silicon-Eutectic interface decrease slightly

with increasing void size due to the reduced difference in contraction between the two materials. The surface quality of the Silicon influences the fracture stress considerably.

Increasing thickness of the eutectic layer was found to increase the magnitude of the residual stresses. Therefore a soldering process using the least possible amount of solder is the most favorable.

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