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THESIS APPROVAL

The abstract and thesis of Marijan Peršun for the master of Science in Electrical and Computer Engineering were presented August 11, 1995, and accepted by the thesis committee and the department.

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ABSTRACT

An abstract of the thesis of Marijan Peršun for the Master of Science in Electrical and Computer Engineering presented on August 11, 1995.

Title: Scaling of the Silicon-on-Insulator Si and $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFETs

Two-dimensional numerical simulation was used to study the scaling properties of SOI p-MOSFETs. Based on the design criteria for the threshold voltage and DIBL, a set of design curves for different designs was developed. Data for subthreshold slope, SCE and threshold voltage sensitivity to silicon film thickness are also given.

Results show that short-channel effects can be controlled by increasing the doping level or by thinning the silicon film thickness. The first approach is more effective for p^+ gate design with high body doping, while the second approach is much more effective for n^+ gate design with low body doping.

The n^+ gate design is more suited for the design of fully depleted (FD) devices since we need to keep the doping low to minimize the threshold adjustment implant dose and to use thin silicon films to control the SCE. The design of both p-MOSFET and $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET requires the implantation for the threshold voltage adjustment.

The p^+ gate design is more suited for the partially depleted (PD) or near-fully depleted device design since we need to use high doping for the threshold voltage adjustment and this results in large threshold voltage sensitivity to silicon film thickness for FD devices. The design of Si SOI p-MOSFET is done by properly adjusting the body doping. For the $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET large reduction in V_{TH} requires large body doping. This increases the parasitic capacitances and slows down the device.

Scaling of the Silicon-on-Insulator Si and $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFETs

by

Marijan Persun

A thesis submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE
in
ELECTRICAL AND COMPUTER ENGINEERING

Portland State University
1995

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CHAPTER 1

INTRODUCTION

1.1 Motivation and Objective

The growth of lattice mismatched (i.e. strained) $\text{Si}_{1-x}\text{Ge}_x$ layers on silicon substrate allows for fabrication of different heterostructure devices. High performance HBTs have been built and there is interest in using the same $\text{Si}_{1-x}\text{Ge}_x$ layer to improve performance of p-MOSFETs. Recent developments in Silicon-on-insulator (SOI) technology and growth of $\text{Si}_{1-x}\text{Ge}_x$ layers have led research in the direction of combining the benefits of both. First, we will summarize the advantages of both technologies and then take a look at their advantages when combined in one structure. As it turns out, using both technologies can improve the characteristics of n and p-MOSFETs and make their characteristics better matched. Better matching is important because hole mobility is lower than electron mobility by 2–3 times. Since current is proportional to mobility $\times$ width product, to compensate for the difference in mobility p-MOSFET width is increased relative to n-MOSFET. Therefore, a p-MOSFET device always consumes more area, roughly 2–3 times, than an n-MOSFET device. Beyond this, use of SOI technology also gives us the means to improve the device performance for the same lithography, i.e. channel length. This comes from reduced parasitic capacitances due to better device isolation.

In order to improve packaging density and speed, MOSFET's channel length is constantly reduced. This process is called scaling. As we reduce the channel length, many

non-linear and two-dimensional effects, such as velocity saturation and short channel effect, not present in long-channel devices, come into play. They are usually referred to as Short Channel Effects – SCEs. Due to their complexity, they are very resistant to analytical modeling and one needs to turn to two-dimensional numerical modeling and experimenting.

When it comes to $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFETs, a variety of experimental devices and some theoretical studies have been presented in literature, but no systematic study of scaling properties of these devices has been presented. In this work, in order to develop a set of design rules, we will study scaling properties of these devices by using two-dimensional simulation. Because of the problem complexity, we will only give certain pointers which can be used for an initial design. This initial design needs to be followed by a more detailed modeling coupled with actual production.

1.2 Comparison Between the Bulk and SOI Technology

CMOS technologies are currently the main technologies for the whole digital electronics industry. They also have some applications in analog electronics, but bipolar technologies are more widely used because of their better performance. Some reasons for using CMOS technologies are [1]:

1. highest density and lowest power per gate
2. fully restored logic
3. zero static power dissipation
4. regular and easily automated layout
5. transmission gates pass both logic levels well

Currently, the major CMOS technology is bulk CMOS technology, but SOI technology is emerging, and is being used more often due to some advantages which it has over

bulk. These technologies are illustrated in Figure 1.1. The main difference between bulk and SOI technology is the way that the devices are insulated between each other and the substrate. In a bulk technology, devices are insulated using reversely biased p-n junctions, while in SOI an insulating layer is used. There are numerous ways to obtain the insulating layer and they are described in detail in [2]. For our purposes, we will assume that this insulation is done by the SIMOX procedure (Separation by IMplanted OXYgen), which is the most successful method to date [3]. SIMOX wafers are commercially available [3]. This technology results in a layer of silicon-dioxide as an insulating layer. Note that SOI MOSFET effectively has two gates: the front gate and the back gate which are separated from the channel by much thicker, buried oxide.

Figure 1.1 Cross section of CMOS inverter realized in bulk and SOI technology.

From Figure 1.1 a list of SOI advantages over bulk technology can be deduced [2],[1]:

1. denser layout (due to the absence of wells and well contacts)
2. reduction in source/drain (S/D) to substrate capacitance (S/D to body area is reduced and SiO_2 has smaller dielectric constant) $\rightarrow$ faster circuits [4], [5]
3. no latchup due to full dielectric insulation
4. no field-inversion problems
5. ease of making shallow junctions (no aluminium spiking)
6. reduction in noise coupling between the devices due to full dielectric isolation $\rightarrow$ attractive for low-noise mixed-mode ICs [6]

Another very important advantage that cannot be deduced from this figure is the relative insensitivity of SOI circuit's speed to the supply voltage as compared with bulk CMOS [4]. This is important, since a reduction in the channel length also requires a reduction in the supply voltage to obtain acceptable device performance and reliability [5]. Furthermore, a reduction in the parasitic capacitances brings a reduction in the dissipated power compared to the bulk case for the same speed. The reason that capacitance reduction is so important, comes from the fact that power that is dissipated in standard CMOS gate for charging/discharging the parasitic capacitances is much larger than the one dissipated because n-MOSFET and p-MOSFET are for a short time short-circuiting the power supply [6]. This improvement in power dissipation is dependent on the exact technology used and is roughly equal to three [5].

One problem associated with SOI technology that needs to be pointed out is self heating. Since the thermal conductivity of silicon-dioxide is much smaller than that of silicon, the dissipated power in the body due to the current flow increases the device temperature

more than in a bulk case. As already mentioned, a reduction in the supply voltage reduces this power dissipation and reduces this shortcoming of SOI technology [7].

1.3 SOI MOSFET Devices

1.3.1 An Overview

The structure of the SOI MOSFET with symbols for dimensions used later in the text is given in Figure 1.2. In SOI we have limited silicon film thickness. This makes it possible to design a device for which the front-gate-induced space charge region (depletion region) needs to be larger than the silicon film thickness. For these so called fully-depleted (FD) devices, the silicon film thickness must be less than the maximum depletion layer width. On the other hand, if the silicon film thickness is larger than two times the maximum depletion layer width the device is said to be partially depleted (PD) [2]. Both of those devices have unique characteristics which will be detailed in the following paragraphs.

Figure 1.2 Structure of the SOI MOSFET

A common feature of all MOSFET devices (bulk and SOI) is a reduction in the carrier mobility compared to the bulk mobility. In a MOSFET, carriers are confined in a narrow inversion layer adjacent to the front gate Si/SiO₂ interface by a strong vertical electric field. Thus, they experience additional scattering because of the surface roughness and surface acoustical phonons. The amount of scattering and mobility reduction is dependent on the vertical electric field, and therefore V_{GS} , because this field is the force that pushes them against the surface. Physics and modeling of these phenomena is very complex and will not be addressed in this work. However, the basic idea of mobility reduction in inversion layers will be used later to qualitatively explain some phenomena in Si_{1-x}Ge_x MOSFETs.

1.3.2 Partially-depleted (PD) Devices

In PD devices there is always a layer of undepleted (neutral) silicon film between the front and back-gate. These devices exhibit the following properties [2],[3]:

1. no coupling between the front and the back gate (there is undepleted/neutral silicon layer between the buried oxide and the edge of the depletion layer)
2. threshold voltage is the same as in the bulk case (see 1. above)
3. threshold voltage is independent of the silicon thickness (see 1. above)
4. kink effect in the output curve (due to floating body), see Figure 1.3
5. reduction of the drain breakdown voltage [8],[9] caused by floating-base bipolar transistor, where source-body-drain regions form emitter-base-collector
6. subthreshold hysteresis/latch phenomena

Effects 4.–6. can be eliminated if body contact is used. Unfortunately, this contact increases the area consumed by the transistor.

Figure 1.3 Illustration of kink effect in SOI n-MOSFET

1.3.3 Fully-depleted (FD) Devices

These devices exhibit the following properties [2],[3]:

1. front and back-gate coupling through the depletion layer
2. threshold voltage dependence on silicon film thickness (amount of the charge in the silicon film under the front gate is proportional to the film thickness)
3. threshold voltage dependence on back-gate voltage (see 1. above)
4. reduced parasitic source/drain to body capacitance (because of the lower body doping in order to get full depletion)
5. sharp subthreshold slope close to ideal, i.e. close 60 mV/dec
6. higher channel mobility due to the reduced vertical electric field at the front gate Si/SiO₂ interface compared to bulk and PD devices [10]
7. reduced body effect ($\approx 30\%$ less than in bulk devices)
8. possible reduction of SCEs through scaling of t_{Si} and t_{BOX}
9. high drain saturation current (see 6. above)

10. reduction of the breakdown voltage with the t_{Si} reduction [8],[9]
11. no kink effect (due to reduced body–source potential barrier compared to PD devices, absence of floating neutral body and reduced drain field [11])
12. subthreshold hysteresis/latch phenomena
13. reduced threshold voltage dependence on temperature

In order to obtain FD devices, a silicon layer thickness less than 100nm with uniformity of $\pm 25 \text{ \AA}$ and reproducibility of $\pm 1\%$ is needed for FD devices [11]. Only SIMOX technology is expected to fulfil these requirements. Reproducibility of thickness is required because of the threshold voltage dependence on silicon film thickness. Another advantage of SIMOX is its compatibility with standard bulk process.

1.3.4 Comparison Between the FD and PD Devices

In the two previous paragraphs a list of properties for both FD and PD devices was given. The importance of each depends on an application of the device in the circuit environment and manufacturing constraints. For analog circuits, kink effect is undesirable and should be avoided. This leads to either FD devices or PD devices with body contact. In digital circuits, the kink effect can be tolerated although it leads to reduced noise margins and gain [12]. Breakdown voltage is very important, and unfortunately it decreases with decreasing silicon film thickness for FD devices. Some drain engineering is needed to obtain acceptable values (e.g. Lightly Doped Drain – LDD and Gate Overlapped LDD – GO LDD). Threshold voltage sensitivity to silicon film thickness is also an important issue which can be addressed in two ways: by designing PD devices or devices which are nearly fully depleted [13]. The later reduces this sensitivity by preserving some of the advantages of fully–depleted devices (e.g. higher mobility and sharp subthreshold slope [14]). Obvious advantages of FD devices are increased mobility, no kink effect and sharp subthreshold slope.

Since there are so many parameters, it is not possible to give a definite answer to the question: PD or FD device? Therefore, we will study scaling properties of both and the results can be used to make a better selection for the final design.

1.4 Basic physical properties of $\text{Si}_{1-x}\text{Ge}_x$

Physics of $\text{Si}_{1-x}\text{Ge}_x$ layer is very complex and many of the issues are still unresolved. The main points of interest to us are:

1. $\text{Si}_{1-x}\text{Ge}_x$ layers grown on silicon experience compressive strain in the plane of growth due to the lattice mismatch [15]
2. compressive strain increases the hole mobility [16], [15]
3. bandgap of $\text{Si}_{1-x}\text{Ge}_x$ is narrower than the silicon one [17]
4. bandgap difference appears almost completely in the valence band [17]
5. there is a maximum thickness of $\text{Si}_{1-x}\text{Ge}_x$ layer that can be grown on top of silicon; exceeding this thickness leads to an unstrained layer and formation of dislocations on Si– $\text{Si}_{1-x}\text{Ge}_x$ interface [18]
6. maximum critical thickness of $\text{Si}_{1-x}\text{Ge}_x$ layer depends on a germanium dose [18] (dose is integrated concentration)
7. it is difficult to grow high-quality oxide on $\text{Si}_{1-x}\text{Ge}_x$ layer [19] (there is no such thing as silicon–germanium oxide)

The fact that hole mobility increases in strained $\text{Si}_{1-x}\text{Ge}_x$ layer can be used to improve the characteristics of p–MOSFETs. This is very interesting since hole mobility in silicon is about one third of electron mobility. Therefore, in circuit design p–MOSFETs always need to be wider to compensate for this difference. Another important fact is the bandgap reduction which is used to confine holes in $\text{Si}_{1-x}\text{Ge}_x$ channel. $\text{Si}_{1-x}\text{Ge}_x$ channel region creates a potential well in which holes 'fall', i.e. they go where they have minimal potential energy.

1.5 SOI $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET

In order to combine the SOI and $\text{Si}_{1-x}\text{Ge}_x$ technologies the following structure was developed [20] (note that p^+ doping spike does not have to present in this structure but is given for completeness):

t_{CAP} = silicon cap thickness

t_{CH} = SiGe channel thickness

t_{BUF} = silicon buffer thickness

Figure 1.4 SOI $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET

The silicon cap is introduced so that the gate-quality oxide can be grown. Recently, a new method for obtaining the gate quality oxide on $\text{Si}_{1-x}\text{Ge}_x$ has been published [19], but we will use this more common structure. Introduction of strained $\text{Si}_{1-x}\text{Ge}_x$ layer in the structure can improve hole mobility by two mechanisms [20]:

1. mobility enhancement in strained $\text{Si}_{1-x}\text{Ge}_x$ layer
2. reduction of surface scattering by removing the holes from the surface, i.e. confining them in the $\text{Si}_{1-x}\text{Ge}_x$ channel

Although 1. is obvious, 2. needs further explanation. For that purpose a diagram of the band structure is given in Figure 1.5 ($\text{Si}_{1-x}\text{Ge}_x$ region is shaded).

Figure 1.5 Bandgap diagram for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET (vertical cross section in the middle of the device, from the front Si-SiO₂ interface to the back Si-SiO₂ interface). p^+ gate. $N_D=1 \times 10^{17} \text{ cm}^{-3}$.

First, we can notice that practically all of the bandgap difference between the silicon and silicon-germanium is accommodated in valence band. In the vertical direction, i.e. perpendicular to the Si-SiO₂ interface, the hole quasi-Fermi level is constant (no current flow). Since the hole concentration is exponentially dependent on the difference between this level and the valence band edge, we can see that hole concentration in the $\text{Si}_{1-x}\text{Ge}_x$ layer will be much higher than in the silicon. Therefore, a majority of current will flow in $\text{Si}_{1-x}\text{Ge}_x$ region for low V_{GS} voltage (e.g. 0.4 V) as shown in Figure 1.6. As we increase the gate voltage, the valence band at the surface 'bends' upward and approaches the Fermi level. Therefore, hole concentration at the surface surpasses the one in the channel and the majority of current will flow at the surface and not in the channel. At this point MOSFET starts behaving like the one without $\text{Si}_{1-x}\text{Ge}_x$ channel. Figure 1.6 shows that as we increase the gate voltage more current is flowing at the surface. Also, we notice that even

for a relatively high gate overdrive of 1.2 volts (threshold voltage is 0.2) two thirds of the current is still flowing in the $\text{Si}_{1-x}\text{Ge}_x$ channel.

Figure 1.6 Integral of the current density along a vertical cross section in the middle of the device for low and high V_{GS} . $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with step doping. p^+ gate. $N_D = 1 \times 10^{17} \text{ cm}^{-3}$.

Different approaches are possible in order to improve the hole confinement in the channel. One approach is to use a graded channel, i.e. to increase the mole fraction of germanium in the channel as we progress closer to the surface. This results in a larger band-gap reduction at the top of the channel. Thus, a built-in electric field exists which pushes holes towards the top of the $\text{Si}_{1-x}\text{Ge}_x$ channel. This approach also brings holes closer to the gate and therefore increases the channel capacitance and consequently the transconductance. The other approach is to place high p-type doping (so called p^+ spike) just underneath the channel (see Figure 1.4). This doping spike serves as a source of holes which are then collected by the $\text{Si}_{1-x}\text{Ge}_x$ channel. Two additional possibilities are: 1) to minimize the Si cap layer which is limited by the requirement to separate the holes from the

surface, and 2) to maximize germanium fraction in order to increase the bandgap reduction. High germanium mole fraction can lead to strain relaxation. That is why a graded channel is better, because for the same average germanium mole fraction we can employ a higher concentration at the top and improve the hole confinement. More details on Si cap and $\text{Si}_{1-x}\text{Ge}_x$ channel engineering can be found in [20].

Silicon cap, $\text{Si}_{1-x}\text{Ge}_x$ channel and silicon buffer are undoped (or very lowly doped) in order to minimize the coulombic scattering of carriers by the ionized impurities. This approach preserves high hole mobility in those layers (sometimes called modulation doping, but we will call it step doping). The advantage of this approach can be seen from Table 1.1. We see that step doped MOSFETs exhibit higher linear transconductance even at higher body doping.

Table 1.1 Peak linear and saturation transconductance for different $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET designs.
 $L_{CH}=1\text{ }\mu\text{m}$. $t_{Si}=0.15\text{ }\mu\text{m}$.

Doping (cm^{-3})	V_{TH} (V)	g_{mL} ($\mu\text{S}/(\text{W}/\text{L})$)	g_{mS} ($\mu\text{S}/(\text{W}/\text{L})$)
3×10^{17} – uniform	0.6	2.6	34
3×10^{17} – step	0.3	7.6	61
1×10^{18} – step	0.5	4.6	51

A plot equivalent to the one in Figure 1.6 for uniformly doped $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET was done. At the equivalent gate overdrive more current is flowing at the surface. This is due to the reduced mobility in the channel. Hence, step doped design is preferable to the uniformly doped one.

The reason for using FD devices is that the presence of buried oxide in the device results in reduced vertical electric field and band bending which further helps the hole confinement compared to that of bulk or PD device [21], [16]. It has been reported that hole concentration at the Si/SiO₂ surface for the same gate overdrive can be over 100

times lower for FD devices compared to bulk one [16]. For our FD and PD devices this difference is much smaller, by the order of 10.

1.6 Design Parameters

Critical design parameters are:

1. choice of gate material
2. threshold voltage and method of threshold voltage adjustment
3. silicon cap thickness
4. gate-oxide thickness
5. $\text{Si}_{1-x}\text{Ge}_x$ profile and thickness
6. channel length

Different gate materials can be chosen for n-MOSFET and p-MOSFET although this complicates the technology. With n^+ polysilicon gate, which is a standard choice today, threshold voltage of n-MOSFET can be easily adjusted by ion implantation, but it gives too large a threshold voltage for p-MOSFET. Boron implantation (p^+ spike) can be used to reduce the threshold voltage, but this spike worsens the SCEs. Fortunately, in SOI devices, scaling the vertical thickness can improve the SCEs [22] and can compensate for this worsening. The advantage of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET is the fact that introduction of $\text{Si}_{1-x}\text{Ge}_x$ channel reduces the threshold voltage by approximately 0.2 V and thus reduces the required dose of p^+ spike. As discussed in [22], this p^+ spike improves the hole confinement in the channel by supplying additional holes. Therefore, n^+ gate design is preferable for higher gate voltage operation.

For the p^+ gate design dopants are located under the channel and the cap which are undoped. This is done in order to reduce the ionized impurity scattering and consequently

to maximize the mobility in those layers. This so called pulse-shaped doping (PSD) mimics the behavior of SOI devices by limiting the vertical thickness of the depletion layer which ends up on this highly doped region. It has the same effect as thinning of the SOI film thickness in SOI and hence it improves SCEs as explained in [23].

Critical thickness imposes an upper limit on $\text{Si}_{1-x}\text{Ge}_x$ layer thickness that can be grown without the relaxation of compressive stress, and is inversely proportional to the germanium dose. On the other hand, increased germanium fraction increases the valence band discontinuity and improves the hole confinement. Note that for high gate voltage, where we need to improve the hole confinement, the majority of holes are at the front $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ interface. In order to reconcile these two conflicting requirements, a graded $\text{Si}_{1-x}\text{Ge}_x$ channel has been introduced [22]. It has a large germanium content at the top $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ interface in order to obtain high valence band discontinuity and a small one at the bottom to keep the dose under critical value. Also note that introducing the graded channel creates a built-in electric field which pushes holes towards the front $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ interface. This results in a better gate control and steeper turn-on.

In order to improve the transconductance of the MOSFET, silicon cap and gate oxide thickness must be minimized in order to increase the gate-channel capacitance. This increases the number of holes in the channel for the same gate voltage. Thinner gate oxide, however, results in reduced breakdown voltage.

CHAPTER 2

SCALING OF THE MOSFET DEVICES

2.1 Why Scaling ?

To satisfy the ever increasing need for more complex and faster integrated circuits, the number of devices on a chip must be increased. Improvements in speed and packaging density for MOSFET devices are usually obtained through reduction of the transistor dimensions. The main dimensions which are scaled are channel length and silicon–dioxide thickness. Scaling the channel length improves the unity current gain frequency f_T as can be seen from the equations (2.1) and (2.2). We can see that by reducing the channel length we can substantially improve f_T since it is inversely proportional to the channel length.

$$f_T = \frac{\mu V_{DS}}{2 \pi L_{CH}^2} \quad \text{for } V_{DS} \leq V_{D,vsat} \quad (2.1)$$

$$f_T = \frac{v_S}{2 \pi L_{CH}} \quad \text{for } V_{DS} \geq V_{D,vsat} \quad \text{velocity saturation !} \quad (2.2)$$

μ = carrier mobility

v_S = carrier saturation velocity

V_{Dsat} = drain voltage which causes velocity saturation

Since transconductance g_m is proportional to gate capacitance, scaling the silicon–dioxide thickness improves the transconductance by increasing the gate capacitance. It also improves SCEs by bringing the gate closer to the channel and thus helping it to main-

tain control of the charge in the channel. From the Equations (2.1) and (2.2) we see that scaling the silicon–dioxide thickness does not influence f_T .

2.2 Problems Introduced by Scaling the MOSFET Devices

As we already mentioned, reduction in the channel length to sub–micron dimensions brings up many non–linear and two–dimensional effects not present in long–channel devices. Some of them are:

1. threshold voltage reduction – short channel effect (SCE)
2. drain induced barrier lowering – DIBL
3. carrier velocity saturation
4. increased leakage
5. hot carrier effects

In the following paragraphs, we will explain and analyze these effects.

2.2.1 Threshold Voltage Reduction – SCE

As the devices are scaled down, depletion layers extending from source/drain to body region start to take up a significant amount of charge effectively reducing the amount of charge under the gate control (Figure 2.1). Note that since the drain–body p–n junction is reversely biased, it has a much larger depletion layer than the source–body junction which is partially forward biased.

Because body doping is lower than drain doping, the depletion layer extends more into this region. This effectively reduces the channel length. Since this channel length reduction depends on drain voltage, it leads to finite output conductance in saturation. This depletion layer is under drain control and therefore it also reduces the charge that is under the gate control. Since the threshold voltage is proportional to the charge under the gate, this leads to threshold voltage reduction (see Figure 2.2).

Figure 2.1 Illustration of short channel effect. n-MOSFET.

As the channel length is reduced, this depletion layer charge becomes comparable in magnitude to the body charge under the gate control, and the threshold voltage is reduced even more. Note that the depletion layer width does not scale with the channel length, since it only depends on doping levels and applied voltage. To compensate for this reduction, the doping level in the channel needs to be increased. This reduces the source/drain depletion layer width that is extending in the channel, and increases the charge under the gate control. As shown in Figure 2.2 for the channel length reduction from 0.25 to 0.1 μm threshold voltage reduction for higher doping is 0.2 volts compared to 0.3 volts for lower doping. Both of these numbers are fairly large if we remember that the threshold voltage for such short channels will be somewhere around 0.4 volts [5]. This means that if we need transistors with two channel lengths on the same chip, we need to either increase the doping or use two different doping levels to adjust the threshold voltages.

Figure 2.2 Threshold voltage vs. channel length for different doping levels. p^+ gate. $t_{Si}=0.15 \mu\text{m}$. $V_{DS}=0.1 \text{ V}$

The negative side of increased doping is the reduction in carrier mobility and increased parasitic capacitance. Mobility is reduced because of the increased ionized impurity scattering. Parasitic capacitance increases because the increase in doping brings up a reduction in the depletion layer width and therefore an increase in the capacitance (capacitance is inversely proportional to the depletion layer width). Another important factor is source/drain junction depth. By reducing it in bulk or PD SOI MOSFETs, we can reduce the SCE and improve the device characteristics [12]. This reduction in junction depth is implicit in SOI FD devices since the film is very thin and the junctions end up at the buried oxide.

2.2.2 Drain Induced Barrier Lowering – DIBL

Increasing the drain voltage will not only influence the potential distribution near the body–drain junction but also throughout the device, all the way to the source–body junction.

tion. This will change the potential distribution between the source and drain and will decrease the potential barrier for holes at the source side. This has the same effect as an increase of the gate voltage [24]. For short channel devices this coupling is much stronger (source and drain are closer) and it can happen that the device is conducting even with gate–source voltage equal to zero. This renders the device useless. Due to the two–dimensional nature of this phenomena, analytical treatment is very complex and one needs to revert to numerical modeling and experimenting [24].

The influence of DIBL on the transfer curve is illustrated in Figure 2.3. For low V_{DS} of 0.1 volts all devices show good turn–off characteristic, i.e. low leakage current. By increasing the drain voltage, some of the devices turn on much earlier and the gate loses control of the drain current. Two points to notice are:

1. increasing the doping from 10^{15} to 10^{16} with silicon film thickness of $0.15\ \mu\text{m}$ decreases the off current by 13 times; this is a classical approach to reducing the DIBL in bulk MOSFETs and is applicable to SOI MOSFETs
2. thinning the silicon film thickness from 0.15 to $0.05\ \mu\text{m}$ for the doping of $10^{15}\ \text{cm}^{-3}$ reduces the off current by 250 times ! Obviously this approach is much more effective; it also results in substantially reduced parasitic capacitances but it is limited by manufacturing constraints (i.e. how thin silicon film can be)

In the presence of p^+ doping spike of $0.75 \times 10^{12}\ \text{cm}^{-2}$ which is used for threshold voltage adjustment, these reductions are 12 times for case 1. and 10^5 times for case 2., (all other parameters are the same). From this data we can see that thinning the silicon film is an extremely effective way of controlling the leakage. This drain–induced barrier lowering is further illustrated in Figure 2.4, which shows potential distribution from source to drain inside the $\text{Si}_{1-x}\text{Ge}_x$ channel. We can see that by thinning the silicon film this barrier increases and therefore the device turns off. Note that the current through MOSFET depends exponentially on this barrier since the device operates in a subthresh-

old region. Therefore, even a small change in this barrier has tremendous influence on the current.

Figure 2.3 Transfer curve for different doping and silicon film thickness for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET. Channel length $0.25 \mu\text{m}$. $V_{DS}=2 \text{ V}$. n^+ gate.

As described in [22], the same approach is possible in bulk MOSFETs if one uses a doping spike of the same type as the channel some distance under the gate (so called Pulse Shaped Doping – PSD). This is the same approach as modulation doping described earlier except that high doping has limited thickness, i.e. it does not extend to the substrate contact in the bulk case. Effectively, this limits the thickness of the depletion layer. Thus it brings the edge of the depletion layer closer to the gate and through two-dimensional coupling it reduces DIBL [24]. This design technique is used for designing the sub micron devices [25], [26].

Figure 2.4 Potential vs. horizontal position. Cross section in the $\text{Si}_{1-x}\text{Ge}_x$ channel. Channel length $0.25\text{ }\mu\text{m}$. $N_D=10^{15}\text{ cm}^{-3}$. $V_{DS}=2\text{ V}$. $V_{GS}=0.4\text{ V}$. n^+ gate.

2.2.3 Carrier Velocity Saturation

At low electric fields, the drift velocity is linearly proportional to the applied field (see Figure 2.5). This is true as long as the time between the carrier scattering is independent of the applied field. This is the case as long as the drift velocity is small compared to the thermal velocity of carriers, which is about 10^8 cm/s for silicon at room temperature. As the drift velocity approaches the thermal velocity, its dependence on the electric field will begin to depart from the linear relationship. At sufficiently large fields, the drift velocity approaches a saturation velocity, i.e. it becomes constant. The critical value of electric field for silicon is about 10^4 V/cm . Since mobility is given as a ratio between the velocity and electric field, and velocity becomes constant while the electric field is still increasing, mobility starts to fall off.

Figure 2.5 Measured drift velocity of carriers in pure silicon vs. applied electric field.

2.2.4 Increased Leakage

Leakage current is the current that flows through MOSFET when the gate voltage is zero or very close to zero. If the drain voltage is also very small, this current is very small. As we increase the drain voltage, this current starts to increase (see Figure 2.3 for $V_{DS}=0.1$ and 2 V results). Since drain–body junction is reversely biased, this current should be limited by the p–n junction saturation current. For very short MOSFETs this may not be the case since we have the influence of drain voltage on source–body potential barrier (DIBL). This influence increases further for low threshold voltage, since the small residual drain–source voltage of the previous gate is slightly turning on the gate of the next MOSFET. This problem becomes worse as the dimensions are scaled down, since requirements for normal operation and high speed also require threshold voltage reduction.

2.2.5 Hot Carrier Effects

A high electrical field at the drain–body junction accelerates carriers to very high velocities. Some of these carriers, so called hot carriers may gain enough energy to cause impact ionization and to overcome the gate–oxide barrier and generate gate current. This problem is more pronounced in n–MOSFETs since electrons have an impact ionization rate which is one to two orders of magnitude larger than the one for holes. They also have a smaller effective mass and thus can be more easily accelerated than holes. All this leads to problems with short and long–term device reliability and limits the power supply voltage. Usually, one also needs to use some drain engineering in order to improve device reliability (e.g. LDD, GO LDD, double diffused drain DDD).

2.3 Existing Approaches to Scaling

Two basic approaches to scaling are numerical and analytical. They both have their advantages, disadvantages and limitations. The analytical approach gives us closed expressions which enables what–if analysis and help us to better understand the issues and tradeoffs involved. Unfortunately, they are limited to calculation of very few variables and they tend to become mathematically very complex and thus loose the attractiveness of helping us to gain intuitive insight into the device operation. Another problem is that they can only treat simple structures. Since our devices will be non–uniformly doped and will have $\text{Si}_{1-x}\text{Ge}_x$ channel there is no simple way of taking the approaches published in the literature and tailoring them to $\text{Si}_{1-x}\text{Ge}_x$ SOI p–MOSFET. Only analytical approach presented in the literature is for calculating the threshold voltage [27]. As we will see later, a simple definition of inversion has been used for calculating the threshold voltage. Thus treatment is applicable only for long–channel devices and low drain–to–source voltages. Therefore, for realistic cases we are limited to numerical modeling. Most recent papers

dealing with scaling exclusively use numerical modeling even in the cases where simulated structures are relatively simple [22], [28], [29], [30]. The reason for that is that one can study variables which are too complex to be treated analytically, like DIBL, but are of great importance for proper device operation.

2.3.1 Analytical Approaches to Scaling

The simplest approach to analytical scaling is to scale all variables defining the MOSFET operation with fixed factor, in order to preserve the electric field contours in the device. This is so called constant field scaling [1]. The problem with this approach is that it requires scaling of the threshold voltage and the supply voltage. A reduction of threshold voltage increases the leakage current through DIBL, but this is not taken into account in this simple theory. Scaling of supply voltage was avoided in the past since it causes incompatibility and system level design problems in interconnecting ICs with different supply voltages. Therefore, the tendency is to keep the supply voltage standardized. Currently, the levels used are 5 V and 3.3 V, although further reduction in the device size will definitely require further reduction in the supply voltage. Improved analytical theories of scaling deal with problems mentioned previously by keeping the supply voltage constant or scaling only the channel length. Unfortunately, they all suffer from the same problems: they do not treat DIBL, mobility reduction due to increased doping, increase in parasitic capacitances due to increased doping, etc. Last two effects mentioned are forcing the device designers to consider non-uniform doping in order to improve the device performance. Analytical modeling of such devices is very complex and the majority of the published work was done by numerical simulations.

2.3.2 Numerical Approaches to Scaling

The main advantage of numerical modeling is that it can treat many variables that can only be treated partially or not treated at all by analytical means. Another advantage of numerical methods is that they do not have any limitations when it comes to device structure. Non-uniform doping, LDD/ GO LDD, $\text{Si}_{1-x}\text{Ge}_x$ channel and any other structure modification does not make this approach progressively more complex until it becomes impossible as is the case with analytical modeling. That is why modern device and technology development usually starts with two-dimensional device and process modeling [13], [31].

The main problem with analytical approaches is the time necessary to perform the simulations and the number of variables that influence the device behavior. It also limits one to explore only a limited number of variables. Another disadvantage is that after the simulations are performed, we do not end up with analytical expressions but with a set of data for simulated devices which can be used to observe general trends. Using modern simulation tools, one can devise an automated setup simulation of a large variety of devices. The devices modeled are simplified versions of the ones to be built. This reduces the time necessary to obtain the results. Once we have a rough idea of trends and issues involved, and have narrowed down the design options, we can revert to a more detailed modeling by including a detailed structure of the device and more complex physical models.

CHAPTER 3

METHODOLOGY AND SIMULATION SETUP

3.1 Our Approach to Scaling of the Si and $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET

As mentioned earlier, we will use two-dimensional numerical simulations in order to study the scaling properties of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFETs. A variety of p-MOSFETs with and without $\text{Si}_{1-x}\text{Ge}_x$ channel will be simulated. The program which will be used is TMA's simulator MEDICI [32]. Using this simulator we will develop an automated setup and will simulate a large variety of device structures. The devices that will be modeled are simplified versions of the ones to be built. This greatly reduces the time necessary to obtain the results and enables us to observe general trends, advantages and disadvantages of each design option simulated.

3.2 Device Description

The general structure of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET that will be simulated is presented in Figure 1.4. A more detailed structure with all dimensions is given in Figure 3.1.

Silicon cap, $\text{Si}_{1-x}\text{Ge}_x$ channel and silicon buffer layer are undoped or very lightly doped (10^{15} cm^{-3}) in order to preserve high mobility in these layers. This is important because the majority of current is going to flow either in $\text{Si}_{1-x}\text{Ge}_x$ channel or at the Si/ SiO_2 interface. We used n-type doping of 10^{15} cm^{-3} . Mobility reduction caused by this doping is negligible for both electrons and holes.

charge on them. The thickness of the silicon film was varied from 0.15 to 0.04 μm . The later one is the minimum dimension currently obtainable [11]. Germanium mole fraction in the channel is 0.3.

3.3 Design Criteria

3.3.1 Threshold Voltage

The threshold voltage (V_{TH}) is one of the most often used parameters for the MOSFET characterization. Unfortunately, this number is not unique at all. There are quite a few definitions and one has to be very careful when this number is given for a certain device to find out which definition was used. Generally we can divide those definitions in two groups:

1. based on carrier concentrations at the front Si/SiO₂ interface
2. based on current flowing through the device

Definitions from the first group are used in theoretical calculations since vertical distribution of carriers in *long-channel* MOSFET can be easily calculated. Definition of the long-channel device comes from the theoretical issues and assumptions used in calculating the threshold voltage. For the sake of simplicity we simply state that the device is long-channel device if measured or simulated threshold voltage coincides with the one obtained using well known formulas [2],[35] (see Chapter 5.1). This definition of the V_{TH} states that the threshold voltage is the voltage on the gate necessary to *invert* the surface. The point of inversion is defined as the condition when the minority carrier concentration at the front gate is equal to the doping level in the bulk [35]. At that point the potential at the surface is equal to twice the doping potential (see Equations (3.1) to (3.3)).

$$\text{Doping potential : } \begin{cases} N_A \gg N_D \Rightarrow \phi_{dop} = -\frac{kT}{q} \ln \frac{N_A}{n_i} & nMOSFET \\ N_D \gg N_A \Rightarrow \phi_{dop} = +\frac{kT}{q} \ln \frac{N_D}{n_i} & pMOSFET \end{cases} \quad (3.1)$$

$$(3.2)$$

$$\text{Surface potential in inversion : } \phi_S = 2 |\phi_{dop}| \quad (3.3)$$

Another assumption built in to these equations is that of *low* drain voltage (typically 0.1 volts and less). In this case the equations turn out to be independent of the drain voltage and thus cannot be used to study the influence of DIBL on the device behavior.

There are two definitions in the second group that are of interest to us. A very important difference from the first group is that they do not require an assumption of the long-channel device. Since we are going to look at the scaling of devices these definitions are better suited for our purpose. One definition of the threshold voltage uses the measured drain current vs. gate voltage curve (transfer curve) for low drain-to-source voltage of typically 0.1 volts or less. This low drain-to-source voltage ensures that MOSFET is operating in the linear region. Threshold voltage is found by linear extrapolation of this curve in its linear region to its crossing of the horizontal axis (see Figure 3.2).

From the same figure we can see why this definition is useless for high drain-to-source voltages ($V_{DS}=2$ V). In this case, the slope of the transfer curve is larger because of increased V_{DS} . Extrapolating this curve to the horizontal axis gives us *larger* threshold voltage, although we need smaller gate overdrive $V_{GS}-V_{TH}$ to obtain the same current in the device. This is also illustrated in Table 3.1 where we see that the threshold voltage for V_{DS} of 2 volts is 0.3 volts larger than the one for small V_{DS} . Therefore, this definition is impractical for quantifying the influence of drain-induced barrier lowering on the device operation.

Figure 3.2 Transfer characteristic for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET. Channel length $0.5 \mu\text{m}$. n^+ gate. $N_D=10^{15} \text{ cm}^{-3}$. $t_{\text{Si}}=0.15 \mu\text{m}$.

A more useful definition is the constant drain current definition. In this method, the V_{TH} is taken to be the voltage on the gate that is needed to obtain a certain current in the device, I_{DSX} [36], [37]. The problem with this definition is that this current should be independent of the device geometry in the same way the slope definition is. Therefore, this current is specified as a current per width over length ratio (Equation (3.4)). Since the current through the MOSFET device is proportional to a width over length ratio, this definition is independent of device geometry. From Table 3.1 we can see that this definition gives threshold voltage reduction with increased drain to source voltage as one would expect. The current level used in this calculation was $I_{\text{DSX}}=100 \text{ nA}$ which is standard value used in the literature [29], [38]. We also see that threshold voltages which are calculated using those two definitions are very close for low V_{DS} . For high V_{DS} , this difference becomes very large (0.4 volts).

$$V_{TH} = V_{GS} \quad @ \quad I_{DS} = \frac{I_{DSX}}{\left(\frac{W}{L}\right)} \quad (3.4)$$

W = device width L = device length I_{DSX} = constant current level

Table 3.1 Comparison of the threshold voltage for different V_{DS} voltage measured by two different methods.

V_{DS} (V)	0.1	2
V_{TH} from slope (V)	-0.92	-1.2
V_{TH} from current (V)	-0.83	-0.79

Figure 3.3 Transfer characteristic for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET on semilog scale. Channel length 0.5 μm . n^+ gate. $N_D=10^{15} \text{ cm}^{-3}$. $t_{\text{Si}}=0.15 \mu\text{m}$.

In the case of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET the situation becomes even more complicated. Since we can have inversion first in the channel or at the front gate interface, if one wants to use the inversion point as definition one needs to determine which case is going to hap-

pen. This depends on the device structure and bias. One theoretical study for the threshold voltage of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET was presented in [27]. As all other theoretical studies, it uses inversion as a definition of the threshold voltage. This means that those results are not applicable for short channel devices, high V_{DS} voltages and cannot be used to study DIBL. Note that the same is true in the case of a simple theory for calculating the threshold voltage of bulk MOSFET. Results between the two cases are compared in Table 3.2. We can see that the difference between the results for low doping levels is substantial and that it is reduced for higher doping. Some of that difference comes from the different structures used: their oxide thickness is 12 nm compared to 7 nm in our case and they do not assume any fixed charge on Si/SiO₂ interface. The rest comes from a different definition for the threshold voltage. As we will later see, simulated results (i.e. the one obtained by current definition) agree very well with measured data which further confirms that constant current level definition is much more useful.

Table 3.2 Comparison of the threshold voltages from our simulation and the ones published in [27]. $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET. Silicon film thickness 0.1 μm . n^+ gate.

Doping (cm^{-3})	1×10^{15}	1×10^{16}	1×10^{17}
V_{TH} from current (V)	0.94	0.98	1.15
V_{TH} from inversion [27] (V)	0.60	0.72	1.2

The acceptable limits for the threshold voltage that we will use are between 0.4 and 0.7 volts. These numbers are somewhat arbitrary and depend on the choice of channel length, supply voltage, long and short term reliability, static power dissipation and other factors [5]. Some of the published data is presented in Table 3.3. Those limits were used in a recent study of scaling of SOI n-MOSFETs and will enable direct comparison with our results [29].

Table 3.3 Threshold and supply voltage for different CMOS technologies.

Channel length (μm)	0.4	0.5	0.25	0.5
Threshold voltage (V)	± 0.45	± 0.25	± 0.4	0.6/-0.8
Supply voltage (V)	3.3	3.5	2.5	5
Reference	[13]	[4]	[39]	[40]

Lower limit on the threshold voltage comes from the leakage current constraints and requirement on static power dissipation. This leakage current is in the ideal case described by the diode equation (3.5) and is equal to the reverse saturation current I_S . This is reverse saturation current of drain-body diode which is reversely biased (see Figure 2.1).

$$I_D = I_S (e^{qV/kT} - 1) \approx -I_S \text{ for reverse bias, i.e. } |V| \gg kT/q \quad (3.5)$$

I_S = reverse saturation current V = diode voltage; negative for reverse bias

Another important factor in digital circuits is noise margins which are reduced as the threshold voltage is reduced [1]. This reduction makes the gate susceptible to switching and power supply noise that may be present at the inputs.

A higher limit on threshold voltage comes from the power supply limitations and acceptable gate overdrive $V_{GS} - V_{TH}$ needed to obtain a certain current level in the device. This gate overdrive also determines the circuit speed and the larger it is the better. For a fixed supply voltage we can increase this overdrive by reducing the threshold voltage, but we are limited by leakage constraints and static dissipation.

3.3.2 Short Channel Effect (SCE)

Once we have a good definition for the threshold voltage, calculation of the short channel effect is a straightforward task. From the definition that the SCE is reduction of

the threshold voltage due to the shortening of the channel we obtain this equation:

$$\Delta V_{TH(SCE)} = V_{TH}(L = 1 \mu m) - V_{TH}(L = x \mu m) \quad (3.6)$$

$$\text{where } x < 1 \mu m$$

In this definition, the channel length of 1 μm is taken to be the length of long-channel device. This means that the threshold voltage calculated theoretically for a device of this length should be close to the one obtained by simulations or measurement. This assumption will be checked later for the devices that we will simulate.

There are no special criteria for acceptable SCE threshold voltage reduction. If we are going to have the transistors with only one channel length on a chip we can compensate for this reduction by increasing the doping and adjusting the threshold voltage to any level we need. In a more complicated case where we have multiple channel lengths on the same chip there are two possibilities. One is to use high doping in the channel in order to reduce the threshold voltage dependence on the channel length. Unfortunately, this at the same time increases the threshold voltage. The other option is to use different doping for different channel lengths. As pointed out in [5] this will slightly increase the processing cost but is already used in DRAM chips where the threshold voltage of the array devices with fixed body biased is increased by using second implantation.

3.3.3 Drain-Induced Barrier Lowering

As in the case of the SCE, once we have a good definition for the threshold voltage, calculation of DIBL is a simple task. As explained, the definition using the constant current level gives consistent results for low and high V_{DS} and will be used in this calculation. Drain induced barrier lowering is defined as:

$$\Delta V_{TH(DIBL)} = V_{TH}(V_{DS} = 0.1V) - V_{TH}(V_{DS} = 2V) \quad (3.7)$$

Acceptable levels are again somewhat arbitrary and depend on the particular application. In our case we are going to use the value of 100 mV per volt of drain voltage which is the standard value used in the literature [28],[29].

$$\frac{\Delta V_{TH(DIBL)}}{V_{DS}} \leq 100 \frac{mV}{V} \quad (3.8)$$

If this criterion needs to be sharpened, one can skip the design curves and find the real threshold voltage reduction due to the DIBL from the available results, and use those numbers in the design process.

3.3.4 Subthreshold Slope S

If we plot the V_{GS} – I_{DS} curve in the subthreshold region (i.e. below the threshold voltage) on a linear–log scale we get a straight line (Figure 3.3). This means that the subthreshold current is exponentially dependent on the V_{GS} . The inverse slope of this line expressed in millivolts per decade is called subthreshold slope (or sometimes inverse subthreshold slope). The steeper the slope is, the smaller the gate voltage needed to turn the device on or off.

In order to get the fastest possible circuits, V_{TH} needs to be reduced as much as possible. With its reduction we increase the gate overdrive (i.e. V_{GS} – V_{TH}) and increase the current charging or discharging the parasitic capacitances connected to the output of the digital gate. The lower limit for the threshold voltage is defined by the leakage current through allowable static power dissipation and the steepness of the subthreshold slope.

The slope is given by the following expression:

$$S \approx \frac{kT}{q} \ln \left(10 \left(1 + \frac{C_D + C_{it}}{C_{ox}} \right) \right) \quad (3.9)$$

C_D = depletion capacitance.

$C_{it} = q D_{it}$ = interface trap capacitance.

D_{it} = interface trap density.

From this equation we can see that the subthreshold slope can be increased by reducing the depletion layer capacitance, i.e. by reducing the doping level. In a fully-depleted device, once the Si film is completely depleted any increase in gate voltage increases the inversion layer charge and leaves C_D unchanged [10]. Therefore, FD devices have a smaller subthreshold slope. The theoretical limit is $kT/q \ln(10)=60$ mV/dec. This slope also indicates if the device is fully or partially depleted since the slope increases abruptly at the transition between the two. For a short-channel device Equation (3.9) is no longer valid, but the subthreshold slope still remains sharper for FD devices [10].

3.3.5 Threshold Voltage Sensitivity to Silicon Film Thickness

Since the depletion layer depth in FD SOI devices is limited by the silicon film thickness, the charge in this layer will also depend on this thickness. This charge defines the threshold voltage and hence we have the threshold voltage dependence on the silicon film thickness. This is of concern from the manufacturing point of view because the silicon film thickness variation across the wafer will modulate the threshold voltage [7]. Such variation requires very tight control of the silicon film thickness. This problem does not exist in the PD and bulk devices, since the depletion layer width is smaller than the silicon film thickness. There are three basic methods to avoid or minimize this dependence. The first one is to build PD devices and thus completely avoid this problem. The second one

is to build devices which are near-fully depleted [14]. These devices will have smaller threshold voltage dependence on the silicon film thickness than the FD ones and will also preserve some advantages of FD devices like higher mobility and sharp subthreshold slope. The third option is to minimize this variation in FD devices by designing a MOSFET to have a constant dose in the body instead of the constant doping level [41]. If one minimizes the *retained* dose variation, the threshold voltage sensitivity will be minimized. This is because the threshold voltage is proportional to the sheet charge under the gate, and not the charge density which is equal to the doping level.

A technology with near-fully depleted devices was developed and presented in [13]. The threshold voltage sensitivity was about 20–30 mV/10 nm, which is about one third of that for FD devices with similar doping.

Assuming that the silicon film thickness variation is about 10 nm [7] and that we want to control the threshold voltage with $\pm 10\%$ we need this sensitivity to be less than 45 mV/10 nm for the threshold voltage of 0.45 V.

3.4 Simulation Setup

3.4.1 Introduction to MEDICI

MEDICI models two-dimensional distributions of potential and carrier concentrations inside the specified device in order to predict its electrical characteristic for specified bias conditions. This is done by solving Poisson's and two continuity equations for a set of discrete points which are used to approximate the device structure. In order to simulate a device, the regions of different materials and the doping profiles need to be specified. Then a mesh needs to be set up, i.e. the set of points (also called nodes) for which solutions are calculated must be determined. Initial mesh has to be set up by "hand". Re-

fining the mesh (regrid) based on doping and potential variations can be used to create a fine mesh in the regions where physical quantities change abruptly.

It is very hard to predict what effect regrid will have, i.e. how many points will be added. It is very likely that the regrid has almost no effect or that the number of allowed points will be exceeded. Since we are going to design an adaptive mesh, where the dimensions of the device are going to change from one simulation to another, this makes it impractical to use regrid function. Instead mesh will be hand crafted and points need to be located where it is expected that physical quantities are going to change substantially within a short distance, e.g. $\text{Si}_{1-x}\text{Ge}_x$ channel and Si/SiO_2 interface where current is flowing, source/drain-body junctions where doping profile is changing abruptly.

Next, a set of models which are going to be used needs to be specified. These models include models for physical quantities such as recombination and mobility, material properties and boundary conditions.

After this, Poisson's and the continuity equations have to be solved. In order to solve these equations the algorithm needs to have an initial guess. This could either be a previous solution or a projection obtained by the last two solutions. This is in most cases the most efficient way to find a solution, and it is used by the program automatically once it has two previous solutions. In order to use projection when starting off with previously saved solutions, two solutions have to be loaded by `LOAD INFILE=<name1>` and `LOAD IN2FILE=<name2>`.

This procedure of simulating the device is outlined in the Figure 3.4. The complete input deck for MEDICI simulation with explanations is given in Appendix A. A detailed explanation of every command in the input deck can be found in [32]. Also refer to Figure 3.1 for device dimensions and coordinate system definition.

Figure 3.4 Simulation procedure in MEDICI. Steps marked as * are not always necessary, especially if we simulate only one simple device. Order of definitions and specification is not strictly fixed except for 10) and 11) which come last.

3.4.2 Mobility Modelling

In the basic three equations that MEDICI solves, certain physical parameters like mobility and recombination appear. There are different models for these physical quantities available in MEDICI and one needs to select the ones which correctly describe the device. One also needs to be careful when interpreting the results since the selection of these models directly determines the set of phenomena that can be analyzed. Also, one has to keep the limitations of any model in mind in order to interpret the results correctly.

A detailed explanation of these models and their applicability to MOSFET modeling can be found in [32]. Values for each of the models are chosen based region's material.

Models and data for silicon and silicon–dioxide are readily available in MEDICI. In the case of strained $\text{Si}_{1-x}\text{Ge}_x$ they are assumed to be the same, except for the bandgap reduction due to Ge content which is appropriately modeled. As pointed out in the introduction, two main physical properties of $\text{Si}_{1-x}\text{Ge}_x$ of interest in p–MOSFET application are band–gap reduction and hole mobility enhancement. The first one is already modeled but the second one is assumed to be the same as in silicon. This would give incorrect results, so we need to change the mobility parameters for $\text{Si}_{1-x}\text{Ge}_x$. First, we will summarize the mobility models available in MEDICI and then see how they can be modified to account for the effect of $\text{Si}_{1-x}\text{Ge}_x$.

There are two basic categories of mobility models in MEDICI:

1. mobility models that depend on transverse electric field *only* at the Si/SiO₂ interface (SFRMOB and SRFRMOB2)
2. mobility models that depend on vertical electric field *anywhere* in the device (PRPMOB, HPMOB, LSMMOB)

Mobility models from group 1. degrade the mobility of the carriers only at the surface and therefore the current reduction is dependent on the number of carriers associated with the nodes at the Si/SiO₂ interface. Therefore, the vertical grid spacing needs to be set up so that the inversion layer width is less than the grid spacing, i.e. so that all carriers are located at the nodes at Si/SiO₂ interface. This makes these models not only grid dependent but also dependent on the gate bias since this bias defines the vertical distribution of the carrier and the width of the inversion layer. This should be avoided and more sophisticated mobility models should be used [42].

Mobility models from group 2. depend on the vertical electric field and are grid *independent* as long as the grid is fine enough. This makes them very useful for mobility mod-

eling in our case since the device structure and thus a grid setup is going to be changed as the simulator is going through the loop.

In order to take into account the hole mobility increase in the $\text{Si}_{1-x}\text{Ge}_x$ we tried to increase the low field mobility by a factor of two as suggested in [15]. For the $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET without p^+ doping spike this results in smooth transconductance curve with improved transconductance. Unfortunately, including p^+ doping spike results in a large peak in the transconductance curve as shown in Figure 3.5. We can also see a smaller second peak. These peaks are associated with the current flow along the bottom and the top silicon-silicon-germanium interface and the electric field direction reversal due to the p^+ spike charge [22]. Since these results were not observed experimentally, it was decided that in order to model the mobility improvement the vertical field dependence of mobility needs to be removed for the $\text{Si}_{1-x}\text{Ge}_x$ layer (line 85 in Figure A.13), as follows.

$$\mu_{S,p} = \frac{\mu_{0,p}}{\sqrt{1 + \left(\frac{E_{\perp,p}}{ECP.MU} \right)^2}} \quad (3.10)$$

$\mu_{S,p}$ = hole mobility, *PRPMOB*

$E_{\perp,p}$ = perpendicular electric field

$\mu_{0,p}$ = low field hole mobility

ECP.MU = critical electric field

since $ECP.MU = 10^{10} \frac{V}{cm}$ and $E_{\perp} \leq 4 \cdot 10^5 \frac{V}{cm}$ @ $V_{GS} = -5 V \Rightarrow$

$$\Rightarrow \mu_{S,p} = \frac{\mu_{0,p}}{\sqrt{1 + \left(\frac{E_{\perp,p}}{ECP.MU} \right)^2}} \approx \mu_{0,p}$$

Figure 3.5 Transconductance of SOI p-MOSFET with different mobility models. n^+ gate. Channel length $1\text{ }\mu\text{m}$. $N_D=10^{15}\text{ cm}^{-3}$.

3.5 Phenomena that can be Evaluated Using Chosen Models

As mentioned before, one needs to be careful when interpreting the results since the selection of models directly determines the set phenomena that can be analyzed. Here we list those phenomena and the MEDICI models required:

1. mobility reduction due to the surface scattering (PRPMOB)
2. velocity saturation and its effects (FLDMOB)
3. threshold voltage (CONTACT, mobility models, FLDMOB)
4. threshold voltage sensitivity to silicon thickness (same as for V_{TH})
5. DIBL (no special models needed, solution of at least one continuity equation is necessary)
6. subthreshold slope (Poisson's and one continuity equation)
7. SCE (Poisson's and one continuity equation)

The phenomena that cannot be evaluated in this setup are breakdown voltage and kink effect. Since they are caused by impact ionization, we need to include this model and the electron continuity equation. For example, with such a setup, Figure 1.3 which illustrates kink effect was generated.

3.6 Range of Variables Simulated

For convenience a complete list of simulated variables is listed here:

1. n^+ and p^+ gate
2. silicon film thickness: 0.15, 0.1, 0.06, 0.05 and 0.04 μm
3. channel length: 1, 0.8, 0.5, 0.25, 0.1 μm
4. p^+ spike dose: 0.25×10^{12} to $1.5 \times 10^{12} \text{ cm}^{-2}$ for V_{TH} adjustment

3.7 Simulation Setup and Results Verification

In order to check the simulation setup and that the results represent reasonable values, a variety of devices similar to the ones published in the literature were simulated. Table 3.4 gives the basic properties of those devices.

Table 3.4 Basic properties of p-MOSFET devices compared in Table 3.5.

Device	t_{ox} (nm)	t_{CAP} (nm)	L_{CH} (μm)	N_{D} (cm^{-3})
SOI SiGe OUR	7	10	1 and 0.25	1×10^{15}
SOI SiGe FROM [16]	6.5	10	10 and 1	1.2×10^{15}
Bulk SiGe FROM [43]	5	10	0.7	5×10^{16}
Bulk SiGe FROM [44]	7	7	1 and 0.25	$> 10^{17}$
Bulk SiGe FROM [45]	7	7	1	?

Data for long-channel devices is given in Table 3.5 and 3.6. Data for linear transconductance for bulk MOSFETs is not available so it is impossible to make any reasonable comparison. For the SOI case, our simulations give 60% larger linear transconductance

than the experiments. This may be connected with the quality of SOI film. In [16] it was noted that their devices exhibit lower mobility than expected. Results for the saturation transconductance in SOI MOSFETs agree well with published results, i.e. within 10%. Also note that improvement due to the $\text{Si}_{1-x}\text{Ge}_x$ channel is consistent with published data which proves that the mobility model used in $\text{Si}_{1-x}\text{Ge}_x$ is appropriate for modeling of this device. Plots of the linear transconductance versus gate voltage for different channel lengths are given in Figure 3.6. Peak linear transconductance is independent of the channel length all the way down to the 0.1 μm when velocity saturation effects come into play.

Table 3.5 Peak linear and saturation transconductance for bulk p-MOSFET device. Long channel device.

Device	g_{mL} ($\mu\text{S}/(\text{W}/\text{L})$)	g_{mS} ($\mu\text{S}/(\text{W}/\text{L})$)
Bulk FROM [44] $L_{CH}=1 \mu\text{m}$	–	52 @ $V_{DS}=-2.5 \text{ V}$
Bulk FROM [45] $L_{CH}=1 \mu\text{m}$	–	30 @ $V_{DS}=-5 \text{ V}$
Bulk SiGe FROM [43] $L_{CH}=0.7 \mu\text{m}$	5.9 @ $V_{DS}=-0.1 \text{ V}$	45.1 @ $V_{DS}=-2.5 \text{ V}$
Bulk SiGe FROM [44] $L_{CH}=1 \mu\text{m}$	–	64 @ $V_{DS}=-2.5 \text{ V}$
Bulk SiGe FROM [45] $L_{CH}=1 \mu\text{m}$	–	46 @ $V_{DS}=-5 \text{ V}$

Table 3.6 Peak linear and saturation transconductance for SOI p-MOSFET device. Long channel device.

Device	g_{mL} ($\mu\text{S}/(\text{W}/\text{L})$)	g_{mS} ($\mu\text{S}/(\text{W}/\text{L})$)
SOI OUR $L_{CH}=1 \mu\text{m}$	6.8 @ $V_{DS}=-0.1 \text{ V}$	65 @ $V_{DS}=-2 \text{ V}$
SOI FROM [16] $L_{CH}=10 \mu\text{m}$	5.2 @ $V_{DS}=-0.1 \text{ V}$	63 @ $V_{DS}=-2.5 \text{ V}$
SOI SiGe OUR $L_{CH}=1 \mu\text{m}$	12 @ $V_{DS}=-0.1 \text{ V}$	75 @ $V_{DS}=-2 \text{ V}$
SOI SiGe FROM [16] $L_{CH}=10 \mu\text{m}$	7.3 @ $V_{DS}=-0.1 \text{ V}$	78 @ $V_{DS}=-2.5 \text{ V}$

In the case of short-channel devices, peak transconductance is reduced due to the velocity saturation effect. Improvement due to the $\text{Si}_{1-x}\text{Ge}_x$ channel is also reduced due to this effect. This shows once more that as we scale down the channel length we need to

reduce the supply voltage in order to obtain the maximum performance. This is also illustrated in Figure 3.7 where we see that reduction in the channel length results in the reduction of the peak saturation transconductance.

Table 3.7 Peak linear and saturation transconductance for p-MOSFET device. Short channel device.

Device	g_{mL} ($\mu S/(W/L)$)	g_{mS} ($\mu S/(W/L)$)
SOI OUR $L_{CH}=0.25 \mu m$	5.25 @ $V_{DS}=-0.1 V$	36 @ $V_{DS}=-2 V$
Bulk FROM [44] $L_{CH}=0.25 \mu m$	–	35 @ $V_{DS}=-2.5 V$
SOI SiGe OUR $L_{CH}=0.25 \mu m$	8 @ $V_{DS}=-0.1 V$	38 @ $V_{DS}=-2 V$
Bulk SiGe FROM [44] $L_{CH}=0.25 \mu m$	–	42 @ $V_{DS}=-2.5 V$

Figure 3.6 Linear transconductance vs. V_{GS} for different channel lengths. $V_{DS}=0.1 V$. $t_{Si}=0.1 \mu m$. $N_D=1 \times 10^{17} cm^{-3}$. p^+ gate.

Figure 3.7 Saturation transconductance vs. V_{GS} for different channel lengths. $V_{DS}=2$ V. $t_{Si}=0.1 \mu m$. $ND=1 \times 10^{17} \text{ cm}^{-3}$. p^+ gate.

CHAPTER 4

Simulation of SOI Si and $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET with n^+ GATE

4.1 Results for SOI p-MOSFET

First, we will take a look at the results for SOI p-MOSFET without $\text{Si}_{1-x}\text{Ge}_x$ channel. In order to get some idea of the doping levels that may result in acceptable threshold voltages, simple calculations were done using the equations from [2]. Note that this threshold voltage is only for long-channel devices and as we scale the channel length the threshold voltage will be reduced due to SCE. Also, as we change the doping level and the silicon thickness the device will change from PD to FD one. In order to know in which regime the device operates, one has to compare the silicon film thickness and the maximum depletion layer width. The later one, for convenience is given in Table 4.1.

Table 4.1 Maximum depletion layer width for different doping levels.

$N_{\text{DOP}} (\text{cm}^{-3})$	1×10^{15}	3×10^{15}	6×10^{15}	1×10^{16}	3×10^{16}
$X_{\text{d,max}} (\mu\text{m})$	0.86	0.52	0.38	0.30	0.18

$N_{\text{DOP}} (\text{cm}^{-3})$	6×10^{16}	1×10^{17}	3×10^{17}	6×10^{17}	1×10^{18}
$X_{\text{d,max}} (\mu\text{m})$	0.13	0.10	0.061	0.044	0.035

The problem with using the equations from [2] for calculating the threshold voltage is the fact that we need to know the surface potential at the silicon–buried oxide interface, i.e. at the back gate. Since there is no formula which we could use to calculate this value we are going to calculate the threshold for two extreme cases:

1. back gate accumulated $\rightarrow$ back surface potential approximately zero
2. back gate inverted $\rightarrow$ back surface potential approx. twice the doping potential

Calculations were done as follows (note that for higher doping we used a thinner device in order to ensure the condition of full depletion for which these equations are derived):

Doping of 10^{15} cm^{-3}

$$\text{Built in potential : } \phi_{fn} = \frac{k T}{q} \ln \frac{N_D}{n_i} = 0.0259 \ln \frac{1 \cdot 10^{15}}{1.5 \cdot 10^{10}} = 0.29 \text{ V}$$

$$\text{Max. Depl. Layer Width : } x_{d,max} = \sqrt{\frac{4 \epsilon_{Si} \phi_{fn}}{q N_D}} = 0.87 \mu\text{m}$$

Back Gate Accumulated

$$\phi_{MS1} = \phi_{n^+} - \left(\chi_{Si} + \frac{E_G}{2q} - \phi_{fn} \right) ; \quad \phi_{n^+} = 4.17 \text{ V}$$

$$\phi_{MS1} = 4.17 - (4.15 + 0.56 - 0.29) = -0.25 \text{ V}$$

$$\text{Depletion Layer Charge : } Q_{depl} = q N_D t_{Si} = 2.4 \cdot 10^{-9} \frac{\text{As}}{\text{cm}^2}$$

$$C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}} = \frac{3.9 \cdot 8.854 \cdot 10^{-14}}{7 \cdot 10^{-7}} = 4.93 \cdot 10^{-7} \frac{\text{F}}{\text{cm}^2}$$

$$C_{Si} = \frac{\epsilon_{Si}}{t_{Si}} = \frac{11.7 \cdot 8.854 \cdot 10^{-14}}{0.15 \cdot 10^{-4}} = 6.91 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$V_{TH1,acc2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} - \left(1 + \frac{C_{Si}}{C_{ox1}} \right) 2 \phi_{fn} - \frac{Q_{depl}}{2 C_{ox1}}$$

$$V_{TH1,acc2} = -0.25 - 0.032 - 0.66 - 0.002 = -0.944 \text{ V}$$

Back Gate Inverted

$$V_{TH1,inv2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} - 2 \phi_{fn} - \frac{Q_{depl}}{2 C_{ox1}}$$

$$V_{TH1,inv2} = -0.25 - 0.032 - 0.58 - 0.002 = -0.864 \text{ V}$$

Doping of 10^{17} cm^{-3} :

$$\text{Built in potential : } \phi_{fn} = \frac{k T}{q} \ln \frac{N_D}{n_i} = 0.0259 \ln \frac{1 \cdot 10^{17}}{1.5 \cdot 10^{10}} = 0.41 \text{ V}$$

$$\text{Max. Depl. Layer Width : } x_{d,max} = \sqrt{\frac{4 \epsilon_{Si} \phi_{fn}}{q N_D}} = 0.1 \mu m$$

$$x_{d,max} = 0.1 \mu m > t_{Si} = 0.06 \mu m \Rightarrow \text{fully depleted device}$$

Back Gate Accumulated

$$\phi_{MS1} = \phi_{n^+} - \left(\chi_{Si} + \frac{E_G}{2q} - \phi_{fn} \right) ; \quad \phi_{n^+} = 4.17 \text{ V}$$

$$\phi_{MS1} = 4.17 - (4.15 + 0.56 - 0.41) = -0.13 \text{ V}$$

$$\text{Depletion Layer Charge : } Q_{depl} = q N_D t_{Si} = 96 \cdot 10^{-9} \frac{\text{As}}{\text{cm}^2}$$

$$C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}} = \frac{3.9 \cdot 8.854 \cdot 10^{-14}}{7 \cdot 10^{-7}} = 4.93 \cdot 10^{-7} \frac{\text{F}}{\text{cm}^2}$$

$$C_{Si} = \frac{\epsilon_{Si}}{t_{Si}} = \frac{11.7 \cdot 8.854 \cdot 10^{-14}}{0.15 \cdot 10^{-4}} = 6.91 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2}$$

$$V_{TH1,acc2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} - \left(1 + \frac{C_{Si}}{C_{ox1}} \right) 2 \phi_{fn} - \frac{Q_{depl}}{2 C_{ox1}}$$

$$V_{TH1,acc2} = -0.41 - 0.032 - 0.94 - 0.1 = -1.5 \text{ V} \quad (4.1)$$

Back Gate Inverted

$$V_{TH1,inv2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} - 2 \phi_{fn} - \frac{Q_{depl}}{2 C_{ox1}}$$

$$V_{TH1,inv2} = -0.41 - 0.032 - 0.81 - 0.1 = -1.35 \text{ V}$$

From the calculations we can see that the threshold voltage is too high. This is a well-known problem with bulk p-MOSFETs with n^+ gate and, as this calculation illustrates,

FD SOI devices also suffer from it. The technique usually used to adjust the threshold voltage to an acceptable level is implantation of boron (p-type dopant) in the channel. This results in a buried channel type device, which is very susceptible to SCE [46]. In the case of $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET this doping would be in the silicon cap and the $\text{Si}_{1-x}\text{Ge}_x$ layer and would therefore decrease the device's performance. That is why in this case the doping is located underneath the channel. Since we want to compare scaling of regular SOI p-MOSFET and $\text{Si}_{1-x}\text{Ge}_x$ one, we will locate this p^+ spike at the same distance from the front gate, i.e. at $0.03\text{ }\mu\text{m}$. Note that the doping profiles presented in [25], [47] and [48] are basically the same as this one except that in their case the doping is the same type as the channel (i.e. n-type for p-MOSFET and vice versa). By properly adjusting the spike dose, one can use body doping from 10^{15} to 10^{17} cm^{-3} . Since this is a large range we have divided results in two groups:

1. doping from 10^{15} to 10^{16} cm^{-3} – low doping
2. doping from 10^{16} to 10^{17} cm^{-3} – high doping

4.1.1 Results for Si SOI p-MOSFET with n^+ Gate and Low Doping

Threshold voltages for the Si SOI p-MOSFET with n^+ gate and low doping without the threshold voltage adjustment (i.e. no p^+ spike) are given in Figures 4.1 to 4.5.

First, we can see that the threshold voltage for a long-channel device of $1\text{ }\mu\text{m}$ is between the two extreme cases we calculated. This threshold is only slightly dependent on the doping level since very low doping was used. It is also very slightly dependent on the silicon film thickness. This is again the result of low doping. If we look at the calculation of the threshold voltage, we can see that the contribution from the depletion layer charge is only about 0.1 volts which is much smaller than the threshold voltage (Equation (4.1)).

Comparing the threshold voltages for different channel lengths we can see that the SCE is minimal for the channel lengths larger than $0.5\text{ }\mu\text{m}$ even in the case of thick films. As we reduce the channel length, we need to reduce the film thickness in order to control the SCE. For a channel length of $0.1\text{ }\mu\text{m}$ even the thinnest film is not thin enough and we would have to reduce it even further. Since the threshold voltage adjustment requires the implantation of p^+ spike which is going to make SCE even worse, as it will be shown later, this is obviously not a good strategy for designing very short channel MOSFETs.

Figure 4.1 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $1\text{ }\mu\text{m}$. No p^+ spike.

Figure 4.2 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.8 \mu\text{m}$. No p^+ spike.

Figure 4.3 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.5 \mu\text{m}$. No p^+ spike.

Figure 4.4 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET, n^+ gate. Channel length $0.25 \mu\text{m}$. No p^+ spike.

Figure 4.5 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET, n^+ gate. Channel length $0.1 \mu\text{m}$. No p^+ spike.

Next, a set of results for the same p-MOSFET with p⁺ spike will be discussed. Three spike doses were simulated: 0.25, 0.5 and $0.75 \times 10^{12} \text{ cm}^{-2}$. As it turned out, the first two spikes did not give any acceptable designs. The threshold voltage was either too high for longer channel devices, or SCE and DIBL were too large for short-channel devices.

From the results a set of design curves was developed. They represent doping levels and the silicon film thickness for which p-MOSFET satisfies design criteria for the threshold voltage and DIBL. The design curves for all channel lengths, except for 1 and 0.1 μm , are given in Figures 4.6 to 4.8. For 1 μm we would need to increase the spike dose even further in order to reduce the threshold voltage below 0.7 volts. Since modern technologies are regularly designed with sub micrometer channel lengths this option was not pursued further. From the available data, we can state that a doping spike of $1 \times 10^{12} \text{ cm}^{-2}$ would probably be sufficient for the threshold voltage adjustment. Such a large dose would result in larger SCE and DIBL and the silicon thickness will probably need to be less than the maximum one considered here, i.e. 0.15 μm .

For 0.8 and 0.5 μm devices, the subthreshold slope is from 80 mV/dec for $t_{\text{Si}}=0.15 \mu\text{m}$ to 64 mV/dec for $t_{\text{Si}}=0.04 \mu\text{m}$. This is independent of the doping level. For the 0.25 μm device these values are 94 mV/dec and 70 mV/dec, respectively.

Figure 4.6 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.8 μm. p⁺ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.7 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.5 μm. p⁺ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.8 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.25 μm. p⁺ spike of 0.75 × 10¹² cm⁻².

For channel length 0.8 μm (Figure 4.6), we can see that even if we use very low doping, DIBL effect is not of a great concern. This is in contrast with bulk MOSFET where such low doping would result in severe DIBL and the device would be useless. Owing to the finite silicon film thickness this is not the case in the SOI device even with relatively high p⁺ spike dose in the channel.

As can be seen from Figure 4.7, this doping spike results in the 0.5 μm device which has acceptable behavior for all silicon film thickness and doping levels. The absolute values of the threshold voltage, SCE and DIBL are shown in Figures 4.9 to 4.11. We can see that the threshold voltage is fairly independent of silicon film thickness and the doping level. Threshold voltage sensitivity is about 5 mV/10 nm which is an excellent value. Also note that the threshold voltage *increases* (in absolute value) with the silicon film decrease. This means that increase in the source/body potential barrier due to the silicon film thin-

ning (see section 3.3.3), is larger than the threshold voltage reduction due to a reduced charge in the body.

From Figure 4.10 we see that DIBL is almost one half of the value we assume to be acceptable. Again, although we have very low doping finite silicon film thickness improves DIBL and makes the device usable.

Figure 4.9 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.5 \mu\text{m}$. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.10 Threshold voltage shift due to the drain-induced barrier lowering for SOI p-MOSFET. n^+ gate. Channel length $0.5 \mu\text{m}$. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.11 Threshold voltage shift due to the short-channel effect for SOI p-MOSFET. n^+ gate. Channel length $0.5 \mu\text{m}$. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.8 gives the design curve for 0.25 μm MOSFET. Although the threshold voltage is within acceptable limits for most of the silicon film thickness and doping levels, the design space is reduced due to the DIBL. We need to use relatively thin films to design a usable device. Threshold voltage sensitivity to silicon film thickness was found to be 19 mV/10 nm. It was also found that the threshold voltage is almost doping independent which alleviates the problem of the doping level control (worst case change is 0.06 volts for doping change from 10^{15} to 10^{16} cm^{-2}).

Figure 4.12 illustrates the reversal of the threshold voltage dependence on the silicon film thickness. For low doping we need to thin the film to control the SCE, and the threshold voltage increases with decreased film thickness as explained before. For a higher doping level, the doping is large enough to control the SCE. In this case, the threshold voltage is reduced as we thin the film because the charge under the gate is reduced.

Figure 4.12 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length 1 μm . p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

4.1.2 Results for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with n^+ Gate and Low Doping

The results for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET are now presented. As expected, the threshold voltage for the same parameters as for SOI p-MOSFET is reduced. The reduction is approximately 0.2 volts as given in Table 4.2, and is independent of the doping level. This value is basically equal to the bandgap reduction of the strained $\text{Si}_{1-x}\text{Ge}_x$, as pointed out in [22]. For 0.1 μm device, SCE are so pronounced that the silicon film thickness must be reduced in order for this reduction to be 0.2 volts.

Table 4.2 Threshold voltage shift due to the insertion of SiGe layer. SOI p-MOSFET without p^+ spike. Low doping.

Channel length (μm)	1	0.8	0.5	0.25	0.1
V_{TH} (V)	0.2	0.2	0.2	0.2	0.2 ⁽¹⁾

⁽¹⁾ Only for t_{Si} less than 0.1 μm .

Our results indicate that for the 0.1 μm device, the threshold voltage satisfies the design criteria when the film thickness is reduced below 0.1 μm . For thicker films, the SCE reduces the threshold voltage below 0.4 volts. In order to control the DIBL, the film thickness must be below 0.06 μm .

Since the $\text{Si}_{1-x}\text{Ge}_x$ channel already reduces the threshold voltage by 0.2 volts, the spike dose can be reduced in comparison with SOI p-MOSFET. This should improve the SCE and DIBL. The following spike doses were used: 0.25, 0.5 and $0.75 \times 10^{12} \text{ cm}^{-2}$. They are the same as for SOI p-MOSFET but in that case the lower two did not result in any acceptable designs. Table 4.3 summarizes the obtained results.

Table 4.3 Design options for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with different p^+ spike doses.

Channel length (μm)	p^+ spike		
	$0.25 \times 10^{12} \text{ cm}^{-2}$	$0.5 \times 10^{12} \text{ cm}^{-2}$	$0.75 \times 10^{12} \text{ cm}^{-2}$
1	–	✓ $\text{ND} \leq 3 \times 10^{15} \text{ cm}^{-3}$	✓
0.8	–	✓	✓
0.5	–	✓	✓
0.25	✓	✓	✓ $t_{\text{Si}} \leq 0.06 \mu\text{m}$
0.1	✓ $t_{\text{Si}} \leq 0.05 \mu\text{m}$	✓ $t_{\text{Si}} \leq 0.05 \mu\text{m}$	–

Note: ✓ means that there are some acceptable designs

From Table 4.3 and other results we can state the following:

1. $0.1 \mu\text{m}$ device can be designed with low p^+ spike dose and very thin film; subthreshold slope is about 80 mV/dec for $t_{\text{Si}} \leq 0.05 \mu\text{m}$; $\Delta V_{\text{TH}}/T_{\text{Si}} = 40 \text{ mV/10 nm}$
2. p^+ spike dose of $0.5 \times 10^{12} \text{ cm}^{-2}$ can be used to design the devices for all channel lengths
3. increasing the dose to $0.75 \times 10^{12} \text{ cm}^{-2}$ worsens the DIBL and SCE in short-channel devices and we need to thin the film to regain the control over DIBL and SCE
4. subthreshold slope is from 65 to 75 mV/dec for $L_{\text{CH}} \geq 0.25 \mu\text{m}$ for $t_{\text{Si}} = 0.04 \mu\text{m}$ and $t_{\text{Si}} = 0.15 \mu\text{m}$ respectively; it is slightly larger for larger p^+ spike

Large threshold voltage dependence on silicon film thickness for $0.1 \mu\text{m}$ device mentioned above in 1., is a consequence of the fact that subthreshold characteristic depends sharply on the film thickness as discussed in section 2.2.2. This is different from the often quoted dependence for highly-doped FD devices where the dependence is caused by the change of the charge under the gate. In all acceptable design cases, this dependence is less than 15 mV/10 nm . An example set of results for $0.25 \mu\text{m}$ device is given in Figures 4.13 to 4.16. From Figure 4.16 we see that we can control SCE and DIBL by either increasing doping (classical approach) or by thinning the silicon film.

Figure 4.13 Threshold voltage vs. silicon thickness for different doping levels for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.5 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.14 Threshold voltage shift due to the drain-induced barrier lowering for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.5 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.15 Threshold voltage shift due to the short-channel effect for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.5 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.16 Threshold voltage design curve for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.5 \times 10^{12} \text{ cm}^{-2}$.

4.1.3 Results for Si SOI p-MOSFET with n⁺ Gate and High Doping

As expected, the threshold voltage in this case is increased compared to the low-doping case and is even further from the acceptable values. Example curves for a 1 and 0.25 μm device are given in Figures 4.17 and 4.18. From the first one, we can see that increased doping increases the threshold voltage dependence on the silicon film thickness. This is a problem from a manufacturing point of view and was explained earlier. For a 0.25 μm device we see that threshold voltage increases for low doping, e.g. 10^{16} cm^{-3} , and decreases for large doping, e.g. 10^{17} cm^{-3} .

Figure 4.17 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n⁺ gate. Channel length 1 μm . No p⁺ spike.

Figure 4.18 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. No p^+ spike.

Since we are using larger doping, we increased the p^+ spike dose and the following values were used in simulations: 0.75 , 1.13 and $1.5 \times 10^{12} \text{ cm}^{-2}$. A design curve for $0.25 \mu\text{m}$ device is given in Figure 4.19. Comparing this curve with the one for low doping in Figure 4.8, we see that acceptable DIBL is extended to larger thickness, which is due to larger doping. Since the doping is larger and we used the same p^+ spike dose, the threshold voltage is acceptable only for lower doping, i.e. from 10^{16} to $3 \times 10^{16} \text{ cm}^{-3}$. Other results show that this low spike dose was not enough to reduce the threshold voltage of long-channel devices to acceptable values.

Figure 4.19 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.25 μm. p⁺ spike of 0.75 × 10¹² cm⁻².

Complete results are summarized in Table 4.4. For all of the designs, the threshold voltage was more sensitive to silicon film thickness than for the low doping case. For a channel length of 0.25 μm and a p⁺ spike dose of 0.75 × 10¹² cm⁻², this dependence was from 14 to 3 mV/10 nm for doping of 1 and 3 × 10¹⁶ cm⁻³ (Figure 4.20). Extremely low dependence in the second case is caused by compensation of two opposite effects. The first one is the V_{TH} decrease (in absolute value) due to the reduction of the silicon film thickness. The same silicon film thickness reduction results in increased source/body potential barrier, and thus V_{TH} increases in absolute value (this is the second effect). The same effect is present for higher spike dose as well, as illustrated in Figure 4.21.

Table 4.4 Design options for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with different p^+ spike doses.

Channel length (μm)	p^+ spike		
	$0.75 \times 10^{12} \text{ cm}^{-2}$	$1.13 \times 10^{12} \text{ cm}^{-2}$	$1.5 \times 10^{12} \text{ cm}^{-2}$
1	–	✓ $N_D \leq 6 \times 10^{16} \text{ cm}^{-3}$	✓
0.8	–	✓	✓
0.5	✓ $N_D < 3 \times 10^{15} \text{ cm}^{-3}$	✓	✓
0.25	✓ $t_{\text{Si}} \leq 0.06 \mu\text{m}$	✓ $t_{\text{Si}} \leq 0.06 \mu\text{m}$	–
0.1	–	–	–

Figure 4.20 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.21 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. n^+ gate. Channel length $0.5 \mu\text{m}$. p^+ spike of $1.13 \times 10^{12} \text{ cm}^{-2}$.

Figures 4.22 to 4.24 show combined design curves for all p^+ spike doses. Note that points designate designs with acceptable V_{TH} and DIBL. Thus, the points which satisfy only one design criteria are excluded. We see that for channel length larger than $0.5 \mu\text{m}$ there are many design options and the film thickness is not critical. For sub $0.5 \mu\text{m}$ devices, film thickness needs to be reduced in order to control SCE and DIBL. These graphs are similar to the ones for low doping. They show that improvement in SCE and DIBL due to the increased doping in body, is compensated by worsening due to the increased spike dose.

Subthreshold slope is above 70 mV/dec for $0.25 \mu\text{m}$ device and from 64 to 75 mV for longer channels, showing that the subthreshold slope sharpness is preserved for this high doping.

Figure 4.22 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.8 μm. All p⁺ spike doses included.

Figure 4.23 Threshold voltage design curve for SOI p-MOSFET. n⁺ gate. Channel length 0.5 μm. All p⁺ spike doses included.

Figure 4.24 Threshold voltage design curve for SOI p-MOSFET. n^+ gate. Channel length $0.25\ \mu\text{m}$. All p^+ spike doses included.

4.1.4 Results for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with n^+ Gate and High Doping

These results parallel the one for low doping. The p^+ spike doses that were simulated are 0.75 and $1 \times 10^{12}\ \text{cm}^{-3}$. Results are summarized in Tables 4.5 and 4.6. The subthreshold slope is between 64 and $80\ \text{mV/dec}$ for 0.04 and $0.15\ \mu\text{m}$ silicon film thickness.

Table 4.5 Threshold voltage shift due to the insertion of SiGe layer. SOI p-MOSFET without p^+ spike. High doping.

Channel length (μm)	1	0.8	0.5	0.25	0.1
V_{TH} (V)	0.2–0.25	0.2–0.25	0.2–0.25	0.2–0.25	0.2 ⁽¹⁾

⁽¹⁾ Only for t_{Si} less than $0.1\ \mu\text{m}$.

Table 4.6 Design options for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with different p^+ spike doses.

Channel length (μm)	p^+ spike	
	$0.75 \times 10^{12} \text{ cm}^{-2}$	$1 \times 10^{12} \text{ cm}^{-2}$
1	✓	✓
0.8	✓	✓
0.5	✓	✓
0.25	✓	✓ ND $\geq 6 \times 10^{16} \text{ cm}^{-3}$
0.1	–	–

Comparing the results for $0.25 \mu\text{m}$ device with and without $\text{Si}_{1-x}\text{Ge}_x$ channel, one can see that there are more design options for a $\text{Si}_{1-x}\text{Ge}_x$ device (see Figures 4.24 and 4.25). This is again due to the reduced p^+ spike dose needed for the threshold voltage adjustment.

Figure 4.25 Threshold voltage design curve for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$.

4.2 Comparison of p-MOSFETs for Channel Length of 0.25 μm

Now, we briefly compare two short-channel p-MOSFET designs. All parameters are the same except for the p^+ spike dose. This dose is smaller in $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET in order to obtain the same threshold voltage of -0.5 volts. Results for silicon film thickness of $0.1 \mu\text{m}$ are presented in Table 4.7. First, we see that the subthreshold slope is somewhat larger for p-MOSFET device owing to the larger p^+ spike, but it is very sharp for both devices. DIBL for p-MOSFET is on the edge of acceptable due to the larger p^+ spike. This can be improved by further thinning the silicon film thickness. Due to the very low doping, both devices show extremely small dependence of the threshold voltage on the silicon film thickness. Linear transconductance shows an improvement of 24 % but the saturation transconductance shows improvement of only 5 %. This is due to the velocity saturation effects. Nevertheless, the current drive is improved for all gate voltages as shown in Figure 4.26. Improvement is 58, 20 and 12 % for gate voltages of 1, 2 and 3 volts, respectively. We can see that as we increase the gate voltage, and thus reduce the number of holes in the $\text{Si}_{1-x}\text{Ge}_x$ channel, the improvement becomes smaller and smaller. Since this channel length will require small supply voltages of about 1.5 volts, we can see that the device will be operated in the regime where we obtain the maximum improvement.

Table 4.7 Characteristics of SOI p-MOSFET with and without $\text{Si}_{1-x}\text{Ge}_x$ channel. Channel length $0.25 \mu\text{m}$. n^+ gate. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-3}$ p-MOSFET and $0.5 \times 10^{12} \text{ cm}^{-3}$ for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET. $N_D = 3 \times 10^{15} \text{ cm}^{-3}$. $t_{\text{Si}} = 0.1 \mu\text{m}$.

DEVICE	S (mV/dec)	V_{TH} (V)	$\Delta V_{\text{TH(DIBL)}}$ (V)	$\Delta V_{\text{TH}}/\Delta t_{\text{Si}}$ (mV/10 nm)	g_{mL} ($\mu\text{S}/\mu\text{m}$)	g_{mS} ($\mu\text{S}/\mu\text{m}$)
Si pMOS	70.9	-0.48	-0.21	18	25	144
SiGe pMOS	64.6	-0.5	-0.07	12	31	152

Note: g_{mL} @ $V_{\text{DS}} = 0.1 \text{ V}$; g_{mS} @ $V_{\text{DS}} = 2 \text{ V}$.

Figure 4.26 Output curve for SOI p-MOSFET. Channel length $0.25 \mu\text{m}$. n^+ gate. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$ p-MOSFET and $0.5 \times 10^{12} \text{ cm}^{-2}$ for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET. $N_D = 3 \times 10^{15} \text{ cm}^{-2}$.

4.3 Buried Channel SOI p-MOSFET

As mentioned before, we need to implant p-type doping in order to adjust the threshold voltage of p-MOSFET. If this doping is not located below the Si/SiO₂ surface but at that interface we end up with buried channel p-MOSFET. Studies of such a device in the bulk case show that it is more prone to DIBL, due to the fact that current is flowing further away from the gate and thus the gate has less control [31].

From the previous results, we see that DIBL can be substantially reduced by reducing the silicon film thickness. Combining the two approaches we devised a buried channel SOI p-MOSFET shown in Figure 4.27.

Figure 4.27 Structure of buried channel SOI p-MOSFET. Dimensions in μm .

A uniform p-type doping of $2.5 \times 10^{17} \text{ cm}^{-3}$ was used for a depth of $0.03 \mu\text{m}$. This results in a dose of $0.75 \times 10^{12} \text{ cm}^{-2}$ which was used in previous designs. Complete results for $0.25 \mu\text{m}$ device are given in Figures 4.29 to 4.31 and Table 4.8. From Figure 4.30 we see that thinning the film does reduce the DIBL and the upper limit on the thickness is about $0.1 \mu\text{m}$ which is larger than in the case when we used p^+ spike. Table 4.8 shows that buried channel device has a larger subthreshold slope. This can be improved by thinning the silicon film thickness, and for a thickness of $0.04 \mu\text{m}$ it becomes 68 mV/dec . The threshold voltage dependence of the film thickness is still very low. Transconductance is reduced compared to the one for a device with p^+ spike. This effect needs further investigation.

It is known that removing the carriers from the Si/SiO_2 surface improves mobility by reducing the surface scattering. This is the idea behind the buried channel device. The mobility model that we are using is dependent on the vertical field and the *location* of the

carriers is not important. Its advantage is that it is grid independent but it does not properly model this situation. Thus, we do not see any improvement in transconductance although carriers are separated from the surface (Figure 4.28). From the same figure, we see that for high gate voltage the device reverts to normal, surface channel p-MOSFET. When this happens there is no improvement compared to SOI p-MOSFET. Since the current is now flowing in the p^+ doped region, carrier mobility is reduced due to increased doping. This partially compensates the mobility improvement due to the carrier removal from the Si/SiO₂ surface. In order to model this device properly one needs to use a position-dependent mobility model and calibrate the improvement due to the buried channel in the bulk case. Then this set of models can be used to model SOI buried channel p-MOSFET. This is a topic for future research.

Table 4.8 Characteristics of SOI p-MOSFET and buried channel SOI p-MOSFET. Channel length 0.25 μm . n^+ gate. p^+ spike of $0.75 \times 10^{12} \text{ cm}^{-2}$ p-MOSFET. p^+ doping of $0.75 \times 10^{12} \text{ cm}^{-2}$ for buried channel p-MOSFET. $N_D = 3 \times 10^{15} \text{ cm}^{-3}$. $t_{\text{Si}} = 0.1 \mu\text{m}$.

DEVICE	S (mV/dec)	V_{TH} (V)	$\Delta V_{\text{TH(DIBL)}}$ (V)	$\Delta V_{\text{TH}}/\Delta t_{\text{Si}}$ (mV/10 nm)	g_{mL} ($\mu\text{S}/\mu\text{m}$)	g_{mS} ($\mu\text{S}/\mu\text{m}$)
pMOS with p^+ spike	70.9	-0.48	-0.21	18	25	144
buried channel pMOS	90	-0.59	-0.18	14	20	104

Figure 4.28 Hole concentration for buried channel SOI p-MOSFET. n⁺ gate. Channel length 0.25 μm . p⁺ dose of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.29 Threshold voltage vs. silicon thickness for different doping levels for buried channel SOI p-MOSFET. n⁺ gate. Channel length 0.25 μm . p⁺ dose of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.30 Threshold voltage shift due to the drain-induced barrier lowering for buried channel SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ dose of $0.75 \times 10^{12} \text{ cm}^{-2}$.

Figure 4.31 Threshold voltage design curve for buried channel SOI p-MOSFET. n^+ gate. Channel length $0.25 \mu\text{m}$. p^+ dose of $0.75 \times 10^{12} \text{ cm}^{-2}$.

CHAPTER 5

Simulation of SOI Si and Si_{1-x}Ge_x p-MOSFET with p⁺ GATE

5.1 Results for SOI p-MOSFET

First, we will do some calculations of the threshold voltage using the equations for long-channel devices. Note that the work function of p⁺ gate is 1.08 volts larger than the one for n⁺ gate (5.25 versus 4.17 volts). From the equations in section 4.1, we can see that this increase in the work function will decrease the threshold voltage of the p-MOSFET which is negative. Thus, we need to use large doping in order to adjust the threshold voltage. Calculations were done for a doping range from 10¹⁷ to 10¹⁸ cm⁻³ and are summarized in Table 5.1. The equations that were used were the ones for bulk MOSFET which also apply to PD device:

Calculation of the Threshold Voltage for *bulk* n-MOSFET and p-MOSFET

$$\text{Doping potential : } \begin{cases} N_A \gg N_D \Rightarrow \phi_{dop} = -\frac{kT}{q} \ln \frac{N_A}{n_i} & n - MOSFET \\ N_D \gg N_A \Rightarrow \phi_{dop} = +\frac{kT}{q} \ln \frac{N_D}{n_i} & p - MOSFET \end{cases}$$

$$\text{Maximum Depletion Layer Width : } x_{d,max} = \sqrt{\frac{4 \epsilon_{Si} |\phi_{dop}|}{q N_A}}$$

$$\text{Work Function Difference : } \phi_{MS} = \phi_M - \left(\chi_{Si} + \frac{E_G}{2q} - \phi_{dop} \right)$$

$$\begin{aligned} \text{Maximum Depletion Layer Charge : } \begin{cases} N_A \gg N_D \Rightarrow Q_{d,max} = -q N_A x_{d,max} & n - \text{MOSFET} \\ N_D \gg N_A \Rightarrow Q_{d,max} = +q N_D x_{d,max} & p - \text{MOSFET} \end{cases} \end{aligned}$$

$$\text{Oxide Capacitance per Unit Area : } C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$V_{TH} = \frac{-Q_{d,max} - Q_{SS}}{C_{ox}} + \phi_{MS} - 2 \phi_{dop}$$

Comparing the silicon film thickness of 0.15 μm for which calculations were done with maximum depletion layer width, we see that the device is partially depleted (see Table 4.1). From this table, we see that the threshold voltage can be easily adjusted by changing the doping level in the channel. The same statement is valid for n-MOSFET with n^+ gate. Therefore, this is the reason that modern CMOS technologies are using dual gate materials, i.e. p^+ gate for p-MOSFET and n^+ gate for n-MOSFET [5], [13], [26].

Table 5.1 Long channel threshold voltage for SOI p-MOSFET with p^+ gate.

$N_{DOP} (\text{cm}^{-3})$	$1 \cdot 10^{17}$	$3 \cdot 10^{17}$	$6 \cdot 10^{17}$	$1 \cdot 10^{18}$
$V_{TH} (\text{V})$	-0.23	-0.52	-0.81	-1.09

The fact that we need to use higher doping leads to the following:

1. devices will exhibit lower SCE and DIBL
2. higher dependence of V_{TH} on the silicon film thickness for FD devices
3. higher subthreshold slope due to higher doping

The threshold voltage for a long-channel device obtained from MEDICI is given in Figure 5.1. We see that the calculated and simulated V_{TH} differ by approximately 0.1 volt. This is a direct consequence of different definitions for the threshold voltage. From Figure 5.2 we see that this threshold voltage is reduced by 0.2 volts for short-channel devices.

It has been mentioned that using fully-depleted devices puts stringent requirements on the uniformity of the silicon film. The reason for that is the threshold voltage dependence on the silicon film thickness. We saw that by using very low doping and n^+ gate we can reduce this dependence to a very acceptable level. Another option is to design the device to be nearly fully depleted. This way, we can still preserve the advantages of the PD devices and relax the requirements on the uniformity of the silicon film thickness. This can be best seen from Figures 5.1 and 5.2 for the doping level of 10^{17} cm^{-3} . When the device is not fully depleted, ($t_{\text{Si}} > 0.1 \text{ } \mu\text{m}$) the threshold voltage does not depend on the silicon thickness, as expected for the PD device. When the device is fully depleted ($t_{\text{Si}} < 0.1 \text{ } \mu\text{m}$), the threshold voltage depends on the silicon film thickness and changes approximately 50 mV/10 nm for $1 \text{ } \mu\text{m}$ device and 18 mV/10 nm for $0.25 \text{ } \mu\text{m}$ device. A reduction in the dependence for the short-channel device comes from the compensation between the V_{TH} *reduction* and *increase*. V_{TH} *reduction* is caused by a reduction of silicon film thickness and thus the reduction of the charge in the body. V_{TH} *increase* comes from the increase in the source/body potential barrier due to the reduction in silicon film thickness.

Figure 5.1 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. p^+ gate. Channel length $1 \mu\text{m}$. Line is the boundary between the FD and PD devices.

Figure 5.2 Threshold voltage vs. silicon thickness for different doping levels for SOI p-MOSFET. p^+ gate. Channel length $0.25 \mu\text{m}$. Line is the boundary between the FD and PD devices.

Design curves for all devices are summarized in Table 5.2. We see that the doping of about $3 \times 10^{17} \text{ cm}^{-3}$ gives an acceptable threshold voltage and DIBL for all channel lengths except for $0.1 \mu\text{m}$ device. We see that even in the case of very high doping, we cannot design a device that would be this short. The design of such short devices is currently a field in which much research is being done and many new and innovative structures are being developed (see for example [12], [38], [25], [48] and [49]).

Table 5.2 Design options for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET with different doping levels.

Channel length (μm)	Doping (cm^{-3})			
	10^{17}	3×10^{17}	6×10^{17}	10^{18}
1	–	✓	–	–
0.8	–	✓	–	–
0.5	–	✓	–	–
0.25	–	✓	✓	–
0.1	–	–	–	–

5.2 Results for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET

First, we look at the threshold voltage reduction due to the insertion of $\text{Si}_{1-x}\text{Ge}_x$ channel, Table 5.3. We see that this reduction depends on the doping level, unlike the n^+ gate case. It also increases in absolute value with increased doping and is independent of the channel length for longer devices. Looking at Figure 5.3, one can see that the threshold voltage for $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET is much less dependent on doping level than the one for p-MOSFET (Figure 5.1).

Table 5.3 Threshold voltage shift due to the insertion of SiGe layer. SOI p-MOSFET. p⁺ gate.

Channel length (μm)	Doping (cm^{-3})			
	1×10^{17}	3×10^{17}	6×10^{17}	1×10^{18}
1	-0.25	-0.37	-0.51	-0.70
0.8	-0.25	-0.35	-0.50	-0.70
0.5	-0.29	-0.40	-0.55	-0.72
0.25	-0.16	-0.31	-0.45	-0.63
0.1	—	-0.16	-0.32	-0.51

Figure 5.3 Threshold voltage vs. silicon thickness for different doping levels for $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. p⁺ gate. Channel length 1 μm .

In order to clarify why this reduction is so large, an additional set of simulations was done. We simulated SOI p-MOSFET without $\text{Si}_{1-x}\text{Ge}_x$ channel, but *with* low doping of 10^{15} cm^{-3} for the first 0.03 μm (we call it step doped p-MOSFET). This is basically $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFET with removed $\text{Si}_{1-x}\text{Ge}_x$ channel. Results for the threshold voltage are given in Table 5.4. We see that due to the reduced doping, the step doped p-MOSFET has a much lower threshold voltage. Adding $\text{Si}_{1-x}\text{Ge}_x$ channel reduces this threshold volt-

age even further. Unfortunately, the threshold voltage is now much less sensitive to the doping in body since the surface which is lowly doped plays a major role in current flow. This shows that for p^+ gate we need to go to doping levels even higher than 10^{18} cm^{-3} . This increases parasitic capacitance tremendously and slows down the device.

Table 5.4 Threshold voltage for Si p-MOSFET and step doped Si p-MOSFET. Channel length $1 \mu\text{m}$. p^+ gate.

$N_D (\text{cm}^{-3})$	1×10^{17}	3×10^{17}	6×10^{17}	1×10^{18}
Step doped Si p-MOSFET	-0.22	-0.4	-0.45	-0.52
Si p-MOSFET	-0.33	-0.64	-0.91	-1.2

Figure 5.4 Hole concentration vs. vertical position for step doped p-MOSFET. Cross section in the middle of the channel. $V_{DS}=0.1 \text{ V}$. $V_{GS}=0 \text{ V}$. p^+ gate.

Figure 5.4 shows the hole distribution in step doped Si p-MOSFET for zero gate voltage. We clearly see hole accumulation at the surface which is for low doping very close to the doping level of 10^{15} cm^{-3} . This implies that the transistor is almost at the threshold point although we did not apply any gate voltage. Since we have p^+ gate and n body, in equilibrium, holes are piling up in the lowly doped part of the body to satisfy

the requirement of constant Fermi level (Figure 5.5). The holes needed in the channel are either thermally generated in MOS capacitor structure or are supplied by the source and drain. Therefore, we have a tendency towards an inversion at the surface even with no gate voltage applied.

Figure 5.5 Band diagram for step doped p-MOSFET.

Comparing the characteristics for FD (Table 5.5) and PD (Table 5.6) p⁺ gate design we conclude that:

1. threshold voltage is very low in both cases → we need even larger doping for acceptable V_{TH}
2. subthreshold slope is very high for PD device and improves significantly for FD device
3. FD device exhibits large V_{TH} dependence on t_{Si} due to high doping
4. linear and saturation transconductance improves in FD device compared to the one for PD device

Table 5.5 Characteristics of PD $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. Channel length 0.25 μm . p^+ gate.
 $N_D=1 \times 10^{18} \text{ cm}^{-3}$. $t_{\text{Si}}=0.1 \mu\text{m}$.

DEVICE	S (mV/dec)	V_{TH} (V)	$\Delta V_{\text{TH(DIBL)}}$ (V)	$\Delta V_{\text{TH}}/\Delta t_{\text{Si}}$ (mV/10 nm)	g_{mL} ($\mu\text{S}/\mu\text{m}$)	g_{mS} ($\mu\text{S}/\mu\text{m}$)
SiGe pMOS	110	-0.34	-0.01	0	13.8	119

Table 5.6 Characteristics of FD $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET. Channel length 0.25 μm . p^+ gate.
 $N_D=1 \times 10^{18} \text{ cm}^{-3}$. $t_{\text{Si}}=0.04 \mu\text{m}$.

DEVICE	S (mV/dec)	V_{TH} (V)	$\Delta V_{\text{TH(DIBL)}}$ (V)	$\Delta V_{\text{TH}}/\Delta t_{\text{Si}}$ (mV/10 nm)	g_{mL} ($\mu\text{S}/\mu\text{m}$)	g_{mS} ($\mu\text{S}/\mu\text{m}$)
SiGe pMOS	80	-0.28	-0.04	60	21	139

From the presented data, we can see that p^+ gate design is applicable only to PD or bulk devices since FD devices exhibit an unacceptably large V_{TH} dependence on the silicon film thickness. DIBL and SCE are not of concern in this design since the doping used is large enough to suppress those effects. Transconductance and subthreshold slopes are worse in PD than in FD device. High doping causes a concern because of large parasitic capacitance between the source/drain and body. One way to reduce this capacitance is to use non-uniform doping (pulse shaped doping) with n^+ spike located underneath the channel to increase V_{TH} , and using lower doping below n^+ spike [22].

CHAPTER 6

CONCLUSIONS

Two-dimensional numerical simulation was used to study the scaling properties of SOI p-MOSFETs. Using the device simulator MEDICI we developed an automated grid setup and simulated a large variety of device structures. Based on the design criteria for the threshold voltage and DIBL, a set of design curves for different design options was developed. Data on subthreshold slope, SCE and threshold voltage sensitivity have also been calculated. This way we can make appropriate initial design decisions, taking into account a set of design criteria.

A complete list of simulated variables is:

1. n^+ and p^+ gate
2. silicon film thickness: 0.15, 0.1, 0.06, 0.05 and 0.04 μm
3. channel length: 1, 0.8, 0.5, 0.25, 0.1 μm
4. p^+ spike dose: 0.25×10^{12} to $1.5 \times 10^{12} \text{ cm}^{-2}$ as needed for V_{TH} adjustment

Results show that short channel effects can be controlled by increasing the body doping level or by reducing the silicon film thickness. The first approach is more effective for p^+ gate design which requires high body doping for threshold voltage control, while the second approach is much more effective for n^+ gate design with low body doping.

6.1 n+ Gate SOI p-MOSFET Design

Si p-MOSFET with n^+ gate exhibits large threshold voltage even for the lowest doping. A p-type doping spike is needed to adjust it. Using the minimal body doping minimizes the required dose for the spike and requires the thinning of the silicon film in order to reduce the DIBL and SCE. This spike can be located at the Si/SiO₂ interface (buried channel device) or some depth under the interface.

Buried channel device was studied only briefly and it was shown that its poor short channel behavior can be controlled by thinning the silicon film thickness. This extra degree of freedom not present in bulk devices extends the applicability of buried channel SOI MOSFET into the sub-micron region. Further modeling with improved mobility models is needed to assess the merits of this design. The same principle can be used to design the buried channel n-MOSFET with n^+ gate.

The Si p-MOSFET with p^+ spike doping can easily be designed down to channel lengths around 0.5 μm . Designing the 0.25 μm device requires the thinning of the silicon film in order to control the SCE & DIBL.

For the Si_{1-x}Ge_x device the Si_{1-x}Ge_x channel already reduces the threshold voltage for 0.2 volts and the spike dose can be reduced in comparison with SOI p-MOSFET. This improves the SCE and DIBL and offers more design options.

Due to the fact that the doping is very low and that the devices are fully depleted they exhibit low dependence of the threshold voltage on the silicon film thickness and sharp subthreshold slope. Low doping also results in high carrier mobility and substantially reduces the parasitic capacitances.

6.2 p^+ Gate SOI p-MOSFET Design

For this design the threshold voltage of Si p-MOSFET can easily be adjusted by changing the doping level in the channel. The same statement is valid for n-MOSFET with n^+ gate. Since the doping level is fairly large, the Si SOI p-MOSFET exhibits very good short channel behavior and large threshold voltage dependence on the silicon film thickness for FD design. For short channel device this dependence is compensated by SCE and is about 18 mV/10 nm.

$Si_{1-x}Ge_x$ SOI p-MOSFET exhibits large threshold voltage reduction compared to SOI p-MOSFET. This gives very low threshold voltage for short channel devices and requires doping levels above 10^{18} cm^{-3} . Such devices exhibit large subthreshold slope and reduced transconductance. Also, high doping causes a concern because of large parasitic capacitance between the source/drain and body.

6.3 Main Results

The best way to control SCE & DIBL in n^+ gate design is through reduction of silicon film thickness. We need to keep the body doping low in order to minimize the p^+ spike dose that is used for V_{TH} adjustment. These requirements result in FD device. The design of both Si p-MOSFET and $Si_{1-x}Ge_x$ p-MOSFET requires the p^+ spike for the threshold voltage adjustment. In $Si_{1-x}Ge_x$ p-MOSFET the required p^+ spike dose is reduced since the channel itself reduces V_{TH} by 0.2 volts.

The p^+ gate design is more suited for the PD or near-fully depleted device design since we need to use high doping for the threshold voltage adjustment and this results in large threshold voltage sensitivity to silicon film thickness for FD devices. For short-channel devices this sensitivity is partially compensated by SCE and results in acceptable values. The design of SOI p-MOSFET is done by properly adjusting the body doping.

For the $\text{Si}_{1-x}\text{Ge}_x$ SOI p-MOSFET large reduction in V_{TH} requires large body doping. This increases the parasitic capacitances and slows down the device.

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APPENDIX A

A.1 Variable Definition (step 1)

In this step we are defining the variables that will be used in the simulation (see Figure A.2). Channel length is in this example defined as 1 μm . We have chosen to create a separate file for each channel length instead of creating a loop in the input deck which would sweep the value of the channel length. The reason for that is connected with possible numerical problems. If any of the bias points for which MEDICI is solving the system fails to converge it terminates execution. The same happens if the file path is specified incorrectly or if any other error occurs. Simulations are very time consuming, and they are run in the background without direct supervision. This would lead to a large loss of time if anything goes wrong. To avoid this, separate input decks are specified for each channel length. They are located in separate directories. Now a simple shell file can be used to run one input deck after another (Figure A.1). If an error occurs in any of the input files and MEDICI terminates, the shell file will automatically run the next input file (i.e. input deck for the next channel length).

```

#!/bin/csh

cd /u/persun/medici/soi/pMOS.sige/scaling/run/nl_gate/p_2/L_1
sleep 30
medici tr_0.1.med > /dev/null
sleep 30

cd /u/persun/medici/soi/pMOS.sige/scaling/run/nl_gate/p_2/L_0.8
sleep 30
medici tr_0.1.med > /dev/null
sleep 30
....

```

Figure A.1 Shell file for running multiple MEDICI simulations.

```

1... TITLE  SIMULATION FOR SiGe p-CHANNEL MOSFET SCALING

2...$*****

3... $ VARIABLE DEFINITION
4... $ LCH=CHANNEL LENGTH
5... ASSIGN NAME=LCH N.VALUE=1
6... $ XDOP=CHARACTERISTIC LENGTH IN X DIRECTION
7... ASSIGN NAME=XDOP N.VALUE=0.035*SQRT(-LOG(1E15/6.4E19))
8... $ DOPING SPIKE
9... ASSIGN NAME=NSPIKE N.VALUE=1E18

```

Figure A.2 MEDICI input deck for variable definition.

As we will see later source/drain doping is specified to be uniform for the extent of $0.4\ \mu\text{m}$ in horizontal direction (see Figure 3.1) and then it falls off following the Gaussian distribution (Equation (A.1)). Si cap, $\text{Si}_{1-x}\text{Ge}_x$ channel and silicon buffer doping is specified to be uniform $10^{15}\ \text{cm}^{-3}$. In order to find the distance for which source/drain doping $N(x)$ penetrates into the channel region we have to equate $N(x)$ to this doping level. This calculation is done in line 7 and the variable is named XDOP. Variable NSPIKE defines the concentration of the p^+ spike. This variable is not used for p^+ gate simulation where the threshold voltage adjustment is done through adjustment of the doping level. It is spe-

cified in cm^{-3} and the total dose can be found by taking into account the mesh spacing at the position where the spike is located. This will be detailed further in the section about the doping profile specification (step 7).

$$N(x) = N.PEAK \exp \left[- \left(\frac{x - X.MAX}{X.CHAR} \right)^2 \right] \quad (A.1)$$

$N.PEAK$ = peak impurity concentration.

$X.MAX$ = maximum x location of impurity profile.

$X.CHAR$ = horizontal characteristic length.

Note that if we were to change the doping *in* the silicon cap, line 7 could not be put before the doping level is specified. In this case XDOP would not be constant and would change for each new doping level. This was done in the case of SOI p-MOSFETs without $\text{Si}_{1-x}\text{Ge}_x$ channel where doping is uniform throughout the device. In this case Equation (A.1) has to be equated with this doping level in order to calculate XDOP.

A.2 Main Loop Definition (step 2)

```

10...$*****
11... $ MAIN LOOP DEFINITION
12... $ TSI=THICKNESS OF THE SILICON
13... $ NDOP=DOPING LEVEL
14... LOOP STEPS=4
15... ASSIGN NAME=NDOP N.VALUE=(1e15,3e15,6e15,1e16)
16... ASSIGN NAME=CHRNDO C1=1e15 C2=3e15 C3=6e15 C4=1e16
17... LOOP STEPS=5
18... ASSIGN NAME=TSI N.VALUE=(0.15,0.1,0.06,0.05,0.04)
19... ASSIGN NAME=CHRTSI C1=t_15 C2=t_10 C3=t_6 C4=t_5 C5=t_4
20... +   C6=t_3 C7=t_2

```

Figure A.3 MEDICI input deck for main loop definition.

This portion of the input deck determines the values of the doping and silicon film thickness for which the device is going to be simulated (Figure A.3). The thickness of the silicon film TSI is looped from 0.15 to 0.04 μm . The range of doping level NDOP depends on the choice of the gate material and this example is for n^+ gate. Character variables CHRNDOP and CHRTSI are used for naming the output files.

A.3 X and Y Mesh Definition (step 3)

X mesh definition is given in Figure A.4 and is done as follows:

1. lines 24&30 and 25&29 specify the regions of silicided S/D contact and uniform S/D doping
2. lines 26&28 specify the characteristic length in x direction as calculated in line 7
3. line 27 specifies the channel region

```

21...$*****
22... $ X AND Y MESH DEFINITION
23... MESH SMOOTH=1
24... X.MESH WIDTH=0.25 H1=0.08 H2=0.02
25... X.MESH WIDTH=0.15 H1=0.05 H2=0.04
26... X.MESH WIDTH=@XDOP H1=0.03 H2=0.01
27... X.MESH WIDTH=@LCH H1=@LCH/60 H2=@LCH/60 H3=@LCH/8
28... X.MESH WIDTH=@XDOP H1=0.01 H2=0.03
29... X.MESH WIDTH=0.15 H1=0.04 H2=0.05
30... X.MESH WIDTH=0.25 H1=0.02 H2=0.08

```

Figure A.4 MEDICI input deck X mesh definition.

Y mesh definition is given in Figure A.5 and is done as follows:

1. lines 31&32 specify the mesh where silicon–dioxide is going to be located
2. line 34 specifies the region of Si cap, $\text{Si}_{1-x}\text{Ge}_x$ channel and Si buffer
3. if the silicon film thickness is larger than $0.04\text{ }\mu\text{m}$ lines 36 to 38 define the mesh for this region
4. line 43 defines the buried oxide region
5. line 44 creates the mesh for the rest of the device

```

31... Y.MESH  N=1  L=-0.007
32... Y.MESH  N=4  L=0.
33... $ SILICON SURFACE
34... Y.MESH  DEPTH=0.04  H1=0.0025
35... $ FILL THE REST OF SILICON
36... IF COND=(@TSI-0.04)
37... Y.MESH  DEPTH=@TSI-0.04  H1=0.0025  H2=0.005
38... IF.END
39... $ FILL THE OXIDE
40... $ H1=0.031 SO THAT THERE IS NO PONT @ Y=0.05
41... $ OTHERWISE ELECTRODE IS EXTENDED TO THAT POINT
42... $ EVEN IF TSI<0.05
43... Y.MESH  DEPTH=0.40  H1=0.031  H2=0.1
44... Y.MESH  DEPTH=2-0.4-@TSI  H1=0.15  H2=0.4

```

Figure A.5 MEDICI input deck Y mesh definition.

Note that the mesh spacing is much smaller for the first $0.04\text{ }\mu\text{m}$ than for the rest of the device. This is done because the majority of the current is going to flow in this region and because a vertical electric field is going to experience a large change in this region. This spacing is set up to be fine by hand, since we will not use any regrid as explained earlier.

A.4 Node Elimination (step 4)

Node elimination can be used to eliminate unwanted points generated initially or by regrid procedure. This is not always necessary, but it reduces the number of points and therefore reduces the time needed for simulation. In order to preserve the fine mesh in the body this elimination is done only for buried oxide and the substrate.

```

45...$*****
46... $  ELIMINATE SOME UNNECESSARY NODES
47... $  IN THE BURRIED OXIDE AND SUBSTRATE
48... ELIMIN  COLUMNS  Y.MIN=@TSI+0.1

```

Figure A.6 MEDICI input deck for node elimination.

A.5 Region Specification (step 5)

The region statement defines the location of materials in the device mesh (Figure A.7). This statement is used by MEDICI to assign appropriate values of the physical models for different materials to specified regions. Note that line 54 will not be in the input deck which is used for the definition of SOI p-MOSFET without $\text{Si}_{1-x}\text{Ge}_x$ channel.

```

49...$*****
50... $ REGION SPECIFICATION
51... REGION  NUM=1  SILICON
52... REGION  NUM=2  OXIDE  Y.MIN=-0.007  Y.MAX=0.
53... REGION NUM=3  OXIDE Y.MIN=@TSI Y.MAX=@TSI+0.4
54... REGION  NUM=4  SIGE  Y.MIN=0.01  Y.MAX=0.02 X.MOLE=0.3

```

Figure A.7 MEDICI input deck for region specification.

A.6 Electrode Definition (step 6)

The electrode statement defines the position of electrodes in the device structure. If the electrode is touching the silicon region it creates an ohmic contact. The electrode definition used in the input deck is given in Figure A.8.

```

55...$*****
56... $ ELECTRODE DEFINITION
57... $ ELECTRODES: #1=DRAIN, #2=GATE, #3=SOURCE, #4=SUBSTRATE
58... ELECTR  NUM=1 X.MIN=2*@XDOP+@LCH+0.55 Y.MAX=0.050 VOID
59... ELECTR  NUM=2 X.MIN=0.35 X.MAX=@LCH+2*@XDOP+0.45 TOP
60... ELECTR  NUM=3 X.MAX=0.25 Y.MAX=0.050 VOID
61... ELECTR  NUM=4 BOTTOM

```

Figure A.8 MEDICI input deck for electrode definition.

A.7 Doping Profile (step 7)

In line 65 the uniform doping of 10^{15} cm^{-3} is specified for the first 30 nm. This is the region of the Si cap, $\text{Si}_{1-x}\text{Ge}_x$ channel and Si buffer. This doping is not specified for uniformly doped SOI p-MOSFET. Then the body doping is specified in line 67. In the case of uniformly doped SOI p-MOSFET this doping is extended all the way to the front Si/SiO₂ interface (i.e. Y.MIN is set to be zero). Line 68 defines the doping for the substrate, and lines 69 to 72 define the source and the drain region, respectively. p⁺ doping spike is defined in line 74. This line only defines the peak concentration in cm^{-3} . Characteristic lengths are set up to be so small that this doping drops effectively to zero before it reaches the next grid point. Note that vertical grid spacing in this region is $0.0025 \mu\text{m}$ as given in the line 34 on Figure A.5. For calculation purposes, MEDICI assumes that the doping level extends as a uniform one from the node for which it is specified to the half-way distance between the two adjacent nodes (Figure A.10).

Knowing this, using the data from lines 9 and 37 one can calculate the p^+ spike dose:

$$DOSE = NSPIKE \frac{1}{2}(X_3 - X_1) = 10^{18} \frac{1}{2} 2 \cdot 0.0025 \cdot 10^{-4} = 0.25 \cdot 10^{12} \text{ cm}^{-2} \quad (\text{A.2})$$

$$d_{12} = d_{23} = 0.0025 \text{ } \mu\text{m}$$

```

62...$*****
63... $ DOPING PROFILES
64... $ 1E15 DOPING IN CAP, SiGe AND BUFFER
65... PROFILE N-TYPE N.PEAK=1E15 UNIFORM Y.MIN=0.0 Y.MAX=0.03
66... + OUT.FILE=pmos.sige.dop
67... PROFILE N-TYPE N.PEAK=@NDOP UNIFORM Y.MIN=0.03 Y.MAX=@TSI
68... PROFILE N-TYPE N.PEAK=1E15 UNIFORM Y.MIN=@TSI+0.4
69... PROFILE P-TYPE N.PEAK=6.4E19 X.MIN=0.0 WIDTH=.40
70... + Y.CHAR=0.035 XY.RAT=1.0 Y.MIN=0.005 Y.MAX=@TSI-0.005
71... PROFILE P-TYPE N.PEAK=6.4E19 X.MIN=@LCH+2*@XDOP+0.4 WIDTH=.40
72... + Y.CHAR=0.035 XY.RAT=1.0 Y.MIN=0.005 Y.MAX=@TSI-0.005
73... $ p+ SPIKE
74... PROFILE P-TYPE N.PEAK=@NSPIKE Y.MIN=0.03 Y.CHAR=1E-5 Y.MAX=0.03

```

Figure A.9 MEDICI input deck for region specification.

Figure A.10 Device mesh detail with doping profile.

Note that this calculation can be used since the mesh in the region where the spike is located is rectangular (no regrid or node elimination was used). If the mesh was non-rectangular, the dose would change with position because the mesh spacing would also change with position. This would be an incorrect way to specify p^+ doping spike.

A.8 Interface Specification (step 8)

At the silicon/silicon-dioxide interface we have an abrupt change in the crystalline structure. This results in a fixed *positive* charge in the silicon-dioxide which is very close to the interface [50]. This charge is modeled as a fixed, positive charge sheet layer at the Si/SiO₂ interface. This sheet charge was taken to be 10^{11} cm^{-2} for the front gate Si/SiO₂ interface and three times this value for silicon buried oxide interface (Figure A.11, lines 77 and 78, respectively). The reason that this charge is assumed to be larger for buried oxide comes from the different procedure used to create this interface. Front gate oxide is thermally grown on silicon and the quality of this interface can be assumed to be very good. Buried oxide is created by oxygen implantation and annealing, and the quality of this interface is always worse.

```

75...$*****
76... $ INTERFACE SPECIFICATION
77... INTERFACE REGION=(1,2) QF=1E11
78... INTERFACE REGION=(1,3) QF=3E11 ^CLEAR

```

Figure A.11 MEDICI input deck for interface specification.

A.9 Contact Properties (step 9)

For the calculation of the threshold voltage, the gate material work function has to be specified. This is done in line 81 of Figure A.12. In this example, gate is n^+ polysilicon

which results in the work function of 4.17 V [32]. Another option that we are going to use is p^+ polysilicon gate with work function of 5.25 V.

```
79...$*****
80... $ SPECIFY CONTACT PROPERTIES
81... CONTACT NUM=2 N.POLYSI PRINT
```

Figure A.12 MEDICI input deck for specification of contact properties.

A.10 Model Specification (step 10)

In the basic three equations that MEDICI solves, certain physical parameters like mobility and recombination appear. There are different models for these physical quantities available in MEDICI and one needs to select the ones which are necessary to correctly describe the device. One also needs to be careful when interpreting the results since the selection of these models directly determines the set phenomena that can be analyzed. Also, one has to keep the limitations of any model in mind in order to interpret the results correctly.

Since we want to study the scaling properties of SOI $\text{Si}_{1-x}\text{Ge}_x$ p-MOSFETs we specified the following models (Figure A.13, line 84):

1. CONMOB – models the mobility dependence on the doping level
2. PRPMOB – models the mobility reduction in the MOSFET device due to the surface scattering
3. FLDMOD – models carrier velocity dependence on the horizontal electric field (i.e. includes velocity saturation effects, Figure 2.5)
4. CONSRH – models SRH recombination with concentration-dependent lifetimes
5. AUGER – models Auger recombination
6. BGN – models band-gap narrowing in the heavily doped regions

```

82...$*****
83... $  MODEL SPECIFICATION
84... MODELS  CONMOB  PRPMOB  FLDMOB  CONSRH  AUGER  BGN  PRINT
85... MOBILITY  ECP.MU=1E10  PRINT  SIGE  PR.TABLE

```

Figure A.13 MEDICI input deck for model specification.

Note that models CONSRH and AUGER (lines 4. and 5.) are needed only if we are doing a two-carrier solution. If we want to simulate the breakdown of the device we need to specify a two-carrier solution and to include the impact ionization model too.

A.11 Symbolic Factorization (step 11) and Solving the System (step 12)

In order to solve the system MEDICI needs an initial guess. The first one is obtained from the charge neutrality assumption (equilibrium solution). This is the starting point for any simulation. After we have a solution for one or two bias points, MEDICI automatically uses them for an initial guess. In a case when we have two previous solutions available, a projection is used to speed up the convergence.

In the symbolic factorization step the Poisson's and the continuity equations are discretized on a simulation grid (Figure A.14). As explained in [32] for equilibrium solution (zero bias) a Poisson solution is sufficient. Thus in line 88 we specify no carriers, i.e. continuity equations are not going to be discretized and included in the system to be solved. Line 89 specifies the numerical methods and parameters to be used. More details can be found in [32].

```

86...$*****
87... $  SYMBOLIC FACTORIZATION
88... SYMB  CARRIERS=0
89... METHOD  ICCG  DAMPED

```

Figure A.14 MEDICI input deck for symbolic factorization. Equilibrium solution.

```

90...$*****
91... $ SOLVING THE SYSTEM FOR EQUILIBRIUM
92... SOLVE   V1=0 V2=0

```

Figure A.15 MEDICI input deck for solving the system. Equilibrium solution.

After we have the equilibrium solution, another symbolic factorization needs to be done (Figure A.16). In line 95 we specify that only Poisson's and hole continuity equation are going to be solved. This can be done since the MOSFET is a majority carrier device. The fact that MEDICI is not solving electron continuity equation reduces the system size and the time necessary to obtain a solution. The electron continuity equation must be included if we want to simulate the device breakdown, as explained in section A.10.

```

93...$*****
94... $ SECOND SYMBOLIC FACTORIZATION
95... SYMB   CARRIERS=1 HOLES NEWTON
96... METHOD ITLIMIT=20 PRINT CR.TOLER=1E-14 ^XNORM XRNORM RHSNORM
97... +     CARR.MIN=1E10 PR.TOLER=1E-20

```

Figure A.16 MEDICI input deck for second symbolic factorization.

A part of input deck that solves for the transfer curve at $V_{DS}=0.1$ V is given in Figure A.17. Initial steps are chosen to be small in order to ensure convergence and then they are increased. This part of the input deck can be changed in order to get the transfer curve at different V_{DS} voltage or to get the output curve.

```

98...$*****
99... $ SOLVING THE SYSTEM FOR TRANSFER CURVE AT VDS=0.1 V
100... SOLVE V1=-0.01
101... SOLVE V1=-0.015
102... SOLVE V1=-0.02
103... SOLVE V1=-0.03
104... SOLVE V1=-0.05
105... SOLVE V1=-0.08
106... $ OPEN THE i-v LOG FILE
107... LOG IVFILE="/tr_0.1/"@CHRTSI"_"@CHRNDO"tr.log"
108... SOLVE V1=-0.1 V2=0.0
109... SOLVE V1=-0.1 V2=-0.0001
110... SOLVE V1=-0.1 V2=-0.0003
111... SOLVE V1=-0.1 V2=-0.0007
112... SOLVE V1=-0.1 V2=-0.001
113... SOLVE V1=-0.1 V2=-0.003
114... SOLVE V1=-0.1 V2=-0.007
115... SOLVE V1=-0.1 V2=-0.01
116... SOLVE V1=-0.1 V2=-0.03
117... LOOP STEPS=9
118... SOLVE V1=-0.10 V2=-0.05:-0.05 SAVE.BIA
119... L.END
120... LOOP STEPS=11
121... SOLVE V1=-0.10 V2=-0.5:-0.15 SAVE.BIA
122... L.END
123... L.END
124... L.END

```

Figure A.17 MEDICI input deck for solving the system for transfer curve.