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<https://doi.org/10.15760/etd.6830>

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THESIS APPROVAL

The abstract and thesis of Sida Zhou for the Master of Science in Electrical and Computer Engineering were presented August 29, 1995, and accepted by the thesis committee and the department.

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ABSTRACT

An abstract of the thesis of Sida Zhou for the Master of Science in Electrical and Computer Engineering presented August 29, 1995.

Title: MOBILITY MODELING AND SIMULATION OF SOI $Si_{1-x}Ge_x$ p-MOSFET

With increasing demand for complex and faster circuits, CMOS technologies are progressing towards the deep-submicron level. Process complexity increases dramatically, and costly techniques are to be developed to create dense field isolation and shallow junctions. Silicon-On-Insulator (SOI) may solve some of these problems. On the other hand, strained $Si_{1-x}Ge_x$ layers have been successfully grown on Si substrates and demonstrated much higher hole mobility than bulk Si. This can be used to build high-mobility p-MOSFET with a buried $Si_{1-x}Ge_x$ channel. A high mobility p-MOSFET would improve both the circuit speed and the level of integration.

The purpose of the present study was to model and simulate the effective mobility (μ_{eff}) of SOI $Si_{1-x}Ge_x$ p-MOSFET, and to investigate the suitability of local mobility models provided by simulator MEDICI for studying SOI $Si_{1-x}Ge_x$ p-MOSFET. The simulation is performed by using the two-dimensional device simulation program (MEDICI). The design parameters, such as Si-cap thickness, Ge profile and back-gate bias, were also investigated.

A long channel (6μ) and a short channel (0.25μ) SOI and bulk $Si_{1-x}Ge_x$ p-

MOSFET were used for the study. Simulation reveals good effective mobility μ_{eff} match with experimental results if SiGe channel of p-MOSFET can simply be treated like a bulk silicon with mobility $250\text{cm}^2/\text{Vs}$. Mobility models provided by MEDICI are two types: a) mobility model (SRFMOB2) that is dependent on transverse electric field **only** at Si/SiO_2 interface, which means that the effective mobility is a function of grid spacing at Si/SiO_2 interface, and b) mobility models (PRPMOB, LSMMOB and HPMOB) that are dependent on transverse electric field **anywhere** in the device. PRPMOB and LSMMOB produce very good μ_{eff} and are insensitive to the grid spacing. HPMOB gives slight over estimation of effective mobility μ_{eff} .

Silicon cap thickness can significantly influence the effective mobility μ_{eff} . In general, the thin silicon cap have better effective mobility μ_{eff} , but it is limited by manufacturing process. Graded $\text{Si}_{1-x}\text{Ge}_x$ channel presents nearly 100% improvement of effective mobility μ_{eff} for p-MOSFET over its bulk counterpart. This improvement is sustained up to gate voltage of 2.5 V. Simulation also indicates that large improvement of effective mobility μ_{eff} requires higher Ge concentration at the top of SiGe channel with steep grading. The influence of back-gate bias on μ_{eff} is small, hence, SOI SiGe MOSFET is well suited to building CMOS circuits.

MOBILITY MODELING AND SIMULATION OF SOI $Si_{1-x}Ge_x$ p-MOSFET

by
SIDA ZHOU

A thesis submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE
in
ELECTRICAL AND COMPUTER ENGINEERING

Portland State University
1995

ACKNOWLEDGEMENTS

I would like to acknowledge the following individuals without whose support and encouragement this study might not have come to fruition:

First and foremost, my love and gratitude go to my wife, Chunping Guo. Her patience, caring and supporting helped me to reach a goal that often seemed elusive and distant.

To Branimir Pejcinovic, Chairman of my Committee, I give special thanks for providing guidance, keeping me focused and friendship throughout the length of the study.

To Malgorzata Chrzanowska-Jeske and Bradford R. Crain, my committee members, I am especially grateful to them who reviewed the thesis and served in my committee.

I am also indebted to Marijan Peršun, a friend and colleague who helped detailed issues of the study and made helpful discussion possible.

To Shirley Clark, Laura Riddell and Ellen E. Wack of the Electrical Engineering Department staff, my thanks for many ways they have helped me with all the procedures needed to finish my study.

Finally, to my child, friends and colleagues who encouraged me along the way. I owe a debt of gratitude.

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Chapter 1

INTRODUCTION

As bulk CMOS technologies are progressing towards the submicron level, process complexity increases dramatically, and costly techniques are to be developed to create dense field isolation and shallow junctions. Silicon-On-Insulator (SOI) technologies provide solutions to these problems in a straightforward manner. Thin SOI MOSFETs exhibit remarkable properties such as maximum subthreshold slope, minimum short-channel effects, absence of kink effect, and reduced hot electron degradation [1]. Recent developments in this field have shown that high-performance SOI devices can be fabricated in thin silicon films on SIMOX substrates [2][3]. This technology also presents a great potential for fabrication of multi-layered three-dimensional devices.

Furthermore, in the past few years, strained SiGe layers have been successfully grown with molecular beam epitaxy (MBE) and low temperature chemical vapor deposition (CVD). This success is most vividly shown by the recent advances in the heterojunction bipolar transistors (HBT)[4] [5] and field-effect transistors [6] incorporating the strained SiGe layer. In bipolar transistors, the presence of germanium exponentially alters the device characteristics (e.g., the collector current). In field-effect transistors (FET's), the strained SiGe offers enhanced carrier mobilities.

The bandgap difference between strained SiGe and unstrained Si appears mostly in the valance band. Hence, further improvement in p-channel FET hole mobility results from hole confinement in a SiGe channel away from the SiO_2/Si interface, and from modulation doping. The interest in high-mobility p-channel FET's results from the inferior performance of silicon p-MOSFET's in CMOS applications caused by the field-effect hole mobility which is typically two to three times lower than the field-effect electron mobility. To minimize asymmetric operation, Si p-MOSFET's are designed with wider gates, thus affecting packing density. A high mobility p-channel FET will improve both the circuit speed and the level of integration.

By combining the advantages of SOI and strained SiGe layer technologies, Nayak [6] has presented a new p-channel SiGe-SIMOX devices. The device contains a $Si/Ge_{0.3}Si_{0.7}/Si$ channel, which, due to reduced vertical electric field and band bending at the surface of a SiGe-SIMOX device, has a hole confinement in the buried channel that is improved over that of a SiGe-bulk device. The effective channel mobility of this device is found to be 90% higher than that of an identically processed conventional SIMOX device. This kind of device, i.e. SOI SiGe pMOSFET, forms the subject of this thesis. The research focus is on the effective mobility of SOI SiGe pMOSFET, the performance of such device as well as its design parameters. All of these will be discussed in the later chapters.

This chapter is organized as follows, SOI MOSFET in general will be discussed in section 1.1; In section 1.2, a comparison between bulk MOSFET and SOI MOSFET is presented, followed by discussions of objectives of this thesis in section 1.3; Finally, the outline of the thesis is given in section 1.4.

1.1 SOI MOSFET

The idea of realizing semiconductor devices in a thin silicon film, which is mechanically supported by an insulating substrate rather than silicon substrate, has been around for several decades. Only recently, the technology has advanced enough to produce a quality film of single-crystal silicon on top of an insulator. Some of them are based on the epitaxial growth of silicon on either a silicon wafer covered with an insulator (homoepitaxial techniques) or on a crystalline insulator (heteroepitaxial techniques). Other techniques are based on crystallization of a thin silicon layer from melt, such as laser recrystallization, e-beam recrystallization and zone melting recrystallization. SOI material can also be produced from a bulk silicon wafer by isolating a thin silicon layer from substrate through the formation and oxidation of porous silicon (FIPOS) or through the ion beam synthesis of a buried insulator layer, such as SIMOX, SIMNI and SIMON [7]. Finally, SOI material can also be obtained by thinning a silicon wafer bonded to an insulator and a mechanical substrate (wafer bonding). Every approach has its advantages and disadvantages, and the type of application of SOI wafer dictates the material to be used in each particular case. SIMOX, for instance, seems to be an ideal candidate for VLSI and rad-hard applications, wafer bonding is more adapted to bipolar and power applications, while laser recrystallization is the main contender for fabrication of 3D integrated circuits. Therefore, SOI wafers contain only silicon and silicon dioxide, and the appearance of SOI wafers is very similar to that of bulk silicon wafers. As a consequence, SOI circuit processing can be carried out in standard bulk silicon processing line.

All SOI MOSFETs are not alike. Their physics is highly dependent on the thickness of the silicon film in which they are made. Three types of devices can be distinguished, depending on both the silicon film thickness and the channel doping concentration: the thick-film and the thin film devices, as well as the “medium thickness” device, which can exhibit either a thin- or a thick-film behavior, depending on the back-gate bias.

In the bulk device, the depletion zone extends from the Si-SiO₂ interface down to the maximum depletion width, x_{dmax} , which is classically given by $\sqrt{\frac{4\epsilon_{si}\phi_F}{qN_A}}$, ϕ_F being the Fermi potential, which is equal to $\frac{kT}{q} \ln(\frac{N_A}{n_i})$.

In the thick-film SOI device, the silicon film thickness is larger than twice the value of x_{dmax} . In such case, there is no interaction between the depletion zones arising from the front and the back interfaces, and there exists a piece of neutral silicon beneath the front depletion zone. If this neutral piece of silicon, called body, is connected to ground by a “body contact”, the characteristics of the device will be exactly those of a bulk device. If the body is left electrically floating, the device will basically behave as a bulk device with the notable exception of two parasitic effects, the first of which is called “kink effect”, the second one being the presence of a parasitic, open base NPN bipolar transistor between source and drain.

In a thin-film SOI device, the silicon film thickness is smaller than x_{dmax} . In that case, the silicon film is fully depleted at threshold, irrespective of the bias which is applied to the back gate (with the exception of the possible presence of thin accumulation or inversion layers at the back interface, if a large negative or positive bias is applied to the back gate, respectively). Thin-film, fully depleted SOI devices

are virtually free of kink effect, if their back interface is not in accumulation. Among all types of SOI devices, fully depleted devices with depleted back interface exhibit the most attractive properties, such as low electric fields, high transconductance, excellent short-channel behavior, and a quasi-ideal subthreshold slope. Thin-film SOI (TFSOI) MOSFETs are often referred to as fully-depleted devices. Because both front and back interfaces can be in either accumulation, depletion or inversion, one can number nine modes of operation in the thin-film SOI transistor as a function of front and back gate voltage.

1.1.1 n-Channel Device

The n-channel TFSOI MOSFET has a p-doped channel region. The thin film nature of the device allows the space charge region below the gate to extend over entire film thickness, above threshold as well as in the subthreshold region. This reduces dramatically the dependence of depletion charge variation on gate voltage variation and gives rise to an excellent coupling between gate voltage and surface potential. As a result, subthreshold slopes values down to 65mV/dec are obtained. Degradation of the the subthreshold slope in submicron TFSOI devices is smaller than in bulk devices. There is a large difference of potential and electric field distribution between TFSOI and more classical “thick-film” SOI devices. The vertical field near the SiO_2 -Si interface is smaller in TFSOI devices, giving rise to mobility enhancement. The limited vertical extension of the depletion zone near the drain retards the onset of pinch-off and increases saturation current. These properties

are responsible for the superiority of TFSOI circuit speed performances over those of “classical” SOI or bulk circuits. Owing to a more uniform distribution of the potential drop between drain and source, TFSOI devices present reduced drain electric field. This phenomenon results in a reduction of hot-electron degradation and in the elimination of the kink effect. The limited vertical extension of the depletion zone below the gate causes little dependence of the charge controlled by the gate upon gate length . As a consequence, much smaller threshold voltage roll-off (short-channel effect) is observed in submicron TFSOI MOSFETs than in their counterparts [7].

1.1.2 p-Channel Device

The thin-film SOI with n^+ -gate (n^+ is the dominant material for the gate) p-channel MOSFET is an accumulation-mode (deep-depletion) device , where the channel is composed of majority carriers (i.e. having an accumulation channel instead of an inversion channel). When the device is turned OFF, the silicon film beneath the gate is fully depleted of holes. When a negative bias is applied to the gate, an accumulation channel is formed, and the device is turned ON. The accumulation-mode device exhibits a high mobility , no kink, very little bipolar effects but is more sensitive to punchthrough than regular “enhancement-mode” devices [7]. In this thesis, we are simulating “enhancement-mode” devices.

1.2 Bulk and SOI MOSFET Devices Comparison

Although most types of devices can be fabricated in SOI films, the preferred application field for Silicon-on-Insulator technology is undeniably CMOS. This is because that SOI devices have several advantages over bulk CMOS, which are summarised in the following sections.

1.2.1 Elimination of Latchup

Parasitic bipolar transistors are a problematic byproduct of all MOS processes. In CMOS processes these transistors are particularly troublesome because an n-p-n-p structure is formed by the n+ source of the NMOS transistor, the p substrate, the n well and the p+ diffusion of the PMOS transistor inside the n well Fig. 1.1. Due to the inherent positive feedback in this structure, when it turns on, ground and power get effectively shorted together, large currents are produced and the circuit is destroyed. This is referred to as CMOS latchup. The pnp transistor is formed by the p source of the PMOS transistor (emitter), n well (base), and p substrate (collector). The npn transistor is formed by the n well (collector), p substrate (base), and n source of the NMOS transistor (emitter). R_{well} and $R_{substrate}$ represent the n well and p substrate resistances to Vdd and GND respectively. When any of these two bipolar transistors is forward biased, it feeds the base of the other transistor, which in turn feeds the base of the first transistor, and this positive feedback increases the current until the circuit burns out. There are several ways of avoiding latchup and all of them focus either on reducing the gain of the bipolar transistor to weaken the

Figure 1.2: Cross section of a SOI CMOS inverter showing drain parasitic capacitances

diffused sources and drains and the substrate. This capacitance increases with substrate doping, and becomes larger in modern submicron devices where concentration in the substrate is higher than in previous MOS technologies. Source and drain capacitance consists not only of the obvious capacitance of the depletion regions associated with junctions, but also of the capacitance between the junction and the heavily-doped channel stop located underneath the field oxide.

If a Silicon-on-Insulator (SOI) substrate is used, quasi-ideal devices can be fabricated. The SOI MOSFET contains indeed the necessary three terminals (a source, a drain, and a gate which controls a channel in which current flows from source to drain), but the full dielectric isolation of the devices prevents the occurrence of most of the parasitic effects experienced in bulk silicon devices as most parasitic effects

in bulk MOS devices find their origin in the interactions between the device and the substrate.

Furthermore, bulk CMOS circuits utilize reverse-biased junctions to isolate devices one from another. Let us consider, for instance, the drain of the n-channel transistor of Figure 1.1. The drain is always positively biased with respect to the substrate (the drain voltage can range between GND and VDD). A depletion capacitance is associated with the drain junction. Its maximum value is reached when the drain voltage is 0 volt and it is dependent on the substrate doping concentration. The higher this dopand the higher the capacitance. Modern submicron circuits tend to use higher and higher dopand concentrations. This increases the junction capacitances. In addition, there also exists an important parasitic capacitance between the junctions and the channel stop implant placed underneath the field oxide to prevent surface leakage between bulk devices.

In SOI circuits, on the other hand, the maximum capacitance between the junctions and the substrate is the capacitance of the buried insulator (the capacitance tends towards zero if thick insulators are used, which is the case in SOS technology). This capacitance is proportional to the dielectric constant of the capacitance material. Silicon dioxide, which is widely used as buried insulator, has a dielectric constant ($\epsilon_{ox} = 3.9\epsilon_o$) which is three times smaller than that of silicon ($\epsilon_{si} = 11.7\epsilon_o$). Therefore, a junction located on a buried oxide gives rise to a parasitic capacitance which is three times smaller than that of a bulk junction giving rise to a depletion depth equal to the buried oxide thickness. Buried insulator thickness does not need to scale down as devices with smaller dimensions are produced, and, hence, parasitic

capacitances do not increase as technology progresses, contrary to what happens in bulk devices. In addition, a lightly-doped, p-type silicon wafer can be utilized as mechanical support. In that case, a depletion layer can be created beneath the insulator, which further reduces the junction-to-substrate capacitances.

1.2.3 Ease of Fabrication

SOI CMOS fabrication schemes are much simpler than conventional bulk processes. All temperature cycles in SOI technology are much shorter and performed at lower temperatures. Processing steps such as well implants and long drive-ins are not needed. Threshold adjustment implants followed by short, low-temperature processing are sufficient for establishing channel regions for n-channel and p-channel devices. Bulk technologies use complex isolation schemes often involving etching of trenches. In SOI technology simple LOCOS oxidation is performed to provide isolation between devices. Undesirable LOCOS “birds beak” is substantially reduced in SOI technology. This guarantees high packing density of SOI. Further increase of packing density can be achieved by merging n- and p-type diffusions.

1.2.4 Ease of Metalization of Shallow Junctions

One of the most challenging tasks in VLSI technologies is metalization of shallow source and drain junctions. Barrier metals are applied in bulk silicon technologies to prevent metal spikes through shallow junctions. In SOI technology source and drain junctions are extended down to buried SiO_2 eliminating the danger of metal

spikes.

1.2.5 Resistance to Radiation Damage

There are three main failure mechanisms in MOS devices operating in harsh environment: single-event upset (soft error), photocurrent generation, and charge build-up in the oxide. Because of the small volume of silicon involved, thin SOI devices are inherently well resistant to single-event upsets (SEU) caused by exposure to alpha particles or energetic heavy ions. Gamma-ray induced photocurrent depend on the area of the junctions in the device, and, therefore, are minimized in thin film SOI MOSFETs where the source and drain diffusions extend throughout the entire film thickness [1].

1.3 Objectives of the Thesis

The goal of this thesis is to focus on studying the characteristics of SOI SiGe p-MOSFET, which takes the advantages of both SOI device and strained $Si_{1-x}Ge_x$ layer. The specific objectives are as follows:

1. The effective carrier mobility (μ_{eff}) of SOI SiGe p-MOSFET. The study of effective carrier mobility is essential for any accurate modeling the SOI SiGe pMOSFET. The simulation is performed by using the two-dimensional device simulation program (MEDICI). The results are compared with published data of SOI SiGe pMOSFET, or compared with SOI Si pMOSFET and Si bulk pMOSFET.

2. The design parameters are also studied by simulation. These parameters include the Si-cap thickness, Ge profile (mole fraction of Ge in $Si_{1-x}Ge_x$ and the manner of grading in the channel) and back-gate bias on the effective mobility.

1.4 Outline of the Thesis

This thesis is organized in the following manner: In chapter 2, the physical properties of strained $Si_{1-x}Ge_x$ layer are presented, which serves as the foundation and justification for the structure of SOI SiGe pMOSFET in this thesis. Chapter 3 deals with the SOI SiGe pMOSFET device under study. The detailed calculation of effective mobility μ_{eff} and modeling of the local MOSFET mobility is discussed and followed by the results of effective carrier mobility μ_{eff} in chapter 4. The design issues are presented in chapter 5 along with some results. Finally, in chapter 6, the conclusions of this thesis are presented.

Chapter 2

PHYSICAL PROPERTIES OF STRAINED $Si_{1-x}Ge_x$ LAYER

Recent developments in epitaxial growth techniques of $Si/Si_{1-x}Ge_x$ heterostructures have demonstrated a significant potential of this system for electron device applications [8][9][10]. In particular, an p-channel SiGe-SIMOX device [6] has achieved 90% higher effective channel mobility compared to all-Si control devices. Garone [11] demonstrated that effective hole mobility enhancements of 50% at room temperature and over 100% at 90 K by placing a buried epitaxial $Si_{1-x}Ge_x$ layer 7.5 to 10 nm beneath the gate oxide of a PMOS transistor. This enhancement is generally attributed to the changes in valence band structure and to the removal of holes from Si/SiO_2 interface. Subsequent sections will deal with this issue in greater detail.

The development of lattice-mismatched heteroepitaxy has resulted in an increase in the study of charge-carrier transport in strained semiconductors. Theoretical and experimental studies show that if a material with bulk lattice constant a_L is grown as film on a comparatively thick substrate with a different lattice constant a_S , the film will grow epitaxially, with an in-plane lattice constant of a_S and an adjustment, via the Poisson effect, in the perpendicular lattice constant. This pseudomorphic growth continues up to a critical thickness determined by a balance between strain and

chemical energy . Beyond this thickness the overlayer relaxes, producing dislocation. The in-plane lattice constant of the film reverts to its bulk value a_L .

For film thickness less than the critical thickness, a large strain can be produced in the film, which can greatly change its band structure, both by changing effective masses and lifting degeneracies. Since the pseudomorphic layer is thermodynamically stable, it is possible to fabricate semiconductor devices with strained layer components. The strain-induced band structure changes may lead to increased charged carrier mobility within the pseudomorphic layer. This, in turn, becomes a useful way to increase the speed of semiconductor device operation.

The heteroepitaxial system of $Si_{1-x}Ge_x$ layer grown on Si substrates is of great technological interest for fabricating semiconductor devices. On the one hand, $Si_{1-x}Ge_x$ ($x > 0$) has a larger bulk lattice constant than Si and thus forms an strained epitaxial layer when grown on Si. This strain raises the heavy-hole and light-hole band degeneracy, hence the reduced effective mass. This may lead to an increase of charge-carrier mobility, over that of Si. On the other hand, the $Si_{1-x}Ge_x$ material system offers an advantage over III-V compound semiconductors of being processable with existing, high-yield silicon processing methods. Optimum semiconductor device design is ultimately based upon a complete understanding and accurate modeling of carrier transport. In this chapter, the physical properties of strained $Si_{1-x}Ge_x$ layer are discussed, which include two important aspects: the valance band structure and the mobility of strained $Si_{1-x}Ge_x$ layer. Those physical properties are the fundamental for the study of the devices presented in this thesis.

2.1 Band Structure

2.1.1 Valence Band Structures

In unstrained $Si_{1-x}Ge_x$ with arbitrary mole fraction x , the valence band of Si and $Si_{1-x}Ge_x$ consists of three valleys with minima at $k=0$ shown in Fig. 2.1. Two of these, the light and heavy-hole bands, are degenerate in the absence of strain [12][13], while the third “spin-orbit” band lies 0.044eV in energy below them as illustrated in Fig. 2.1. Application of strain removes the degeneracy of the light and heavy holes. For strained $Si_{1-x}Ge_x$ on Si, the light-hole band moves up while the heavy-hole band moves down. The resultant split in energy can be approximated by solution of a secular equation of the strain Hamiltonian, for heavy-hole (h.h.), light-hole (l.h.), and spin-orbit (s.o.), respectively, by [12][13]:

$$\Delta E_v(h.h.) = \varepsilon \quad (2.1)$$

$$\Delta E_v(l.h.) = \frac{1}{2}(\varepsilon + \Lambda) + \frac{1}{2}\sqrt{9\varepsilon^2 + \Lambda^2 - 2\varepsilon\Lambda} \quad (2.2)$$

$$\Delta E_v(s.o.) = -\frac{1}{2}(\varepsilon + \Lambda) - \frac{1}{2}\sqrt{9\varepsilon^2 + \Lambda^2 - 2\varepsilon\Lambda} \quad (2.3)$$

where ε is the strain energy representing the strength of the strain, with positive values for compressive strain and negative value for tensile strain [12], [13], and Λ is the spin-orbit energy. If compressive, the heavy-hole band is higher, while if tensile, the light-hole band is higher, as schematically shown in the Fig. 2.1. It is reasonable to assume that the effect of strain is to create the energy shifts, and the shape of the valence band structure is the same as that of the unstrained case [13]. The lift of

heavy-hole or light hole band results in smaller effective mass compared with bulk Si, hence, strained $Si_{1-x}Ge_x$ has better hole mobility.

Figure 2.1: Valence structure consisting of heavy-hole, light-hole and spin-orbit bands

2.1.2 Conduction Band Structure

The modeling of hole mobility, the results are affected by the structure of the conduction band due to electron-hole scattering. The conduction band has six valleys located along the $[100]$ or Δ axes as indicated in Fig. 2.2. They are split under strain into a two- and fourfold degeneracy, separated by an energy difference which has been measured for small values of x (x is the mole fraction of Ge) and to a linear approximation it is $0.6x$ eV [14]. For the case of strained $Si_{1-x}Ge_x$ grown on (001) Si, the four valleys in the plane of growth (here after called transverse) shift down in energy, while the two normal to the growth plane (longitudinal) shift

up.

This induced valley separation results in a repopulation of electrons between the transverse and longitudinal valleys, with more electrons now residing in the lower transverse valleys. It is this repopulation which we can exploit in device design due to the highly skewed effective mass tensor of silicon. Electrons in the transverse valley traveling normal to the growth plane experience an effective mass of $m_t^* = 0.19m_0$, while those traveling in the plane see a mass of $m_l^* = 0.91m_0$. The reverse is true for electrons in the longitudinal valleys, and so the mobility is anisotropic.

Figure 2.2: Schematic constant-energy surfaces of the conduction bands of silicon. Showing six conduction band valleys in $\langle 100 \rangle$ direction of momentum space.

Figure 2.3: Band lineup at the $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ heterojunction with (a) is type I line-up and (b) is type II line-up

2.2 The Band Lineup

It has been reported [12][14] that the band lineup at the heterointerface of $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ is schematically shown in Fig. 2.3. Depending on which side is relaxed, there are two types of line-up. Type I consists of relaxed Si and strained $\text{Si}_{1-x}\text{Ge}_x$, type II consists of relaxed $\text{Si}_{1-x}\text{Ge}_x$ and strained Si. An estimate of ΔE_v for a pseudomorphic Ge/Si heterointerface was obtained by Van de Walle [15]. For $\langle 001 \rangle$ oriented interface ΔE_v for Ge on Si was calculated for three cases, corresponding to:

1. Growth on Si substrates, with in-plane lattice constant $a_{||} = 5.431 \text{ \AA}$, resulting in cubic Si and strained Ge.
2. Growth on Ge substrates, $a_{||} = 5.66 \text{ \AA}$, resulting in cubic Ge and strained Si.
3. Growth on $\text{Ge}_{0.38}\text{Si}_{0.62}$ substrates, $a_{||} = 5.52 \text{ \AA}$, hence both Si and Ge strained.

Van de Walle's [15] results indicated that the Ge valence band edge lies above the Si valence band edge in all above cases. The ΔE_v is well described by the relation [14]:

$$\Delta E_v[(Ge, Si)/Si \text{ on } [001](Ge, Si)] = (0.74 - 0.53x_s)x \quad (2.4)$$

where x denotes the Ge content in the epilayer and x_s denotes the Ge content in the substrate. The relationship is plotted in Fig. 2.4 with Ge content of the epilayers as parameter for $x=1.0$, 0.5, and 0.2. Based on Fig. 2.4, ΔE_v for growth of $Ge_{0.2}Si_{0.8}/Si$ heterojunctions on $\langle 001 \rangle$ Si substrates, is type I band alignment with $\Delta E_v = 0.15\text{eV}$. From the results in Fig. 2.4, we see that the type of band alignment and the value of ΔE_v for pseudomorphic Ge_xSi_{1-x}/Si heterointerfaces is sensitive to the state of strain in the Si epilayers.

Figure 2.4: Calculated valence band offsets for Ge_xSi_{1-x}/Si heterostructures grown on Ge_xSi_{1-x}/Si substrates

In general, as far as the valence band lineup is concerned, the Si side is always a potential barrier and the $Si_{1-x}Ge_x$ side is a potential well to the holes, regardless of which side is relaxed and strained, or if both are strained [12][14]. This is in sharp contrast with behavior of conduction band, whose lineup is reversed depending on which side of the heterojunction is relaxed [12][14]. Since the valence band lineup is such that the Ge-rich side is a potential well and Si-rich side is always a potential barrier to the holes, this effect can be used in the buried $Si_{1-x}Ge_x$ channel in p-MOSFET to confine the holes.

2.3 Mobility

Hole transport in the strain $Si_{1-x}Ge_x$ system has been studied by several researchers using various methods [13][16] [17]. There are several important results which are listed below:

1. The hole mobility in Ge is $2000cm^2/Vs$, which is much better than that of Si, $450cm^2/Vs$ [18]
2. The hole mobilities, as a function of temperature for intrinsic strained $Si_{1-x}Ge_x$ (The doping concentration $< 10^{16}cm^{-3}$), are higher than bulk Si in the entire temperature range [16]. This fact can be understood from the change of the valence-band structure. Under strain, both interband and intraband scattering are reduced due to the smaller density of states (DOS) than those of the bulk Si. In the high temperature range, carriers occupy a higher en-

ergy level where both interband and intraband scatterings are significant. As the temperature decreases, most carriers are expected to be located near the valence-band top whose degeneracy is lifted in strained $Si_{1-x}Ge_x$, resulting in reduced interband scattering. This decrease of interband scattering greatly enhances the mobility.

3. The hole mobilities, as a function of doping concentration for $Si_{1-x}Ge_x$ (for example $x = 0.2$), are greatly enhanced compared to bulk Si for low doping concentration region ($900 cm^2/V \cdot s$). This enhancement is mostly due to the lifting of the degeneracy of the valence bands and large spin-orbit splitting energy, which reduce the interband scattering. For high doping concentrations, the hole mobility become comparable to bulk Si due to the fact that the ionized impurity scattering becomes dominant in this region [16][17].
4. The hole mobilities, as a function of Ge mole fraction is higher with increases of Ge content. The effect of the Ge content variation is reflected in the density of states and the splitting of the spin-orbit band. In general, the higher the Ge content, the smaller the DOS and the larger the spin-orbit splitting energy. The decrease of the DOS reduces both interband and intraband scattering and the increase of the spin-orbit splitting energy also reduces the interband scattering rate [16].
5. The hole mobilities, as a function of valance-band effective masses, are significant improved over bulk Si, since the valance-band effective masses decreases as the Ge content increases. This is due to presence of a biaxial stress in the

strained $Si_{1-x}Ge_x$ layer. In general, the biaxial stress can be decomposed into hydrostatic term and an uniaxial term. The hydrostatic stress term simply shifts all of the energy levels of valance bands equally, not affecting the effective mass. On the other hand, the uniaxial stress splits the heavy and light hole bands and changes the valance-band structure severaly. Since the lattice constant of Ge is larger than that of Si by 4.17%, strained SiGe layer will experience an increasing strain as the difference of the Ge content between the film and the substrate increases. Thus the change of the effective mass will become more significant for a larger difference of the Ge content between the substrate and the film. More detailed discussion regarding the effective mass can be found in [16].

In summary, we have reviewed the physical properties of strained $Si_{1-x}Ge_x$ layer in this chapter, which will serve as fundamentals for analysis and study of any strained $Si_{1-x}Ge_x$ based devices. The strained $Si_{1-x}Ge_x$ system provides a higher hole mobilities than the bulk Si. This also provides an incentive for us to study the SOI $Si_{1-x}Ge_x$ pMOSFET. In following chapters we will focus on the effective mobility study of SOI $Si_{1-x}Ge_x$ pMOSFET.

Chapter 3

DEVICE DESCRIPTION, SIMULATION AND VERIFICATION

The mobility of carriers in the inversion layer of a MOSFET is significantly less than that of carriers in the bulk semiconductor. The mobility reduction is caused by surface scattering of the carriers, which are closely confined to the Si/SiO_2 interface by strong transverse electric field of the gate. This fact is particularly troublesome for Si pMOS devices since CMOS device performance has been limited by the lower intrinsic mobility of holes. It has been proposed and demonstrated by several research groups that moving the holes away from the Si/SiO_2 interface and by confining them in a $Si_{1-x}Ge_x$ quantum well would improve their mobility. In the previous chapter, the physical properties of strained $Si_{1-x}Ge_x$ layer have been reviewed. There are two important results, which is very useful for building the device. Those properties are:

1. At $Si/Si_{1-x}Ge_x$ heterojunction, the valence band lineup is that the Si side is always a potential barrier and the $Si_{1-x}Ge_x$ side is a potential well to the holes, regardless of which side is relaxed and strained, or if both are strained.

2. Due to the lifting of the degeneracy of the valence bands and large spin-orbit splitting energy of strained $Si_{1-x}Ge_x$ layer, this degeneracy also causes valance-band effective mass reduction, therefore, the hole mobility in the layer is higher than Si bulk. For example, given doping less than 10^{17} and mole fraction $x = 0.2$, the hole mobility of strained $Si_{1-x}Ge_x$ alloy is above $900cm^2/Vs$, which is the twice of Si bulk's hole mobility [17].

Based on above properties, a SOI $Si_{1-x}Ge_x$ p-MOSFET structure is presented which will be used for the simulation study of in this thesis. The device is build in such a way that it can take advantages of both SOI device and strained $Si_{1-x}Ge_x$ layer channel. The geometries, characteristics and parameters of such SOI $Si_{1-x}Ge_x$ p-MOSFET are discussed in detail in this chapter. The definitions and calculations of effective mobility (μ_{eff}) and effective electrical field (E_{eff}) are also discussed in this chapter. Finally, the simulation procedures and MEDICI—Two-dimensional device simulation program are discussed.

3.1 SOI $Si_{1-x}Ge_x$ p-MOSFET

By combining the SOI and strained $Si_{1-x}Ge_x$ layer technologies, the structure in Fig. 3.1 is developed for simulation study of the effective mobility and device design parameters. The characteristics and functionality of the constituent parts in above device need to be discussed in detail. The parts include $Si_{1-x}Ge_x$ channel, silicon cap, band diagram, Ge profile and p^+ spike.

Figure 3.1: SOI $Si_{1-x}Ge_x$ p-MOSFET with t_{CAP} is the silicon cap thickness, t_{CH} is SiGe channel thickness and t_{BUF} is the silicon buffer thickness

3.1.1 The $Si_{1-x}Ge_x$ channel and the Silicon Cap

When compared with the regular SOI device, one noticeable difference of the device presented in Fig. 3.1 is the introduction of strained $Si_{1-x}Ge_x$ layer in the structure. This structure improves the hole mobility by two mechanisms [11]:

1. Mobility enhancement in strained $Si_{1-x}Ge_x$ layer or channel (see chapter two for details).
2. Reduction of surface scattering by removing the holes from the Si/ SiO_2 interface and confining them in the $Si_{1-x}Ge_x$ well.

If a relative small negative gate voltage is applied, one can modulate the number of holes in the $Si_{1-x}Ge_x$ well, eventually forming an inversion layer within it, as

shown in Fig. 3.2. As the gate voltage is increased further, an inversion layer will also begin to form at Si/SiO_2 interface, and eventually the dominant hole population will reside at the Si/SiO_2 interface. Based on this observation, we expect that for certain range of gate voltages the mobility should be greatly improved, which is the topic of this thesis.

The silicon cap is introduced to serve two purposes, 1) the gate quality oxide can be grown, and 2) moving the $Si_{1-x}Ge_x$ channel away from the interface of gate oxide to reduce the surface scattering as much as possible.

3.1.2 The Bond Diagram

As mentioned above, The mobility improvement can be obtained by placing a buried $Si_{1-x}Ge_x$ layer under the gate of a p-MOSFET transistor. A well for holes is then created, since the bandgap discontinuity is predominantly in the valance band. The band structure of such a device near flat band is shown in Fig. 3.2.

From the Fig. 3.2, we can notice that the band gap difference between the silicon and silicon-germanium is all accommodated in valence band. In the direction perpendicular to the Si/SiO_2 interface, the hole quasi-Fermi level is constant. The hole concentration is exponentially dependent on the difference between this level and the valence band edge. Hence, the hole concentration in the $Si_{1-x}Ge_x$ channel is much higher than in the silicon. We expect, therefore, that a majority of current will flow in $Si_{1-x}Ge_x$ region for low gate voltage as illustrated in Fig. 3.3.

As the gate voltage increases, the valence band at the surface “bends” upward

Figure 3.2: Band diagram for $Si_{1-x}Ge_x$ SOI p-MOSFET at vertical cross section in the middle of the device, with 30% Ge uniform distribution in the channel

and gets closer to the hole quasi-Fermi level. Hence, the hole concentration at the surface surpasses the one in the channel and the majority of current will flow at the surface instead of in the channel. The SOI $Si_{1-x}Ge_x$ p-MOSFET starts behaving just like the regular p-MOSFET.

3.1.3 Germanium Profile and p^+ Spike

There are several ways to improve the hole confinement in the channel. Voinigescu [19] pointed out that use of graded channel can significant improve the hole confinement. For uniform 25% Ge and the graded 0-50% Ge channel p-MOSFETs, the low field mobility is $250cm^2/Vs$ and $400cm^2/Vs$ for the uniform and graded devices respectively. The graded channel has higher mobility due to larger Ge mole fraction

Figure 3.3: Integrated Hole concentration along a vertical cross section in the middle of the device for low and high V_{GS} . $Si_{1-x}Ge_x$ SOI p-MOSFET with modulation doping and n^+ gate. SiGe channel has a graded profile with 45% Ge at the top and 25% Ge at the bottom

at the top of the channel. A built in quasi-electric field exists which pushes holes towards the top of the $Si_{1-x}Ge_x$ channel. This approach also brings holes closer to the gate and therefore increases the channel capacitance and consequently the transconductance. With the graded channel in the Fig. 3.3, we can notice that even for relatively high gate over-drive of 2.0 volts (threshold voltage is 0.35 volts) three fourths of the holes are still confined to the $Si_{1-x}Ge_x$ channel.

Another approach to improving hole confinement is to place high p-type doping (so called p^+ spike) just underneath the channel as illustrated in Fig. 3.1. This doping spike serves as a source of holes which are then collected by the $Si_{1-x}Ge_x$ channel. In the n^+ poly Silicon gate case, the p-type doping (p^+ spike) also serves

to adjust the threshold voltage.

Two additional possibilities for hole confinement adjustment are: 1) to minimize the Si cap layer which is limited by the requirement to separate the holes from surface; 2) to maximize germanium fraction in order to increase the band gap reduction. But we should keep in mind that high germanium mole fraction can lead to strain relaxation and defects if the critical thicknesses for coherently strained SiGe growth is exceeded. This is why a graded channel is a better choice since the same average germanium mole fraction we can employ a higher concentration at the top and improve the hole confinement [19].

3.2 Simulation Parameters and Characteristics of SOI $Si_{1-x}Ge_x$ p-MOSFET

Two fully-depleted SOI $Si_{1-x}Ge_x$ p-MOSFETs have been used to study the effective mobility. They are long and short channel devices with channel length 6μ and 0.2μ respectively. The schematic diagram of the long channel device is presented in Fig. 3.4. The geometries, structures, doping profiles and other parameters are listed in the following table 3.1.3. In the following sections, we will discuss structures of both long and short channel device in detailed along with simulation verifications. The verifications are done by comparing our simulation results with

Figure 3.4: SOI $Si_{0.7}Ge_{0.3}$ p-MOSFET with channel length 6μ

published experimental or simulation results.

3.2.1 Long Channel Device

The long channel device was following the structure presented in [6] and is shown in Fig. 3.4. The substrate doping (n-type) is 1.2×10^{15} and it is uniform doped, the 1500 Å SOI layer is results in a fully depleted device. This structure consists of a SIMOX like substrate, 100 Å Si layer, a 100-Å $Si_{0.7}Ge_{0.3}$ strained layer for hole confinement, and a 100 Å Si-cap layer. The SiO_2 gate oxide thickness is 70 Å. The gate oxide was kept small in order to minimize thermal relaxation of strain in $Si_{0.7}Ge_{0.3}$ [6]. The SiGe channel is uniform. Source and drain doping profiles are simulated by using TMA-SUPREM-4 , and then ported to MEDICI for simulation. A p^+ spike was included at 300 Å below top SiO_2 interface. In Nayak and et al's original

Table 3.1: The Parameters of the SOI $Si_{1-x}Ge_x$ p-MOSFET under study

Device Parameters	Long Channel Device	Short Channel Device
Channel Length (μ)	~ 6	~ 0.2
t_{OX} ($\text{\AA}$)	70	70
t_{CAP} ($\text{\AA}$)	100	50
t_{CH} ($\text{\AA}$)	100	80
t_{Si} (μ)	0.15	0.05
t_{BOX} (μ)	0.4	0.4
t_{BUF} ($\text{\AA}$)	100	70
S&D doping (cm^{-3})	6.4×10^{19}	5×10^{20}
Substrate doping (cm^{-3})	1.2×10^{15}	3×10^{17}
p^+ doping (cm^{-3})	2.7×10^{18}	7.0×10^{18}

paper [6], this p^+ spike is unintentionally doped during the initial phase of epilayer growth by MBE. Our simulations find the p^+ spike can greatly improve the transconductance of the device. Therefore, in this thesis, the p^+ spike is included in the devices.

There are two variations of the long channel device that have been studied in this thesis: one is the SOI device without the SiGe channel and its structure is the same as the one with SiGe channel as shown in Fig. 3.4, the other one is with the SiGe channel. Simulation results reveal that the threshold voltage of SOI p-MOSFET is -0.274 V which is very different from the -0.83 V in the paper [6], and for SOI SiGe

p-MOSFET threshold voltage is -0.182 V which is very close to -0.19 V given in the paper [6]. We find that the sub threshold characteristics of the devices have slopes of 61 and 73 mV/decade for SOI and SOI SiGe p-MOSFET devices, respectively. These numbers are smaller than reported ones in [6] which is 76 and 80 mV/decade for SOI and SOI SiGe p-MOSFET devices, respectively. This indicates in this case that SiGe channel will worsen somewhat the subthreshold characteristics of the device.

Figure 3.5: The transconductance g_m for Si and $Si_{0.7}Ge_{0.3}$ devices using different mobility models

The results for transconductance g_m are presented in Fig. 3.5. In the simulation, several mobility models (mathematical models in the simulator account for scattering mechanisms in electrical transport) have been used, which are enhanced surface mobility model (SRFMOB2) and mobility dependence on perpendicular electric field

(PRPMOB). The mobility models will be discussed in detail in the next chapter. When the SRFMOB2 model is used, g_m shows qualitative behavior observed in experiments [6], i.e. an extended maximum in g_m . Other models (only PRPMOB is shown) show two peaks that are associated with conduction along bottom and top interface of SiGe channel. The latter behavior has not been observed in experiments. To correct this, it is necessary to make the mobility in SiGe channel bulk-like, by neglecting the mobility dependence on transverse field inside SiGe channel. Also, no increase in low-field mobility is needed. g_m for this case is shown in Fig. 3.5 under PRPMOB* label. As expected, g_m is virtually the same for SRFMOB2 and PRPMOB*.

Input gate capacitance was calculated using small-signal a.c. simulation and is presented in Fig. 3.6. As in experiments, a characteristic change of slope (“plateau”) is observed. The p^+ spike contributes significantly to the plateau, which signifies hole confinement in the buried SiGe channel.

3.2.2 Short Channel Device

The short channel device is following the structure presented in [20], which is bulk SiGe p-MOSFET. It has the channel length of 0.2μ , $70\text{\AA}$ thick gate oxide, $50\text{\AA}$ thick Si cap layer, and $80\text{\AA}$ wide SiGe channel. The SiGe channel has a graded profile with 45% Ge at the top and 25% Ge at the bottom resulting in a stable SiGe layer. The channel doping levels are adjusted such that the corresponding threshold voltage for devices with effective channel length 0.20μ is -0.35V . n^+ poly silicon gate

Figure 3.6: $Si_{0.7}Ge_{0.3}$ device a.c. gate capacitance C_G vs. gate voltage.

is used in this structure, which implies that a large boron dose is needed for such a low threshold voltage. The total integrated boron dose required to achieve the desired $-0.35V$ threshold voltage is $2.0 \times 10^{12}/cm^2$, and the exact doping profile is shown in Fig. 3.7.

Based on this bulk device design, an SOI SiGe p-MOSFET is constructed by putting in a $4000\text{\AA}$ SiO_2 , and the thickness of Si layer between gate and the SiO_2 is about $500\text{\AA}$, which ensures that the device is fully depleted device. The transconductance of both bulk SiGe p-MOSFET, SOI SiGe p-MOSFET and bulk p-MOSFET are illustrated in Fig. 3.8. g_m shows improvement of both SOI and bulk SiGe p-MOSFET over bulk Si p-MOSFET with an extended maximum in g_m , but the difference between SiGe p-MOSFET and SOI SiGe p-MOSFET is very small. g_m

Figure 3.7: The 0.2μ SiGe n^+ -gate MOSFET's channel doping profiles, the peak is the p^+ spike. The Si cap doping is 1×10^{14}

for the bulk SiGe p-MOSFET is very close to the simulation results in [20]. The subthreshold characteristics are $100(mV/dec)$ and $87(mV/dec)$ for SiGe p-MOSFET and SOI SiGe p-MOSFET devices, respectively. Its short channel behavior in terms of drain-induced barrier lowering (DIBL) is 67 and 127 mV with ($V_{DS} = 2.5V$) for SiGe p-MOSFET and SOI SiGe p-MOSFET devices, respectively.

Figure 3.8: Transconductance g_m for Si and SiGe devices using LSMMOB mobility model without perpendicular electric field dependence at $V_{DS} = 0.05V$.

Chapter 4

MOBILITY MODELING AND SIMULATION RESULTS

Mobility in semiconductors is an important parameter that reflects carrier transport mechanisms. In MOSFET structures, the strong gate field confines carriers to a very thin inversion channel. This is in contrast to the transport mechanism in bulk. The thin channel, for instance, causes quantization effects and conductance anomalies [21]. The magnitude of low field mobility in the channel is smaller than in bulk at room temperature. A SOI $Si_{1-x}Ge_x$ p-MOSFET has been proposed to improve the channel mobility in the previous chapter. Modeling the channel mobility is one of the topics of this chapter. However, a direct measurement of mobility is very difficult. For this and other reasons, an **effective mobility** is often calculated from I-V measurements. In the following we will address the issues related to effective mobility as well as **local mobility** modeling by using the devices presented in the previous chapter.

4.1 μ_{eff} and E_{eff} Definitions and Calculations

Modeling of the carrier mobility in the inversion layer of MOSFET transistors is of crucial importance for accurate device characterization and comparison between

different technologies. It has been reported that the normal electric field dependence of the mobility is described by a “universal” curve if the measurements are analyzed in terms of an effective normal electric field E_{eff} . Mobility calculated in this fashion is the effective channel mobility (μ_{eff}) and is essentially independent of the gate oxide thickness (t_{OX}), impurity concentration near Si/SiO_2 interface, and over a wide range of MOS technologies. There are two different approaches to calculate the μ_{eff} and E_{eff} values:

1. μ_{eff} and E_{eff} are calculated from terminal I_{DS} , device geometry and doping by using simple analytical expressions. This approach is well suited for experimental device characterizations. Hereafter, we will call this approach experimental approach.
2. μ_{eff} and E_{eff} are determined directly from the distribution of carriers and electric field given by the numerical device simulator. This is the theoretical value. We will call this approach analytical approach.

Calculation of μ_{eff} and E_{eff} is done by extracting the data from device simulator.

In general, two-dimensional numerical device simulators use fine grid structures such that converged or unique spatial distributions of free charge carriers, electrostatic potential and electric field are obtained, i.e. the solutions are grid independent beyond some grid density. In widely used simulators such as MEDICI and MINIMOS, fine grid structures are intended for use in device simulation, where the carrier mobility in the inversion charge layer is spatially varying, and depending on the local electrical field. However, from the measured terminal current I_{DS} , only

μ_{eff} and E_{eff} can be determined, which are “average” quantities. The connection between local mobility (say μ) and effective mobility μ_{eff} is not easily established. In addition, the extraction of E_{eff} is based on the assumption that the inversion charge layer is a charge sheet of infinitesimal thickness and E_{eff} is the average of the fields at Si/SiO_2 and inversion-depletion interfaces. Keeping this in mind, the mathematical formule for experimental and analytical approaches are as follows:

Experimental approach: The extraction of μ_{eff} and E_{eff} from simulated I_{DS} of p-channel MOSFETs at low drain biases is based on the following analytical expressions:

$$\mu_{eff} \simeq -\frac{L}{W} \frac{\partial I_{DS} / \partial V_{DS}}{Q_{inv}} \quad (4.1)$$

$$E_{eff} \simeq -\frac{[\eta Q_{inv} + Q_b]}{\epsilon_{si}} \quad (4.2)$$

where η is a constant, $\eta = 1/3$ is for holes and $\eta = 1/2$ is for electrons [22]

$$Q_{inv} \simeq -C_{OX} [V_{GS} - V_{TH} - \frac{V_{DS}}{2}] \quad (4.3)$$

and

$$Q_b \simeq -C_{OX} K_1 \sqrt{\phi_s - V_{BS}} \quad (4.4)$$

In equation (4.1) to (4.4), Q_{inv} is the inversion charge in (*coulomb/cm₂*) and Q_b is the depletion charge in (*coulomb/cm₂*). V_{GS} , V_{DS} and V_{BS} are the gate, drain and backgate (body) biases. L and W are the effective channel length and width, C_{OX} is the gate oxide capacitance (*F/cm₂*), and ϵ_{si} is the dielectric constant of the silicon. V_{TH} , the threshold voltage, is defined as the intercept of the extrapolated

I_{DS} vs V_{GS} curve from its inflection point minus $V_{DS}/2$ [23]. The parameter ϕ_s is the surface potential at the source end of channel when $V_{BS} = 0V$, and K_1 is body factor which is $\sqrt{2q\epsilon_{si}N_A}/C_{OX}$.

Analytical Approach: The exact values of Q_{inv} and Q_b are determined from numerical integration of detailed free charge carrier and charge depleted impurity concentration distributions. The μ_{eff} is determined as:

$$\mu_{eff} = -\frac{I_{DS}}{\frac{W}{L}Q_nV_{DS}} \quad (4.5)$$

and the mobile carrier density Q_n for holes is obtained via numerical integration by:

$$Q_n = -q \int_0^{y_i} p(y)dy \quad (4.6)$$

The drain-to-source voltage (V_{DS}) is assumed to be small and the spatial variation of the local normal electric field, mobility, and electron density is assumed to be small in the horizontal (x) direction. Since the distributions of local electric field and free charge carriers in the inversion layer are very nonlinear, E_{eff} is then determined using the following definition [23][24]:

$$E_{eff} \simeq E_{eff}(x = L/2) = \frac{\int_0^{y_i} E_y(L/2, y)p(L/2, y)dy}{\int_0^{y_i} p(L/2, y)dy} \quad (4.7)$$

where the x coordinate points from source to drain, the vertical (y) coordinate points from the Si/SiO_2 interface into the channel, and y_i is the depth at which n becomes negligible. By carrying out this procedure, the effective mobility of SOI SiGe devices can be calculated.

Since there are two ways to calculate μ_{eff} and E_{eff} , an evaluation is performed to examine the consistency between the μ_{eff} and E_{eff} extracted from I_{DS} using a

set of analytical expressions (equations 4.1 and 4.2) and the μ_{eff} and E_{eff} calculated from distributions of carriers and electric field given by the numerical simulator (equations 4.5 and 4.7). The simulation results indicate those two approaches are consistent, except at very low electric field there are some differences as shown in Fig. 4.1. Therefore, we only use the analytical approach to calculate the effective mobility through out this thesis.

Figure 4.1: Comparison between two approaches to calculate the effective Mobility

4.2 Simulation Setup and Data Analysis Procedure

4.2.1 Introduction to MEDICI

The two dimensional drift-diffusion device simulator MEDICI [25] was employed in this study. MEDICI calculate the two-dimensional distributions of potential and carrier concentrations in a given device, such as a MOSFET or a bipolar transistors, and predicts its electrical characteristics for certain bias conditions. This is done by solving the Poisson's equation and two current continuity equations (hole and electron) self-consistently using a control-volume discretization and the Fermi-Dirac statistics.

MEDICI provides non-uniform and user-controlled triangular simulation grid and it can model any device geometry with both planar and nonplanar surface topography. It also provides the mechanism for auto refinement of the simulation grid during the simulation process. Additional nodes are added according to user-specified quantity such as potential or impurity concentrations. MEDICI also provides Heterojunction Device Advanced Application Module. This module capability provides the means to perform analysis and optimization of semiconductor devices that employ multiple semiconductor materials with varying band structure. Both abrupt and graded heterojunction devices are allowed. All this flexibility of MEDICI makes modeling of complicated structures like SOI $Si_{1-x}Ge_x$ MOSFET devices possible.

4.2.2 Procedures to Setup Simulation

Simulation starts with defining the device geometry and structure, which includes different material regions and their sizes, contact and doping profiles. Based on the geometry and structure, a mesh has to be set up to start the simulation. The mesh is a collection of grids (nodes) for which solutions are calculated. The correct allocation of grid is a crucial issue in device simulation. The number of nodes in the grid has direct influence on the simulation time. We also note that since different regions or parts of a device have very different electric behavior, it is usually necessary to allocate fine grid in some regions and coarse grid in others. It is desirable not to allow the fine grid to spill over into regions where it is unnecessary in order to keep simulation time within reasonable bounds. The meshes for devices (long and short channel), which are studied in this thesis, are presented in Fig 4.2 and Fig. 4.3. Notice that in the channel, interface and junctions have far more grid points than any other places.

The general procedure for device simulation is presented in the Fig. 4.4. Order of definitions and specifications in the Fig. 4.4 is not strictly fixed. The input deck for our simulation with comments for each every step is also shown in APPENDIX A.

One important aspect of the input deck is the model specification. In order for MEDICI to simulate device, certain physical parameters like mobility, electron and hole recombination, band-gap narrowing etc, need to be specified. MEDICI provides different models for these physical quantities, and we have to make selections ac-

Figure 4.2: The mesh for long channel device

cording to our needs. Selection of specific models will determine a set of phenomena that can be analyzed in a given device. We have to be careful when interpreting of simulation results and keep in mind model limitations.

Since the objective is to study the effective mobility of SOI $Si_{1-x}Ge_x$ p-MOSFET, the models in the MEDICI input deck are specified as follows:

1. CONMOB—Doping level dependent mobility model.
2. PRPMOB—Perpendicular electric field reduction dependent mobility model, and other models also used in the simulation which are discussed in section 4.4.
3. FLDMOB—Carrier velocity and horizontal electric field dependent mobility model.

Figure 4.3: The mesh for short channel device

4. CONSRH-SRH recombination with concentration dependent lifetime model
5. AUGER—Model for Auger recombination.
6. BGN—Model for band-gap narrowing in heavily doped regions.

Detailed explanations and applications of above listed model can be found in [25]. SiGe layer automatically has a reduced value of bandgap, depending on Ge mole fraction. The mobility models are discussed in section 4.4.

Figure 4.4: General Procedure for Simulation in MEDICI

4.3 Mobility Model for the $Si_{1-x}Ge_x$ Channel

4.3.1 Modeling the Mobility in MEDICI

Carrier mobilities in semiconductor material are determined by a large variety of physical mechanisms. Electrons and holes are scattered by thermal lattice vibrations, ionized impurities, neutral impurities, vacancies, interstitials, dislocations, surfaces and electrons and holes themselves. Unfortunately, many of these mechanisms, especially their interactions, are extremely complicated and hence difficult to model [26]. In MEDICI, a dozen of mobility models are available, which model the physical mechanisms like ionized impurities, carrier to carrier scattering, surface scattering, velocity saturation etc. In general, modeling the mobility in MEDICI

starts with a bulk mobility, which is then reduced by the electric field (both vertical and parallel electric field). The simulator also takes into consideration different scattering mechanisms e.g. surface scattering, and makes necessary reduction of bulk mobility. The following is the description of this process.

Assume that we start with the bulk mobility, which we term μ_n and μ_p (subscripts n, p denote electrons or holes, respectively). In the low electric field, the fundamental process for carrier scattering in a pure crystal is the interaction with thermally generated vibrations of the atoms of the crystal. These lattice vibrations are a function of temperature. They yield a certain value for silicon bulk mobility.

The bulk carrier mobility is further reduced in the semiconductor devices by the scattering mechanisms in low field. The first scattering mechanism to be considered is ionized impurity scattering. It is a function of the lattice temperature and the local concentration of ionized impurities.

In conjunction with ionized impurity scattering one should deal with neutral impurity scattering. However, since the impurities are almost completely ionized at temperatures above 77K this effect is ignored. Another scattering mechanism which one should, in principle, take into account is carrier-carrier scattering. However, for our MOSFET devices it is of minor importance.

The next scattering mechanism is termed surface scattering. The effect is of fundamental importance for MOS transistors since they contain a rough Si/SiO_2 interface. Theoretically, surface scattering is comprised of many different mechanisms like surface roughness scattering, scattering by interface charges and scattering by surface phonons. Although the application to MOS structures has received a

great deal of attention, the problem associated with conduction at surfaces have not been investigated as deeply as one would expect. Therefore, all models which are presently used have been constructed on a largely empirical basis with hope that they reflect the main experimental findings as well as possible. Nevertheless, there exist physical reasoning to support the empirical basis.

In the high field, the phenomenon we need to consider is the saturation of the drift velocity. This effect has to be accounted for by the reduction of the mobility since the magnitude of the drift velocity is the product of the mobility and the force which drives the carriers i.e. the electric field.

The mobility which takes into account the lattice scattering, ionized impurity scattering, surface scattering, velocity saturation etc, is the **local** mobility which we use for the two-dimensional simulation of MOS device behavior. Detailed procedures to select mobility models for using MEDICI are discussed in [25].

4.3.2 Modeling Mobility in $Si_{1-x}Ge_x$ channel

For SOI $Si_{1-x}Ge_x$ p-MOSFET, the channel mobility is improved by confining holes in a buried SiGe well. Improvement in channel mobility comes from two factors: reduction of carrier scattering at Si/ SiO_2 interface by moving channel away of Si/ SiO_2 interface, and higher in-plane hole mobility of biaxially strained SiGe layer.

In-plane hole mobility of a strained SiGe layer has been calculated, and has been shown to be significant higher than that of bulk Si as shown in table 4.3.2 [17]. This

is because the biaxial strain lifts valence-band degeneracy between heavy and light hole bands, and the spin-orbit band is lowered in energy. This reduces interval scattering. Furthermore, in-plane effective mass of strained SiGe is smaller than that of Si. Both these effects improve mobility at low and high fields.

Table 4.1: The in-plane hole drift mobility for strained $Si_{1-x}Ge_x$ as a function of Ge fraction with doping concentration less than $5 \times 10^{16} cm^{-3}$

Ge Fraction (%)	Silicon	5%	10%	15%	20%	25%	30%
Mobility (cm^2/Vs)	450	575	680	780	900	1000	1100

Hole confinement in $Si_{1-x}Ge_x$ well PMOS, however, depends strongly on the applied gate bias. At a higher gate overdrive (*higher* $|V_{GS} - V_{TH}|$, where V_{GS} is the gate voltage and V_{TH} is the threshold voltage), holes at the Si/ SiO_2 interface dominate channel conduction and the device behaves more like a conventional surface-channel Si device.

As pointed out above, the two main physical characteristics of strained $Si_{1-x}Ge_x$ are band-gap narrowing and hole mobility enhancement. The band-gap narrowing is already modeled by the Heterojunction Device Advanced Application Module of MEDICI. The hole mobility in MEDICI is assumed the same as in silicon, which means no hole enhancement. This would not give correct simulation results in all cases. Therefore, we need to modify the parameters of mobility model in strained $Si_{1-x}Ge_x$. The easiest way to model the strained $Si_{1-x}Ge_x$ channel is to make the channel have constant hole mobility as long as the holes are in the channel. When the

holes are away from the channel, then they should be treated as rest of the silicon. This is justifiable since $Si_{1-x}Ge_x$ channel is very thin, and the holes are either inside the channel or scatter out of the channel. We found out that the constant strained $Si_{1-x}Ge_x$ mobility of $250cm^2/Vs$ gives best results when compared with published data [20]. Several mobility models have been tested in our study, and they will be discussed in detail.

4.4 Carrier Mobility Models

Modeling the carrier mobility for Si bulk p-MOSFET has been studied for decades, and many models have been developed. All models which are presently used have been constructed to fulfill one or more of the following conditions:

1. Fully empirical based with aim to reflect the main experimental findings as well as possible, and also with some physical reasonings to support the empirical basis [26].
2. Semi-empirical basis with fundamental physical support, but still using parameters to fit the experimental findings as accurately as possible [27].
3. Suitable to be implemented in a device simulator of non planar devices, and still of reasonable size in terms of CPU time, which in turn requires that the mobility model be expressed in terms of “local” function. By local function it is meant any single-valued and possibly continuous function of any variable, such as electric potential, electric field, carrier concentration, etc, defined at

any grid point of semiconductor region [27].

4. Not functions of the distance between a generic grid point and the semiconductor/insulator interface¹.

The model for carrier mobility in silicon inversion layers and in the bulk of the semiconductor is the one which mostly affects the accuracy of the results of the terminal current calculation in two- and three-dimensional MOSFET simulation programs. In the following, we will review several mobility models which are used in this study, and modify them to model the strained $Si_{1-x}Ge_x$ channel.

4.4.1 Lombardi Mobility Model (LSMMOB)

A semi-empirical model for carrier mobility in silicon inversion layers is presented by Lombardi [27]. The model, strongly emphasizing the “locality”, “continuity” and “physical” basis of mobility function, is set up in terms of a simple Matthiessen’s rule and provides a careful description of MOSFET operation in a wide range of gate electric fields, channel impurity concentrations and temperatures. The carrier mobility model is based on the following Matthiessen’s rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \quad (4.8)$$

¹Functions of the distance between a generic grid point and the semiconductor/insulator interface is not acceptable in a general purpose device simulator as discussed by Lombardi [27]. for example, if several semiconductor-insulator interfaces are present—as in a silicon-on-insulator structure—several distances are associated to every grid point of the semiconductor region. As a consequence, the carrier mobility, in the general case, is a multivalued function. The same situation occurs if a single, nonplanar semiconductor-insulator interface is present. On the other hand, the discontinuity introduced by some “degradation factor”, reducing the carrier mobility only at semiconductor-insulator interfaces, may cause results of the terminal current calculation strongly dependent on the grid size.

where μ_{ac} is the carrier mobility limited by the scattering with surface acoustic phonons, μ_b is the carrier mobility in bulk silicon, and μ_{sr} is the carrier mobility limited by surface roughness scattering.

In the Matthiessen-like rule expressed by (4.8), the various scattering mechanisms limiting the total carrier mobility are neatly separated. There are three advantages as pointed out by Lombardi [27]:

1. Model parameters pertaining to a specific scattering mechanism can be extracted from experimental data taken in appropriate experimental conditions where that specific scattering mechanism is known to dominate the carrier mobility.
2. The initial estimate of the model parameters, in fitting procedure, may be obtained from approximate first-principles considerations and material properties of silicon.
3. More scattering mechanism may be easily included in the model without altering the structure of equation 4.8.

The mathematic expression of Lombardi model for holes are as follows:

A. Surface Acoustic Phonons — $\mu_{ac,p}$

$$\mu_{ac,p}(E_{\perp}, T) = (B_p \frac{T}{E_{\perp}} + C_p \frac{N_{total}^{\beta_p}}{E_{\perp}^{1/3}}) \frac{1}{T} \quad (4.9)$$

Where B_p , C_p , and β_p are fitting parameters, their values can be found in [25]. N_{total} is the total local concentration, and T is temperature and $E_{\perp}$ is perpendicular electric field.

B. Bulk Mobility — $\mu_{b,p}$

$$\mu_{b,p} = \mu_{0,p} \exp\left(\frac{P_c}{N_{total}}\right) + \frac{\mu_{max,p}}{1 + (N_{total}/C_{r,p})^{\alpha_p}} - \frac{\mu_{l,p}}{1 + (C_{s,p}/N_{total})^{\gamma_p}} \quad (4.10)$$

where

$$\mu_{max,p}(T) = \mu_{2,p} \left(\frac{T}{300}\right)^{-\zeta_p} \quad (4.11)$$

and $\mu_{0,p}$, $C_{r,p}$, α_p , $C_{s,p}$, $\mu_{l,p}$, $\mu_{2,p}$, ζ_n and ζ_p are fitting parameters, their values can be found in [25].

C. Surface Roughness — $\mu_{sr,p}$

$$\mu_{sr,n}(E_{\perp}) = \frac{\delta_p}{E_{\perp}^2} \quad (4.12)$$

where δ_n and δ_p are fitting parameters, their values can be found in [25].

By using the default parameters provided by MEDICI, the relative contributions of each components of Lombardi mobility model to the “local” effective mobility are illustrated in Fig. 4.5. From Fig. 4.5, the “local” effective mobility at low field $E_{\perp}$ is mainly determined by surface acoustic phonons, but at high fields it is the surface roughness that dominates.

Therefore, the modeling of strained $Si_{1-x}Ge_x$ channel is very simple. We can properly select the parameters so that $\mu_{ac,p}$ and $\mu_{sr,p}$ are much greater than $\mu_{b,p}$ in the strained $Si_{1-x}Ge_x$ channel region. $\mu_{b,p}$ then dominates in the region, and the total μ is nearly constant. The magnitude of $\mu_{b,p}$ is determined by $\mu_{max,p}$ which can be easily set to any value we need.

Figure 4.5: The effects of components of Lombardi mobility model on the local mobility

4.4.2 Yamaguchi Mobility Model (PRPMOB)

Drift velocity in bulk Si saturates in the high field region. In order to simulate the $v-E$ relation, several field-dependent mobility models have been proposed [28], [29]. Functions which vary as E^{-1} in a high field, for example, $\mu_0\{1 + (E/E_c)^\beta\}^{-1/\beta}$, piece-wise linear approximation, etc., are frequently used. These are empirical but useful as design aids.

Thornber [30] theoretically studied the relation of drift velocity to low-field mobility and high-field saturation velocity for bulk Si, based on the Boltzmann transport equation. The following are interesting results under uniform field conditions and in steady state:

1. If the rates associated with all scattering processes are increased by the same

numerical factor, then the saturation velocity is unaltered.

2. If the magnitude of the momentum is scaled so as to alter the saturation velocity, then the mobility is left invariant.

Based on above findings, the low-field mobility and saturation velocity could serve as independent parameters in discussing $v - E$ relation. Also, the parameters, measured and determined under uniform field conditions, can be used under nonuniform field conditions.

There are significant difference between the bulk Si and MOSFET, when the drift velocity is studied. A MOSFET fundamentally operates under the influence of two external forces. One is the gate field which induces carriers in the inversion layer and constructs a narrow channel. The other is the drain field which transports carriers from the source to the drain. These two fields must be defined regarding $v - E$ relation. Yamaguchi, based on the theoretical study of Thornber [30], presented the $v - E$ relation for the MOS interface as follows:

$$v_d = \mu(N, E_{GS}) E_{DS} f(N, E_{GS}, E_{DS}) \quad (4.13)$$

where E_{DS} and E_{GS} are electric field to source for drain and gate respectively. $\mu(N, E_{GS})$ is low field mobility, which consists of a factor with the impurity density dependence and a factor that is dependent on the gate field E_{GS} . The last term $f(N, E_{GS}, E_{DS})$ expresses velocity saturation effect which is not our main concern in this thesis. Detailed discussion of this term can be found in [21].

Effects of the surface quantization and the surface roughness scattering on the low-field mobility $\mu(N, E_G)$ can be phenomenologically treated as a dependence on

the gate field. As an empirical expression which fits experimental results very well, the gate field dependence is assumed to be of the following form [31]

$$g(E_{GS}) = (1 + \alpha E_{GS})^{-1/2} \quad (4.14)$$

The low drain-field surface mobility is then expressed as

$$\mu(N, E_{GS}) = \mu(N) \times g(E_{GS}) \quad (4.15)$$

Equations (4.14) and (4.15) are an empirical expressions, but they fit well the experimental data. This model is also known as Yamaguchi mobility model. the present mobility model can be applied to any range of gate and drain field. In the strained $Si_{1-x}Ge_x$ channel, in order to make the channel have constant mobility, we need to choose α small enough to get rid of gate field E_G dependence.

4.4.3 Enhanced Surface Mobility Model (SRFMOB)

The enhanced surface mobility model, which is provided by MEDICI, takes into account phonon scattering, surface roughness scattering, and charged impurity scattering. This model is empirical by nature, and can be described by the following expressions:

$$\frac{1}{\mu_{eff,p}} = \frac{1}{\mu_{p1}} \left(\frac{E_{eff\perp,p}}{10^6} \right)^{k_{1p}} + \frac{1}{\mu_{p2}} \left(\frac{E_{eff\perp,p}}{10^6} \right)^{k_{2p}} + \frac{1}{\mu_{p3}} \left(\frac{E_{eff\perp,p}}{10^6} \right)^{k_{3p}} \quad (4.16)$$

This model is dependent on the perpendicular electric field **only** at the Si/ SiO_2 interface. Hence, the simulation results is dependent on the grid. By adjusting the spacing of grid, the value of μ_{eff} can be changed.

4.4.4 HP Mobility Model (HPMOB)

This is a model developed at Hewlett-Packard, and it takes into account dependence on both parallel and perpendicular electric fields relative to the direction of current flow. The expressions for the model are as follows:

$$\mu_p = \frac{\mu_{\perp,p}}{\sqrt{1 + \frac{(\frac{\mu_{\perp,p} E_{\parallel,p}}{V_{cp}})^2}{\frac{\mu_{\perp,p} E_{\parallel,p}}{V_{cp}} + G_p} + (\frac{\mu_{\perp,p} E_{\parallel,p}}{V_{sp}})^2}} \quad (4.17)$$

The expression for $\mu_{\perp,p}$ is given by

$$\mu_{\perp,p} = \frac{\mu_{po}}{1 + \frac{E_{\perp,p}}{E_p}} \quad (4.18)$$

Where V_{cp} , G_p , V_{sp} and E_p are fitting parameters, and the default values can be found in MEDICI [25]. Using this model in the strained $Si_{1-x}Ge_x$ channel, parameters can be choose to ensure that μ_p is constant in that region. This can be achieved by setting all the fitting parameters very large.

4.5 Simulation Results

By using above discussed mobility models, the long channel and short channel devices presented in chapter 3 have been simulated by using two-dimensional device simulator MEDICI. Note that the effective mobility is our concern in this section. The simulation results are presented in the following sections. In general, all simulation results indicate that SiGe channel device can significantly improve the effective mobility up to 100% over the bulk devices. Detailed discussion about the agreement

and disagreement with published experimental data are presented in the following sections.

4.5.1 Grid Sensitivity of Mobility Model

The above reviewed mobility models can be classified into two categories:

1. Mobility model, i.e. Enhanced Surface Mobility Model (SRFMOB2), is dependent on transverse electric field **only** at the Si/SiO_2 interface.
2. Mobility models, i.e. Lombardi Mobility Model (LSMMOB), Yamaguchi Mobility Model (PRPMOB) and HP Mobility Model (HPMOB), are dependent on vertical electric field **anywhere** in the device.

Mobility model in the first category degrade the mobility of the carriers only at the Si/SiO_2 interface, hence, the current reduction is dependent on the number of carriers associated with the nodes at the Si/SiO_2 interface. In order to account for all carriers located at the nodes of Si/SiO_2 interface, the vertical grid spacing has to be setup larger than the inversion layer width. This makes results obtained by using SRFMOB2 not only dependent on grid (spacing) but also on the gate bias since this gate bias determines the vertical distribution of carriers and the width of the inversion layer. Given these uncertainties, it should be avoided and used only as a last resort. Results in Fig. 4.6 indicates a large variation of effective mobility μ_{eff} with grid. The best fit requires grid spacing of 75Å. PRPMOB model results are taken as a reference due to its extensive experimental verification and insensitivity to the grid spacing.

Figure 4.6: Effective hole mobility vs effective transverse field for Si and $\text{Si}_{0.7}\text{Ge}_{0.3}$ devices using SRFMOB2 mobility model. Three grid spacings: 25, 30 and 75Å, at top Si/SiO_2 interface are used

Mobility models in category two depend on the vertical electric field and are grid independent. Therefore, the results are more consistent and more reliable than the model in category one.

4.5.2 The Long Channel SOI SiGe p-MOSFET

When SRFMOB2 is applied to SiGe device without any modification, μ_{eff} from Fig. 4.7 is obtained. When compared with experiments in [6], the improvement is already large enough to account for the experimentally observed improvements of 40–90%. Therefore, in this model the removal of carriers from the interface can, on its own, account for the observed μ_{eff} increase.

Category two models are essentially independent of where the hole flow occurs.

Figure 4.7: Hole effective mobility in $\text{Si}_{0.7}\text{Ge}_{0.3}$ p-channel SOI MOSFET using SRF-MOB2 and $75\text{\AA}$ grid spacing.

For any change in μ_{eff} to occur they require that the low-field mobility μ_0 inside the SiGe channel be increased. In strained SiGe μ_0 is expected to roughly double [17]. The results for μ_{eff} with doubled μ_0 in SiGe channel are given in Fig. 4.8. Compared with experimental results given by [6] which indicates that mobility in the channel is $181\text{cm}^2/\text{Vs}$, the results in Fig. 4.8 are too high for low field. But Nayak and et al [6] also pointed out that their device is based on SIMOX which has low mobility due to the presence of a large number of interface states. Compared with bulk Si device, the μ_{eff} for SiGe device is 40% to 90% larger which is consistent with results reported by Nayak et al [6] and Garone [11]. Unlike other models, HPMOB exhibits improvement even at very large effective fields E_{eff} when holes are predominantly at the top interface and μ_{eff} is expected to revert to Si values;

experimental data, however, is lacking in this regime. Even though the effective mobility seems correct with the double the “local” mobility in the channel, but The results for transconductances g_m are presented in Fig. 3.5. The category two models (only PRPMOB is shown) show two peaks that are associated with conduction along bottom and top interface of SiGe channel. This behavior has not been observed in experiments. To correct this it is necessary to make the mobility in SiGe channel bulk-like, by, e.g, neglecting the mobility dependence on transverse field inside SiGe channel. Also, no increase in low-field mobility is needed. μ_{eff} and g_m for the this case are shown in Fig. 4.8 under PRPMOB* label. As expected, g_m is virtually the same for SRFMOB2 and PRPMOB*.

Figure 4.8: Hole effective mobility in $\text{Si}_{0.7}\text{Ge}_{0.3}$ p-channel SOI for various non-localized, $E_{\perp}$ dependent models.

4.5.3 The Short Channel SOI SiGe p-MOSFET

Unlike the long channel device, the simulation of short channel device is based on the fixed SiGe channel mobility of $250\text{cm}^2/\text{V}\cdot\text{s}$. In Fig. 4.9, with the use of LSMMOB mobility model, the simulated effective mobility μ_{eff} is compared with experimental data in [20]. The results are reasonably close given the condition that experimental data is based on a very long channel (100μ) and the threshold voltage is unknown.

Figure 4.9: Simulated and experimental hole effective mobility with graded SiGe channel.

In Fig. 4.10, category two models are used on the short channel **bulk** SiGe p-MOSFET. Compared with bulk p-MOSFET, the effective mobility presents more than 100% enhancement and over a wide range of E_{eff} . This is due to graded channel and p^+ spike (more detailed discussion in chapter 5). We also noticed that PRPMOB

and LSMMOB give close effective mobility, and HPMOB gives substantially higher value.

Figure 4.10: Hole effective mobility in bulk graded SiGe p-channel MOSFET.

In Fig. 4.11, category two models are used on the short channel SOI SiGe p-MOSFET. The simulation results are similar to Fig. 4.10. Compared with SOI p-MOSFET, the effective mobility presents more than 100% enhancement over a wide range of E_{eff} . This is due to graded channel and p^+ spike. PRPMOB and LSMMOB give almost identical effective mobility, while HPMOB also gives values very close to PRPMOB and LSMMOB ones.

In Fig. 4.12, LSMMOB model is used to make a comparison between different devices. The SiGe device which include bulk SiGe p-MOSFET and SOI SiGe p-MOSFET have about 100% effective mobility improvement over both SOI

Figure 4.11: Hole effective mobility in SOI graded SiGe p-channel MOSFET.

p-MOSFET and bulk p-MOSFET. This improvement has been experimentally observed [11].

Figure 4.12: Comparison of hole effective mobility among bulk p-channel MOSFET, SOI p-channel MOSFET, bulk SiGe p-channel MOSFET and SOI SiGe p-channel MOSFET, and the SiGe channel are graded.

Chapter 5

DESIGN PARAMETERS AND THEIR INFLUENCE ON EFFECTIVE MOBILITY

In chapter 4 the effective mobility of long and short channel devices with fixed device parameters were discussed along with the mobility modeling issues. We will carry further the study of effective mobility in this chapter by looking at some of the design parameters which will influence the effective mobility of the device.

One of the SOI SiGe MOSFET design objectives is to maximize the device transconductance. This can be accomplished by maximizing the number of high mobility holes confined to the SiGe channel while minimizing the density of low mobility holes which flow at Si/SiO_2 interface. The critical design parameters are the choice of gate oxide thickness, silicon cap thickness, gate material, threshold voltage, $Si_{1-x}Ge_x$ profile and back-gate voltage. Given the interest in effective mobility, we are going to study the influence of silicon cap thickness, $Si_{1-x}Ge_x$ profile and back-gate voltage on the effective mobility. The impact of these design parameters on device performance is investigated with the use of two-dimensional device simulation program MEDICI. All simulations discussed in this chapter are performed for short channel device with n^+ polysilicon gate which was discussed in Chapter 3.

Also keep in mind that SiGe channel (local) mobility is kept on constant with value of $250\text{cm}^2/\text{Vs}$ and **independent** of mole fraction of SiGe channel. Therefore, all the results in this chapter address only the issue of hole confinement.

5.1 Influence of Silicon Cap Thickness on μ_{eff}

To maximize the gate-to-channel capacitance and hence increase the SOI SiGe p-MOSFET transconductance, it is important to minimize the thickness of the silicon cap. MEDICI simulations indicate that decreasing the Si cap thickness increases the hole confinements in the SiGe channel. This is illustrated in Fig. 5.1 where the integrated hole density along the y-axes is plotted. For $t_{CAP} = 25\text{\AA}$, nearly all the holes are confined in the SiGe channel even with gate voltage $V_{GS} = -2.0\text{V}$, while only three fourths of holes are confined in the SiGe channel with $t_{CAP} = 50\text{\AA}$.

The effective mobility μ_{eff} is shown in Fig. 5.2 which demonstrates that the effective mobility μ_{eff} for $t_{CAP} = 25\text{\AA}$ is greater than that of $t_{CAP} = 50\text{\AA}$. This is because the hole confinement for $t_{CAP} = 25\text{\AA}$ is better than that of $t_{CAP} = 50\text{\AA}$. The improved transconductance for $t_{CAP} = 25\text{\AA}$ can be seen from Fig. 5.3. In general, we can conclude that a thin Si cap results in better performance of SOI SiGe p-MOSFET. However, as pointed out by Verdonckt-Vandebroek and et al in [20], several trade-offs affect SOI SiGe p-MOSFET's with thin Si cap. A thin Si cap layer does not permit a thermal re-oxidation of the source and drain areas after polysilicon gates are etched. In addition, since the current flows less than $25\text{\AA}$ away from the gate oxide, interface scattering will degrade the hole mobility. Conversely,

Figure 5.1: The hole confinement for SOI SiGe p-MOSFET with $t_{CAP} = 50\text{\AA}$ and $t_{CAP} = 25\text{\AA}$ with $V_{DS} = 0.05V$, $V_{GS} = 2.0V$ and channel width $80\text{\AA}$.

with a thin Si cap, the holes in the SiGe channel flow closer to the gate and the channel-to-gate capacitance increases. Therefore, the Si cap thickness needed to optimize the transconductance is determined by mobility/capacitance tradeoff.

5.2 Influence of $Si_{1-x}Ge_x$ Profile on μ_{eff}

Hole confinement in the SiGe channel is also dependent on the shape of the SiGe channel and Ge mole fraction. To maximize the hole concentration in the SiGe channel and insure adequate confinement up to high gate voltages, a large valence band discontinuity at the top Si/SiGe heterojunction is required, but pseudomorphic epitaxial SiGe films are highly strained and must remain stable throughout device fabrication. This places a limitation on a $Si_{1-x}Ge_x$ thickness that can be

Figure 5.2: The effective mobility for SOI SiGe p-MOSFET with $t_{CAP} = 50\text{\AA}$ and $t_{CAP} = 25\text{\AA}$.

grown without the relaxation of compressive stress. This maximum thickness is called critical thickness and is inversely proportional to the germanium dose (dose is integrated Ge concentration). On the other hand, increased germanium fraction increases the valence band discontinuity and improves the hole confinement. For high gate voltage, where we want to improve the hole confinement, the majority of the holes is at the front $Si/Si_{1-x}Ge_x$ interface. In order to get the maximum from two conflicting requirements on Ge dose, a graded $Si_{1-x}Ge_x$ channel has been introduced [20][19]. It has a large germanium mole fraction on top and small one at bottom to keep the dose under critical value. In addition, introducing the graded channel creates the following benefits:

1. A quasi-electric field is induced in the channel, and it is directed from the sub-

Figure 5.3: The transconductance for SOI SiGe p-MOSFET with $t_{CAP} = 50\text{\AA}$ and $t_{CAP} = 25\text{\AA}$.

strate toward the gate, thereby pushing the holes towards the top $Si/Si_{1-x}Ge_x$ interface, where the Ge mole fraction and mobility are the highest. This results in a better gate control and steeper turn-on at low gate voltage. Obviously, in order to improve the transconductance of the MOSFET, silicon cap and gate oxide thickness must be minimized in order to increase the gate-channel capacitance. This also increases the number of holes in the channel for the same gate voltage.

2. In addition to improving mobility, the large Ge mole fraction near the top of the channel provides a larger barrier in the path of high energy holes that try to transfer from the SiGe channel to Si cap layer. The expected outcome is a performance leverage over a wider range of gate voltages as compared to Si

or uniform channel SiGe devices, which are demonstrated in Fig. 5.4 and Fig. 5.5.

Figure 5.4: The effective mobility for SOI SiGe p-MOSFET with graded channel from 50% at top to 0% at bottom of SiGe channel

Both uniform and graded channel SOI SiGe p-MOSFET with different mole fractions have been simulated. The LSMMOB model has been used for all of the simulations with SiGe channel mobility set at $250\text{cm}^2/\text{Vs}$. All the device parameters are the same as indicates in the chapter 3. There are three kinds of comparisons which will be presented here:

1. Comparing devices with different uniformly distributed Ge mole fractions in the channel.
2. Comparing a device with a graded channel with a device of the same average Ge mole fraction but uniformly distributed.

Figure 5.5: The effective mobility for SOI SiGe p-MOSFET with graded channel from 45% at top to 25% at bottom of SiGe channel

3. Comparing devices with different grading.

Uniform doped channel: There are three uniform doped channel devices with Ge mole fraction 25%, 35% and 45% respectively. The results for these devices have been illustrated in Fig. 5.6, and they indicate that the channel with 35% Ge concentration has better effective mobility μ_{eff} than that of the channel with 25% and 45% Ge concentration, which is consistent with theoretical analysis and experimental findings [20][19].

Graded channel vs Uniform doped channel: Two SiGe channel grading schemes, i.e. graded profile with 45% Ge at the top and 25% at bottom (hereafter, we call it grading A), and graded profile with 50% at top and 0% at bottom (hereafter, we call it grading B), have been simulated. The simulation results are presented in

Figure 5.6: The effective mobility for SOI SiGe p-MOSFET with uniform doped channel, the Ge mole fraction are 25%, 35% and 45% respectively.

Fig. 5.5 and , Fig. 5.4. Notice that the average Ge mole fraction for grading A and grading B are 35% and 25% respectively. Fig. 5.5 demonstrates that graded channel with grading A have significantly improved effective mobility μ_{eff} over the uniform doped channel with 35% Ge mole fraction. The same is true for graded channel with grading B.

Graded channel vs graded channel: The grading A channel and grading channel B are also compared with each other. Fig. 5.7 demonstrates this comparison. The results indicate that the SiGe channel with graded profile of grading B has much better effective mobility than the device with SiGe channel of graded profile of grading A even though the average Ge mole fraction of graded profile of grading B is smaller. This further confirms that higher Ge mole fraction at top and large

gradient of Ge mole fraction result in much better hole confinement.

Figure 5.7: The effective mobility for SOI SiGe p-MOSFET with two different graded channel i.e. 45% to 25% graded channel and 50% to 0% graded channel

Transconductance: The transconductances of the devices with above mentioned graded channels are presented in Fig. 5.8. The results demonstrate that transconductance of the device with grading B is somewhat smaller than the device with grading A, which also demonstrates the trade off between gate capacitance and mobility.

5.3 Influence of Back-Gate Voltage on μ_{eff}

The issue of back-gate bias is important because p-MOS in SOI CMOS circuit may be at constant back-gate bias, for example, in SOI inverter, the back gate (the underlying silicon wafer) is common to both n- and p-type devices and it is usually grounded. Hence, the back-gate voltage is 0V for the n-channel device, but

Figure 5.8: The transconductance for SOI SiGe p-MOSFET with two different graded channel i.e. 45% to 25% graded channel and 50% to 0% graded channel

it is equal to $-V_{DD}$ for the p-channel transistor (the source voltage being always used as a reference). As a consequence, SOI p-channel transistors have usually to be designed for operating with a back-gate bias. Therefore, one of the major differences between SOI and bulk design is difference in body effect and in body/back gate bias conditions. The body effect in thin film SOI devices, which is dependent on back-gate bias, is significant if we are to determine performance of a circuit using this SOI CMOS technology. Hence, to understanding the behavior of effective mobility μ_{eff} with respect to back-gate bias is very important. For different back-gate bias (0V, -2.5V, and -5V), the effective mobility μ_{eff} are obtained from MEDICI and simulation results are presented in Fig. 5.9. Fig. 5.9 reveals that low field effective mobility μ_{eff} decreases with decreasing the back-gate bias, but the changes are

small; high field μ_{eff} is even less affected.

Figure 5.9: The influence back-gate bias on effective mobility of SOI SiGe p-MOSFET

Chapter 6

CONCLUSIONS

6.1 Main results

In this thesis, two-dimensional numerical simulation was used to study and model effective channel mobility of SOI SiGe p-MOSFET. Using the device simulator MEDICI, a long channel device and short channel device were constructed by following the devices presented by Nayak and et al [6] and Verdonckt-Vandebroek et al [20], respectively. Specifically, by using these two devices, we have fulfilled following two objectives:

1. Studying and modeling effective carrier mobility (μ_{eff}) of SOI SiGe p-MOSFET.

The issues include the modeling of the mobility in the SiGe channel, and investigation of the suitability of mobility models provided by simulator MEDICI for studying SOI SiGe p-MOSFET. There are four mobility models that are involved in this study: 1) Enhanced surface mobility model (SRFMOB2); 2) Mobility dependence on perpendicular field (PRPMOB); 3) Lombardi surface mobility model (LSMMOB); 4) Hewlett-Packard mobility model (HPMOB).

2. Investigating the influence of design parameters on effective carrier mobility (μ_{eff}) of SOI SiGe p-MOSFET. These parameters include the Si-cap thickness, Ge profile (mole fraction of Ge in $Si_{1-x}Ge_x$ and the manner of grading in the channel) and back-gate bias.

Based on the mobility model and the method of simulation explained in previous chapters, we conclude that:

- Modeling the mobility in SiGe channel of p-MOSFET can simply be treated like a bulk silicon with mobility $250cm^2/V - s$. Simulation reveals this treatment generates reasonably good effective mobility μ_{eff} when compared with experimental results.
- Mobility models used in this study can be classified into two categories; Category one is the mobility model (SRFMOB2) that depends on transverse electric field only at Si/SiO_2 interface. Therefore, the effective mobility is a function of grid spacing at Si/SiO_2 interface. When this model is used, special cautions should be paid to this grid spacing dependence in order to avoid incorrect modeling. Category two consists of the mobility models (PRPMOB, LSMMOB and HPMOB) that depend on transverse electric field anywhere in the device. Simulation proves that PRPMOB and LSMMOB produce very good results and are insensitive to the grid spacing. HPMOB gives slight over-estimation of effective mobility μ_{eff} .
- Study reveals that graded SiGe channel presents nearly 100% improvement of effective mobility μ_{eff} for p-MOSFET over its bulk counterpart. This im-

provement is sustained up to gate voltage of 2.5 V. Simulation also indicates that better improvements for effective mobility μ_{eff} require higher Ge concentration at the top of SiGe channel with steeper grading.

- Silicon cap thickness can significantly influence the effective mobility μ_{eff} . In general, thinner silicon caps result in better effective mobility μ_{eff} , but the thickness is limited by physical limitations of manufacturing process, and the trade-off with surface scattering.
- The influence of back-gate bias on effective mobility μ_{eff} is not significant, hence, SOI SiGe MOSFET is well suited to building CMOS circuits.

6.2 Suggestions for further Study

This study focus on effective mobility of SOI SiGe p-MOSFET as well as some related design issues, which are only some of the aspects of SOI SiGe p-MOSFET operation and design and there are many things to be done. Among them are:

- *Further Study of μ_{eff}* : Further study of μ_{eff} with more complete and more readily available experimental data. The scope and the final results of this thesis were limited by a lack of reliable and systematic data.
- *Small Signal Analysis*: Figures of merit for Steady-state d.c (transconductance, subthreshold characteristics and etc) along can not be sufficient describe device performance; Study presented in thesis should be extended to steady-state small-signal a.c analysis.

- *Deep-Submicrometer Channel Design for SOI SiGe MOSFET:* As we move to higher and higher frequencies of operation, this requires even short channel length. A careful examination of the design tradeoffs focusing on short-channel effect, drain-induced barrier lowering, effective channel mobility and transconductance in the deep-submicrometer region is necessary.
- *Channel Profile Engineering:* In this thesis, effective inversion hole mobility was studied. Channel profile engineering study should be extended to maximize effective mobility while maintaining acceptable short-channel effects and threshold voltage.
- *Low Voltage Operations:* Supply voltage reduction from 5V to 3V is mainstream trend, and further reduction is imminent. Circuit operation at low voltages helps to circumvent several device level problems, such as device breakdown attributed to impact ionization and short channel effects. Low voltage operation also introduces performance reduction related concerns such as the necessary and problematic reduction and control of threshold voltages, reduction in drive currents, and increase in proportional effects of parasitic capacitances. Hence, to study the relationships between performance criteria and various design parameters for low voltage operation is essential for designing better SOI SiGe MOSFET.

Appendix A

The MEDICI Input Deck for Short Channel Device Simulation

The following MEDICI input deck is to generate the mesh of 0.25μ device.

```
COMMENT    DEVICE DEFINITION
COMMENT    LCH=CHANNEL LENGTH

ASSIGN     NAME=LCH N.VALUE=0.25

COMMENT    *****
COMMENT    SPECIFY SOME VARIABLES
COMMENT    =====
COMMENT    TSI=THICKNESS OF THE SILICON IN TOTAL
COMMENT    NDOP= SUBSTRATE DOPING LEVEL
COMMENT    JUL= SOURCE AAND DRAIN JUNCTION LENGTH

ASSIGN     NAME=NDOP N.VALUE=1.0e17
ASSIGN     NAME=TSI  N.VALUE=1.0
ASSIGN     NAME=JUL  N.VALUE=0.11
ASSIGN     NAME=XDOP N.VALUE=0.09

COMMENT    *****
COMMENT    SPECIFY A RECTANGULAR MESH (X AND Y)
COMMENT    =====
MESH       SMOOTH=1 OUT.FILE=pMOS.ngate.sige.mesh
X.MESH     WIDTH=0.25 H1=0.08 H2=0.02
X.MESH     WIDTH=0.15 H1=0.05 H2=0.04
X.MESH     WIDTH=@XDOP H1=0.04 H2=0.01
X.MESH     WIDTH=@LCH H1=@LCH/60 H2=@LCH/60 H3=@LCH/8
X.MESH     WIDTH=@XDOP H1=0.01 H2=0.04
X.MESH     WIDTH=0.15 H1=0.04 H2=0.05
```

```

X.MESH      WIDTH=0.25  H1=0.02  H2=0.08

Y.MESH      N=1    L=-0.007
Y.MESH      N=4    L=0.
Y.MESH      DEPTH=0.01  H1=0.0025
Y.MESH      DEPTH=0.01  H1=0.0025
Y.MESH      DEPTH=0.01  H1=0.0025
Y.MESH      DEPTH=0.01  H1=0.0030
Y.MESH      DEPTH=0.02  H1=0.0025
Y.MESH      DEPTH=@TSI-0.15 H1=0.003 H2=0.2

COMMENT      *****
COMMENT      ELIMINATE SOME UNNECESSARY NODES
COMMENT      =====
ELIMIN      COLUMNS  Y.MIN=@JUL+0.06
ELIMIN      COLUMNS  Y.MIN=@JUL+0.06 X.MIN=0.4 X.MAX=0.8

COMMENT      *****
COMMENT      SPECIFY OXIDE AND SILICON REGIONS
COMMENT      =====
REGION      NUM=1  SILICON
REGION      NUM=2  OXIDE Y.MIN=-0.007 Y.MAX=0.
REGION      NUM=3  OXIDE Y.MIN=0.05 Y.MAX=0.45
REGION      NUM=4  SIGE Y.MIN=0.005 Y.MAX=0.013 X.MOLE=0.45
+           X.END=0.25 Y.LINEAR

COMMENT      ELECTRODES: #1=DRAIN, #2=GATE, #3=SOURCE,
+           #4=SUBSTRATE
ELECTR      NUM=1  X.MIN=2*@XDOP+@LCH+0.55 Y.MAX=0.050 VOID
ELECTR      NUM=2  X.MIN=0.35 X.MAX=@LCH+2*@XDOP+0.45 TOP
ELECTR      NUM=3  X.MAX=0.25 Y.MAX=0.050 VOID
ELECTR      NUM=4  BOTTOM

COMMENT      *****
COMMENT      SPECIFY IMPURITY PROFILES AND FIXED CHARGE
COMMENT      =====
COMMENT      SUBSTRATE DOPING
PROFILE      N-TYPE N.PEAK=@NDOP Y.MIN=0.013 Y.MAX=@TSI
+           UNIFORM
COMMENT      P+ SPIKE
PROFILE      P-TYPE N.PEAK=7.0E18 Y.MIN=0.02 Y.CHAR=0.002
+           XY.RAT=2.5

```

```

COMMENT      LOAD THE PREDEFINED CHANNEL DOPING
PROFILE      1D.ASCII IN.FILE=read_in_n.file Y.COL=3 N.COL=4

COMMENT      SPECIFY THE SOURCE AND DRAIN DOPING
PROFILE      P-TYPE  N.PEAK=5.0E20  X.MIN=0.0 WIDTH=.49
+            XY.RAT=0.1 Y.MIN=0.04 Y.MAX=0.07 Y.CHAR=0.023
PROFILE      P-TYPE  N.PEAK=5.0E20  X.MIN=@LCH+2*@XDOP+0.31
+            WIDTH=.49 XY.RAT=0.1 Y.MIN=0.04 Y.MAX=0.07
+            Y.CHAR=0.023

COMMENT      *****
COMMENT      SPECIFY THE INTERFACE AND CONTACT
COMMENT      =====
INTERFACE    REGION=(1,2) QF=1E11
CONTACT      NUM=2  N.POLYSI  PRINT

COMMENT      *****
COMMENT      SPECIFY PHYSICAL MODELS TO USE
COMMENT      =====
MODELS       CONMOB  PRPMOB  FLDMOB  CONSRH  AUGER  BGN  PRINT
MOBILITY     ECP.MU=1E10  PRINT  SIGE  PR.TABLE

COMMENT      *****
COMMENT      SOLVE FOR EQUILIBRIUM
COMMENT      =====
SYMB         CARRIERS=0
METHOD       ICCG  DAMPED
SOLVE        V1=0.0  V2=0.0

```

The following is the input deck for MEDICI, the purpose of this deck is to input the mesh, which is generated from above MEDICI file, then solve for different bias point. Those solutions from this MEDICI file will serve as data source for the postprocess (i.e. to calculate the effective mobility)

```

COMMENT      *****
COMMENT      ELECTRODES: #1=DRAIN, #2=GATE, #3=SOURCE,
+            #4=SUBSTRATE
COMMENT      =====

```

```

ASSIGN      NAME=OUTPUTF1  C.VALUE=PMOS.NGATE.SIGE.MESH  DELTA=1

COMMENT     READ IN THE MESH STUFF AS GENERATED BY GRID.GEN
MESH        INFILE=@OUTPUTF1

COMMENT     *****
COMMENT     SPECIFY PHYSICAL MODELS TO USE
COMMENT     =====

MODELS      LSMMOB  FLDMOB  CONSRH  AUGER  BGN  PRINT

COMMENT     *****
COMMENT     CHANGE PARAMETERS OF LSMMOB TO ENSURE THE CONSTANT
COMMENT     MOBILITY IN SIDE THE SIGE CHANNEL
COMMENT     =====

MOBILITY    MUP2.LSM=250.0  EXP4.LSM=2.0  DP.LSM=1.0E+20  SIGE PRINT

COMMENT     *****
COMMENT     INITIAL SOLUTION, REGRID ON POTENTIAL
COMMENT     =====

SYMB        CARRIERS=0
METHOD      ICCG  DAMPED
SOLVE       V2=0  V1=0

COMMENT     *****
COMMENT     OBTAIN INITIAL GATE BIAS WITH DRAIN=0, USING 2-CARRIER
+           NEWTON
COMMENT     =====

SYMB        CARRIERS=2  NEWTON
METHOD      AUTONR
SOLVE       V1=0.0  V2=0  ELEC=1  VSTEP=-0.02  NSTEP=3
SOLVE       V1=-0.05  V2=0  ELEC=2  VSTEP=0.05  NSTEP=10
LOG         IVFILE = DC_SOI_CSF

SOLVE       V1=-0.05  V2=0.5  ELEC=2  VSTEP=-0.05  NSTEP=9

COMMENT     *****

```


COMMENT SOLVE FOR DIFFERENT BIAS POINTS
COMMENT =====

LOOP STEPS = 20
ASSIGN NAME=OUTPUT2 C.VALUE=HOLES_INT_005 DELTA=5
ASSIGN NAME=VV2 N.VALUE=-0.05 DELTA=-0.05
ASSIGN NAME=OUTPUTS1 C.VALUE=SOLUTION_005 DELTA=5
SOLVE V1=-0.05 V2=@VV2 SAVE.BIA OUTFILE=@OUTPUTS1
PLOT.1D HOLES INTEGRAL X.START=0.6333 X.END=0.6333
+ Y.START=0.0 Y.END=1.0 OUTFILE = @OUTPUT2
L.END

LOOP STEPS = 15
ASSIGN NAME=OUTPUT3 C.VALUE=HOLES_INT_100 DELTA=10
ASSIGN NAME=OUTPUTS2 C.VALUE=SOLUTION_100 DELTA=10
ASSIGN NAME=VV3 N.VALUE=-1.0 DELTA=-0.1
SOLVE V1=-0.05 V2=@VV3 SAVE.BIA OUTFILE=@OUTPUTS2
PLOT.1D HOLES INTEGRAL X.START=0.6333 X.END=0.6333
+ Y.START=0.0 Y.END=1.0
OUTFILE = @OUTPUT3
L.END

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