Portland State University

PDXScholar

Dissertations and Theses

Dissertations and Theses

Spring 5-22-2019

Very High Frequency Bipolar Junction Transistor Frequency Multiplier Drive Network Design and Analysis

Daniel Dale Schaeffer
Portland State University

Follow this and additional works at: https://pdxscholar.library.pdx.edu/open_access_etds

Part of the [Electrical and Computer Engineering Commons](#)

Let us know how access to this document benefits you.

Recommended Citation

Schaeffer, Daniel Dale, "Very High Frequency Bipolar Junction Transistor Frequency Multiplier Drive Network Design and Analysis" (2019). *Dissertations and Theses*. Paper 5031.
<https://doi.org/10.15760/etd.6907>

This Thesis is brought to you for free and open access. It has been accepted for inclusion in Dissertations and Theses by an authorized administrator of PDXScholar. Please contact us if we can make this document more accessible: pdxscholar@pdx.edu.

Very High Frequency Bipolar Junction Transistor Frequency Multiplier Drive Network
Design and Analysis

by

Daniel Dale Schaeffer

A thesis submitted in partial fulfillment of the
requirements for the degree of

Master of Science
in
Electrical and Computer Engineering

Thesis Committee:
Richard Campbell, Chair
Branimir Pejcinovic
Hong Lei

Portland State University
2019

© 2019 Daniel Dale Schaeffer

Abstract

The function of a frequency multiplier is verbatim – a frequency multiplier is a circuit that takes a signal of particular frequency at the input and produces harmonic multiples of the input signal's frequency at the output. Their use is widespread throughout history, primarily in the application of frequency synthesis. When implemented as a part of a large system, a chain of multipliers can be used to synthesize multiple reference signals from a single high-performance reference oscillator.

Frequency multiplier designs use a variety of nonlinear devices and topologies to achieve excitation of harmonics. This thesis will focus on the design and analysis of single ended bipolar junction transistor frequency multipliers. This topology serves as a relatively simple design that lends itself to analysis of device parasitics and nonlinearities. In addition, design is done in the Very High Frequency (VHF) band of 30-300 MHz to allow for design and measurement freedoms. However, the design methodologies and theory can be frequency scaled as needed.

The parasitics and nonlinearities of frequency multipliers are well explored on the output side of circuit design, but literature is lacking in analysis of the drive network. In order to explore device nonlinearities on the drive side of the circuit, this thesis implements novel nonlinear reflectometry systems in both simulations and real-world testing. The simulation nonlinear reflectometry consists of intelligently configured voltage sources, whereas directional couplers allow for real world nonlinear reflectometry measurements. These measurements allow for harmonically rich reflected waveforms to be accurately measured, allowing for waveform engineering to be performed at the drive network. Further, nonlinear reflectometry measurements can be

used to explain how load- and source-pull obtained drive and load terminations are able to achieve performance increases.

Acknowledgments

I would like to thank my thesis committee for participating in my thesis process. Through editing this thesis, I have fully grasped how much of a task reading an 80-something page academic paper can be, and I appreciate the time commitment and consideration that my thesis committee has granted me.

I would like to doubly thank my thesis advisor, Dr. Richard Campbell, for inspiring the work in this thesis and guiding me through the thesis process. Through his excellent classes and the two theses I've worked on under his advice, I have been exposed to many unique problems and problem-solving approaches. His patience with my work on this thesis has allowed me to explore the subject to a depth that has been incredibly enriching. He has been a great positive influence in my growth as an engineer.

Additionally, I would like to thank my friends, colleagues, and teachers in the Portland State University Maseeh College of Engineering for allowing and encouraging my growth as an academic, student, and engineer. In particular, I'd like to recognize Portland State's Electronics Prototyping Lab and its staff for providing such a welcoming and useful environment for students endeavoring in personal projects and research. Without their resources, the work done in this thesis would have cost much more in time, money, and resources. Also, I'd like to thank Dr. Branimir Pejcinovic for granting me access to the Integrated Circuit Design and Test Laboratory, and for his classes on microwave theory. The knowledge and resources gained from those classes and his continued guidance on the subject and in the lab has served as a strong foundation for the work in this thesis.

Finally, I would like to give a special thanks to my parents for supporting me throughout my academic journey. Their support on all fronts has greatly facilitated my success thus far.

Table of Contents

Abstract.....	i
Acknowledgments	iii
List of Tables	vii
List of Figures.....	viii
1 Introduction.....	1
1.1 Frequency Selection: An Argument for Scalability	1
2 Frequency Multiplier Theory	3
2.1 Figures of Merit.....	5
2.1.1 Conversion Gain	6
2.1.2 Bandwidth.....	6
2.1.3 Drive Range	6
2.1.4 Suppression of Unwanted Harmonics	7
2.1.5 Efficiency.....	7
2.2 Reflection and Transmission	8
2.3 Frequency Multiplier Topologies.....	9
2.4 Device Modeling	12
2.4.1 Simulation Modeling	12
2.4.2 Analytical Modeling	12
2.5 Application of Amplifier Classes of Operation.....	13
2.5.1 Class A.....	14
2.5.2 Class AB/B	15
2.5.3 Class C	15
2.5.4 Other Classes	17
2.6 Port Networks.....	18
2.6.1 Harmonic Terminations	19
2.6.2 Harmonic Load/Source Pull and Harmonic Reflections	20
2.6.3 Drive Network: A Call for Analysis.....	20
3 Design	22
3.1 Bill of Materials	23
3.2 Device Selection.....	24
3.2.1 Device Measurement	24
3.3 Base Bias	27

3.4 Emitter Circuit.....	28
3.5 SPICE Signal Source: Nonlinear Reflection Measurements.....	32
3.6 Collector Network.....	33
3.7 Output Network.....	35
3.8 Drive Network.....	37
4 Build Results and Analysis.....	45
4.1 Build Methodology	45
4.2 Layout.....	46
4.3 Circuit Manufacturing	47
4.4 Testing Setup.....	48
4.4.1 Nonlinear Reflectometry	49
4.5 Frequency Multiplier Core: Biased Transistor.....	52
4.5.1 Port Networks: Variable Dependency	55
4.6 Input Reflectometry and Drive Network.....	59
4.7 Frequency Doubler.....	65
4.7.1 Drive Network Performance Comparison	68
4.8 Higher Order Harmonic Multipliers.....	73
4.8.1 Gain and Saturation Effects	74
4.8.2 Higher Order Frequency Multiplier Input Reflectometry	75
4.8.3 Double Tuned Circuit	77
5 Conclusion	81
5.1 Higher Frequency Designs	81
5.2 General Applicability to Nonlinear Circuits	82
5.3 Future Work	82
5.4 Closing Remarks	83
References.....	84
Appendix A	87

List of Tables

Table 2.1: Ideal frequency multiplier signal property transforms with multiplication factor N [5].....	3
Table 3.1: Bill of materials	23
Table 4.1: Test equipment.....	48
Table 4.2: Performance data for doubler with and without drive network.	70
Table 4.3: Doubler drive range data table.....	72
Table 4.4: Performance metrics for higher order multiplier terminations with 7 dBm input power.....	74
Table 4.5: Reflection coefficient for higher order frequency multipliers with drive network and 7 dBm input power.....	77
Table 4.6: Performance data for frequency sextupler with double tuned output circuit seen in Figure 4.26.	79

List of Figures

Figure 2.1: Frequency multiplier functional block diagram	3
Figure 2.2: Power spectrum of A) ideal sine wave signal, and B) real world sine wave signal	4
Figure 2.3: Harmonic components of reduced conduction angle current waveform [20].	16
Figure 3.1: Frequency multiplier circuit block diagram	22
Figure 3.2: SS9018 measured and simulated I-V curves.....	25
Figure 3.3: SS9018 measured and modified model simulated I-V curves.	26
Figure 3.4: Base bias network schematic.....	27
Figure 3.5: Addition of emitter biasing circuit to multiplier schematic	28
Figure 3.6: Conduction angle change with sweep of RE.....	29
Figure 3.7: Emitter voltage with swept capacitor CE.....	31
Figure 3.8: Nonlinear S-parameter measuring source	32
Figure 3.9: Addition of collector network to frequency multiplier.	33
Figure 3.10: AC response at collector for circuit in Figure 3.9	34
Figure 3.11: Collector waveform for circuit in Figure 3.9	35
Figure 3.12: Multiplier schematic with added output capacitive network.....	36
Figure 3.13: Voltage waveform at load for circuit shown in Figure 3.12	37
Figure 3.14: Base voltage waveform for circuit in Figure 3.12.....	38
Figure 3.15: Simulation nonlinear S-parameter measurement for circuit in Figure 3.12.	39
Figure 3.16: Simulation nonlinear S-parameter measurement for circuit in Figure 3.12 with increased CE to provide roughly DC voltage at device emitter.	39
Figure 3.17: Frequency multiplier with added input resonant circuit.....	40
Figure 3.18: Voltage waveform at base of circuit in Figure 3.17	41
Figure 3.19: Simulation nonlinear S-parameter measurement for circuit in Figure 3.17.	41
Figure 3.20: Final frequency doubler simulation circuit schematic	42
Figure 3.21: Base voltage waveform for circuit in Figure 3.20.....	42
Figure 3.22: Simulation nonlinear S-parameter measurement for circuit in Figure 3.20.	43
Figure 3.23: Output voltage waveform for circuit in Figure 3.20.	43
Figure 4.1: Circuit modules connected by male-to-male connectors	46
Figure 4.2: Layout of transistor and biasing circuit.....	47
Figure 4.3: Testing setup.....	49
Figure 4.4: Directional coupler reflectometry setup	50
Figure 4.5: Directional couplers set up in-line with signal generator and DUT	51
Figure 4.6: Frequency multiplier core schematic	53
Figure 4.7: Frequency multiplier core output for 7 dBm input power, RE tuned for maximal second harmonic output	54
Figure 4.8: S11 of frequency multiplier core with 7 dBm input power.....	56

Figure 4.9: S11 of frequency multiplier core with RE tuned for second harmonic at 7 dBm input power.....	58
Figure 4.10: S22 of frequency multiplier core for the same sweeps shown in Figure 4.8 and Figure 4.9.	59
Figure 4.11: Reflected waveforms for input power of 7 dBm.	60
Figure 4.12: FFT of RE=0 reflected waveform seen in Figure 4.11.	61
Figure 4.13: Multiplier core with input resonant circuit.....	62
Figure 4.14: Reflected waveforms of multiplier core circuit with input resonator for input power of 7 dBm.	62
Figure 4.15: FFT of RE=0 reflected waveform seen in Figure 4.14	63
Figure 4.16: Frequency multiplier core with full drive network	64
Figure 4.17: Reflected waveforms of multiplier core circuit with input resonator and reflection reduction for input power of 7 dBm.	65
Figure 4.18: Full frequency doubler schematic	66
Figure 4.19: S22 for full doubler design, RE tuned to second harmonic generation, 7 dBm input power	67
Figure 4.20: Input reflected waveform of doubler with (blue) and without (red) drive network for 7 dBm input power.....	68
Figure 4.21: Doubler without drive network	69
Figure 4.22: Doubler output spectra for 7 dBm input without (left) and with (right) drive network	69
Figure 4.23: Gain curves for doubler.	71
Figure 4.24: Reflected spectra of higher order multipliers with 7 dBm input power.	75
Figure 4.25: Reflected waveforms of higher order multipliers with 7 dBm input power.	76
Figure 4.26: Double tuned output termination.....	78
Figure 4.27: Output frequency spectrum of frequency sextupler with drive network and double tuned output circuit seen in Figure 4.26.....	79

1 Introduction

The function of a frequency multiplier is verbatim – a frequency multiplier is a circuit that takes a signal of particular frequency at the input and produces harmonic multiples of the input signal’s frequency at the output. Their use is widespread throughout history, primarily in the application of frequency synthesis. When implemented as a part of a large system, a chain of multipliers can be used to synthesize multiple reference signals from a single high performance reference oscillator [1].

Many early frequency multipliers were implemented using vacuum tubes [2], and the devices used for frequency multiplication have since diversified. Any nonlinear device – tubes, diodes, transistors, and sometimes even transformers [3] and other circuitry – can be used to excite higher harmonics from a signal. For the purpose of this thesis, design will be done with the bipolar junction transistor (BJT) as the nonlinear component. This thesis presents the theory and design behind single ended frequency multipliers and develops an intuitive understanding of BJT parasitics and nonlinear operation through the design of a very high frequency (VHF) frequency multiplier, with a focus on drive network analysis utilizing novel nonlinear reflectometry measurements.

1.1 Frequency Selection: An Argument for Scalability

Though modern frequency multiplier research is often focused on reaching progressively higher frequencies for use in ultra-high frequency (UHF), super-high frequency (SHF), millimeter wave, and higher frequency band circuitry, the circuit designed in this thesis will be designed for VHF band frequencies. VHF provides a nice middle ground for circuitry between the complications of higher frequencies, and the

necessity of large reactive components for lower frequencies. In the VHF range of 30 MHz to 300 MHz, the wavelength of signals is still on the order of meters, so any reasonably sized traces shorter than a few centimeters should have negligible effects on circuit impedance. At these frequencies, reactive components tend to be convenient values that are easily available in the form of lumped components. This is fortunate, since lumped components are much easier to swap out than distributed elements when quick circuit modification is wanted, and distributed elements at VHF tend to be quite large.

This circuit being designed in VHF does not negate the applicability of theory and design methodology for higher frequencies. Much of the lumped component circuitry used in the following designs can be effectively replaced at higher frequencies by distributed elements such as transmission line stubs, resonant lines, and coupled line filters.

VHF is also convenient because quartz crystal resonators with resonances in or around low VHF ranges are relatively easily attainable, reliable, and low cost. This means that a frequency multiplier with a VHF output frequency can use a quartz crystal oscillator as its reference oscillator, and, as will be discussed in the next section, reap the benefits of the quartz crystal signal's high spectral purity. For this reason, this project uses 24 MHz as the input signal, which has various useful harmonic multiples. The 3rd multiple (72 MHz) is usable for remote control aircraft, the 5th multiple (96 MHz) could be usable for down conversion of FM radio in a super heterodyne receiver, and the 6th multiple (144 MHz) is in the 2-meter amateur radio band [4].

2 Frequency Multiplier Theory

As previously stated, a frequency multiplier takes a signal on its input at a particular frequency, and outputs a harmonic or harmonics of the input signal's frequency. Figure 2.1 shows a simplistic ideal block diagram for the circuit.

Figure 2.1: Frequency multiplier functional block diagram

For an ideal frequency multiplier, several signal properties of the input signal are transferred or transformed to the multiplier's harmonic output signal. The major effects of ideal frequency multiplication on signal properties can be seen in Table 2.1.

Table 2.1: Ideal frequency multiplier signal property transforms with multiplication factor N [5]

Property of Input Signal	Input Function	Output Function
Frequency	f_0	Nf_0
Fractional Frequency	$\frac{\Delta f}{f}$	$\frac{\Delta f}{f}$
Phase Noise	$L(f)$	$L(f) + 20 \log N$

With multiplication factor N , the fractional frequency of the input signal transfers directly to the output signal. So, if an ideal frequency multiplier has a signal at its input that has an accuracy of ± 10 ppm, the output will have an accuracy of ± 10 ppm. This becomes obvious when looking at the full expression for fractional frequency. From Equation 2.1, it can be seen that if all frequencies present on the right side of the equation are multiplied by N , all the N coefficients cancel out, leaving the original expression.

$$\frac{\Delta f}{f} = \frac{f(t) - f_0}{f_0} \quad (2.1)$$

Phase noise ($L(f)$) is an important, if not the most important, qualifier for an oscillator. Phase noise is defined as the “single sideband power due to phase fluctuations referenced to total power”[6]. It is effectively a measurement of the short-term stability of a signal. Ideal signals have a single valued spectral power (Figure 2.2 A), which corresponds to a perfect sine wave. An ideal signal, therefore, has zero phase noise. Real world signals, however, have phase and variations that cause the spectral power to be spread out over the frequency spectrum (Figure 2.2 B). This spread out power is then characterized as phase noise by measuring the power in a 1 Hz bandwidth at a specified offset from the carrier signal, in units of dBc/Hz [6].

Figure 2.2: Power spectrum of A) ideal sine wave signal, and B) real world sine wave signal

From Table 2.1, frequency multiplication adds phase noise at a rate of $20 \log N$. Since addition of logarithmic power is equivalent to multiplication of power magnitude, this addition makes sense. With frequency multiplication, the spread of power of the input signal is being further distributed by a factor of N .

The preservation of the input signal’s fractional frequency, and its addition of phase noise at the rate of $20 \log N$ are selling points for the frequency multiplication

when considering the performance of various oscillators. At frequencies below 100 MHz, crystal technologies, which have stability figures potentially orders of magnitude better than LC oscillators, are available [7]. The downside of crystal oscillators is that crystals manufactured with resonances beyond 100 MHz are fragile, hard to manufacture, and expensive. To reach higher frequencies, in the hundreds of MHz or GHz ranges, LC oscillators and other less stable types of oscillators must be used, or a premium must be paid for more exotic or complex frequency synthesis methods [8]. Frequency multipliers avoid this issue by allowing the use of a lower frequency, high performance reference oscillator, preserving frequency stability and only increasing phase noise by a factor of N instead of by orders of magnitude. Of course, large multiplier chains can make relatively small instabilities in a reference oscillator's frequency large enough to effect system applications, such as in satellite telemetry transmitters [9], but this just implies that the reference oscillator's performance needs to be increased to meet system specifications.

2.1 Figures of Merit

Since many of the signal characteristics and transforms due to frequency multiplication described previously are essentially static, other signal properties must be used to characterize a frequency multiplier. The figures of merit that will be used in this work are: conversion gain, bandwidth, drive range, unwanted harmonic suppression, efficiency, and reflection coefficients.

2.1.1 Conversion Gain

The primary purpose of a frequency multiplier is to produce a harmonic from a source frequency. The conversion gain (CG) of a frequency multiplier is the measurement of how powerful the desired harmonic output signal is compared to the signal being multiplied. Hence, for frequency multiplier of order N , and for a given drive power level, the equation for conversion gain is:

$$CG = \frac{P_{out}(Nf_0)}{P_{in}(f_0)} \quad (2.2)$$

2.1.2 Bandwidth

The conversion gain will not only be valid at the exact design frequency. The conversion gain will remain around its maximum value for a frequency span. The bandwidth used in this work will be fractional bandwidth, defined as the range over which conversion gain is within 3 dB of the maximum conversion gain.

2.1.3 Drive Range

Many frequency multipliers require a minimum drive level to function. Others simply have lower conversion gain outside of the designed drive range. Drive range for this work will be defined as the range of input drive power over which conversion gain is within 3 dB of the maximum conversion gain at design frequency.

2.1.4 Suppression of Unwanted Harmonics

The harmonic selectivity of a frequency multiplier is not intrinsic to the nonlinear device used. At the device level, the device excites many harmonics from the input signal. So, in frequency multiplier designs, suppression of unwanted harmonics is important. An ideal frequency multiplier would have only the desired harmonic(s) at its output, but in real world applications, nearby harmonics will always be present.

Harmonic suppression, therefore, is defined as the ratio of the unwanted harmonic to the desired harmonic. So, for frequency multiplier of order N , the following equation is used:

$$M^{th} \text{ Harmonic Suppression} = \frac{P_{out}(Mf_0)}{P_{out}(Nf_0)} \quad (2.3)$$

2.1.5 Efficiency

For many high gain devices, simple drain or collector efficiency is a sufficient efficiency metric due to the small impact of relatively small input drive levels on calculation. For a nonlinear circuit such as a power amplifier, large input drive levels are often required for operation, and gain is often in the single digits. For this reason, power added efficiency (PAE) can be a preferable efficiency metric. Power added efficiency takes into account the power input to the device. Due to the particular harmonic operation of frequency multipliers, the input and output powers' frequencies must be specified in the PAE equation. The equation is as follows:

$$PAE = \frac{P_{out}(Nf_0) - P_{in}(f_0)}{P_{DC}} \quad (2.4)$$

However, this equation is only meaningful for frequency multipliers with gain. If there is instead conversion loss, this metric loses meaning. So, in place of PAE, collector efficiency will be reported. The collector efficiency is defined as follows:

$$\eta_{collector} = \frac{P_{out}(Nf_0)}{P_{DC}} \quad (2.5)$$

2.2 Reflection and Transmission

For circuit analysis, scattering parameters (S-parameters) are often used for characterizing linear circuits. S-parameters characterize a circuit through exciting a circuit's port with an incident wave, then observing reflected waves at the excitation port and transmitted waves at other ports. By exciting and observing all possible port combinations with appropriate port terminations, a linear circuit can be fully characterized. For example, the equation below shows the S-parameter matrix used to characterize a two-port network, where V_n^- is the wave reflected or transmitted from port n , and V_n^+ is the wave incident on port n [10].

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \quad (2.6)$$

Scattering parameters are useful in that they can easily be used to indicate impedances, gain, and isolation between ports. The drawback is their applicability. They are inherently tied to the specific operating condition under which they were defined. So, an S-parameter matrix can characterize a circuit at a specific bias, frequency, and drive level. For small signal devices, drive level can often be ignored, bias can be seen as constant, and, assuming a linear circuit, evaluating at a single frequency isn't an issue. When it comes to nonlinear circuitry such as a frequency multiplier, however, the

specificity of S-parameters becomes an issue. As will be discussed, depending upon circuit topology, bias and drive level can be inherently tied together. This means that correct characterization of a nonlinear circuit may not be possible without exciting multiple ports at once, which violates the definition of S-parameters. Also, for a frequency multiplier, different ports of the circuit are operating at different frequencies, so a characterization of the circuit at the fundamental will not capture the full harmonic behavior of the circuit.

In the single frequency dependence of S-parameters, they can be thought of as a measurement best displayed in the frequency domain, with S-parameter data being displayed for a variety of discrete frequencies. What is needed for nonlinear circuitry measurement is a transient time domain view of reflected and incident waveforms, where harmonic content can be appropriately analyzed. This paper will demonstrate methods of nonlinear circuit reflectometry in both simulation and real-world measurements.

2.3 Frequency Multiplier Topologies

As previously stated, frequency multipliers use a variety of nonlinear devices. Though exotic frequency multipliers exist at higher frequencies, and other unconventional nonlinear devices, such as magnetic reactors, have been used in the past, semiconductor based nonlinear devices will be focused on. These semiconductor devices and their accompanying frequency multipliers can be divided into two groups: passive and active. In this set, passive frequency multipliers consist primarily of diode-based circuits, whereas active frequency multipliers come in many forms.

Passive diode frequency multipliers come in multiple forms. Varactor multipliers utilize the nonlinear relationship between device capacitance and drive level for comb generation. Another popular form of passive diode multiplier is the step recovery diode (SRD). SRDs store charge when forward biased that is quickly discharged as the device is subsequently reverse biased. This discharge pulse is rich in harmonics, working as a comb generator [5]. The comb generation offered by diode multipliers is often useful in system applications. It offers a compact way to achieve higher order multiplication [11]. Also, given a comb signal, several harmonics can be extracted and used as needed in different sub-circuits of a system. However, step recovery diodes, and other diodes used in frequency multiplication, are noisy due to recombination effects and shot noise [12]. Diodes also often require high input powers of 20 dBm or more and have conversion loss, not conversion gain. These losses and the high drive level needed often require power amplifiers before and/or after the multiplier [1], [13], increasing system complexity, and possibly decreasing efficiency.

Active multiplication topologies serve as a solution to many of these issues. Active multipliers in application can be viewed as power amplifiers that are overdriven to clipping, biased to a reduced conduction angle, and/or take advantage of other device nonlinearities to create a harmonic rich signal on the output. Due to the multiplication and power amplification being combined into one package, an active frequency multiplier can provide conversion gain, or alternatively more broadband operation, and can decrease the overall circuit complexity. The input levels required can be 0 dBm or lower. Avoidance of passive losses also increases efficiency. One downside to active multiplication is the commonly low multiplication order achievable due to output spectra

attenuation at higher frequencies. However, replication of diode multiplier's comb generation has been performed using a BJT multiplier [12].

Active multipliers can be further divided into two groups: balanced and single ended. Balanced multipliers can be used to great effect to cancel out either odd or even harmonics, depending on how the push-pull or push-push circuit is connected [14] [15]. Single ended designs tend to be more efficient, lower power circuits, but tend to have tighter bandwidth of operation due to the high Q resonators or reflectors that are often necessary for operation [8].

This work aims to explore device parasitics and their influence on multiplication, so the single ended topology lends well to this with its single device. This still leaves the choice of device to question, though.

BJTs and field effect transistors (FETs) (and their various higher performance counterparts) stand as the primary transistor types used for active multiplication. Each has its merits, and unique device characteristics. For this work, the BJT will be used for several reasons. Along with the author's familiarity with BJTs, the BJT allows for easier control over conduction angle, since FET gate-source breakdown voltage often limits negative biasing[16]. Also, the junctions of the BJT offer interesting capacitive nonlinearities that will be discussed more in the proceeding section.

2.4 Device Modeling

In order to design a frequency multiplier, nonlinear device models must be used for both the simulation and analysis of results.

2.4.1 Simulation Modeling

LTspice is the simulator of choice due to its availability to amateurs and professionals alike. It provides sufficient time domain analysis to tackle the problem of nonlinear devices. While a more robust simulator (in this case, meaning pre-packed with tools) with harmonic balance simulation abilities could have been used, this was avoided since many of these simulators are not readily available outside of academia and select professional settings, and several other studies have used such simulators to automatically optimize their designs. The goal of this thesis is not to get the highest performance frequency multiplier – it is to develop an intuitive understanding of the parasitics and non-linear mechanisms at play in the frequency multiplier. LTspice provides just enough features to achieve this and comes at the right price: free.

LTspice uses the Gummel Poon model [17] for BJTs. The complexities of this model allow it to represent many nonlinear behaviors of the BJT, but it does not lend itself easily to direct analysis in application. For this reason, a simpler model representation is used for analysis.

2.4.2 Analytical Modeling

To be able to effectively think about what's happening in a BJT in nonlinear circuit applications, it's helpful to have a simple representation of the BJT. A simple

model of a BJT running in common emitter (CE) configuration is one that looks at the BJT as a three terminal transconductance device with reverse biased varactor diodes between the collector and base and collector and emitter [18]. This simple model matches well with the structure of BJTs, considering a BJT is essentially just a pair of opposing diodes smashed together [18].

In small signal operation, these varactors are at relatively constant drive levels, so small signal linear parameters such as S-parameters are more applicable to the device. Once significant drive is applied, the capacitances change depending upon the drive level, and may change during each conduction cycle to appreciably affect operation [18]. Even if the average/DC voltage across these varactors stays constant, the nonlinear voltage-capacitance curve of a varactor can cause AC voltages of differing amplitude over the varactor to cause different average capacitance.

Aside from the addition of these varactors, the analytical model used in discussion will be the commonly used hybrid-pi model.

2.5 Application of Amplifier Classes of Operation

Considering that an active frequency multiplier is essentially a power amplifier with different harmonic input and output, it is important to understand PA classes of operation and how they can be used in frequency multiplication. Be aware that this is not an exhaustive list of amplifier classes, but only includes single ended classes pertinent to the analysis that will be conducted.

2.5.1 Class A

In conventional power amplifiers and low noise amplifiers, the main advantage of Class A biasing is its linearity. The Q point on the load line is chosen to give maximal headroom for the output waveform to be linearly amplified from input to output. For frequency multiplication, this is the worst-case scenario – a signal on the input that is transferred to the output with minimal additional harmonics.

This, however, does not make class A useless for frequency multiplication. If sufficient amplification is performed, the signal on the output can be clipped on its positive and negative peaks. From looking at the signal with Fourier analysis in mind, it should be clear that a symmetrically clipped waveform is rich in odd order harmonics. As amplification increases, and more of the signal is clipped, the signal approaches the shape of a square wave, which is composed only of odd harmonics. This design approach has been used, and it should be noted that careful biasing must be used to ensure optimal symmetrical clipping is performed for odd order harmonic generation [1].

Several downsides exist for Class-A operation. One major downside is stability. The device is biased so that quiescent DC current is constantly running through it, meaning that small signal gain is high. So, at RF frequencies, when presented with particular impedances, the transistor can be prone to oscillation. Even if this oscillation is at the output frequency of interest, this can still be problematic. The oscillation happening in the transistor can be much less stable than that coming from a reference oscillator (though some designs have successfully used self-oscillation as the reference oscillation [19]), so an oscillatory frequency multiplier will add considerable phase noise. Class A

design often warrants stabilization networks, which adds complexity and can incur losses on the system.

With the constant DC current also comes a loss of efficiency. Ideally, the maximum efficiency of a class A amplifier is 25%, which is the lowest of all amplifier classes.

2.5.2 Class AB/B

Class AB and B are both reduced conduction angle modes of operation. Class AB runs the transistor at a conduction angle of between 180 and 360 degrees, while class B runs the has a conduction angle of 180 degrees, working as an amplifying half wave rectifier. Class AB runs into similar stability issues as Class A since the Q point has DC current constantly running through the device. Class B is biased to have a near 0 DC current Q point, however, so small signal amplification is discouraged, and circuit stability is less of an issue.

In multiplier application, Class AB has been used for comb generation similar to that of SRDs [12]. Class B operation offers an output waveform that is rich in second and low in third harmonic component. This bias point can then be used well in doubler applications where high suppression of the third harmonic is crucial [13].

2.5.3 Class C

Further reduction in conduction angle below 180 degrees produces Class C operation. In this mode, the transistor is only amplifying a portion less than half of the input signal. Much like with Class B, Class C amplifiers are much less prone to

oscillation due to having no quiescent dc current, and hence small signal gain is miniscule. Also, Class C is the most efficient class discussed yet, with efficiency possible in the range of 70%.

Figure 2.3: Harmonic components of reduced conduction angle current waveform [20]. Note that this is for current waveforms that are normalized to have $I_{\max} = 1$.

Class C amplifiers also work as a sort of “Jack of all trades” when it comes to harmonic frequency generation. The reduced conduction angle output signal is rich in higher harmonics. Figure 2.3 shows the amplitude of harmonic components in the collector current with decreasing conduction angle.

Previous statements about other amplifier classes can be verified here. Ideal Class A output signals are entirely made up of DC and fundamental components. Class B offers

a point of increased second harmonics, and minimal third harmonics. Class C, though, encompasses all the conduction angle range that includes the peaks for harmonics. So, a Class C amplifier ends up being the most versatile of the amplifier classes for harmonic generation, since a simple change in bias and re-adjustment of reactive circuitry should allow higher harmonics to be successfully excited and output. For this reason, a Class C amplifier will be the starting point for design in this work.

2.5.4 Other Classes

The previous discussions treat the transistor in a power amplifier as a current source, with the only parameter changing being the biasing. With other classes of operation, more variables are introduced.

With the basic Class E amplifier, the transistor is treated as switch, in a pseudo-class C biasing system. The transistor then has two states: on and off. With this, current and voltage waveforms have minimal crossover, meaning minimal power dissipation. Efficiency is then limited only by the switching time for the transistor [16]. This leads to the addition of load and source harmonic terminations to encourage a faster switching time, and a more square waveform, such as in Class F amplifiers [21]. Of interest in these topologies for frequency multiplication is the square wave current waveform. Square waves are inherently rich in odd harmonics, as discussed in the Class A section. But, with Class E, the stability and efficiency issues of Class A are not present. Further, Class E, by adjusting the Class C “conduction angle”, gives the ability to adjust the square wave output duty cycle. Though this can require complexity in load network, this allows higher harmonics to be excited with lower duty cycles [22].

Class J goes back to using the transistor as a current source, biasing the device in Class AB or Class C. Similar harmonic termination methods are used in Class J as Class E and F. In Class J, the design focuses primarily on playing with second and higher harmonic tuning on the output. The higher harmonics are used to boost the fundamental, and phase shifting of the output voltage waveform with specific harmonic terminating impedances helps to increase efficiency by minimizing current and voltage waveform crossover [20], [23], [24].

These are all power amplifier topologies, but their techniques of harmonic reflection and waveform engineering provide a useful framework for thinking about frequency multiplication.

2.6 Port Networks

As is apparent from Class J, Class E, and Class F design, differing port networks can greatly affect harmonic generation. Biasing to a harmonically rich Class C conduction angle alone doesn't generate high harmonic output. Correct biasing more allows those harmonics to be encouraged by intelligent port network design. Drive and output terminations that encourage the wanted harmonics, while still allowing the necessary harmonics to propagate, are necessary for successful generation and delivery of harmonic power. The following methods can be thought of as recycling generated harmonics created by the nonlinear device [13].

2.6.1 Harmonic Terminations

The simplest form of altering harmonic terminating impedances is in applying resonant circuits for specific harmonics at the ports. In the case of lumped circuit implementation, this means shorting and open-circuiting harmonics with series and parallel resonant LC circuits. In several studies, sets of harmonic terminations were either open circuited or short circuited at the drive and output ports. Trends in optimal terminations prevailed through all reports. For the input, short circuiting the Nf_0 harmonic is reported as optimal, no matter the configuration. Also, as expected, passing through f_0 on the input and Nf_0 on the output is always optimal. [11], [25]–[27]

Otherwise, optimal terminations may be dependent on biasing [27]. Also, several of these studies were based on FET designs, so conclusions may not directly translate to BJT designs and their unique nonlinear behavior [25], [27].

Of interest when discussing output circuitry for frequency multipliers and power amplifiers is that real power is only present in whatever signal reaches a circuit's resistive load. So, theoretically, a device can create large amounts of wideband harmonic reactive power at the device's output terminal (the collector in the case of a BJT), but the only real power present in the output circuit is that which is delivered to the load. This is used to great effect in high efficiency PA topologies such as Class-E and Class-J, where a square wave (or other harmonically rich waveform) is developed at a device's output terminal, but the signal delivered to the load is sinusoidal. In this, the additional harmonics required to create the harmonically rich waveform at the device output terminal are purely reactive in nature, and thus do not factor into circuit efficiency. Similarly, in frequency multipliers, additional harmonics can be excited at the device output terminal

to ideally excite wanted harmonics, but only the signal outputted to the load impacts real DC current draw, and hence efficiency.

2.6.2 Harmonic Load/Source Pull and Harmonic Reflections

Power amplifiers' port networks aren't just a matter of "matching" each port to its load to minimize reflections. An integral part of power amplifier design is presenting the transistor with impedances that maximize gain and efficiency. Popular forms of finding these impedances are the numerical and testing methods of load pull and source pull.

In load and source pull, the transistor is presented with a series of impedances at the source or load of the transistor, and contours for efficiency and gain are produced. This technique, with some modifications, also applies to frequency multipliers. With frequency multipliers the load pull is simultaneously done at the fundamental and harmonic frequencies to produce the highest harmonic output for the frequency of interest. This can be done as simply sweeping component values in a given circuit topology to maximize a given circuit's effectiveness [19]. A more advanced technique used in [13] and [1] uses frequency multiplexing to find the exact optimal impedances to present at source and load for each harmonic. Then, impedance transformation structures can be realized to satisfy the source and load requirements. High precision nonlinear models can allow highly accurate results using this method.

2.6.3 Drive Network: A Call for Analysis

For the load network, thorough analysis for PA drain/collector current waveforms exists, which allowed for the previously mentioned class J, E, and F designs. Each uses

“waveform engineering” [28], [29] in its own way to reach specific design goals. Much of the analyses provide a reasoning framework for why the designed or load-pull found impedances are capable of boosting circuit performance. In these analyses, though, the drive network is often not discussed in detail, sometimes simply citing that harmonic terminations were used to ensure a sine wave input. Though this is sufficient reasoning for the purpose of design, this thesis aims to analyze the mechanisms at play in the frequency multiplier drive network.

3 Design

The design procedure used in this work is intended to be general use, capable of producing frequency multipliers of various orders over a wide frequency range. This section follows the design procedure – from device selection to circuit layout – for a 24 MHz VHF single ended BJT frequency doubler in a 50-ohm system. The drive level of choice will be 7 dBm, which is approximately 0.7 V_p in a 50-ohm system. This drive level is large enough to easily drive a BJT into nonlinearity with proper biasing and is a useful power level in various RF applications, including mixers.

All design and optimization is done in LTspice, while concurrently comparing real world results with simulations.

Below is a block diagram for the frequency multiplier.

Figure 3.1: Frequency multiplier circuit block diagram

The design procedure will proceed through design in the following order, constructing the circuit along the way:

1. Device Selection
2. Base Bias Network Design
3. Emitter Bias Network Design
4. Collector Network Design
5. Output Network Design
6. Drive Network Design

3.1 Bill of Materials

Most components come from component kits readily available on Amazon. The individual components used from these kits won't be listed but will be visible in circuit schematics.

Table 3.1: Bill of materials

Product	Manufacturer P/Ns
WINGONEER Capacitor 0603 Sample Book [30]	Murata GRM Series
OneBelief 0603 SMD Inductor Sample Book [31]	Unknown
Yobett 0603 5% Resistor and Capacitor Combo Kit [32]	Yageo RC0603J, Murata GRM Series
Joe Knows Electronics Semiconductor Kit [33]	Fairchild SS9018
Rogers Laminate PCB Material [34]	16 mil Rogers RO4003C
2.5-22 pF Variable Capacitor	Vishay BFC280811229

3.2 Device Selection

Advances in nonlinear devices, particularly high power, high frequency semiconductors, continue to provide designers with devices capable of achieving greater performance for frequency multiplication [1], [13] Though high power/high performance transistors could be used in this design, the author decided to use what was available, and work with a grab-bag transistor as a way of demonstrating the generalized approach of this work. This is doable because f_t and other figures of merit are applicable mostly to linear operation. In nonlinear operation of the frequency multiplier, f_t can be close to design output frequency since small signal gain isn't the major mechanism at play [18]

The transistor selected for this application is the SS9018H NPN BJT [35] from a transistor kit [33]. The simulation model used was from an LTspice transistor model library [36].

3.2.1 Device Measurement

To ensure that LTspice models behaved in a way that was conducive to design, device measurements were made using a Keysight B1500A Semiconductor Device Parameter Analyzer.

Figure 3.2: SS9018 measured and simulated I-V curves. Simulated data is dashed, measured is solid, similarly colored lines have the same V_{be} .

For the device measurement seen in Figure 3.2, 9V was selected as the maximum for the VCE sweep due to that being the planned supply voltage. 9V holds many conveniences as a supply voltage. 9V is usable in mobile applications with a 9V battery, which can power a device running at 20 mA for approximately a full day. Also, in automotive applications, such as for sensing applications, the 12V battery voltage can be regulated down to 9V.

The simulation model obviously doesn't behave entirely like the real thing, as seen in Figure 3.2. As both base bias and Vce increase, more non-linear behavior can be seen in device measurements. It's likely that the curve tracer is exciting thermal runaway effects in the BJT that are not included in the LTspice model.

Figure 3.3: SS9018 measured and modified model simulated I-V curves. Simulated data is dashed, measured is solid, similarly colored lines have the same V_{be} .

Figure 3.3 shows the I-V curve comparison once again with lowered forward beta, and vastly lower Early voltage to capture more of the nonlinear aspects of the measured IV curve. The SS9018 is rated for 50 mA, and quiescent current will likely be kept at 30 mA and lower. If a load line from 30 mA to 9 V is considered, correlation between the simulation and measurements is good enough for the purposes of the simulations being performed. Other works sufficiently explore designing frequency multipliers with highly accurate models [1], [13], [19].

3.3 Base Bias

The base bias circuit for this design is a resistive voltage divider, as seen in Figure 3.4. More complex and robust biasing networks exist, such as those using an RF choke or active biasing, but this section of the design does not have much effect on functionality (beyond setting bias point) as long as the resistors are high enough value to not influence input impedance, while still being low enough to supply a small base bias current without appreciably changing the base voltage.

Figure 3.4: Base bias network schematic

A Class C bias point is chosen due to the benefits discussed in Section 2.5.3, including increased stability, harmonic agility, and efficiency. To allow for full conduction angle availability from 0 to 180 degrees, the small signal bias for the device is approximately Class B at this stage of design.

Given the 9-volt supply voltage, the bias network sets the base bias to 620 mV. This bias point is set to where with no drive signal, the transistor is in an off state with miniscule base current. Though this is a Class C design, this bias network will bias the transistor right at pinchoff (Class B), with around a hundred microamps running through the collector. This very small collector current indicates that bias is set correctly, just on the cusp of threshold voltage.

R3 and C1 form a high pass filter to aid in filtering out power supply noise and signal cross contamination between collector and base power supply lines.

3.4 Emitter Circuit

The emitter circuit in this design is the key to achieving Class C operation. The circuit can be seen in Figure 3.5.

Figure 3.5: Addition of emitter biasing circuit to multiplier schematic

Being that this design is meant for a Class C bias point, the 7 dBm drive signal will be large enough that the biasing point will be affected by the drive signal. If this signal were applied to the circuit shown in Figure 3.4, the circuit would always be stuck at a fixed conduction angle of approximately 180 degrees. The addition of the potentiometer RE allows for the bias to be adjusted across the Class C conduction angle range. As this large drive signal begins to forward bias the base emitter junction, the transistor will turn on and conduct current from collector to emitter, but only for a limited portion of the input signal cycle. This reduced conduction angle current waveform has a DC component (see Figure 2.3) that then develops a DC voltage across potentiometer RE. This DC voltage then effectively reduces the V_{be} , which in turn reduces conduction angle. Therefore, the potentiometer RE can be adjusted to directly influence the conduction angle. At $RE = 0$, the conduction angle is approximately that of a Class B amplifier. Once the resistor value is increased, conduction angle is reduced. This effect can be seen in Figure 3.6.

Figure 3.6: Conduction angle change with sweep of RE. RE is swept from 20 to 200 in decade sweep of 10 points. The light green trace with highest current draw is 20, the brown trace with lowest current draw is 200.

Not only does this adjustable emitter resistor allow for conduction angle adjustment, but it decouples the conduction angle's dependence from the transistor's current gain characteristics. Transistors can often have beta values that deviate, even between discrete transistors of the same model. A change in beta would cause a change in collector current, which would in turn effect the biasing of the transistor appreciably. Using a potentiometer in RE allows optimal conduction angle to be chosen for a given harmonic, even given transistors with varying beta values. For now, RE is set to 30 to give a conduction angle of about 120 degrees, which is approximately the optimal conduction angle for second harmonic generation (see Figure 2.3).

Also, having an emitter resistor helps to alleviate temperature dependence of collector current, overriding the highly temperature dependent internal transresistance [18].

At this point in the design, capacitor CE is considered a simple AC bypass capacitor, allowing the transistor's CE gain to be limited only by transistor internal transconductance. But, when swept, interesting characteristics begin to show, as seen in Figure 3.7.

Figure 3.7: Emitter voltage with swept capacitor CE. CE is swept from 100 pF to 100 nF in decade sweep with 1 point per decade. Green trace is 100 pF, blue is 1 nF, red is 10 nF, and light blue is 100 nF.

As expected, RE and CE form a low pass filter. If simple fundamental amplification were wanted, the higher value of 100 nF for maximum stable bias condition would be preferable. But, for frequency multiplication, the harmonic content of the voltage waveforms with ripple becomes advantageous. In the sweep shown in Figure 3.7, CE values of 10 and 100 nF are too flat to be interesting. 100 pF dissipates the voltage too quickly, and ultimately ends up hurting AC current gain due to its appreciable impedance at design frequency. 1 nF stands as a nice middle ground between all options. The shape of this waveform is that of a low harmonic order reverse sawtooth wave. Fortunately, sawtooth waveforms are rich in both even and odd harmonics. Later in the design, this capacitor, along with RE, will be adjusted to provide optimal harmonic performance and biasing condition.

3.5 SPICE Signal Source: Nonlinear Reflection Measurements

At this stage, RF drive has now been applied to the circuit. This drive could have been applied by a simple 50-ohm source, but this method has limitations when it comes to taking simulation measurements. LTspice allows for the extraction of S-parameters for a simulation, given a source and load, but these measurements are taken using an AC analysis simulation, which uses a small signal DC solution for setting up voltages at the device ports. This is problematic, since the DC operating point calculated by LTspice at the emitter for all waveforms shown in Figure 3.7 is 6 mV. Therefore, in AC analysis simulations, the device is not at all operating as it is in transient simulations. To get around this limitation, a one port S-parameter measurement is instead taken for the transient simulation using the circuit seen in Figure 3.8 (also in Figure 3.5 and all subsequent LTspice simulation figures). This circuit was adapted from Dr. Campbell's lecture notes on reflections [37].

Figure 3.8: Nonlinear S-parameter measuring source

This circuit allows S11 (reflection coefficient) to be taken in the time domain, with proper real-time biasing being provided by the source. VSource1 and Rs1 produce

the signal that one would expect from a 50-ohm RF signal generator. VSource2 is what supplies the S11 measurement at point S11 by simply subtracting a synchronized half amplitude sine wave from the input's signal. This circuit results in waveforms at point S11 that indicate reflection coefficient accurately and reliably. The amplitude of the signal at S11 is the reflection coefficient amplitude scaled by .35 V, and the phase between the signals at Ref and S11 are the reflection coefficient's angle.

3.6 Collector Network

To feed dc power to the collector of the transistor and allow the transistor to develop an AC collector waveform, a collector load is necessary. At this stage, this consists only of a 100 nH inductor, as seen in Figure 3.9.

Figure 3.9: Addition of collector network to frequency multiplier. C3 is a placeholder for future circuitry.

The 100 nH inductor was chosen somewhat arbitrarily for the transistor's DC feed, other than to get the largest inductor possible while avoiding impactful parasitics.

100 nH is about as large as a grab-bag SMD inductor should be for 48 MHz output frequency, given some of Murata's lowest specified inductors has a series resonant frequency of 240 MHz [38]. Its actual value isn't terribly important right now, but its functionality is. C3 is a placeholder for the future output network and helps with that output networks design. L1 and C3 form the reactive AC load for the transistor. The frequency response at the collector can be seen in Figure 3.10.

Figure 3.10: AC response at collector for circuit in Figure 3.9

The LC tank circuit formed by C3 and L1 provide high resistance at the resonant frequency of 48 MHz, the output frequency of the doubler. To the transistor, which is acting as a CE amplifier, this increases the ratio of load impedance to emitter impedance at 48 MHz, giving very high gain at that specific frequency. So, to excite and output the doubled 48 MHz harmonic, L1 needs to be resonated with a capacitance of approximately 108.5 pF.

Figure 3.11: Collector waveform for circuit in Figure 3.9

As can be seen in Figure 3.11, the resulting collector voltage is a clean 48 MHz sine wave with an amplitude of twice the supply voltage. This extra headroom is allowed by L1, which reacts to every current pull of the resistor by resonating with C3. This tank circuit can be thought of as a bell that is being periodically rung by the transistor at exactly the right times to constructively create a perfect tone.

Without a load resistance, the Q of the LC tank circuit is incredibly high, meaning that, going back to the bell metaphor, the bell is nearly frictionless, will ring without considerable losses, and is re-rung before the losses become apparent. Once a real-world load is introduced, the issue becomes more complicated.

3.7 Output Network

The output network is designed to develop harmonic power at the device collector and deliver wanted harmonic power to a load. For this design, the load is 50 ohms.

A sufficiently high Q tuned circuit at the transistor collector, as found in the previous section, will develop needed harmonic power at the device collector – the

difficult part is transferring that harmonic power to the load while still developing that harmonic power. This is achieved by transforming the 50-ohm load into a higher impedance as seen by the collector through an impedance transforming network, while still resonating with L1 to create resonance. Since the output network is not the focus of this work, a simple yet functional two element capacitive network is used, as seen in Figure 3.12.

Figure 3.12: Multiplier schematic with added output capacitive network

The capacitive network works as a total capacitance that resonates with L1 to develop harmonic components at the collector. These capacitance values were found by performing a basic load pull with the given topology to get maximum conversion gain. This optimized impedance is one that provides a high enough impedance in the resonant circuit to allow for a high Q for harmonic generation, while not being so high to block transfer of harmonic power to the load. In other words, it performs a balancing act between reflecting 2nd harmonic power to the collector and leaking 2nd harmonic power to the load. Cdc is simply an extra DC block capacitor. This circuit results in an output

voltage at the load seen in Figure 3.13. Though the waveform is not entirely clean, this signal can be filtered in subsequent stages or circuitry to achieve desired spectra.

Figure 3.13: Voltage waveform at load for circuit shown in Figure 3.12

As an aside, if bias is increased to Class AB operation, the circuit in Figure 3.12 without input drive network can be directly connected to a crystal resonator with resonance equal to f_0 , and the circuit creates a functional overtone crystal oscillator. So, with a single resistor value change, this circuit can be a self-contained oscillator, though circuit performance without further circuit alteration is questionable.

3.8 Drive Network

In its simplest form, the drive network consists of a simple DC blocking capacitor (C2 in previous schematics). In this configuration, device nonlinearities cause the drive signal to become distorted (as seen in Figure 3.14), which can alter the large signal bias point.

Figure 3.14: Base voltage waveform for circuit in Figure 3.12

The sagging on the top of the base waveform is likely due to the base current draw and modulated capacitance in the form of the varactors described in Section 2.4.2. The base current draw varies depending on input voltage. When the transistor isn't being driven, the signal source simply sees a high impedance at the base of the transistor. Once the drive signal increases the base-emitter voltage to conduction levels and beyond, large collector current develops, which in turn decreases internal transistor transresistance, and modulates the transistor's internal varactors. This means that the input impedance of the circuit is constantly in flux, and highly dependent on drive level.

Alternatively, this can be viewed through the lens of incident and reflected waves at the device input using the nonlinear 1-port S-parameter source detailed in Section 3.5. Measurements taken from this source can be seen in Figure 3.15

Figure 3.15: Simulation nonlinear S-parameter measurement for circuit in Figure 3.12. Blue is the input waveform reference, green is the reflection coefficient waveform.

Considering the $V(s_{11})$ trace, there is considerable reflected power, and that reflected waveform is harmonically rich. Once again, this appears to be a sawtooth waveform. This is partially due to the waveform present at the device emitter, but even when the waveform at the emitter is cleaned up, a harmonically rich (though not as shapely) reflected waveform remains, as seen in Figure 3.16.

Figure 3.16: Simulation nonlinear S-parameter measurement for circuit in Figure 3.12 with increased CE to provide roughly DC voltage at device emitter. Blue is the input waveform reference, green is the reflection coefficient waveform.

Attempting to take a reflection coefficient reading from the above traces would be ill advised, unless harmonics were separated to generate a series of harmonic reflection coefficients (which may produce interesting results). However, a simpler approach is used to circumvent this harmonically rich waveform.

To counter this slumping of the input waveform peaks, or thinking alternatively, clean up the reflected waveform so that a proper fundamental frequency reflection coefficient and impedance can be read, harmonic terminations can be applied. Multiple topologies of resonant circuits were tested for this purpose, and the circuit decided upon is an LC tank circuit resonant at the fundamental frequency, as seen in Figure 3.17.

Figure 3.17: Frequency multiplier with added input resonant circuit

This circuit is the simplest implementation for the purpose of peak recovery and reflection filtering in drive network design, but it serves well for the purpose of the design and analysis being performed. This circuit was able to raise conversion gain by approximately 1 dB, with no significant change in output signal spectra or DC power draw, and cleaned up the signal at the base considerably, as seen in Figure 3.18.

Figure 3.18: Voltage waveform at base of circuit in Figure 3.17

Figure 3.19: Simulation nonlinear S-parameter measurement for circuit in Figure 3.17. Blue is the input waveform reference, green is the reflection coefficient waveform.

As expected, the reflection waveform also cleaned up. Now, a proper reflection coefficient measurement can be taken. The reflection coefficient is approximately $.9 \angle 0$. To further increase circuit performance, a network can now be applied to minimize reflected input power, maximizing the power applied to the transistor base.

Figure 3.20: Final frequency doubler simulation circuit schematic

To minimize reflections, C2 and L3 in Figure 3.20 were swept to find optimal values for input reflection reduction. Starting with the reflection coefficient of $.9 \angle 0$, reducing L3 from its value in Figure 3.17 brings the impedance to the unity resistance circle on a Smith chart. C2 then brings the impedance in line with the 50-ohm source. In this way, voltage at the device base is increased, as seen in Figure 3.21 (compare to Figure 3.18).

Figure 3.21: Base voltage waveform for circuit in Figure 3.20

Figure 3.22: Simulation nonlinear S-parameter measurement for circuit in Figure 3.20. Blue is the input waveform reference, green is the reflection coefficient waveform.

The success of this drive network can also be seen in Figure 3.22, where the S11 waveform is nearly zero. The waveform is a bit ugly, but when its magnitude is as relatively small as it is (with peaks indicating a maximum reflection coefficient magnitude of .114, giving a VSWR of less than 1.3), this ugliness is of little consequence.

Figure 3.23: Output voltage waveform for circuit in Figure 3.20.

The output voltage waveform seen in Figure 3.23 shows a 3.8 dB increase in output signal over that from Figure 3.17. Therefore, this drive circuit is able to

appreciably increase gain, but it also increased current draw by a factor of 1.8, from 9.7 mA draw to 17.6 mA. However, for now, this apparent downfall will be ignored. As will be discussed in the next section, real world results show an opposite trend when the drive circuit is applied.

Circuit performance can also possibly be further increased by adjusting RE and CE. While sweeps revealed a lower RE of 9 ohms would increase conversion gain marginally, it also appreciably increased DC current consumption. Sweeps of CE also showed marginal improvements depending upon value, but 1 nF was already within a sweet spot, so the circuit in Figure 3.20 is the final schematic for the purpose of simulations.

4 Build Results and Analysis

The circuits developed in the previous section – from the most simple functional form present in Figure 3.9, to the full design in Figure 3.20– will be built and analyzed in this section. Note that the design developed in the previous section used simulations based upon a transistor model that was expected to be only accurate qualitatively, not quantitatively, so comparison between simulated and measured data will not be presented. The previous section is presented first as a design methodology utilizing readily available simulation software and device models, and now methodology for implementing, optimizing, and analyzing an analogous real-world design will be demonstrated.

4.1 Build Methodology

VHF design allows for freedoms in building and testing that otherwise would not be valid in higher frequency designs. Since even an eighth wavelength at the upper bound of this frequency range is still over 10 cm long, the transmission line effects of traces on the order of centimeters long have negligible effects on circuit performance, especially considering the design in this work is operating at the lower bounds of VHF.

With this in mind, a modular design methodology is used for building and testing. The design was split into four sections: transistor and biasing, input resonant circuitry, input impedance transform networks, and harmonic output terminations. This allows for the transistor and biasing network to be kept as a constant and keep the variables in the design constrained to the input and output circuitry. Modules are connected by end launch female SMA ports and male-to-male connectors, as seen in Figure 4.1, to minimize inter-module transmission line effects.

Figure 4.1: Circuit modules connected by male-to-male connectors

These modular interconnects are small features when considering Smith chart analysis. The ability to design modularly makes VHF a very attractive band for conceptual and theoretical design work. Once design concepts, theory, and measurements are well explored in VHF, designs can be scaled to higher frequencies. In this, a more complete understanding of circuit operation at any frequency can be gained.

4.2 Layout

Layout for the circuits was performed in Autodesk Eagle. The layout for the transistor and biasing can be seen in Figure 4.2.

Figure 4.2: Layout of transistor and biasing circuit

Power supply connections are made using pin headers. Layout for other modules are presented in Appendix A.

4.3 Circuit Manufacturing

Circuit manufacturing was performed in Portland State University's Electronics Prototyping Lab (EPL). The circuit was routed on 16 mil Rogers RO4003C [34] using the EPL's Accurate CNC A406 router. Vias were constructed from pressed 28-gauge copper wire. A microstrip construction was decided upon for ease of assembly with hand soldered surface mount components.

4.4 Testing Setup

The test bench for measuring the frequency multiplier is fairly simple. The circuit requires a single signal generator to supply excitation, and a single DC power supply to power the active device. Output signal analysis was mainly performed using a spectrum analyzer. Reflectometry was performed using an oscilloscope in conjunction with a pair of directional couplers, and results from this measurement will be compared with results from a VNA. The specific models of test equipment used can be seen in Table 4.1, and the testing setup can be seen in Figure 4.3.

Table 4.1: Test equipment

Equipment	Make and Model
DC Power Supply	Tektronix PS2520G
250 kHz to 20 GHz Signal Generator	Agilent E8251A
DC to 8 GHz Spectrum Analyzer	Tektronix RSA3308A
300 kHz to 20 GHz Vector Network Analyzer	Agilent E5071C
6 GHz Digital Signal Analyzer Oscilloscope	Agilent Infinium DSA80000B
2 X 10-1000 MHz Directional Coupler	Merrimac CRM-10-500

Figure 4.3: Testing setup

4.4.1 Nonlinear Reflectometry

As previously discussed in Section 2.2, S-parameters are a common tool for characterizing linear circuits. The VNA is able to quickly and easily measure S-parameters over a frequency range, but its shortcomings are similar to that of LTspice's AC analysis S-parameter readings. A VNA only stimulates one port at a time, so it's not guaranteed that proper steady state operation will be reached in a circuit such as the frequency multiplier being considered. Also, though a VNA sweeps through a range of

frequencies, each discrete data point is measured at a discrete frequency and doesn't consider the harmonic content of reflected signals.

As an alternative to the VNA, a system composed of two directional couplers and an oscilloscope is proposed as a nonlinear single frequency reflectometer. The operation of this reflectometer is analogous to the nonlinear reflection measuring signal source in Section 3.5. A simple block diagram of the measurement setup can be seen in Figure 4.4, and the directional couplers can be seen in Figure 4.5

Figure 4.4: Directional coupler reflectometry setup

Figure 4.5: Directional couplers set up in-line with signal generator and DUT

The back to back unidirectional directional couplers allow for the incident and reflected waves at the input of the device to be read directly off the input feed. Between the two couplers is a male-to-male SMA connector that adds minimal electrical length, and the cables from each coupled port to the oscilloscope inputs are matching, so the phase added to the incident and reflected waves is similar. In this way, it's possible to take approximate reflection coefficient measurements directly from the oscilloscope by

taking a simple ratio of reflected to incident waveform for the magnitude, and the taking the difference between the two signals' phases as the angle. Of course, there are magnitude and slight phase errors between the reflected and incident readings, but these errors were easily calibrated out using a short open load (SOL) 3-term calibration Octave script that was made specifically for this testing setup.

As seen in the simulations, reflections in nonlinear circuits can be rich in harmonics, and this measurement system allows transient waveforms of the reflected signal to be captured. The use of a modern oscilloscope further increases ease of analysis by providing live FFT processing of the received waveforms. With the information gained from these measurements, waveform engineering (like that often used on the device output circuitry) can be used for drive network design and analysis.

4.5 Frequency Multiplier Core: Biased Transistor

In this build, to start, the transistor core circuit without port reactive networks will be analyzed this. From this, conclusions can be made about the circuit in general without choosing a harmonic output. The schematic for the frequency multiplier core can be seen in Figure 4.6

Figure 4.6: Frequency multiplier core schematic

This circuit is very similar to the circuit in Figure 3.9, but with a DC blocking capacitor on both input and output, CE is tuned for better circuit operation, and RE is represented by its real world 200-ohm potentiometer. This circuit functions as a very basic comb generator, with tunable harmonic output through adjustment of RE. A sample output spectrum from this circuit can be seen in Figure 4.7.

Figure 4.7: Frequency multiplier core output for 7 dBm input power, RE tuned for maximal second harmonic output

Even though the circuit was tuned for second harmonic output, the periodic harmonic peaks can be seen, demonstrating the coinciding local maxima predicted by Figure 2.3. As expected, tuning the biasing for second harmonic output also accentuates fifth harmonic output. Though these relative peaks exist, the general trend of conversion gain is very much so that sizable losses are incurred as harmonic order increases. Even at the fifth harmonic, where biasing should be fitting for generation, approximately 15 dB of conversion loss is being incurred. This follows the expectation that higher harmonics are inherently going to be less efficiently generated, due to lower gain at higher frequencies, and circuit parasitics having more effect on the signal.

4.5.1 Port Networks: Variable Dependency

At this point in the design, measurements were made at the drive and load ports to determine dependencies that the ports had to variances in input power and changes in bias (through tuning RE).

Through testing it was found that depending on the port, a VNA could be used as a design and analysis tool, even if it could not necessarily always be trusted as a direct measurement tool. It was found that VNA S11 measurements of the circuit at this stage in development were mostly unhelpful and untrustworthy.

Figure 4.8: S11 of frequency multiplier core with 7 dBm input power. Red trace is for RE tuned for second harmonic generation (approximately 25 ohms), blue trace is for RE of 0 ohms, purple trace is for RE of 50 ohms. The VNA used for this and following measurements is the Agilent E5071C ENA Vector Network Analyzer. Frequency for traces increases clockwise about the smith chart.

The attempted measurements seen in Figure 4.8 are quite ugly as measurements go. Not only are the measurements not clean, smooth curves or series of loops as might be expected of a simple input circuit, but various spikes protrude from the squiggles at random. This behavior is likely due to the harmonic reflections at the input, which may either be confusing phase or magnitude information for the VNA.

Also, it can be gleaned that biasing has major effect on input impedance. The trend seems to be that as R_E is decreased, capacitance increases. If the collector-base varactor were the primary mechanism, the higher base current draw due to a lower R_E would mean a lower average base voltage, and hence a higher average collector-base voltage. For a varactor, then, a lower R_E would cause a lower capacitance – the opposite of the effect being seen. On the other hand, the diffusion capacitance would increase with the increased emitter current that results from lower R_E . Likely, the base voltage change due to bias change is relatively minor – on the scale of a hundred millivolts or so – while the emitter current draw is likely changing by tens of mA, which for a device that's drawing tens of mA is a lot. So, for changing bias, diffusion capacitance is the primary mechanism. However, due to the sporadic nature of these readings, this measurement and analysis must be taken with a grain of salt.

Figure 4.9: S11 of frequency multiplier core with RE tuned for second harmonic at 7 dBm input power. Red is 7 dBm input power, purple is 0 dBm, and blue is -7 dBm. Frequency for traces increases clockwise about the smith chart.

The data in Figure 4.9, is much more readable than that in Figure 4.8. The trend appears to roughly be that as input power increases, capacitance increases. With the nonlinear relationship between voltage and capacitance in varactors, it's likely that the larger input signals (and collector/output signals) are causing the collector-base voltage to

have a larger swing that encompasses nonlinearly larger capacitance values as the voltage swing gets linearly larger. So, the trend seen is that of increasing average capacitance.

On the output, readings are simpler and even more readable, mainly due to the inductor connected in shunt to the collector. This inductor absorbs much of the parasitic reactance that the transistor would otherwise supply. This leads to an S22 reading that is mostly agnostic to input power level and biasing, as seen in Figure 4.10.

Figure 4.10: S22 of frequency multiplier core for the same sweeps shown in Figure 4.8 and Figure 4.9. Frequency for traces increases clockwise about the smith chart.

4.6 Input Reflectometry and Drive Network

For the input, even the more readable traces in Figure 4.9 don't look quite right. So, nonlinear reflectometry can be used to see what's happening at the input in the time domain.

Figure 4.11: Reflected waveforms for input power of 7 dBm. Green is $R_E \approx 200$ ohms, blue is 100 ohms, red is 0 ohms.

As expected, there is some interesting behavior at the peaks of the reflected waveform. As the voltage reaches conduction, the voltage sags, then it appears as if the circuit has a delayed reaction and tries to compensate for the sagging. This results in a harmonically complex signal, as seen in Figure 4.12.

Figure 4.12: FFT of RE=0 reflected waveform seen in Figure 4.11. This signal has the most distorted waveform of the reflections.

Without a resonant circuit on the output, the spectrum of the input reflected waveform has a high fundamental component, then tapering higher harmonic components. No harmonic clearly stands out.

Even at this level, the input circuit discussed in the design section can be implemented to clean up and eliminate reflections. The results of applying just the parallel resonant circuit (Figure 4.13) can be seen in Figure 4.14 and Figure 4.15.

Figure 4.13: Multiplier core with input resonant circuit

Figure 4.14: Reflected waveforms of multiplier core circuit with input resonator for input power of 7 dBm. Green is $RE \approx 200$ ohms, blue is 100 ohms, red is 0 ohms.

Figure 4.15: FFT of RE=0 reflected waveform seen in Figure 4.14

The signals have been cleaned up considerably, regardless of the biasing condition. The spectrum of the RE = 0 signal has gone from the nearest harmonic being about 8 dB lower than the fundamental to separation being 20 dB. The amplitude between the three measured reflections are fairly consistent, with the RE = 0 trace having just a slight phase difference. Thus, the application of this LC tank circuit appears to have absorbed some of the parasitic variable reactances intrinsic to the transistor.

These waveforms were used to calculate reflection coefficients, and an approximate average coefficient of $.22 \angle 75$ was found. A 150 nH series inductor on the input supplied a sufficient impedance shift to almost perfectly eliminate reflections

and transform the input to 50 ohms (Figure 4.16). The resultant reflected waveforms (or absence thereof) can be seen in Figure 4.17.

Figure 4.16: Frequency multiplier core with full drive network

Figure 4.17: Reflected waveforms of multiplier core circuit with input resonator and reflection reduction for input power of 7 dBm. Green is $RE \approx 200$ ohms, blue is 100 ohms, red is 0 ohms.

Though the reflections don't appear to be fully eliminated, a maximum calibrated reflection coefficient of $.06 \angle -33$ was measured, giving a VSWR of 1.13. Though it's difficult to tell right now how this will affect targeted output terminated harmonic generation, it's at least evident that this drive network topology is capable of reducing input VSWR for a variety of nonlinearly operating circuits.

4.7 Frequency Doubler

Now that the frequency multiplier core has been verified to work as expected, an output network can be applied to target a specific harmonic; in this case, the second harmonic. The simple capacitive network used can be seen in Figure 4.18.

Figure 4.18: Full frequency doubler schematic

Once again, even if the VNA can't necessarily be trusted as a direct measurement device, it still proved useful in output network design. To ensure the output circuit's response was approximately centered on the second harmonic, S22 at 48 MHz was tuned to be close to the real line on the smith chart, and a limited load pull was used to move S22 back and forth along the real line until a conversion gain relative maxima was found. The resultant S22 plot for this termination can be seen in Figure 4.19.

```

m3
freq=48.08MHz
xA302_7R15..S(2,2)=0.368 / -178.256
impedance = Z0 * (0.462 - j0.012)

```

Figure 4.19: S22 for full doubler design, RE tuned to second harmonic generation, 7 dBm input power

The continued expected performance of the drive work can be verified by again observing the reflected waveforms in Figure 4.20. The reflection coefficient of the doubler with drive network is able to reduce reflections greatly, with a resultant reflection coefficient magnitude of .06, giving a VSWR of 1.13.

Figure 4.20: Input reflected waveform of doubler with (blue) and without (red) drive network for 7 dBm input power

4.7.1 Drive Network Performance Comparison

Now that the circuit is targeted on a specific harmonic, evaluating its figures of merit becomes meaningful. Throughout the evaluation of this circuit, metrics will be compared between the full schematic (Figure 4.18) and the circuit without drive network (Figure 4.21).

Figure 4.21: Doubler without drive network

The first figures of merit that will be evaluated are conversion gain, harmonic suppression, and efficiency. The measurements necessary for these metrics were taken in the form of spectrum analyzer readings. The outputs for the doubler with and without the drive network can be seen in Figure 4.22, with data from the test presented in Table 4.2.

Figure 4.22: Doubler output spectra for 7 dBm input without (left) and with (right) drive network

Table 4.2: Performance data for doubler with and without drive network. Input power is 7 dBm.

	Without Drive Network	With Drive Network
Current Draw	21 mA	15 mA
Fundamental Power	-5.0 dBm	-7.3 dBm
2 nd Harmonic Power	11.8 dBm	11.8 dBm
3 rd Harmonic Power	-12.3 dBm	-3.3 dBm
Conversion Gain	4.8 dBc	4.8 dBc
Harmonic Suppression	-16.8 dB	-15.0 dB
Collector Efficiency	8.0%	11.1%

Comparing these two spectra, both have virtually the same conversion gain.

Where their behavior diverges is in their harmonic suppression and efficiency. The difference of 1.8 dB in harmonic suppression is not very large. Also, subsequent filtering would likely be able to achieve any performance metric desired. The difference in efficiency figures, however, are meaningfully different. The doubler without drive network draws 40% more current than the doubler with the drive network, giving efficiency figures that are several percentage points better. This efficiency performance difference is likely due to the more efficient delivery of input power to the device base, and avoidance of base voltage sag. Also, note the change in spectra at much higher harmonics. The doubler with drive network tapers off more smoothly, while the doubler without the drive network has a less smooth spectra. This is likely due to the harmonic components present at the base of the doubler without the drive network. Reduced higher harmonic output may also be a factor in the increased efficiency of the doubler with drive network.

Next, the circuit can be evaluated on the metric of bandwidth. The full doubler circuit has a bandwidth of 9.4 MHz at the second harmonic output, with the center frequency being 49.3 MHz, giving a fractional bandwidth of 19%. Realistically, this metric isn't terribly interesting for this work's single ended design as the output network is inherently narrow band for harmonic suppression – high bandwidth designs exist, but this is not one of them. The bandwidth is mostly controlled by the Q of the input and output networks, and can be adjusted to achieve the bandwidth desired, albeit at the possible cost of other performance metrics.

Figure 4.23: Gain curves for doubler. Red is without drive network, blue is with. Solid is RE tuned to 7 dBm input power, dashed is tuned to 0 dBm input power.

Table 4.3: Doubler drive range data table. All power values are input referenced.

	Without Drive Network		With Drive Network	
Tuned to	7 dBm	0 dBm	7 dBm	0 dBm
Max Gain	8.8 dBc @ -1 dBm	10.0 dBc @ -2 dBm	7.0 dBc @ 2 dBm	7.0 dBc @ 2 dBm
Drive Range	-7 to 6 dBm	-7 to 4 dBm	-3 to 9 dBm	-3 to 9 dBm

Finally, drive range comes as the last metric. As defined in Section 2.1.3, the drive range is the range of input drive power over which conversion gain is within 3 dB of the maximum conversion gain at design frequency. The gain curves and data table can be seen in Figure 4.23 and Table 4.3 respectively. This data shows how the drive network is fit specifically for devices in nonlinear drive range. While the doubler without drive network has higher maximum gain, and more mobility of the gain curve with tuning, the doubler with the drive network has its gain curve centered higher. In the plot, it can also be seen that all the curves intercept at around 7 dBm in. After this point, the gain for the doubler without drive network tapers off at about -.8 dB per dB raised drive level, whereas the doubler with the drive network tapers at a lower -.5 dB per dB raised drive level. The doubler without drive network likely has better performance at lower drive levels due to constructive reflections at the transistor base allowing for more conduction, and the input termination may be more ideal for smaller signal operation. The doubler with drive network eliminates these reflections and trades them for more efficient power delivery in nonlinear operating conditions, making it more fit for high drive levels.

Through the data collected, it becomes clear that for the case of a doubler, the drive network presented provides performance increases in efficiency and higher input

power drive range, while not sacrificing meaningful amounts of harmonic suppression, bandwidth, or conversion gain.

4.8 Higher Order Harmonic Multipliers

As previously discussed, the benefit of using a parallel resonant drive network topology is that it works regardless of the multiplier order, since all circuit components in the drive network are designed for the fundamental frequency. With this in mind, harmonic output terminations were made for harmonics up to the sixth harmonic (144 MHz), with an additional double tuned termination at the sixth harmonic to display the capabilities of extra filtering on the output. Note that only limited load pull was performed for these output terminations, so these do not represent ideal terminations. The design for these terminations involved simply attempting to achieve approximately the same S_{22} (at the circuit's targeted harmonic) that was achieved with the doubler at 48 MHz, and slightly tuning the circuit for better conversion gain. The purpose of these terminations is to explore and analyze any circuit phenomena unique to higher order terminations and lower conversion gain operation. The higher harmonic output termination circuit schematics can be seen in Appendix A. Once again, results will be compared between the circuits with and without the drive network. Limited metrics will be shown in this section to highlight specific phenomena in these higher order multipliers.

4.8.1 Gain and Saturation Effects

Table 4.4: Performance metrics for higher order multiplier terminations with 7 dBm input power.

Multiplier Order (N)	3		4		5		6	
Drive Network	No	Yes	No	Yes	No	Yes	No	Yes
Conversion Gain (dBc)	1.0	2.3	-4.4	-2.6	-6.7	-4.9	-9.0	-8.5
Output Power at Nf_0 (dBm)	8.0	9.3	2.6	4.4	0.3	2.1	-2.0	-1.5
Harmonic Suppression (dB)	-11.9	-12.2	-7.9	-8.1	-6.3	-6.7	-7.1	-5.3
Collector Efficiency (%)	7.0	8.0	2.9	4.4	2.4	2.9	.5	.6

As seen in Table 4.4, similar trends to the doubler emerge. The multipliers with drive network consistently have better efficiency and gain, with harmonic suppression being mostly similar between multipliers with and without the drive network. So, the generality of the drive network design is proven.

Note that for several of the multipliers, there were multiple RE settings that supplied local gain maxima. The RE setting that drew the most current consistently had the best performance, except in the case of the quintupler, where the multiplier without the drive network performed better at a higher current, but that higher current and biasing point/conduction angle was not achievable with the multiplier with the drive network. Still, the multiplier with drive network and lower current biasing point had better performance than the multiplier without drive network at the higher current biasing point. The data presented in the table is for comparable biasing points/conduction angles.

4.8.2 Higher Order Frequency Multiplier Input Reflectometry

In the doubler, it was difficult to see how much the input reflected signal's spectra correlated with output spectra, due to the second harmonic only having one nearby harmonic peak to compare to. With higher order multipliers, the reflected spectra's design harmonic can be compared to its surrounding harmonic peaks to determine if there is correlation between reflected signal spectra and design output harmonic. The following measurements were made on multipliers without the drive network.

Figure 4.24: Reflected spectra of higher order multipliers with 7 dBm input power. Top left is 3rd order, top right is 4th, bottom left is 5th, bottom right is 6th.

Figure 4.25: Reflected waveforms of higher order multipliers with 7 dBm input power. Top left is 3rd order, top right is 4th, bottom left is 5th, bottom right is 6th.

From Figure 4.24 and Figure 4.25, it can be seen that each multiplication order has unique reflected waveform and spectra, with clear correlation between output frequency and spectra peaks. So, it can be reasoned that differing harmonic output terminations affect input reflection spectra, and/or some sort of signal transfer is occurring from output to input. Biasing condition, however, is also likely a major mechanism in reflected spectra. The multipliers of order 3-5 were biased to draw 10 mA or less, while the 6th order multiplier was biased to 14 mA. The reflected spectra for that multiplier shows significantly more lower order harmonic content than other multipliers. The 6th order multiplier spectrum has the 6th and lower harmonics higher than -20 dBm.

For all other multipliers, only the targeted harmonic, and sometimes the immediately surrounding harmonics, are higher than -20 dBm.

Regardless of differing harmonic content of reflections, the drive network was well able to perform as expected. The input reflection coefficients can be seen in Table 4.5. With a maximum reflection coefficient of .059, it's plain to see that reflections have been aptly reduced.

Table 4.5: Reflection coefficient for higher order frequency multipliers with drive network and 7 dBm input power

Harmonic Order	Reflection Coefficient (S11)
3rd	.052 $\angle$ -75.5 °
4th	.050 $\angle$ -46.6 °
5th	.051 $\angle$ -42.5 °
6th	.059 $\angle$ -86.4 °

4.8.3 Double Tuned Circuit

To show how the questionable spectrum of previously presented output stages can be easily cleaned up, the double tuned output termination in Figure 4.26 is applied to the frequency multiplier core. This circuit was adapted from designs present in Dr. Campbell's white paper on VHF signal sources [39].

Figure 4.26: Double tuned output termination

This circuit works through two parallel LC tank circuits formed from trim capacitor C1 and the inductor on the multiplier's collector, and trim capacitor C2 and inductors L1 and L2. These two tank circuits are coupled through the low capacitance C3. This low coupling capacitance allows for each tank circuit's impedance to be more independent of the other, making the tuning process easier. This double tuned circuit allows for suppression of non-target harmonics, as seen in Figure 4.26 and Figure 4.27.

Performance differences are hard to spot at this point. The gain of the multiplier with drive network has slightly higher gain, but slightly worse harmonic suppression. Note that with tuning, the multiplier with drive network harmonic suppression figure can be improved to match or exceed the multiplier without, at the cost of some of the extra gain. At this high frequency, with such lossy multiplication, differences in efficiency can be hard to measure, but the multiplier with drive network is slightly more efficient than the one without.

Figure 4.27: Output frequency spectrum of frequency sextupler with drive network and double tuned output circuit seen in Figure 4.26. Input power is 7 dBm.

Table 4.6: Performance data for frequency sextupler with double tuned output circuit seen in Figure 4.26. Input power is 7 dBm

	Without Drive Network	With Drive Network
Conversion Gain (dBc)	-15.1	-14.4
6 th Harmonic Output Power (dBm)	-8.1	-7.4
Harmonic Suppression (dB)	-26.7	-25.0
Collector Efficiency (%)	0.1	0.1

Readings for the reflected input waveform were also taken but are not reported as they are very similar to readings taken for the previous sextupler. Similarly, the frequency multiplier with drive reflection has a small reflection coefficient magnitude of .06 at the input. So, once again, the pattern of the drive network improving performance and reducing input reflections prevails.

5 Conclusion

A general design methodology for a simple single-ended BJT frequency multiplier of any harmonic order has been presented. Through most of this work, a simple output network was used to allow focus to be centered on the oft-ignored drive network. It was found that a parallel LC tank circuit with input reflection reduction through impedance transformation was able to consistently increase conversion gain and efficiency, and allowed for better performance for higher input powers, while sacrificing some performance in more small-signal operating regions. The LC tank circuit also allows device intrinsic parasitics that are affected by drive level and bias to be absorbed into the tank circuit's reactance, allowing for less variability in the drive network design. For multistage multipliers, the tank circuit can act as an additional filtering stage, with the Q of the tank adjusted for required harmonic suppression.

5.1 Higher Frequency Designs

For higher frequency designs using this design methodology, it may be wise to pay more attention to reverse leakage of harmonics in the transistor. At VHF, transistors have relatively good reverse isolation, but as frequency goes up, signals on the collector and emitter of a BJT increasingly find their way to the device base. This may require targeted termination of prominent harmonics. It is still recommended that some form of bandpass filtering is performed on the base signal due to the harmonics that are present due purely to device nonlinearities. Especially in devices drawing relatively large current, device nonlinearities can cause wider band harmonic content in the input reflected signal.

5.2 General Applicability to Nonlinear Circuits

This design methodology and its considerations do not only apply to frequency multipliers; frequency multipliers just stand as an interesting subset of nonlinear circuitry. Consider that a “first order frequency multiplier” using the design methodology in this work would simply be a class C amplifier. As was shown, device nonlinearities at high drive levels, and explicitly nonlinear circuitry such as class C amplifiers, cause possibly difficult to deal with and detrimental harmonic reflections. So, filtering transistor base waveforms (or otherwise harmonically terminating these reflections) can be an added tool in a designer’s toolkit.

Also, the measurement and simulation tools shown hold wider applicability to circuitry beyond the nonlinear. The LTspice reflection measurement circuit (Figure 3.8) can be used in any simulation to get reflection coefficient data on any circuit, even when simulation DC solutions don’t represent accurate transient biasing conditions. Along with its use as a nonlinear device measurement instrument, the reflectometry setup also serves as a simple, cost effective single frequency VNA. Hence, the measurement, testing, and design methods represented in this paper have wide applicability.

5.3 Future Work

Preferably, study on this work could be continued with a proper live load- and source- pull setup to further explore the reflectometry at the device’s input. In this way, performance maxima that were otherwise possibly not found in this work could be further explored, and waveform engineering could be more effectively performed on the transistor’s input.

5.4 Closing Remarks

This work has been a great opportunity of academic growth for the author. Not only is this the longest, most in depth project the author has completed to date, many concepts were introduced, and lessons were learned.

One of the lessons was that one should always question measurement instruments, and whether they are applicable to what is being measured. The VNA – an amazing piece of measurement technology – stands as a prime example of this in respect to the nonlinear circuitry explored. The VNA input measurements shown in this work does not begin to tell the full story, and additional measurements were required to get a better picture. In the end, it was found that simple, well thought out, custom measurement setups could be used to get unique measurements to aid in analysis.

This thesis also provided first time experience in working with devices in large signal operation, and the nonlinearities that come along with that. With this came an exploration of device parasitics that required a more apt look into practical device conceptualization.

This work has given the author a chance to go in depth on a subject, and truly explore its intricacies. This thesis will be a major addition to the author's portfolio and serves as a fitting capstone to a Master of Science degree in electrical engineering at Portland State University.

References

- [1] K. Yuk, C. Wong, and G. R. Branner, "Design of a high power x-band frequency tripler using a AlGa_N/Ga_N HEMT device," in *The 40th European Microwave Conference*, 2010, pp. 612–615.
- [2] G. Hetland and R. R. Buss, "Microwave oscillator stability," *Trans. IRE Prof. Group Electron Devices*, vol. 1, no. 2, pp. 1–8, Apr. 1954.
- [3] A. Boyajian, "Theory of D-C. Excited Iron-Core Reactors and Regulators," *Trans. Am. Inst. Electr. Eng.*, vol. XLIII, pp. 919–936, Jan. 1924.
- [4] "Band Plan," ARRL. [Online]. Available: <http://www.arrl.org/band-plan>. [Accessed: 22-Nov-2018].
- [5] R. M. Cerda, "Frequency Multiplication Techniques," *Microwave Product Digest*, Apr-2013. [Online]. Available: http://www.crystek.com/documents/appnotes/Frequency_Multiplication_Techniques.pdf. [Accessed: 15-Jul-2018].
- [6] K. Gheen, "Phase Noise Measurement Methods and Techniques," *Agilent Technologies*, 2012. [Online]. Available: https://www.keysight.com/upload/cmc_upload/All/PhaseNoise_webcast19Jul12.pdf. [Accessed: 29-Nov-2018].
- [7] P. Horowitz, *The Art of Electronics*, 3rd ed. New York, NY: Cambridge University Press, 2015.
- [8] K. Yuk and G. R. Branner, "Advances in active microwave frequency multipliers," in *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011, pp. 1–4.
- [9] R. Rick and C. Lin, "Telemetry transmitter frequency stability evaluation," in *2016 IEEE Aerospace Conference*, 2016, pp. 1–8.
- [10] D. M. Pozar, *Microwave Engineering*, 4th ed. Hoboken, NJ: Wiley, 2012.
- [11] J. Gonda and J. M. Kiker, "The AR6A Single-Sideband Microwave Radio System: Microwave carrier supply," *Bell Syst. Tech. J.*, vol. 62, no. 10, pp. 3391–3408, Dec. 1983.
- [12] P. Srivastava, P. P. Kumar, and C. V. N. Rao, "Design and development of multi-frequency comb generator for space borne microwave active sensors," in *2008 International Conference on Recent Advances in Microwave Theory and Applications*, 2008, pp. 445–447.
- [13] K. Yuk, G. R. Branner, and C. Wong, "High power, high conversion gain frequency doublers using SiC MESFETs and AlGa_N/Ga_N HEMTs," in *2010 IEEE MTT-S International Microwave Symposium*, 2010, pp. 1008–1011.
- [14] J. M. Cloeren and C. Hamilton, "Precision crystal oscillator for interplanetary radio science," in *Proceedings of 1996 IEEE International Frequency Control Symposium*, 1996, pp. 761–766.
- [15] Y. Zheng and C. E. Saavedra, "A Broadband CMOS Frequency Tripler Using a Third-Harmonic Enhanced Technique," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2197–2203, Oct. 2007.

- [16] E. Sandhiya, D. Denis, and I. C. Hunter, "Novel Design Methodology for High Efficiency Class E Microwave Frequency Triplers," in *2006 IEEE MTT-S International Microwave Symposium Digest*, 2006, pp. 1825–1828.
- [17] H. K. Gummel and H. C. Poon, "An integral charge control model of bipolar transistors," *Bell Syst. Tech. J.*, vol. 49, no. 5, pp. 827–852, May 1970.
- [18] J. Fielding, "Transistor Frequency Multipliers," *VHF Communications*, no. 4, 2006.
- [19] C. Rauscher, "High-Frequency Doubler Operation of GaAs Field-Effect Transistors," *IEEE Trans. Microw. Theory Tech.*, vol. 31, no. 6, pp. 462–473, Jun. 1983.
- [20] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston: Artech House, 2006.
- [21] Y. Park, "Class-F Technique as Applied to Active Frequency Multiplier Designs," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3212–3218, Dec. 2009.
- [22] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. 10, no. 3, pp. 168–176, Jun. 1975.
- [23] P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3196–3204, Dec. 2009.
- [24] F. H. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 8, pp. 1462–1468, Aug. 2001.
- [25] J. E. Johnson, G. R. Branner, and J.-Mima, "Design and optimization of large conversion gain active microwave frequency triplers," *IEEE Microw. Wirel. Compon. Lett.*, vol. 15, no. 7, pp. 457–459, Jul. 2005.
- [26] P. Kutín and M. Kasal, "Novel Optimization Method of Active Frequency Multiplier Utilizing Harmonic Terminating Impedances with DGS," *2006 Int. Conf. Microw. Radar Wirel. Commun.*, vol. 15, no. 2, pp. 6–11, 2006.
- [27] D. G. Thomas and G. R. Branner, "Optimization of active microwave frequency multiplier performance utilizing harmonic terminating impedances," *IEEE Trans. Microw. Theory Tech.*, vol. 44, no. 12, pp. 2617–2624, Dec. 1996.
- [28] A. Raffo, V. Vadalà, G. Bosi, F. Trevisan, G. Avolio, and G. Vannini, "Waveform engineering: State-of-the-art and future trends (invited paper): RAFFO et al.," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 27, no. 1, pp. 1–16, Jan. 2017.
- [29] P. J. Tasker, "Practical waveform engineering," *IEEE Microw. Mag.*, vol. 10, no. 7, pp. 65–76, Dec. 2009.
- [30] "WINGONEER Capacitor 0603 (0.5pF-2.2uF) 90 Value x 50pcs = 4500pcs SMD SMT Capacitor Combo Sample Book Kit: Amazon.com: Industrial & Scientific." [Online]. Available: <https://www.amazon.com/gp/product/B072FNVRKP/>. [Accessed: 07-Mar-2019].
- [31] "OneBelief [L0603] SMD Inductor (1NH-22UH) 52 value x 50 pcs Combo Sample Book [Accuracy Tolerance 5%] [2600 PCS]: Gateway." [Online]. Available: <https://www.amazon.com/gp/product/B07332DJCR/>. [Accessed: 07-Mar-2019].
- [32] "Yobett 0603 (15pF-1uF)&(0 ohm-2M ohm) 5% 80 Value 3725pcs SMD Resistor and Capacitor Combo Kit: Amazon.com: Industrial & Scientific." [Online].

- Available: <https://www.amazon.com/product/dp/B00IN2314E/>. [Accessed: 07-Mar-2019].
- [33] “Amazon.com: Joe Knows Electronics Semiconductor Kit (320 Transistors & Diodes): Toys & Games.” [Online]. Available: <https://www.amazon.com/gp/product/B00GPZQ5B2/>. [Accessed: 26-Nov-2018].
- [34] “Rogers RO4000 Series Laminates Data Sheet,” *Rogers Corporation*, 2018. [Online]. Available: <https://www.rogerscorp.com/documents/726/acs/RO4000-LaminatesData-sheet.pdf>. [Accessed: 01-Jan-2019].
- [35] “SS9018 AM/FM Amplifier, Local Oscillator of FM/VHF Tuner,” *Fairchild Semiconductor Corporation*, 2002. [Online]. Available: <https://joeknowselectronics.com/wp-content/uploads/2019/01/SS9018.pdf>. [Accessed: 29-Nov-2018].
- [36] “Standard.bjt - LTwiki-Wiki for LTspice,” *Linear Technology Corporation*, 2012. [Online]. Available: <http://ltwiki.org/index.php?title=Standard.bjt>. [Accessed: 10-Nov-2018].
- [37] R. Campbell, “Reflections.” [Online]. Available: <http://web.cecs.pdx.edu/~campbell/Lecture1Reflect.pdf>. [Accessed: 18-Feb-2019].
- [38] “Chip Inductors (Chip Coils),” *Murata Manufacturing Co.*, 2017. [Online]. Available: <https://www.murata.com/~media/webrenewal/support/library/catalog/products/inductor/chip/o05e.ashx>. [Accessed: 29-Nov-2018].
- [39] R. Campbell, “2m Weak Signal Sources,” Jan-2018. [Online]. Available: <http://web.cecs.pdx.edu/~campbell/Sources.pdf>. [Accessed: 24-Feb-2019].

Appendix A

Figure 0.1: Pi module layout.

Figure 0.2: Reflection reduction circuit. Uses layout in Figure 0.1.

Figure 0.3: 72 MHz output circuit. Uses layout in Figure 0.1.

Figure 0.4: 96 MHz output circuit. Uses layout in Figure 0.1

Figure 0.5: 120 MHz output circuit. Uses layout in Figure 0.1

Figure 0.6: 144 MHz output circuit. Uses layout in Figure 0.1.

Figure 0.7: Parallel module layout.

Figure 0.8: Drive network LC tank circuit. Uses layout in Figure 0.7.

Figure 0.9: Multi-pi module layout.

Figure 0.10: Double tuned output circuit. Uses layout in Figure 0.9.

Figure 0.11: General purpose module layout.

Figure 0.12: 48 MHz output circuit. Uses layout in Figure 0.11.