Circuit Implementation of a High-speed Continuous-time Current-mode Field Programmable Analog Array (FPAA)

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THESIS APPROVAL

The abstract and thesis of Osama K. Shana'a for the Master of Science in Electrical and Computer Engineering were presented May 10, 1996, and accepted by the thesis committee and the department.

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ABSTRACT


Title: Circuit Implementation of a High-Speed Continuous-Time Current-Mode Field Programmable Analog Array (FPAA).

The growing interest in programmable analog circuits has led to the development of Field Programmable Analog Arrays (FPAA). An FPAA consists of:
1) a programmable cell that can be reconfigured to perform several analog functions.
2) an architecture that interconnects a number of copies of the programmable cell.

In this thesis, the full monolithic circuit implementation of the analog part of the programmable cell is presented. Chapter I gives an introduction to the idea of FPAA and introduces the FPAA architecture and the cell block diagram. Chapter II deals with the design and verification of a differential current-mode four-quadrant multiplier. The weighting-summing circuit with the normalizing stage is discussed in Chapter III. Chapter IV presents the design of a current-mode low-voltage programmable integrator-gain circuit.

Programmability was achieved by changing the bias current in the designed circuits; no analog switches were used in the signal path. This shows no effect on the performance of the circuits. The presented programming method, however, relies on the
availability of a programmable current source with a storage capability. The design of this current source is discussed in chapter V. Conclusions are summarized in Chapter VI.

The presented designs throughout the whole thesis were supported by detailed analytical derivations with the necessary SPICE simulations to verify the performance.
CIRCUIT IMPLEMENTATION OF A HIGH-SPEED CONTINUOUS-TIME CURRENT-MODE FIELD PROGRAMMABLE ANALOG ARRAY (FPAA)

by

OSAMA K. SHANA’A

A thesis submitted in partial fulfillment of the requirements for the degree of
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CHAPTER I

INTRODUCTION

1.1 The idea of Field Programmable Analog Array (FPAA):

Over the past two decades, there has been a growing interest in programmable circuits. The interest in a single IC that can be reconfigured to perform several digital functions has led to the success of circuits like Programmable Logic Arrays (PLAs) and Field Programmable Gate Arrays (FPGAs).

Analog circuits on the other hand lagged digital circuits due to the challenge of introducing programmability without degrading the performance. But the need for flexible, programmable low cost circuits kept the research in Field Programmable Analog Array (FPAA) alive.

Several FPAA solutions have been presented in the literature. Tunable filters, were the first form of programmable analog circuits in which the cutoff frequency and quality factor are tuned (programmed) by changing certain bias condition. Neural Networks are another popular class of programmable analog circuits. In neural networks, a set of simple analog cells (neurons) are interconnected in a fixed architecture. Tunable filters and neural networks do not meet the full programmability criteria since their topologies are fixed and only the transfer function coefficients are
programmable. As pointed out in the literature [11], it would be advantageous to devise an IC strategy whereby the analog network topology is user programmable, using some type of reusable generic prototyping medium. Moreover, the programmable IC to be built should be continuous-time for best electrical performance and speed, and consequently can address many desired applications. In order to accomplish this, two things are required:

1. A fully programmable cell which can perform different analog functions according to a programming code.

2. An efficient architecture which interconnects a number of these cells. This architecture should contribute minimally to signal interference, cross talk and noise.

Field Programmable Analog Arrays, FPAAs, were first introduced by Lee and Gulak [1]. The idea was to implement a universal programmable cell that can be programmed to perform several analog functions. The complete FPAA consists of a number of these cells connected with each other according to a programmable architecture. The presented FPAA was implemented in CMOS and programmability was implemented through analog switches in the signal path which enable/disable several parts of the cell. This however degraded the frequency response of the cell due to the finite ON resistance and parasitic capacitance of the switches.
Another improved FPAA cell block diagram and architecture was presented by Pierzchala and Perkowski [2], and is shown in Fig. 1(a) and (b) respectively. The cell processes current-mode, differential signals. Its core consists of high-speed continuous-time current-mode circuits which implement the different blocks. Programmability in this approach is achieved by electronically controlling the bias of the different stages. No switches were used. This speeds up the cell and sustains good electrical performance.

Fig. 1(a) FPAA cell block diagram

Fig. 1(b) The FPAA architecture
In analog systems, a cell usually contains a gain element, some linear time-domain operation such as summation and integration, and some nonlinear block to enhance functionality such as multiplication. The suggested cell of Fig. 1(a) has all this. It is capable of receiving four different inputs from neighboring cells in the FPAA structure presented by Pierzchala et. al. [3] and shown in Fig. 1(b), two sets of weighted copies of those inputs are generated via a weight-sum block whose output is fed then to a multiplier which can be also programmed to be a "multiply by 1" stage. The multiplier’s output is fed to a programmable gain-integrator block which can be programmed to work as a gain stage or as an integrator or both. Several copies of the output of the cell are generated to be fed to the four neighboring cells. With this suggested block diagram of the cell and the corresponding FPAA structure, it was shown that the FPAA is capable of implementing several analog functions[4], and the user can switch easily from one function to the other by reprogramming the FPAA.

The following is a list of some possible functions that can be realized:

1. \( Y = X_i \)
2. \( Y = k( \sum_{w_i \in W_{1or2}} w_i X_i) \)
3. \( Y = kX_i X_j \)
4. \( Y = kX_i^2 \)
5. \( Y = k( \sum_{w_i \in W_1} w_i X_i)( \sum_{w_j \in W_2} w_j X_j) \)
6. \( Y = k \ min(X_1, \ldots, X_n) \)

7. \( Y = k \ max(X_1, \ldots, X_n) \)

8. \( Y = kY_{i-7} \frac{1}{s + a} \), \( Y_{i-7} \) is any of the above functions (1 to 7)

9. \( Y = k \ sign(Y_{i-8}) \), \( Y_{i-8} \) is any of the above functions (1 to 8)

An eighth order elliptic filter has also been demonstrated as an example of a practical application of the FPAA [4]. Fig. 2(a) shows the schematic of the eighth order elliptic band-pass filter realized as an OTA-C ladder. Instead of voltage-mode cells (OTA-C), current-mode cells of the programmable device (FPAA) are used to implement the same filter. The cells are arranged as shown in Fig. 2(b). Each cell works in integration mode except the cell 6 which realizes "infinite" gain. Cells 1 and 10 realize lossy integrators. Unused cells and interconnects are marked in dotted lines.

Most ladder and biquad filters can be mapped into the presented FPAA structure which provides the way to realize different continuous-time filters by means of programmability.
Fig. 2(a) Schematic of an eighth order elliptic band-pass OTA-C ladder filter

Fig. 2(b) Current-mode implementation of the filter in 2(a) using the FPAA
There are many other potential applications for a successful FPAA. In personal communication services, FPAA technology would allow the design of a single universal hand-held set that can be reprogrammed for various standards around the world. This in turn would lower the price of such a set dramatically and could be the first step towards unifying the world's standards.

Disk drives also could benefit from such an FPAA, since this could be the solution for a single programmable analog filter that can be used instead of the two or three filters that are currently used. Since these filters do not operate simultaneously, replacing them with a single FPAA programmable filter where the transfer function and its coefficients can be dynamically reprogrammed, appreciable saving in space and power could result.

1.2 Thesis objective:

In this thesis, we have implemented the several analog blocks that comprise the FPAA cell shown in Fig. 1(a); which means the full monolithic implementation of the weight-sum block, the multiplier block and a redesign of the integrator-gain block suggested by Pierzchala [2] for reduced complexity and lower power consumption. We also have designed a programmable-storage current source which is the key to programmability in the entire design.
Key issues in the design of these blocks were linearity, dynamic range, bandwidth and overall response vs. programmability, since programmability should be accomplished without jeopardizing the performance of the cell. The trade off between circuit complexity and available power budget will also influence the design technique.

The design was accompanied by detailed mathematical derivations with the necessary SPICE simulations to show the performance. The Tektronix/MAXIM CPI 8GHz bipolar process was used to implement the circuits; simulations were carried out using the Tektronix Analog Design System, ADS.
CHAPTER II
MULTIPLIER CIRCUIT DESIGN

2.1 Circuit specifications:

An ideal four-quadrant multiplier would perfectly relate its output to its two inputs by the expression

\[ Z = KXY \]

where \( K \) is a constant for all values of \( X \) and \( Y \) including polarity.

As stated by Gilbert [5], all practical multipliers suffer from one or more of the following shortcomings:

1. A nonlinear dependence on one or both of the inputs.
2. A limited rate of response.
3. A residual response to one input when the other is zero.
4. A scaling constant that varies with temperature and/or supply voltage.
5. An equivalent DC offset on one or both inputs.
6. A DC offset on the output.

Much work has been done to design multipliers exploiting the non-linear characteristics of the devices, like the square-law device, or the exponential characteristic of a diode connected transistor. This kind of multiplier, however, suffers
from strong temperature dependencies and/or a small dynamic range for any degree of useful linearity.

The multiplier circuit we need for our FPAA cell should minimize these limitations and strive to encompass the following specs.:

1) good linearity characteristic over a wide dynamic range of operation.
2) low sensitivity to circuit device parameter variation ($\beta$, $I_s$, $R_e$, etc.) and very low temperature dependence.
3) It should be a current mode four-quadrant multiplier so it will be compatible with the other blocks of the FPAA cell. This will also give a wide band frequency response.

2.2 Multiplier circuit design:

The circuit that meets the above specifications better than any other circuit is the venerable Gilbert four-quadrant multiplier [5] as shown in Fig. 3. The circuit consists of two pairs of transistors, $Q_2$-$Q_3$ and $Q_5$-$Q_6$, having their collectors crossed-connected, and driven on the base by a further pair of diode connected transistors, $Q_1$-$Q_4$. It is the addition of this pair of diodes that linearizes the circuit. The $X$ signal input is the pair of currents $xI_B$ and $(1-x)I_B$. The $Y$ signal input is $yI_E$ and $(1-y)I_E$, where $x$ and $y$ are dimensionless variables varying between zero and one.
Fig. 3. The basic current-mode four-quadrant Gilbert multiplier[5].

It has been shown [7] that the ratio of the emitter currents in the $Q2-Q3$ and $Q5-Q6$ pairs is the same as that in the $Q1-Q4$ pair, independent of the magnitudes of $I_B$ and $I_E$ (neglecting second order effects). We can write:

$$V_{s_1} - V_{s_4} + V_{s_3} - V_{s_2} = 0$$  \hspace{1cm} (1)

$$V \ln \frac{I_{s_1}}{I_{s}} - V \ln \frac{I_{s_4}}{I_{s}} + V \ln \frac{I_{s_3}}{I_{s}} - V \ln \frac{I_{s_2}}{I_{s}} = 0$$  \hspace{1cm} (2)

If $I_{s_1} = I_{s_2} = I_{s_3} = I_{s_4} = I_s$

$$\Rightarrow \frac{I_s I_{s_3}}{I_{s_2} I_{s_4}} = 1$$  \hspace{1cm} (3)

substituting the correct current values yields

$$\frac{x I_B (y I_E - I_c)}{I_{c_2} (1-x) I_B} = 1$$  \hspace{1cm} (4)
\[ I_{c2} = xyI_E \] (5)
\[ I_{c3} = (1-x)yi_E \] (6)

Similarly, it can be found that
\[ I_{c5} = x(1-y)i_E \] (7)
\[ I_{c6} = (1-x)(1-y)i_E \] (8)

The differential output current is
\[ I_{out} = I_{c2} + I_{c6} - I_{c3} - I_{c5} \] (9)

Thus the normalized output \( Z \) is
\[ Z \approx \frac{I_{out}}{I_E} = xy + (1-x)(1-y) - (1-x)y - (1-y)x \] (10)
\[ = 1 - 2y - 2x + 4xy \] (11)

It is seen that the circuit is balanced when \( x \) and \( y \) are equal to 0.5. If we apply bias currents such that the bipolar signals \( X \) and \( Y \) can be used as the inputs, with
\[ X = 2x - 1 \] (12)
\[ Y = 2y - 1 \] (13)

yields
\[ Z = XY. \] (14)

where \( X \) and \( Y \) are in the range -1 to +1.
This is the exact large-signal analysis, with no assumptions about temperature.

We did, however, assume that the transistors have:

1) perfectly matched emitter diodes.
2) perfect exponential characteristics (no ohmic resistance).
3) infinite $\beta$, i.e. no base currents.

The transistors used for the $Q1-Q4$ should be biased to provide as low an input impedance as possible. Moreover, the $Q3-Q5$ and $Q2-Q6$ transistor pair should provide as large an output impedance as possible. The $X$ and $Y$ input signals should see a symmetrical input impedance.

We will use the CPI process' minimum size npn device for the cell's core. This will save both area and power. We will bias these devices at 200$\mu$A for maximum current gain $\beta$. The resulting resistance for the diode connected transistors, assuming the temperature $T=25^\circ$C, will then be around 130$\Omega$, which is acceptably low as the input impedance of the multiplier.

The Gilbert four-quadrant multiplier circuit with the necessary biasing sources is shown in Fig. 4. Note that $Q20-Q21$ represent the input stage of the gain-integrator circuit which is attached to the output of the multiplier.
Fig. 4 The Gilbert four-quadrant multiplier with the necessary bias

Inspection of the circuit in Fig. 4 shows that three reference currents are required to control the biasing of the whole circuit. In the normal multiplication mode, $I_{ref1}$, $I_{ref2}$ and $I_{ref3}$ are set equal to each other; this sets $I_B = I_E$. Note that the multiplier has to be designed so it can be set to a “multiply by 1” mode where it behaves as a buffer for the $X$ input. In this case, $I_{ref2}$ is set to zero and the value of $I_{ref3}$ is set to be twice the value of $I_{ref1}$ so that $I_B$ remains equal to $I_E$ to get the multiply by 1 value.
$Q_1$-$Q_4$ and $Q_2$-$Q_3$-$Q_5$-$Q_6$ represent the basic Gilbert multiplier. $Q_{11}$ and $Q_8$ provide bias current for $Q_1$ and $Q_4$ respectively (that sets the bias current $I_B$). $Q_{14}$ and $Q_{16}$ provide the emitter bias current $I_E$. $Q_9$ and $Q_{10}$ provide the collector bias currents for the four transistors $Q_2$-$Q_3$-$Q_5$-$Q_6$. $Q_{17}$ and $Q_{18}$-$Q_{19}$ supply base current for the pnp and npn bias transistors respectively. Note that the emitter voltage of $Q_2$, $Q_3$, $Q_5$ and $Q_6$ is approximately at ground potential. This will give a $V_{CE}$ voltage for these transistors of approximately 0.78 V.

When $y = x = 0.5$, the circuit is balanced and each of the four transistors $Q_2$-$Q_3$-$Q_5$-$Q_6$ conducts $0.25I_E$. If $y = 0.5$ and $x = 0$, $Q_6$ and $Q_3$ will share all the emitter current $I_E$. If $x = 0.5$ and $y = 0$, $Q_5$ and $Q_6$ will share $I_E$. For 100% mismatch, $y = x = 0$, $Q_6$ will conduct all $I_E$ with all other transistors of the basic cell being cut-off ($Q_5$ will be the case for $x = +1$ and $y = 0$; $Q_2$ if $x = +1$ and $y = +1$; $Q_3$ for $x = 0$ and $y = +1$).

Note that the overall current swing is controlled by changing the bias currents. This circuit should be biased so that each transistor conducts a quiescent current of 200µA for maximum $\beta$ and $f_t$; we can however lower the bias current for power saving purposes, but that will result in lowering the speed of the circuit.

2.3 Circuit simulation:

Several types of simulations should be carried out to investigate the performance of the multiplier circuit. We will simulate and analyze the transfer curves,
frequency response and large signal input and output impedance. We will also examine the effect of the mismatch of some circuit parameters, like the emitter resistance and the device saturation current, on the linearity of the circuit.

2.3.1 The transfer curves:

What we mean by "transfer curves" is the set of curves relating the output of the multiplier to one of its inputs for a fixed DC value at the other input. These sets of curves are important to measure the linearity of the multiplier. The nonlinearity of the multiplier (some times called the linearity error) is defined as the maximum difference between the actual and the "best straight-line" theoretical output for all pairs of X and Y input values.

The linearity error usually is specified as a percentage of full scale. Thus, for example, a 1% linearity error in a multiplier with ±200µA output current means that the output will not deviate more than ±2µA from the best fit straight line for the maximum deviation of any one input with the other input held constant [13].

To generate the transfer curves, two differential current signals are applied at the X and Y inputs, respectively. Note that the differential signal at the X input can have current values from -I_B to +I_B; similarly, the signal at the Y input can have values between -I_E to +I_E. The reference current is set to 200µA and for generating the transfer curves, we will sweep the X input from -500µA to +500µA for three values
of the \( Y \) input equal to \( \pm 0.5I_E, 0 \) and \( \pm I_E \) and display the differential output current. The output current is taken to be the difference between the currents flowing in the two diode connected transistors which represent the input stage of the next stage. The results are shown in Fig. 5(a).

The circuit demonstrates excellent linear behavior over a wide dynamic range as can be seen in Fig 5(b) which displays the derivative of the output characteristics with respect to the input.

![Graph](image)

**Fig. 5(a)** The transfer curves set for the Gilbert four-quadrant multiplier; the differential output current is displayed vs. the \( X \) input for fixed increment values of the \( Y \) input.
Fig. 5(b) Derivatives of the set of curves in 5(a) which shows the gain of the multiplier over the dynamic range, linearity error was found to be 0.9% over a dynamic range of 399µA (99.7% of the bias current).

From Fig. 5(a), the linearity error was measured to be 0.9% over a dynamic range of 399µA (which is 99.7% of the bias current!) This shows how linear the multiplier is specially when looking to the wide dynamic range which is close to the bias current of the circuit.

### 2.3.2 Frequency response:

The high-frequency capability of an analog multiplier is described in terms of its bandwidth. Simulating the response of multipliers and the degree these simulations
reflect the actual behavior of the circuit is one of the main problems that faces designers due to the non-linear operation of mixing or multiplication. The mixer in Fig. 3, however, can be considered as a "Linear" multiplier in which it behaves as an amplifier for one of the inputs with a fixed DC value at the other input that sets the gain; this makes the linearizing AC analysis we used to predict the frequency response of the multiplier valid.

With fixed DC currents of $\pm 0.5I_E$ and $\pm I_E$ at the $Y$ input, the frequency response of the multiplier with $X$ being the AC input is shown in Fig. 6(a). It can be seen from Fig. 6(a) that the circuit has a wide band response (2.18 GHz) relative to the $f_t$ of the transistors for this process. The circuit shows only a small sensitivity to the DC operating point of the $Y$ input.

Fig. 6(b) shows the frequency response of the multiplier for fixed DC values at the $X$ input with $Y$ being the AC input. The bandwidth ranges between 3.4-4 GHz. Note that by comparing the frequency response in Fig. 6(a) and (b), it can be seen that there is some asymmetry in the bandwidth between the two graphs. This is because when using $X$ as the AC input, the multiplier circuit will have a common-emitter configuration (transistors $Q2, Q3, Q5$ and $Q6$ each will behave as a CE amplifier). On the other hand, when $Y$ is used as the ac input, the circuit is configured as a common-base which has a wider bandwidth than the CE configuration for a certain load (which is in this case the diode-connected transistors $Q20$ and $Q21$). The dependency of the
bandwidth on the DC operating point of the $X$ input (apparent from the graph in Fig. 6(b)) is due to the ac resistance of the diode connected transistors $Q1$ and $Q4$ which are connected to the base of the quad transistors $Q2$, $Q3$, $Q5$ and $Q6$ each configured as a $CB$. This resistance contributes to the value of the dominant-pole of the circuit and consequently affects the bandwidth. Generally, the circuit has a wide frequency response which is very much consistent with the high-speed spec. mentioned before.

Fig. 6(a) Multiplier frequency response, $X$ is the AC input, the response was plotted for fixed DC values at the Y input of $\pm 0.5 I_E$ and $\pm I_E$, bandwidth = $2.18 \text{GHz}$
Fig. 6(b) Multiplier frequency response, $Y$ is the AC input, the response was plotted for fixed DC values at the $X$ input of $\pm 0.5I_B$ and $\pm I_B$, bandwidth ranges between 3.4-4 GHz.

2.3.3 Input and output resistance:

The input resistance of the $X$ input is shown in Fig. 7(a). The resistance is plotted vs. the large signal input current. It can be seen that the differential input resistance is quite low and acceptable for a current-mode environment. The input resistance remains relatively low over the dynamic range except at very small currents where the $g_m$ of the transistor gets very small and so the two diode connected transistors will have a higher resistance.
The differential input resistance for the X input is given by:

$$R_{sid} = \frac{V_T}{xI_B} + \frac{V_T}{(1-x)I_B} = \frac{V_T}{I_B} \left[ \frac{1}{x(1-x)} \right]$$

(15)

The minimum input resistance $R_{sid_{\text{min}}} = 4V_T/I_B$ occurs when $x=0.5$, which is for $I_B=400\mu A$. $R_{sid_{\text{min}}} = 260\Omega$. The input impedance increases in a relatively slow rate as $x$ deviates from 0.5. For $x=0.2$ and by substitution in Eq. (15), the input impedance increases by 150% from the minimum value; and when $x=0.1$ the amount of increase is 250% which is still considered low specially when compared with the output impedance of the driving circuit (the weight-sum circuit that is going to be discussed later).

![Fig 7(a) Differential input resistance of the X input of the Gilbert multiplier vs. the DC input current $I_x$ at the X input.](image)
The differential input resistance of the \( Y \) input is shown in Fig. 7(b) vs. the input current. Note that the \( X \) and \( Y \) inputs are almost identical.

![Graph of differential input resistance](image)

Fig. 7(b) Differential input resistance of the \( Y \) input vs. the DC input current \( I_y \) at the \( Y \) input.

The differential output resistance of the multiplier is shown in Fig. 8 vs. the DC output voltage. By looking at Fig. 8, we can see that the output resistance of this circuit is quite large specially when you compare it to the input resistance of the next stage which is simply a diode connected transistor. The output resistance, however, is limited by the pnp current sources that is used to bias the circuit.
2.4 Intermodulation distortion:

In telecommunication applications, the designer is usually concerned about how much undesired harmonic signal the circuit can generate from the fundamental input signal. This is known as the intermodulation distortion and one way to measure it is by finding the difference in dB between the fundamental and the third harmonic signals (the third harmonic is the largest generated harmonic).
Fig. 9 FFT of the output current for intermodulation distortion measurement of the multiplier circuit. The third harmonic was 35dB below the fundamental signal.

In practice, two sinusoidal signals with frequencies $\omega_1$ and $\omega_2$ are injected at the input of the circuit. The output is plotted in the frequency domain. The intermodulation distortion is measured by the difference in dB between the signal at $\omega_1$ and the harmonic signal at $2\omega_1 - \omega_2$ or the difference in dB between the signal at $\omega_2$ and the harmonic signal at $2\omega_2 - \omega_1$ whichever difference is the worst case.

For the multiplier circuit, two sinusoidal signals of frequencies 200 MHz and 225 MHz, with differential amplitude of 200µA each, are injected at the $X$ input with the $Y$ input held constant. The FFT of the output current is shown in Fig. 9. Two main harmonics show up, one at 175 MHz and the other is at 250 MHz. The
intermodulation distortion was found to be 35dB which is quite low specially when one looks at the amplitude of the applied signal which can have an instantaneous value equal to the bias current. This result compares favorably with specs. for this type of circuits in commercial products.

2.5 Effect of circuit mismatch on transfer curves:

2.5.1 Effect of mismatched non-zero DC emitter resistance:

One of the major cause of nonlinearity in the multiplier circuit is the mismatch of the non-zero emitter resistance between devices. These resistors represent all the bulk resistance of the diffusions, particularly the base resistance, referred to the emitter circuit. In fact, these elements will be current dependent, due to the crowding effect and beta nonlinearities. The current dependency was not included in the simulation because it is very difficult to model.

The mathematical derivations for the effect of any mismatch in the emitter DC resistance are discussed by Gilbert [5]. To show the effect, we inserted 10Ω resistors in series with the emitter of the devices Q1 and Q4. This creates a 100% mismatch. The multiplier was re-simulated with this mismatch condition. The transfer curves are plotted in Fig. 10. The linearity error (deviation from the ideal line) was found to be 4% over a dynamic range of 399µA (99.7% of the bias current), which shows a clear degradation in the linearity of the circuit due to this mismatch. In reality, the $R_e$
mismatch between devices due to layout and process imperfections would not exceed 10 to 20%.

Fig. 10 derivatives of the transfer curves for 100% $Re$ mismatch, linearity error was found to be 4% over a dynamic range of 399µA (99.7% of the bias current).

### 2.5.2 Device saturation current mismatch:

The device saturation current mismatch effect was also discussed by Gilbert [5] with all required derivations to predict the amount of distortion. The simulation for the multiplier performance under worst case saturation current mismatch of 10% is shown in Fig. 11, ($Q1$ and $Q4$ were perfectly matched and their saturation currents were set to the nominal value. $Q2$ and $Q6$ have a +10% mismatch, $Q3$ and $Q5$ have a -10% mismatch). The linearity error has increased to become 5.2% of the output over the
dynamic range of 399µA, which indicates that careful layout procedures should be followed to ensure best device matching.

Note that 10% mismatch in the saturation current between devices was exaggerated just to demonstrate the effect. In reality the mismatch does not exceed 1~ 3% for this process as a worst case.

Fig. 11 Derivative of the transfer curves with 10% saturation current mismatch, the maximum deviation from the ideal line was found to be 5.2% over the dynamic range of 399µA (99.7% of the bias current).
CHAPTER III
WEIGHTING-SUMMING CIRCUIT

3.1 The function of the circuit:

As was shown in the block diagram of the FPAA cell, Fig. 1, each cell receives 4 inputs in differential form. These inputs are fed into two "weighting-summing" circuits. The role of the weighting-summing circuit is to multiply each of these inputs by a certain weighting factor, which can be positive, negative or zero and then sum the resulting output currents.

The weighting-summing circuit should have the following characteristics:

1) it has to be a current mode circuit capable of receiving differential input currents and producing a weighted differential output current.

2) the circuit should be a four-quadrant multiplier since the weight (gain) can be positive or negative as mentioned above, with the differential input current signal as one input and the weight being the other one.

3) the circuit should provide good linear behavior over the dynamic range of operation.

4) the circuit should provide a wide bandwidth response.

5) circuit simplicity and power consumption should be kept in mind.
3.2 Circuit implementation

3.2.1 The Four-Transistor multiplier cell:

The minimum number of transistors required to implement a four-quadrant multiplier with both input and outputs being in differential form is 4 transistors, as shown in Fig. 12 [6].

For this circuit:

\[ I_{c1}I_{c4} = I_{c3}I_{c2} \quad (16) \]
\[ (1-x)I_yI_c = ((1-y)I_y - I_{c4})(1+x)I_y \quad (17) \]
\[ I_{c4}((1-x)+(1+x)) = (1+y)(1+x)I_y \quad (18) \]
\[ I_{c4} = \frac{(1+y)(1+x)I_y}{2} \quad (19) \]
\[ I_{c1} = (1 + y)I_y - I_{c4} \]  
(20)

\[ \Rightarrow I_{c3} = \frac{(1 + y)(1 - x)I_y}{2} \]  
(21)

\[ I_1 = I_{c4} + I_{c1} = \frac{(1 + y)(1 + x)I_y}{2} + (1 - x)I_x \]  
(22)

\[ I_2 = I_{c7} + I_{c2} = \frac{(1 + y)(1 - x)I_y}{2} + (1 + x)I_x \]  
(23)

if \( I_y = 2I_x \) yields

\[ I_1 = I_x (2 + y(1 + x)) \]  
(24)

\[ I_2 = I_x (2 + y(1 - x)) \]  
(25)

\[ \Rightarrow I_{rd} = I_1 - I_2 = 2xyI_x \]  
(26)

since both \( x \) and \( y \) can be positive or negative (each can vary from -1 to 1), this circuit implements a four-quadrant multiplier, and the weight is \( y \).

3.2.1.1 Circuit full implementation and simulation:

The full implementation of the four-transistor multiplier circuit is shown in Fig. 13. Two programmable reference currents are required to bias the circuit. \( I_{ref1} \) sets the current \( I_x \). \( I_{ref2} \) sets the weight current \( (1 + y)I_y \). In the case of unused weight cells, \( I_{ref1} \) and \( I_{ref2} \) are shut off.
The output of the cell is connected to diode connected transistors which represents the input stage of the multiplier discussed in Chapter 1; this keeps the base-collector voltages of $Q_1$-$Q_2$ at about 0.7V and for $Q_3$-$Q_4$ at 1.4V.

![Diagram of the four-transistor multiplier](image)

Fig. 13. Full implementation of the four-transistor multiplier

We need to evaluate this circuit for linearity which is an important issue in the performance of the whole FPAA. The transfer curves of the four-transistor multiplier are shown in Fig. 14(a). The differential output current was plotted vs. the DC input current for fixed weight values. The derivatives are shown in Fig. 14(b).
Fig. 14(a) Transfer curves of the 4-transistor multiplier, the output current was plotted vs. the input current for different weight values.

Fig. 14(b) Derivatives of the set of curves in Fig. 14(a), the linearity error was found to be 12.5% over a dynamic range of 399µA (99.7% of the bias current)
From Fig. 14(a) and (b), the linearity error was found to be 12.5% over a dynamic range of 399µA (99.7% of the bias current). Therefore, the four-transistor multiplier has shown not to have the linearity expected from a translinear circuit; this can be seen clearly from Fig. 14(b). The analysis for this distortion is discussed in the next section.

3.2.1.2 Distortion analysis:

As seen from Fig. 14(b), the four-transistor multiplier circuit is not as accurate as that of the six transistor multiplier circuit discussed in Chapter 1. The main reason is the distortion resulting from the lumped non zero emitter resistance, (which we neglected in our derivations), which does not cancel out at the output.

Assuming a non-zero emitter resistance; and 100% matched transistors, the circuit equations can be rewritten to:

\[ R_x I_4 + v_{BE4} + R_x I_1 + v_{BE1} = R_x I_3 + v_{BE3} + R_x I_2 + v_{BE2} \]  
(27)

\[ \frac{I_2 I_3}{I_4 I_1} = e^{\frac{R_x}{V_T} (I_4 + I_3 - I_2)} \]  
, assuming \( IR_x \ll V_T \)  
(28)

\[ \Rightarrow \frac{2(1+y) I_i - I_4 (1+x) I_4}{I_4 (1-x) I_i} = 1 + \frac{R_x}{V_T} [-(1-x)I_i + I_i + 2(1+y)I_i + I_4 - (1+x)I_i] \]  
(29)

\[ \frac{2(1+y)(1+x) I_i - (1+x)I_2}{I_4 (1-x) I_i} = 1 + \frac{R_x}{V_T} [-2xI_i - 2(1+y)I_i + 2I_4] \]  
(30)
\[ 2(1 + y)(1 + x)I_x - (1 + x)I_x = \frac{R_e}{V_T} I_4 (1 - x) \left[ 1 - 2I_x (1 + x + y) + 2I_4 \right] \] (31)

\[ (1 + y)(1 + x)I_x = I_4 - \frac{R_e}{V_T} (1 - x)I_4 \left[ I_x (1 + x + y) - I_4 \right] \] (32)

\[ \Rightarrow I_4 = (1 + y)(1 + x)I_x + \frac{R_e}{V_T} (1 - x)I_4 \left[ I_x (1 + x + y) - I_4 \right] \] (33)

Similarly, it can be verified that

\[ I_5 = (1 + y)(1 - x)I_x + \frac{R_e}{V_T} (1 - x)I_4 \left[ I_x (1 - x + y) - I_5 \right] \] (34)

\[ \Rightarrow I_{6d} = I_4 - I_5 = 2x(1 + y)I_x + \frac{R_e}{V_T} I_4 (1 - x)(2xI_x - I_{6d}) \] (35)

From Eq. (35), the impact of a non-zero emitter resistance on the circuit linearity becomes apparent. First, this non linear error term does not cancel out and appears in the differential output current. Moreover, we have assumed that all transistors have the same emitter resistance which is incorrect because this resistance is current dependent, due to factors like emitter crowding, and since each transistor conduct its own current, the emitter resistance will vary between transistors and the nonlinear error will get even worse!
3.2.2 The six transistor multiplier cell:

This circuit was discussed in details in Chapter 1; we can use it to construct a weighting summing circuit with the emitter tail currents of $Q2-Q3-Q5-Q6$ being used to set the weight. This circuit has the advantages over the four-transistor multiplier of better accuracy and linearity. Moreover, it is less sensitive to transistor mismatching and emitter resistance.

Since we have two weighting summing blocks, two weighted copies for each input to the FPAA cell should be generated. However, we do not need an extra 6 transistors for the other weight, in fact, we need only 4 more transistors. On the other hand, to get another weight using the four-transistor multiplier, we need an extra full cell, this means that the extra hardware we spend using the six transistor multiplier instead of the four transistor one is only two transistors per input which is a small price to pay for the resulting improvement in performance.

The circuit to generate two weighting copies for any differential input using the six transistor multiplier is shown in Fig. 15. $Q1, Q2, Q3, Q4, Q5$ and $Q6$ represent the first weight circuit. Transistor $Q7, Q8, Q9$ and $Q10$ are added to get the second weight for the same input. Five programmable reference currents are required to bias the circuit.
Fig. 15 The weighting circuit based on the six-transistor multiplier cell

$I_{\text{ref}1}$ sets the bias current $I_B$. $I_{\text{ref}2}$ and $I_{\text{ref}3}$ set the first weight $w_1$ where $w_1=+1$ when $I_{\text{ref}2}=0$ and $I_{\text{ref}3}=I_B$, $w_1=-1$ when $I_{\text{ref}2}=I_B$ and $I_{\text{ref}3}=0$, and $w_1=0$ when $I_{\text{ref}2}=I_{\text{ref}3}=0.5I_B$. $I_{\text{ref}4}$ and $I_{\text{ref}5}$ set the second weight $w_2$ for the given input current.

Simulation shows that the linearity of the circuit is not affected by using this configuration instead of using two separate cells. The transfer curves are displayed in Fig. 16(a) and (b). The linearity error was found to be 0.9% over the dynamic range of 399µA (99.7% of the bias current). Accordingly, for our FPAA, the six-transistor multiplier circuit shown in Fig. 15 will be used to implement the weight-sum circuit.
Fig. 16(a) The transfer curves of the weighting circuit based on the six-transistor multiplier's cell; one of the outputs was plotted vs. the DC input current for fixed weight values.

Fig. 16(b) The derivatives of the set of graphs in 16(a). Linearity error was found to be 0.9% over a dynamic range of 399µA (99.7% of the bias current)
3.3 The normalizing circuit:

3.3.1 The need for such a circuit and its function:

Each differential output current of the weighting circuit can swing the full dynamic range. This means that at the summing point we will have a current that can swing to $n$ times the full dynamic range, where $n$ is the number of outputs of the weighting circuits. As a result, if all stages in the FPAA cell have the same biasing, clamping and consequently distortion will occur.

As a solution to this problem, we need to build a circuit that accepts full swing input currents and produces a controllable full swing output current which still represents the sum of all input currents. This circuit is called the "normalizing circuit".

3.3.2 Current-mode normalizing circuit implementation:

![Translinear normalizing circuit](image-url)

Fig. 17 Translinear normalizing circuit[6],[9]
For the circuit of Fig. 17:

\[
\frac{I_1}{I_1} = \frac{I_k}{I_k} \ldots \ldots = \frac{I_n}{I_n}
\]

(36)

\[
I_1 = \frac{I_1}{I_k} \quad \text{also} \quad I_2 = \frac{I_2}{I_k} \quad \ldots \quad I_n = \frac{I_n}{I_k}
\]

(37)

\[
\Rightarrow I_1 + I_2 + \ldots + I_n = \frac{I_k}{I_k} (I_1 + I_2 + \ldots + I_n)
\]

(38)

this yields to

\[
I_k = I_k \frac{I_e}{\sum_{k=1}^{n} I_k}
\]

(39)

Eq. (39) shows that the current \(I_e\) sets the final swing of the output current at the sum point. Take for example \(n=2\) and assume the input signals (in this case there are two) have the same swing \(I_k\). Substituting in equation (40) yields that \(I_k^*\) for each input will be half \(I_e\). This means that the output full swing \(I_e\) is shared equally by the two input signals. Same thing applies for any number of input signals \(n\), where the output swing current, \(I_e\), is shared evenly by these input signals with each contributing \(I_e/n\) of the full output swing. It is worth noting that this circuit is similar to the type ‘A’ multiplier cell in having good beta immunity. Thus, it can operate with ratios of \(I_k/I_k^*\) as low as \(1/\beta\) [6].
3.3.3 Circuit Simulation:

Fig. 18 is part of the differential normalizing circuit in which the output of a weighting circuit is fed to the $Q1-Q2$ pair of transistors. The output is taken from the collectors of the $Q3-Q4$ pair. Each output of the weighting circuits is fed to a circuit similar to that of Fig. 18. The emitter tail point (the point connecting the emitters of $Q3-Q4$) of all of these circuits are then connected together to a tail current source $I_{EE}$ that will determine the final swing of the sum current. The corresponding collectors are also connected together to sum all outputs.

Fig. 18 full implementation of the differential normalizing circuit
With the normalizing circuit of Fig. 18 as a subcircuit, Fig. 19 shows the configuration to test the performance of the normalizing circuit with the outputs of the weighting-summing circuit connected to drive it. As shown in Fig. 19, each output of the weighting circuit is connected to a circuit similar to that in Fig. 18. The tail point of these circuit are connected together to a tail current $I_{EE}$ that will determine the final output swing at the summing node where the outputs of the normalizing circuit are connected together.

Fig. 19 weighting-sum circuit plus the normalizing circuit, top level circuit
Fig. 20(a) Transfer curves of the normalizing circuit, the differential output was plotted vs. the input current.

Fig. 20(b) Derivative of the set of curves in 20(a), the circuit has a linearity error of 1.8% over a dynamic range of 399µA (99.7% of the bias current).
The weighting-summing circuits was programmed so that all its outputs will have same swing. The output current at the summing point of the normalizing circuit was plotted vs. the DC input current to the weighting circuit for increment values of the weight parameter. The results are shown in Fig. 20 (a), and to show linearity, the derivative is shown in Fig. 20(b). The linearity error was found to be 1.8% over a 399µA dynamic range (99.7% of the bias current).

3.3.4 Distortion analysis:

The transfer curves in Fig. 20(b) shows some non-linear behavior of the normalizing circuit. To see where this kind of behavior is coming from, let’s take another look at the circuit of Fig. 18. In our previous calculations, we assumed zero emitter resistance for the transistors, but in reality that is not true. To demonstrate this effect, let us assume that all transistors have equal emitter resistance $R_e$ and we are going to rewrite the equations that describes the normalizing circuit to include this effect.

For the normalizing circuit in Fig. 18, considering the emitter resistance, one can write:

$$-v_{BE1} - R_e I_1 + v_{BE3} + R_e I_3 - v_{BE4} - R_e I_4 + v_{BE2} + R_e I_2 = 0 \quad (40)$$

$$\frac{I_2}{I_4} = 1 + \frac{R_e}{V_T}(I_1 + I_4 + I_3 + I_2) \quad (41)$$
\[
\frac{I_1I_2}{I_1I_4} = 1 + \frac{R_e}{V_T}[(1-x)I_x + 2I_{EE} - 2I_3 - (1+x)I_x]
\]  
(42)

\[
\frac{I_3(1+x)I_x}{(1-x)I_x(2I_{EE} - I_x)} = 1 + \frac{R_e}{V_T}(2I_{EE} - 2I_3 - 2xI_x)
\]  
(43)

\[
I_3(1 + x) = (1 - x)(2I_{EE} - I_x) + \frac{R_e}{V_T}(1 - x)(2I_{EE} - I_x)(2I_{EE} - 2I_3 - 2xI_x)
\]  
(44)

\[
\Rightarrow I_3 = (1 - x)I_{EE} + \frac{R_e}{V_T}(1 - x)I_x(I_{EE} - I_3 - xI_x)
\]  
(45)

\[
I_4 = (1 + x)I_{EE} + \frac{R_e}{V_T}(1 - x)I_4(I_{EE} - I_4 + xI_x)
\]  
(46)

\[
\Rightarrow I_{od} = I_4 - I_3 = 2xI_{EE} + \frac{R_e}{V_T}(1 - x)I_4(2xI_x + I_x - I_4)
\]  
(47)

\[
I_{od} = I_4 - I_3 = 2xI_{EE} + \frac{R_e}{V_T}(1 - x)I_4(I_{od} - I_{od})
\]  
(48)

Eq. (48) shows that the non-zero emitter resistance causes a nonlinear behavior of the circuit. This effect is similar to what we have seen in previous circuits. Closer inspection of Eq. (48) shows that the effect of \(R_e\) can be completely eliminated if we make the input and output differential currents exactly equal. This can be achieved by making: \(I_x = I_{EE}\).

To demonstrate the above results, we simulate the circuit for two different values of \(I_{EE}\), Fig. 21(a) is the transfer curve for the circuit of Fig. 17 with \(I_{EE} < I_x\) and
Fig. 21(a) The derivative of the transfer curve of the normalizing circuit with $I_{EE} = 0.5I_x$, linearity error is 0.6% over the dynamic range.

Fig. 21(b) The derivative of the transfer curve of the normalizing circuit with $I_{EE} = I_x$, the linearity error is 0.13% over the dynamic range.
Fig. 21(b) is the transfer curve for $I_{EE} = I_x$. We can see that the circuit has better linearity when $I_x = I_{EE}$. Unfortunately, we can’t apply this result to our normalizing circuit in its current shape. Connecting the emitters of the cells together forces the output swing to be smaller than the input swing by a factor of $n$, where $n$ is the number of inputs to the normalizing circuit.

### 3.3.5 Intermodulation distortion:

The intermodulation distortion for the weighting and the normalizing circuits of Fig. 19 is shown in Fig. 22.

![Image](image.png)

Fig. 22. FFT for the output signal of the weighting circuit connected to the normalizing circuit. Third harmonic signal is 29dB below the fundamental input signal.
Two sinusoidal signals at 200 MHz and 225 MHz, with a 200µA differential amplitude each, were injected at each input of the weighting circuit. The FFT of the output signal is shown in Fig. 22. The third harmonic component was 29dB below the fundamental signals. Note that the instantaneous amplitude of the applied signal can hit the bias current limit, and still the harmonic distortion generated by the circuit nonlinearities is quite low.
CHAPTER IV
INTEGRATOR-GAIN CIRCUIT

4.1 The Integrator:

Continuous-time filters operating at cutoff frequencies exceeding 10MHz constitute a large potential market. With the trend towards low-voltage and low-power circuits, it is becoming increasingly difficult to design high-speed, highly-linear, wide-dynamic-range voltage-mode continuous-time analog filters. This has led to a growing interest in current-mode domain signal processing because of its speed and immunity to parasitics due to the low impedance environment [10].

The integrator still represents the key block in continuous-time filter design. In ladder-filters for example, it is the main block used for the implementation.

Our FPAA cell contains a programmable integrator-gain block which can be configured to function as either an integrator with tuned (programmable) $g_m$, or as a programmable gain stage, or both.

A suggested implementation for the integrator-gain block for the FPAA was presented by Pierzchala in [4]. That design uses the basic Gilbert current-gain cell for implementation but the design suffers from some draw backs. The implementation is complex, and this is reflected in area and power consumption which are key issues in
this kind of circuits. Secondly, the design uses a trans-impedance stage to convert current to voltage for the feedback signal. This is undesirable for all-current-mode circuits. In this chapter, we will present another implementation that is still based on the Gilbert current-gain cell with a $g_mC$ based integrator. The presented circuit is simpler than the design presented in [4] and uses an all-current-mode implementation, while sustaining the electrical performance necessary for such a block in our high-speed FPAA.

The basic building block of the proposed integrator consists of current mirrors and capacitors only, no resistors are involved, which makes it easy to implement in a monolithic integrated circuit. This integrator can operate from a power supply as low as 1.5V. The integrator circuit is shown in Fig. 23(a). It is a differential-in differential-out current-mode integrator. The small signal model is shown in Fig. 23(b).

For the circuit of Fig. 23(b):

\[(g_{m1} + sC_1)V_1 + g_{m4}V_2 - I^+_i = 0\]  \hspace{1cm} (49)

\[(g_{m3} + sC_2)V_2 + g_{m2}V_1 - I^-_i = 0\]  \hspace{1cm} (50)

By subtracting equation (50) from (49) yields

\[(g_{m3} + sC_2 - g_{m4})V_2 - (g_{m1} + sC_1 - g_{m2})V_1 = I^+_i - I^-_i\]  \hspace{1cm} (51)
Fig. 23(a) Differential current-mode $g_m$-$C$ integrator

Fig. 23(b) The $AC$ model for the integrator circuit in 23(a)

if $g_{m_1} = g_{m_2} = g_{m_3} = g_{m_4} = g_m$ and $C_1 = C_2 = C$, Eq. (51) simplifies to

$$I^+ - I^- = (V_1 - V_2)sC$$

but

$$I^+ = -g_{m_6}V_2 ; \quad I^- = -g_{m_5}V_1$$
Assuming \( g_{m5} = g_{m6} = g_m \) gives:

\[
I_o^+ - I_o^- = g_m(V_1 - V_2) \tag{54}
\]

Combining Eq. (53) and Eq. (54) gives the ideal integrator function relationship

\[
\frac{I_{od}}{I_{id}} = \frac{I_o^+ - I_o^-}{I_i^+ - I_i^-} = \frac{g_m}{sC} \tag{55}
\]

between the differential input and output currents. The \( g_m \) of the integrator can be tuned by changing the DC bias current which will be used as the "programming" parameter.

The DC gain of the integrator theoretically seems to be infinite and the pole is at zero frequency. Eq. (55), however is the first order approximation of a lossless integrator with transistors of infinite current gain \( \beta \). Next, we will consider the second order effects due to finite current gain \( \beta \) on the circuit of Fig. 23(a). Other factors, like devices output resistance, have minor effect and will not be considered here.

With finite \( \beta \), equations (49) and (50) are modified to:

\[
\left[ g_{m1}(1 + \frac{3}{\beta}) + sC_1 \right] V_1 + g_{m4}V_2 = I_o^+ \tag{56}
\]

\[
\left[ g_{m3}(1 + \frac{3}{\beta}) + sC_2 \right] V_2 + g_{m2}V_i = I_o^- \tag{57}
\]

which, with \( g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_{m6} = g_m \) and \( C_1 = C_2 = C \), result in the
nonideal integrator function

\[
\frac{I_{\text{int}}}{I_{\text{int}}} = \frac{I_{u}^+ - I_{u}^-}{I_{i}^+ - I_{i}^-} = \frac{g_m}{sC + 3g_m/\beta}
\] (58)

Eq. (58) shows that for a value of \(\beta=100\), the integrator will have a DC gain of about 30.5dB. Note that the pole is located at \(w = \frac{3g_m}{\beta C}\), which for \(\beta=100\), \(C=10\text{pf}\) and a 10\(\text{\mu A}\) bias current, is around 180 KHz.

Fig. 24 shows the simulated ac response of the integrator with these element values and bias conditions. The DC gain and pole location agree with the theoretical values. Note that the base-emitter capacitances of \(Q1, Q2, Q3, Q4, Q5\) and \(Q6\) load the value of the custom capacitors \(C1\) and \(C2\) and contribute a small error in the pole location compared to the calculated value. This should be kept in mind.

The useful band of the integrator is usually determined by the designer according to the amount of tolerable phase error. Some designs can tolerate phase error in the integration as high as 5%; other designs specially those with high quality factors can not tolerate phase errors exceeding 0.5% [12]. As seen from the phase plot in Fig. 24, the integrator is useful over a bandwidth of 61.3 MHz (tuning range is between 1.7 and 63 MHz) where the phase of the integrator is 90°±5%. The useful bandwidth jumps to 134 MHz for a 10% phase error; but for a 1% phase error, the useful band is only 15 MHz over a tuning range from 6 to 21 MHz.
The integrator is quite suitable for high-speed applications where the demand is to build filters with cutoff frequency of 10 MHz and above.

Fig. 24. Integrator frequency response, magnitude and phase, with C=10 pf, \( I_{bias} = 10 \mu A \) and \( \beta = 100 \)

The power consumption for the integrator circuit is equal to:

\[ Power = 6VCC I_{bias} \]

which for a 10\( \mu \)A bias current and a supply voltage of 1.5V, results in a power consumption of a mere 90\( \mu \)Watts!
4.2 The Gain circuit:

The gain circuit in our FPAA cell should have the following requirements:

1. It should be a differential current-mode circuit with wide bandwidth response.

2. Linear response over a wide dynamic range.

3. Low sensitivity to temperature, parasitics and device parameters.

4. Programmable gain.

The Gilbert Current-Gain cell [7], as shown in Fig. 25, will do the job. The circuit is very simple, has excellent characteristics, and meets the above requirements. The circuit band width is close to that of the individual devices, it has low sensitivity to device parameters and temperature. Moreover, it has a good linear gain over a wide dynamic range.

![Gilbert Current-Gain cell diagram](image)

Fig. 25 the Gilbert Current-Gain cell [7]
The gain equation will be repeated here for the convenience of the reader.

For the circuit of Fig. 25:

\[ V_{FE} - V_{BE} + V_{FIU} - V_{FI2} = 0 \]  

(59)

\[ V \ln \frac{I_1}{I_{s1}} - V \ln \frac{I_4}{I_{s4}} + V \ln \frac{I_3}{I_{s3}} - V \ln \frac{I_2}{I_{s2}} = 0 \]  

(60)

If \( I_{s1} = I_{s2} = I_{s3} = I_{s4} = I_s \)

\[ \Rightarrow \frac{I_1 I_3}{I_2 I_4} = 1 \]  

(61)

substituting the correct values of currents one gets

\[ \frac{x I_B (1-a) I_E}{a I_E (1-x) I_B} = 1 \]  

(62)

Equation (62) leads to the conclusion that \( a=x \).

Thus the magnitude of the output currents are:

\[ I_2 = x I_E \quad \text{and} \quad I_3 = (1-x) I_E \]  

(63)

Consequently, the DC current gain will be

\[ G = \frac{I_E}{I_B} \]  

(64)

The maximum gain one can get from the Gilbert cell is around \( \beta/10 \), after that, the base current starts to play a significant role in producing gain error and some non-linear effect [7]. Note that the gain of the Gilbert current-gain cell can be varied (programmed) easily by changing the tail current \( I_E \). Consequently, programmability is
accomplished away from the signal path and as a result, the performance is not affected.

We will use two of the Gilbert current-gain cell in cascades, this will give a maximum DC current gain of about 40dB per FPAA cell, assuming $\beta=100$. Fig. 26 shows the frequency response of the gain cell for different gain values. The gain cell has a wide bandwidth relative to the device $f_c$. The bandwidth ranges from 0.6GHz (gain of 8) to 1.4 GHz (gain of 1).

Fig. 26. Frequency response of the Gilbert current-gain cell
4.3 Combined Integrator-Gain cell:

The combined programmable Integrator-Gain circuit is shown in Fig. 27. The programming code for different modes of operations is as follows:

**Integrator-mode:**

$I_{c5}$, $I_{c6}$, $I_{E2}$ and $I_{E3}$ are turned off; the circuit then becomes a gain block followed by the integrator circuit, the user has the option to set the gain block to any arbitrary gain or just set the gain to unity; on the other hand the current sources $I_{c3}$, $I_{c4}$, $I_{c13}$ and $I_{c14}$ will be used to set the $g_m$ of the integrator.

Fig. 27 Combined integrator-gain cell
Gain-mode:

$I_{e3}, I_{e4}$ and $I_{e1}$ are turned OFF; the circuit then will be two Gilbert current-gain cells in cascades while the integrator circuit is totally isolated and eventually OFF. The overall gain can be programmed by setting the value of the current sources $I_{e2}$ and $I_{e3}$. 
CHAPTER V

THE PROGRAMMABLE CURRENT SOURCE

5.1 Introduction:

One of the key circuits required for the FPAA is a programmable current source that can be programmed to generate the desired output current. This current source circuit is required in all the subcircuits used in the FPAA cells since the programming scheme in the entire FPAA relies on the availability of such programmable current sources. A DAC will be used as the interface between the programmer and the current sources. The programmer sets the “code” which carries the information about the required value for each current source, with the aid of some control logic. This leads to programming the DAC, which in turn scans each of these current sources and sets the value of their output currents. The current source then has to store the programmed value with minimum loss till the next DAC refresh. With the assumption that the DAC refreshing circuit has a voltage output, a voltage-controlled current source (VCCS) with storage capability, needs to be built.
5.1 The design of a storage voltage-controlled current source (VCCS):

The circuit of Fig. 28 is a simple VCCS. The output current is related to the input voltage by:

\[ I_0 R_1 = -v_{BE4} + v_{BE3} + v_{in} \]  \hspace{1cm} (65)

with the approximation \( v_{BE4} \approx -v_{BE3} \)

\[ \Rightarrow I_0 \approx \frac{v_{in}}{R_1} \]  \hspace{1cm} (66)

![Fig. 28. simplified VCCS circuit](image)

Eq. (66) above describes how the output current of this simple VCCS is linearly related to the input voltage (provided by the DAC).
The problem is not solved yet. The proposed design has a relatively poor DC input resistance: the DC input current is not zero and consequently if we connect a storage element, like a capacitor, to the input, the leakage due to the DC input current will bleed the stored charge, resulting in an unacceptable drop in the output current. We need to have an “impedance interfacing” circuit which has the required high DC input resistance. The circuit as shown in Fig. 29, is a modified version of the circuit of Fig. 28. Q7 and Q6 are used to mirror the output current to Q3. This will reduce the output current error to: 
\[ \text{error} = \frac{V_r}{R_1} \ln \frac{I_{spp}}{I_{spp}}. \]

The p-JFETs Q1 and Q2 are used to provide the impedance interface circuit with the required high DC input impedance. Q1 was set as a current source with zero \( V_{gs} \), with the drain of Q1 being the source of Q2, this forces the drain current of both transistors to be equal, which in turn forces \( V_{gs} \) of Q2 to be zero, the same as \( V_{gs} \) of Q1 (assuming perfect device matching). This will transfer any applied input voltage at the gate of Q2 to the drain of Q2 with negligible error and consequently, this voltage sets the base voltage of Q3 which in turn sets the output current as derived earlier in Eq. (66). Fig. 30 shows the DC transfer characteristics that relate the input voltage to the voltage across the resistor \( R_I \). As seen from Fig. 30, the maximum DC error for the VCCS is less than 1.5%, which is quite acceptable. In theory, it might be thought that the error might even brought to zero by making the emitter-base voltage of Q3 and Q4
to be exactly equal. This means that the current mirror $Q_6$ and $Q_7$ should be modified to give a current ratio of $1:I_{sp}/I_{sn}$ instead of $1:1$. Simulation showed however, that the error did not improve by doing that. This is because there are other factors that contribute to the total error such as the finite output resistance of the JFETs which changes the $V_{gs}$ of $Q_2$ any time the input voltage changes. Moreover, the finite output resistance and the finite current gain $\beta$ of $Q_6$ and $Q_7$ themselves also contribute to the error. Finally, it is very difficult to sustain the current ratio equal to $I_{sp}/I_{sn}$ over the operating temperature range.

Fig. 29. Improved storage VCCS.
Fig. 30 The DC transfer characteristics of the VCCS, the voltage across $R_1$ is plotted vs. the input voltage $v_{in}$. Max. error was 1.5%.

The DC input current to the circuit is equal to the gate current of $Q2$ which represents the reverse bias saturation current of the gate-source junction of the p-JFET which is in the range of 10pA. Fig. 31 shows the transient simulation of the voltage across the 0.4pf capacitor connected to the input of the VCCS (the gate of $Q2$). As can be seen from Fig. 31, simulation shows that a 0.4pf capacitor was enough to hold a voltage of 1V for 0.2ms with less than 1% loss.
Fig. 31. Transient response of the storage-programmable VCCS, the stored voltage across the 0.4pf capacitor was plotted vs. time.
CHAPTER VI

CONCLUSION

This research addresses a new but promising direction in the design of analog circuits. Most analog ICs fall in the ASIC category where the design is optimized for a particular application. Analog circuits, in contrast with digital circuits, lack the flexibility feature in which one programmable circuit is used to perform different analog functions. The main obstacle to progress in that direction was the difficulty to introduce programmability to analog circuits without affecting performance.

Field Programmable Analog Arrays, in which the array can be programmed in both structure and function to perform different analog signal processing functions, were introduced recently; but the problem of programmability vs. performance was not addressed in detail.

A successful current-mode Field Programmable Analog Array, its architecture and the basic cell block diagram was introduced in [4]. The full implementation of the analog stages of the cell are presented in this thesis. Current-mode circuits were found to be the best vehicle for the implementation because of their simplicity, high frequency response and immunity to parasitics.

The thesis also demonstrates an efficient programming method for the basic cell in which programmability was achieved by changing the bias current for the different
parts of the basic cell, so the controlling scheme was totally isolated from the signal path.

The designed circuits for the cell exhibit high-speed and highly-linear characteristics. This was shown throughout this thesis, supported by mathematical derivations and simulations. It was also shown clearly that the programming scheme has little or no effect on the performance of the designed circuits.

More effort should be put in completing the design of the whole cell. This includes the design of the control logic, the DAC refreshing circuit, and the programming software that carries the programming code for the FPAA. The main challenge in the design of FPAAAs besides those mentioned earlier, is the trade off between complexity, performance and power consumption. The basic cell should be kept as simple as possible to reduce area. Moreover, the programming scheme should have minimum interference with the signal in order not to degrade the overall performance. Finally the available power budget usually dictates the design technique for the entire circuit.

In conclusion, we have demonstrated the feasibility of a high-speed, highly-linear, low-voltage, low-power, programmable FPAA with commercial potential. The proposed FPAA can implement a wide variety of analog functions with an overall performance comparable to the present available ASICs with comparable functionality.
REFERENCES


