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THESIS APPROVAL

The abstract and thesis of Zhaohui Yan for the Master of Science in Electrical and Computer Engineering were presented October 9, 1995, and accepted by the thesis committee and the department.

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ABSTRACT

An abstract of thesis of Zhaohui Yan for the Master of Science in Electrical and Computer Engineering presented on October 9, 1995.

Title: Performance Analysis of A Banyan Based ATM Switching Fabric with Packet Priority

Since the emergence of the Asynchronous Transfer Mode (ATM) concept, various switching architectures have been proposed. The multistage interconnection networks have been proposed for the switching architecture under the ATM environment. In this thesis, we propose a new model for the performance analysis of an ATM switching fabric based on single-buffered Banyan network. In this model, we use a three-state, i.e., “empty”, “new” and “blocked” Markov chain model to describe the behavior of the buffer within a switching element. In addition to traditional statistical analysis including throughput and delay, we also examine the delay variation. Performance results show that the proposed model is more accurate in describing the switch behavior under uniform traffic environment in comparison with the “two-state” Markov chain model developed by Jenq, et. al.[4] [6] . Based on the “three-state” model, we study a packet priority scheme which gives the blocked packet higher priority to be routed forward during contention. It is found that the standard deviation of the network delay is reduced by about 30%.

PERFORMANCE ANALYSIS OF A BANYAN BASED ATM
SWITCHING FABRIC WITH PACKET PRIORITY

by

ZHAOHUI YAN

A thesis submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE
in
ELECTRICAL AND COMPUTER ENGINEERING

Portland State University

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CHAPTER 1

Introduction

1.1 ATM and B-ISDN Brief

The Broad-band Integrated Services Digital Network (B-ISDN) is a computer communication network which provides multimedia services including voice, video and data traffic with high bandwidth capacity and flexible switching technology. The B-ISDN environment is defined in terms of a layered protocol architecture consisting of services and signaling descriptions, adaptation formats, a common information transfer and a number of physical layers such as Synchronous Optical Network (SONET) or Synchronous Digital Hierarchy (SDH). A layered structure of the B-ISDN protocols is shown in Fig. 1.1 .

Figure 1.1 Structure of B-ISDN Protocol Stack

The Asynchronous Transfer Mode (ATM) has been recommended by CCITT (now ITU) and ATM Forum as the transport technology to support future B-ISDN. ATM is a cell-based fast packet switching technology in which information from different sources is packetized into small packets called ATM cells with the same length (53 bytes) and transmitted over a single broad-band network. As a communications protocol, ATM can be used to transfer data, digitized voice and digitized video over various physical communications mediums.

Because of its high bandwidth switching capability, ATM is being applied in both local area and wide area communications environments. As the essential part of ATM networking, the switching architecture and its performance have been studied extensively by many researchers in the data communication area. In recommendation I.150 the ITU has adopted ATM as the network transport layer for wide area broadband ISDN services that will operate over SONET/SDH facilities. An ATM network application example is shown in Fig. 1.2 on page 7 .

1.2 ATM Switching

Packet switching was first proposed by Baran in 1964 [14]. In packet switching, blocks of data packets are transmitted from a source to a destination through multiple switches in the communication network. Switching of packets is done by

computers running communication processes rather than by dedicated hardware. Conventional packet switching seems to be similar to ATM switching from the viewpoint of making a block of data into a packet or a cell and routing the packet by its label. However, ATM switching differs from conventional packet switching in various ways. The use of a high speed digital transmission facility with excellent error performance allows for simple link level protocols. In particular, there is no flow control or error correction done at the link level such as X.25 . The high level protocol functions such as error control and flow control are implemented on an end-to-end and application dependent basis. The fixed-length packets also simplify the packet processing and synchronization aspects thus making the ATM switching more hardware intensive rather than software intensive.

Among the many candidates of the ATM switching fabrics, Banyan networks have been proposed in several publications [1] - [18] for the implementation of an ATM switching node. The Banyan network is a multistage interconnection network that was originally proposed for supporting communication between processors and memory modules in large scale multiprocessor system. Because of its self-routing characteristic and simplicity in hardware, it has also been used for fast packet switching fabrics in communication networks.

1.3 Review of Related Work

Since the switch plays a critical role in the overall performance of the computer network, the performance analysis of the switching fabric is important for researchers and designers of ATM networks. The performance analysis of the Banyan network has been under extensive study in past few years. Patel [2] analyzed the performance of an unbuffered Banyan network under uniform traffic pattern and provided a recursive algorithm for the throughput of the switching network. Kruskal and Snir [5] further provided the asymptotic solution for this recursive algorithm for the Banyan network with infinite buffer size. Jenq [4] as well as Dias and Jump [3] extended Patel's work by analyzing the performance of a single-buffered Banyan network under uniform traffic. In Jenq's paper [4], a simple analytic model is provided in recursive form to analyze the throughput and delay of the single-buffered Banyan network that consists of 2×2 crossbar switching elements (SE). Yoon, et, al.[6] extended Jenq's model by analyzing the performance of multibuffered Banyan networks consisting of SEs with arbitrary size. On the other hand, Wu [8] and Kim [9] studied the performance of buffered Banyan networks under nonuniform traffic patterns. The performance of buffered Banyan networks placed in parallel was also studied by Kim [9] [11].

Since the Banyan network is a blocking network, contention occurs when two packets from different buffers within the same SE are destined for the same output port of that SE. In this case, one packet has to be blocked for one clock cycle. In the

previous studies, it is assumed that the blocked packet will generate a new random destination during the next clock cycle. This assumption causes inaccuracy in the performance evaluation of the Banyan switch. As was pointed out by Yoon [6], the analytic results based on this assumption are more optimistic than simulation results.

1.4 Overview of the Thesis

In this thesis, an analytical method will be found to evaluate the performance of the buffered Banyan network based ATM switch. In order to more accurately describe the behavior of the switching element in a single-buffered Banyan network, we introduce a “three-state” Markov chain model to distinguish a packet that has not been blocked before in a buffer with a packet that has been blocked for at least one time in that buffer. This model should improve the accuracy of previous models by Jenq [4] and Yoon [6]. In this new model, it is assumed that the blocked packet will still be destined for the same output port in the next clock cycle. In previous work, only the throughput and delay were studied. However, for ATM switches, the variation of the delay is also an important parameter for delay sensitive services like audio and video. In this paper, we use the moment generating function to analyze the variance of the network delay for the proposed “three-state” model. We also introduce a packet priority scheme by giving the “blocked” packet higher priority for being able to move forward when it is contending for the same output port with a

packet that has never been blocked before. By doing this, one can expect to reduce the variance of the network delay .

In Chapter 2, the structure and operation of single-buffered Banyan network are described. We then proposed a “ three-state” Markov chain model for the analysis of the behavior of the single buffer within a switching element of the switch.

Following the Markov chain description of the SE is a complete mathematical model in Chapter 3 that describes the relations among the steady-state probabilities in the “three-state” model. Some fundamental assumptions on the traffic patterns and the independence between the switching elements are stated in this chapter. We then investigate the performance of the switching network with different size and under various traffic loads and compare the performance results with the previous model.

In Chapter 4, a new routing scheme with packet priority is introduced to reduce the variance of the network delay and modifications on the previous analytical model as well as performance results are obtained. Comparisons are then made between the switch with the priority scheme and the switch without the priority scheme.

Finally, the thesis concludes in Chapter 5 by summarizing important findings of this thesis and outlining further research areas.

ATM Network Application

CHAPTER 2

Structure and Modeling of Single-Buffered Banyan Switch

2.1 Introduction

The function of a switch is to connect the traffic arriving at its inputs to appropriate outputs. The $N \times N$ switch architecture has N input ports where the traffic arrives and N output ports where the traffic leaves. In this thesis, we only consider packetized traffic. Fixed length packets arrive at the N inputs in time-slotted fashion. Each packet has the address of the output of the switch to which it is destined. This address of the packet is used by the switch to route each incoming packet to its appropriate output port.

A switch is usually constructed with switching elements and links (i.e. data paths). The 2×2 switching element, as shown in Fig. 2.1 , has two inputs and two outputs and directs the packets to the appropriate output ports according to the control signal obtained either from centralized controller or from the packet itself to route the packets. The former routing technique is called routing by a central control; the latter one is called self-routing. The switching elements may be of different sizes. The links are the passive data paths that connect different switching elements. Each input port of a switching element is fully connected to each output

port of that switching element. Normally, there are buffers allocated at the input ports or output ports of each switching element.

Fig. 2.1 A 2 x 2 Switching Element

2.2. Structure of the Single-Buffered Banyan Switch

The single-buffered Banyan network is a multistage interconnection network with stages consisting of an array of switching elements. Each switching element is a 2 x 2 crossbar switch with a single buffer at each of its input links. The switching element is linked to its adjacent stages in a particular interconnection pattern such that a unique path can be established from any one of the input ports of the network

to any one of its output ports. The structure of a 16 x 16 single-buffered Banyan network is shown in Fig. 2.2. For a Banyan network with N input ports and N output ports, the number of stages in the switching network is $\log_2 N$. A more detailed description of the interconnection patterns among the switching elements of the Banyan network is given by Patel [2].

Fig. 2.2 Structure of A 16 x 16 Single - Buffered Banyan Network

2.3. Operation of A Single - Buffered Banyan Switch

The Banyan network based ATM switch operates synchronously. In the first part of the clock cycle, control signals are passed across the network from the last stage toward the first stage, so that every port of the network can determine

whether to send or hold its packets. Then in the second part of the clock cycle, packets move in accordance with the control signals.

The switching element in the first stage sends the packet according to the first bit of the destination address. “0” or “1” will route the packet to the upper output port and to the lower output port, respectively. The n th stage switching element will perform the same function according to the n th bit of the destination address.

A packet is allowed to advance to the next stage if the buffer in the next stage is empty or if the buffer is about to become available because its packet can advance at the same clock cycle. A conflict arises when there are packets in both the upper and lower buffers that are destined to the same output port. In this case, a “blocked” packet has the higher priority of moving forward if it is competing with a “new” packet. Otherwise, one packet is chosen randomly to advance to the next stage, and the other one remains in the buffer. This scheme of packet priority during contention is expected to reduce the variance of the network delay.

2.4. Markov Chain Model of Switching Element with Single Buffer

In this section, we describe the Markov chain model for the single buffer in a switching element of the Banyan network under uniform traffic. The model proposed here is based on the “two-state” Markov chain model developed by Jenq [4]. In the previous “two-state” model, it is assumed that the blocked packet will

generate a new random destination during the next clock cycle. This is not a realistic assumption because the packet that has been blocked in the previous clock cycle will assume the same output port in the next clock cycle. In order to distinguish between the state in which the buffer contains a packet that has just arrived in the previous clock cycle and the state in which the buffer contains a packet that has been blocked at least once, we introduce a third state for the case that the buffer contains a blocked packet to modify the previous model. The following is a brief description of the states of the new model:

“e” : the state that the buffer in a switching element is empty;

“n” : the state that the buffer in a switching element contains a “ new” packet;

“b” : the state that the buffer in a switching element contains a “blocked” packet.

A “new” packet is a packet in the buffer that has just arrived in the previous clock cycle. A “blocked” packet is a packet in the buffer that has been blocked at least once.

We first define the following probabilities to be used in the analytical model:

1. $P_{i,j}^k$: the steady state probability that there is i packet of type j in the buffer of an SE at stage k , where $i = 0, 1$ and $j = \text{“e”}, \text{“n”}, \text{“b”}$, corresponding to the three states of the buffer in the Markov chain model. Notice that when $i = 0$, j can only be “e”.

2. q^k : the probability that a packet is ready to come to a buffer of an SE at stage k.
3. r_n^k : the probability that a “new” packet is able to move forward to the next stage given that there is a “new” packet in the buffer of an SE at stage k.
4. r_b^k : the probability that a “blocked” packet is able to move forward to the next stage given that there is a “blocked” packet in the buffer of an SE at stage k.

We use Markov chain to describe the transition of the three states of a single buffer. As shown in Fig. 2.3 The state of a buffer changes from “e” to “n” when there is a packet ready to come to this buffer. The state of a buffer remains at “e” when there is no packet ready to come to this buffer. When the state of the buffer is in “n”, it changes to state “e” when there is no packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage. When there is a packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage, the buffer remains in state “n”. When the packet in the buffer is not able to move forward, the state of the buffer changes from “n” to “b”. When the state of the buffer is in “b”, it changes to state “e” when there is no packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage. When the packet in the buffer is not able to move

forward, it remains in state “b”. The state of the buffer changes from “b” to “n” when there is a packet able to come to the buffer and the packet in the buffer is ready to move forward to the next stage.

Fig. 2 .3 The State Transition Diagram of A Single Buffer

CHAPTER 3

Performance Analysis of the Buffered Banyan Switch without Packet Priority

3.1. Introduction

The performance of the single-buffer Banyan network has been evaluated with “two-state” model under the uniform traffic pattern [4] [5] [6]. The results of these studies are potentially optimistic since this model can not accurately describe the behavior of the switching element during contention. In this chapter, we provide a complete performance analysis based on the new “three-state” model. We first present the state transition equations that govern the behavior of the single buffer of a switching element in the Banyan switching fabric. We then derive the relations among the steady state probabilities and obtain an recursive algorithm for calculating the performance parameters of the switch. Finally, we show the performance results based on the proposed “three-state” model and compare them with those of the previous “two-state” model.

3.2. The Traffic Pattern

We assume that packets arriving at each input link at the first stage of the switching fabric are destined uniformly (or randomly) for all output links at the last stage. We also

assume a uniform load for each input link at the first stage. Thus, we assume that the loads are balanced in the whole switching network. Under these assumptions, the state of a switching element at stage k is statistically not distinguishable from that of another switching element of the same stage. Therefore, the state of a “stage” can be reduced further to that of a single buffer. It is also assumed that the buffers within the same SE are statistically independent. As was pointed by Jenq [4] this independence assumption is reasonable in that the performance results do not differ too much when the independence assumption is removed.

3.3. The Analytic Model

In this section, a complete mathematical description is given to the “three-state” Markov chain model. Equations for the relationships among important state parameters are then established.

3.3.1. The State Transition Equations

The state transition equations of the Markov chain model of the Banyan switching fabric described in Chapter 2 are stated as follows:

$$\begin{pmatrix} p_{0,e}^k(t+1) \\ p_{1,n}^k(t+1) \\ p_{1,b}^k(t+1) \end{pmatrix} = T \cdot \begin{pmatrix} p_{0,e}^k(t) \\ p_{1,n}^k(t) \\ p_{1,b}^k(t) \end{pmatrix} \quad (3.1)$$

where T is the state transition matrix and

$$T = \begin{pmatrix} 1-q^k & (1-q^k)r_n^k & (1-q^k)r_b^k \\ q^k & q^k r_n^k & q^k r_b^k \\ 0 & 1-r_n^k & 1-r_b^k \end{pmatrix} \quad (3.2)$$

3.3.2. Derivation of r_n^k

Let us now derive the recursion for evaluating r_n^k .

A “new” packet is able to move forward if the following conditions hold at the same time:

- 1) it wins contention with its neighbor within the same SE;
- 2) the destined buffer at the next stage is able to accept a packet.

Condition 1) is satisfied when one of the following events occurs:

- a) there is no packet in the neighboring buffer within the same SE (this occurs with probability $p_{0,o}^k$);

b) there is a “new” packet in the neighboring buffer but the considered packet is

still able to move forward (this occurs with probability $0.75p_{1,n}^k$);

c) there is a “blocked” packet in the neighboring buffer but the considered packet

is still able to move forward (this occurs with probability $0.75p_{1,b}^k$).

Summing the probabilities in a), b) and c) , we have the corresponding probability for condition 1)

Pr (the “new” packet wins the contention with its neighboring buffer)

$$= p_{0,o}^k + 0.75p_{1,n}^k + 0.75p_{1,b}^k$$

Condition 2) is satisfied when one of the following events occurs:

a) there is no packet in the destined buffer of the SE at the next stage (this

occurs with probability $p_{0,e}^{k+1}$);

b) there is a “new” packet in the destined buffer of the SE at the next stage and it

is able to move forward during the next clock cycle (this occurs with

probability $p_{1,n}^{k+1}r_n^{k+1}$);

c) there is a “blocked” packet in the destined buffer of the SE at the next stage

and it is able to move forward during the next clock cycle (this occurs with

probability $p_{1,b}^{k+1}r_b^{k+1}$).

Summing the probabilities in a), b) and c) , we have the corresponding

probability for condition 2)

$$\Pr_{accept}^{k+1} = p_{0,s}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1}$$

Therefore, we have

$$\begin{aligned} r_n^k &= (p_{0,o}^k + 0.75p_{1,n}^k + 0.75p_{1,b}^k) \cdot \Pr_{accept}^{k+1} \\ &= (p_{0,o}^k + 0.75p_{1,n}^k + 0.75p_{1,b}^k) \cdot (p_{0,o}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1}) \\ (k &= 1, 2, 3, \dots, n-1) \end{aligned}$$

and

(3.3)

$$r_n^* = p_{0,o}^* + 0.75p_{1,n}^* + 0.75p_{1,b}^*$$

(3.4)

at the last stage of the switch.

3.3.3. Derivation of r_b^k

Let us now derive the recursion for evaluating r_b^k .

A “blocked” packet is able to move forward if both of the following conditions hold at the same time:

- 1) It wins contention with its neighbor within the same switching element;
- 2) The destined buffer at the next stage is able to accept a packet.

Condition 1) is satisfied when one of the following events happens :

- a) there is no packets in the neighboring buffer (this occurs with probability

$$p_{0,o}^k);$$

b) there is a “new” packet in the neighboring buffer but the considered packet is

still able to move forward (this occurs with probability $0.75p_{1,n}^k$);

c) there is a “blocked” packet in the neighboring buffer but the considered packet

is still able to move forward (this occurs with probability $0.75p_{1,b}^k$).

Summing the probabilities in a), b) and c), we have the corresponding probability for condition 1)

Pr (the “blocked” packet wins the contention with its neighboring buffer within the same SE)

$$= p_{0,o}^k + 0.75p_{1,n}^k + 0.75p_{1,b}^k$$

Suppose that the corresponding probability for condition 2) is Pr_{accept}^{k+1} . In this case, since the considered packet has been blocked and it is still destined for the same input buffer at the next stage (stage $k+1$). Therefore, we know that the destined buffer at stage $k+1$ can be in either one of the following situations:

a) It received a packet from the neighboring buffer at stage k in the previous clock cycle. Therefore, it is in state “new” at the beginning of the current clock cycle;

b) It did not receive any packet from stage k in the previous clock cycle.

Therefore it is in state “ blocked” at the beginning of the current clock cycle.

Therefore, the probability that the buffer at stage $k+1$ can accept a packet is

$$\frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} \cdot r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} \cdot r_b^{k+1}$$

Hence we have,

$$r_b^k = (p_{0,e}^k + 0.75p_{1,n}^k + 0.75p_{1,b}^k) \left(\frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right)$$

$$(k = 1, 2, 3, \dots, n-1)$$

(3.5)

and for $k = n$, we have

$$r_b^n = p_{0,e}^n + 0.75p_{1,n}^n + 0.75p_{1,b}^n$$

(3.6)

at the last stage of the switch.

3.3.4. Derivation of q^k

As mentioned before, q^k is defined as the steady state probability that a packet is ready to come to a buffer of an SE at stage k . This probability is given as follows:

$$q^k = 0.75(1 - p_{0,e}^{k-1})(1 - p_{0,e}^{k-1}) + 0.5p_{0,e}^{k-1}(1 - p_{0,e}^{k-1}) + 0.5(1 - p_{0,e}^{k-1})p_{0,e}^{k-1}$$

$$(k = 2, 3, 4, \dots, n)$$

(3.7)

Also notice that q^1 is the input load of the switch network.

With the above discussions, a recursive algorithm can be formed to calculate the steady state probabilities of the buffered Banyan switch at each stage.

3.4. Performance Parameters Formulations

In the performance analysis of the single buffered Banyan switching fabric, three important parameters are considered. They are network throughput, network delay and the delay variation.

3.4.1 The Network Throughput

Let λ^k be the throughput per port at stage k of the network. We define

$$\lambda^n = p_{1,n}^n r_n^n + p_{1,b}^n r_b^n \quad (3.8)$$

as the normalized network throughput, where n is the number of stages of the Banyan switch.

3.4.2 The Network Delay

The network delay is defined to be the average clock cycles required to transmit a packet across the Banyan network. Here we use the normalized delay as the mean delay at one stage of the Banyan network.

$$d = \frac{1}{n} \sum_{k=1}^n \left(1 + \frac{1 - r_n^k}{r_b^k} \right) \quad (3.9)$$

Detailed derivation of d can be found in Appendix A.

3.4.3 The Delay Variation

In the performance analysis of ATM switching fabrics, the variation of the switch delay is an important parameter. As for audio services, we want to minimize the delay variation as much as possible. In this paper, we use the moment generation function to derive a closed form expression for the variance of the delay. The normalized standard deviation of the network delay can be shown as follows:

$$\sigma = \frac{1}{n} \sum_{k=1}^n \sqrt{\frac{(1-r_b^k) + r_a^k(r_b^k - r_a^k)}{(r_b^k)^2}} \quad (3.10)$$

Detailed derivation for the delay variation can be found in Appendix B.

3.5. Performance Results and Comparisons

Equations (3.1) - (3.10) form a complete set of equations for the calculation of the performance parameters of the Banyan switch in a recursive fashion. The calculation starts from the last stage of the network and propagates back to the first stage. Given different input loads, we can obtain curves of performance parameters versus input loads. Further more, the size of the network (in terms of number of stages) can also be changed so that a set of performance plots can be obtained. In order to compare the performance results with that of the “two-state” model, a corresponding set of performance plots are drawn according to the algorithm provided by Jenq [4].

Performance results in comparison with the previous “two-state” model by Jenq [4] and Yoon [6] are plotted in Fig. 3.1 - Fig. 3.3 . These figures include plots for both the two state model and the three-state model at various number of stages, i.e. $n=1, 2, 4, 6, 10$.

3.5.1. Throughput

In Fig. 3.1, normalized throughput vs. input load $q(1)$ are plotted at various switch sizes. It is seen from the result plots that for Banyan switch of small size, the “three-state” model has nearly the same throughput as the two-state model. But as the number of stages goes beyond 4, there is significant difference in throughput between the two models. As was pointed out by Yoon [6], the analytic results of the “two state” model are more optimistic than simulation results. For a single buffered Banyan network with stage $n = 6$, at input load $q(1)=1.0$, the analytic throughput is about 49% while the throughput from simulation [6] is about 40%. The analytic throughput of the “three-state” model under the same network condition is 42% , which is much closer to the simulation result than the previous model. Therefore, the newly proposed “three-state” model gives more accurate predictions for the performance evaluation of the switching fabric. Also it is shown from Fig.3.1 that as input load $q(1)$ approaches 1.0, the normalized throughput tends to converge to an asymptotic value of 36% for a large Banyan switch (1024×1024).

Fig. 3.1 Normalized Throughput versus Input Load

3.5.2. Delay

The normalized network delays for various network sizes are plotted versus input load in Fig. 3.2. Again, for small size network, there is not much difference in delay between the two models. However, as the network size increases to beyond 6, there is some noticeable difference in delay between the two models. The “two-state” model tend to have more optimistic results. For $n = 6$, the normalized delay of the “three-state” model is about 1.55 clock cycles with input load equal to 1.0. The normalized delay of “two-state” model under same network condition is about 1.51 clock cycles . The normalized delay from simulation [7] is about 1.57 clock cycles with the same network size. This again shows that the “three-state” model is more accurate than the “two-state” model. It can be seen from the plot that switches with larger size tend to have higher delay. This is due to the fact that for blocking switch, contention will occur more often in larger network and therefore results in a higher network delay. Also notice that for small size switch, the delay increases almost linearly with input load.

Fig. 3.2 Normalized Network Delay versus Input Load

3.5.3. Delay Variation

The normalized standard deviation of the network delays for various network sizes are plotted vs. input load in Fig. 3.3. There is a significant difference in the standard deviation of delays between the two models. Again, the “two-state” model tend to have more optimistic results. This is due to the fact that a blocked packet will assume the same output port of an SE at the next clock cycle is not considered in the “two-state” model. For $n = 6$, the normalized standard deviation of the delay for the “three-state” model is about 1 clock cycle with input load equal to 1.0. The normalized standard deviation of the delay for the “two-state” model under same network condition is about 0.86 clock cycles . It can be seen from the plot that larger networks tend to have higher delay variation. This is due to the fact that for blocking switches, contention will occur more often in larger networks and therefore produce a higher network delay variation.

Fig. 3.3 Normalized Standard Deviation of Network Delay vs. Input Load

CHAPTER 4

Performance Analysis of Buffered Banyan Switch with Packet Priority

4.1. Introduction to The Packet Priority Scheme

Since Banyan based ATM switches are internally blocking switches, contention occurs when two packets in different buffers within the same switching element are going to the same output port of that SE. The ATM switching fabric described in the previous sections resolves the contention by choosing at random one of the two contending packets regardless of whether the packet has been blocked before or not. Under this routing algorithm, if a packet that has been blocked in the previous clock cycle happens to be not chosen to move forward to the next stage at the current clock cycle, it will experience more delay than a “new” packet which is chosen to move forward at the current clock cycle. This tends to enlarge the variation of the network delay. For delay sensitive services like audio and video supported by ATM, we wish to reduce the variance of the delay as much as possible. In this section, we introduce a new routing scheme by giving the “blocked” packet higher priority to move forward when it is contending with a “new” packet. In case when two contending packets are of the same type, i.e. both are “new” or “blocked”, one is chosen at random by the

routing logic to move forward. With this new scheme, we expect that the variance of the network delay will be reduced.

4.2. Modification on Expressions for r_n^k and r_b^k

With the introduction of the routing priority scheme for the blocked packet during contention, the first term in equation (3.3) for r_n^k needs to be modified, i.e. , the probability that a “new” packet is ready to move forward is

$$p_{0,e}^k + 0.75p_{1,n}^k + 0.5p_{1,b}^k$$

Notice that when a “new” packet is competing with a “blocked” packet in the same switching element to go to the same output port of that switching element, the “blocked” packet is always given higher priority to be routed forward, while the “new” packet in this case will have to wait in the buffer for one clock cycle. It is only when the “new” packet and the “blocked” packet are destined for different output ports of the same switching element, i.e. , “new” packet is destined for the upper port and “blocked” packet is destined for the lower port or “new” packet is destined for the lower port and “blocked” packet is destined for the upper port, that the “new” packet is ready to move forward.

Therefore, we have the modified expression for r_n^k

$$r_n^k = (p_{0,e}^k + 0.75p_{1,n}^k + 0.5p_{1,b}^k) \cdot (p_{0,e}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1})$$

$$(k = 1, 2, 3, \dots, n-1)$$

(4.1)

and for $k = n$, we have

$$r_n^n = p_{0,e}^n + 0.75p_{1,n}^n + 0.5p_{1,b}^n$$

(4.2)

at the last stage of the switching network.

Similarly, we have a modified expression for r_b^k

$$r_b^k = (p_{0,e}^k + 0.75p_{1,b}^k + p_{1,n}^k) \left(\frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right)$$

($k = 1, 2, 3, \dots, n-1$)

(4.3)

and for $k = n$, we have

$$r_b^n = p_{0,e}^n + 0.75p_{1,b}^n + p_{1,n}^n$$

(4.4)

at the last stage of the switching network.

Notice that when a “blocked” packet is competing with a “new” packet in the same switching element to go to the same output port of that switching element, it is

always given higher priority to be routed forward, in other words, a “blocked” packet in the buffer is always ready to move forward.

4.3. A Variable Priority Probability

In the above discussion , we assume that when contention occurs between a “blocked” packet and a “new” packet, the “blocked” packet will have the priority of being chosen to move forward (with priority probability = 1) . It is interesting to see how the switch performance, especially the variation of the delay, is affected when the degree of packet priority varies. To do this, let’s introduce a variable priority probability P to the Banyan switch’s routing control scheme.

P = the probability that a “ blocked” packet is chosen to move forward when it is contending with a “new” packet.

The value of P can vary from 0 to 1. When $P = 1$, it is the case studied above. When $P = 0.5$, there is no packet priority. This corresponds to the situation described in Chapter 3. When $P = 0$, the “new” packet will be chosen with higher priority to move forward when it is contending with the “blocked” packet.

We expect that the variance of the switch delay will decrease as P goes from 0 to 1.

With the introduction of this probability P , the expressions for r_n^k and r_b^k are therefore adjusted as follows:

$$r_n^k = [p_{0,e}^k + 0.75p_{1,n}^k + 0.5p_{1,b}^k + 0.5(1-P)p_{1,b}^k] \cdot (p_{0,e}^{k+1} + p_{1,n}^{k+1}r_n^{k+1} + p_{1,b}^{k+1}r_b^{k+1}) \quad (4.5)$$

where the term $0.5(1-P)p_{1,b}^k$ is coming from the event that both the “new” and “blocked” packets are going to the same output port but the “new” packet is chosen to move forward, and

$$r_b^k = (p_{0,e}^k + 0.75p_{1,b}^k + 0.5p_{1,n}^k + 0.5P \cdot p_{1,n}^k) \left(\frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right) \quad (4.6)$$

where the term $0.5P \cdot p_{1,n}^k$ is coming from the event that both the “blocked” and “new” packets are destined to the same output port but the “ blocked” packet is chosen to move forward.

The remaining part of the analysis, including the formulation of the switch performance parameters, remains the same as that in Chapter 3. In a similar fashion, a recursive algorithm can be formed to calculate the probabilities in the model with packet priority and the performance parameters.

4.4 Performance Results and Comparisons

The calculation of the performance parameters starts from the last stage of the network and propagates back to the first stage. Given different input loads, we can obtain curves of performance parameters versus input loads. Performance results of the “three-state” model with packet priority are plotted in Fig. 4.1 - Fig. 4.9. In order to compare the results with that of the switch without packet priority scheme, we also obtain plots corresponding to $P = 0.5$ in Fig. 4.1 ~ 4.4 .

4.4.1. Network Performance Versus Input Load

The network performance including throughput, delay and standard deviation of delay versus input load are plotted in Fig. 4.1 ~ 4.4 for both $P = 1.0$ and $P = 0.5$. In Fig. 4.1, the switch has $n = 6$ stages. When the switch input load equals to 1.0 and $P = 1.0$, the normalized throughput is about 48%; the normalized network delay is about 1.5 clock cycles; the standard deviation of the delay is about 0.74 clock cycle. In the case of no packet priority ($P = 0.5$), at input load equals to 1.0, the normalized throughput is about 42%; the normalized network delay is about 1.55 clock cycles; the standard deviation of the delay is about 1.05 clock cycles. In comparison with the switch without packet priority, the one with packet priority given to the “blocked” packet has better performances at various input loads. There is a significant reduction in delay variation (about 0.3 clock cycle) when the packet priority scheme is used. Similar observations can also be made from plots in Fig. 4.2 ~ Fig. 4.4. However, the improvements in throughput and delay are relatively insignificant at $n = 6$.

It can also be seen that as the number of switch stages increases, the difference in throughput between the switch with packet priority and the switch without packet priority becomes insignificant. Same conclusion can be drawn on the switch delay.

For throughput, the difference between the two types of switches become significant only when the input load reaches beyond 0.5. For large size ($n = 8$) switch, the switch delays for both types of switches are nearly the same.

Fig. 4.1 Network Performance versus Input Load at $n = 6$

Fig. 4.2 Network Performance versus Input Load at $n = 3$

Fig. 4.3 Network Performance versus Input Load at $n = 4$

Fig. 4.4 Network Performance versus Input Load at $n = 8$

4.4.2. Network Performance Versus Packet Priority Probability

In order to show how network performance, especially the variance of the network delay, is affected by the packet priority probability, the performance of the network versus P is plotted in Fig. 4.5 ~4.8 with various input loads and network sizes. The

performance results show that as the packet priority probability increases from 0 to 1, the variance of the delay decreases significantly. At input load equal to 1.0, switch size $n = 6$, the standard deviation of the network delay decreases almost linearly with the increase of P . There is an approximate 30% reduction in standard deviation of the delay when P goes from 0.5 to 1. Also it is interesting and delighted to notice that the other two performance parameters, throughput and delay are also improved slightly (almost linearly) when P increases. In Fig. 4.5, the throughput is improved by about 10% as P goes from 0.5 to 1. When $P = 0$, this corresponds to the case when the “new” packet will always be given higher priority to be moved forward when it is contending with a packet that has been blocked before. In this case, the switch has the largest delay variance.

The performance results in Fig. 4.1 - Fig. 4.8 confirm our earlier conjecture that by introducing the packet priority probability, the variance of the network delay is indeed reduced and also the throughput and delay is improved slightly.

Fig. 4.5 Network Performance versus Packet Priority Probability at $n = 6$, $q(1) = 1.0$

Fig. 4.6 Network Performance versus Packet Priority Probability at $n = 3$, $q(1) = 1.0$

Fig. 4.7 Network Performance versus Packet Priority Probability at $n = 4$, $q(1) = 0.7$

Fig. 4.8 Network Performance versus Packet Priority Probability at $n = 8$, $q(1) = 0.3$

4.4.3. The Asymptotic Property

In order to see the asymptotic character of the network performance, plots of the normalized throughput with $P=1.0$ and $P=0.5$ versus network size n is shown in Fig. 4.9. It is seen that at input load equal to 1.0, as the network size increases the

normalized throughput approaches to about 35% for the “three-state” model with packet priority probability equals to 1.0 . In the case of no packet priority ($P=0.5$), the normalized throughput approaches to about 28% . Again it is shown that the throughput is improved when using the packet priority.

Fig. 4.9 Normalized Throughput versus Network Size n

CHAPTER 5

Conclusion

5.1 Summary

In this thesis, we proposed a new model for the performance analysis of single-buffered Banyan network based ATM switching fabric. In the new model, we described the behavior of the switching element in the Banyan network by introducing a third state into the Markov chain model to deal with the situation where a blocked packet will still attempt to access the same output port in the next clock cycle. The proposed model is therefore more accurate in evaluating the performance of the Banyan switch than the previous model. Analytical results based on the new “three-state” model show that the maximum throughput of a single-buffered Banyan network under uniform traffic is about 42% for a switch of size 64×64 .

A simple routing control mechanism to deal with contention in the switching element is implemented in the proposed ATM switching fabric by giving the “blocked” packet higher priority to move forward to the next stage when it is

competing with a packet that has never been blocked before. The variation of the network delay is significantly reduced (by 30%) when the “ packet priority” is used.

Also in this paper, we studied the variance of the network delay analytically by using the moment generating function and provide the analytical methods for the computation of the network delay and its standard deviation.

5.2 Future Research

The traffic pattern that we used for the performance analysis in this paper is uniform. However, for a more realistic ATM environment, a study of the performance of the proposed “ three-state “ ATM switch model with cell priority under nonuniform traffic is necessary. Also, the author feel the analytical model developed in this paper could be extended to analyze the Banyan networks with multibuffers and switching elements with arbitrary size.

It is also necessary to investigate the cost of implementation. The cost of implementation is difficult to estimate because it depends on the technology in which the network is implemented. However, an approximate estimate of the cost will assist in selecting the appropriate multistage network for a fast packet switching architecture in the Broadband ISDN environment.

Appendix A

Derivation of the Mean Delay

Consider the probability distribution of the delay for a packet at one stage which is a discrete random variable. Let p_i be the probability that the delay at stage k is i clock cycle(s). Table 1 lists the probability distribution for the packet delay at one stage.

Therefore, we have

$$p_i = r_b^k (1 - r_b^k)^{i-2} (1 - r_n^k) \quad (i = 2, 3, 4, \dots)$$

and $p_1 = r_n^k$

Let $P(z)$ be the moment generating function of the delay. Thus

$$\begin{aligned} P(z) &= \sum_{k=0}^{\infty} p_k z^k \\ &= p_1 z + p_2 z^2 + p_3 z^3 + p_4 z^4 + \dots \\ &= r_n^k z + (1 - r_n^k) r_b^k z^2 + (1 - r_n^k)(1 - r_b^k) r_b^k z^3 + (1 - r_n^k)(1 - r_b^k)^2 r_b^k z^4 + \dots \\ &= z \{ r_n^k + (1 - r_n^k) [r_b^k z [1 + (1 - r_b^k) z + (1 - r_b^k)^2 z + (1 - r_b^k)^3 z + \dots]] \} \\ &= z \left\{ r_n^k + \frac{(1 - r_n^k) r_b^k z}{1 - (1 - r_b^k) z} \right\} \end{aligned} \quad (A.1)$$

Take the first derivative of (A.1), we have

$$P(z) = r_n^k + (1 - r_n^k) r_b^k z \left\{ \frac{1}{1 - (1 - r_b^k) z} + \frac{1}{[1 - (1 - r_b^k) z]^2} \right\} \quad (\text{A.2})$$

Table 1

Delay at one stage	Probability
1	$p_1 = r_n^k$
2	$p_2 = r_b^k (1 - r_n^k)$
3	$p_3 = r_b^k (1 - r_b^k) (1 - r_n^k)$
4	$p_4 = r_b^k (1 - r_b^k)^2 (1 - r_n^k)$
...	...
i	$p_i = r_b^k (1 - r_b^k)^{i-2} (1 - r_n^k)$

Therefore, the mean delay at stage k , $d(k)$ is expressed as follows:

$$\begin{aligned}
 d(k) &= P'(1) \\
 &= r_n^k + (1 - r_n^k)r_b^k \left\{ \frac{1}{1 - (1 - r_b^k)} + \frac{1}{[1 - (1 - r_b^k)]^2} \right\} \\
 &= r_n^k + (1 - r_n^k) \left(1 + \frac{1}{r_b^k} \right) \\
 &= 1 + \frac{1 - r_n^k}{r_b^k}
 \end{aligned}
 \tag{A.3}$$

Hence the normalized network delay d is expressed as follows:

$$d = \frac{1}{n} \sum_{k=1}^n \left(1 + \frac{1 - r_n^k}{r_b^k} \right)
 \tag{A.4}$$

Appendix B

Derivation of the Delay Variance

From (A.2) we have the second moment

$$P'(z) = (1 - r_n^k) r_b^k \left\{ \left[\frac{1}{1 - (1 - r_b^k)z} + \frac{1}{[1 - (1 - r_b^k)z]^2} \right] + z(1 - r_b^k) \left[\frac{1}{[1 - (1 - r_b^k)z]^2} + \frac{1}{[1 - (1 - r_b^k)z]^3} \right] \right\} \quad (\text{B.1})$$

Therefore,

$$P''(1) = \frac{2(1 - r_n^k)}{(r_b^k)^2} \quad (\text{B.2})$$

Hence the variance of the delay at stage k is

$$\begin{aligned} & \text{Var}\{\text{delay}(k)\} \\ &= E\left\{\left[\text{delay}(k) - E[\text{delay}(k)]\right]^2\right\} \\ &= E\left\{\left[\text{delay}(k) - d(k)\right]^2\right\} \\ &= E\left\{[\text{delay}(k)]^2\right\} - d^2(k) \\ &= P''(1) + P'(1) - [P'(1)]^2 \\ &= \frac{2(1 - r_n^k)}{(r_b^k)^2} + \frac{1 + r_b^k - r_n^k}{r_b^k} + \frac{(1 + r_b^k - r_n^k)^2}{(r_b^k)^2} \end{aligned}$$

$$\begin{aligned}
&= \frac{(1-r_n^k)(2+r_b^k)+(r_b^k)^2}{(r_b^k)^2} - \frac{(1+r_b^k-r_n^k)^2}{(r_b^k)^2} \\
&= \frac{1-r_b^k+r_n^k r_b^k-(r_n^k)^2}{(r_b^k)^2} \\
&= \frac{(1-r_n^k)(1+r_n^k-r_b^k)}{(r_b^k)^2} \\
&= \frac{(1-r_b^k)+r_n^k(r_b^k-r_n^k)}{(r_b^k)^2}
\end{aligned}$$

(B.3)

In this paper, we use the normalized standard deviation of the network delay

$$\begin{aligned}
\sigma &= \frac{1}{n} \sqrt{\text{Var}[\text{delay}(k)]} \\
&= \frac{1}{n} \sum_{k=1}^n \sqrt{\frac{(1-r_b^k)+r_n^k(r_b^k-r_n^k)}{(r_b^k)^2}}
\end{aligned}$$

(B.4)

where $\text{delay}(k)$ is the delay at stage k of the network, which is a random variable.

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