4-15-2008

Design of Radio-Frequency Filters and Oscillators in Deep-Submicron CMOS Technology

Haiqiao Xiao
Portland State University

DISSERTATION APPROVAL

The abstract and dissertation of Haiqiao Xiao for the Doctor of Philosophy in Electrical and Computer Engineering were presented April 15, 2008, and accepted by the dissertation committee and the doctoral program.

COMMITTEE APPROVALS: _____
Rolf Schaumann, Chair

_____
W. Robert Daasch

_____
Branimir Pejcinovic

_____
Xiaoyu Song

_____
Charles Balogh
Representative of the Office of Graduate Studies

DOCTORAL PROGRAM APPROVAL: _____
Malgorzata Chrzanowska-Jeske, Director
Electrical and Computer Engineering
Ph.D. Program

ABSTRACT

An abstract of the dissertation of Haiqiao Xiao for the Doctor of Philosophy in Electrical and Computer Engineering presented April 15, 2008.

Title: Design of Radio-Frequency Filters and Oscillators in Deep-Submicron CMOS Technology

Radio-frequency filters and oscillators are widely used in wireless communication and high-speed digital systems, and they are mostly built on passive integrated inductors, which occupy a relative large silicon area. This research attempted to implement filters and oscillators operating at 1-5 GHz using transistors only, to reduce the circuits' area. The filters and oscillators are designed using active inductors, based on the gyrator principle; they are fabricated in standard digital CMOS technology to be compatible with logic circuits and further lower the cost. To obtain the highest operating frequency, only parasitic capacitors were used.

Two new active-inductor circuits are derived from this research, labeled all-NMOS and all-NMOS-II. The all-NMOS active inductor was used to design high-Q bandpass filters and oscillators, which were fabricated in TSMC's 0.18-μm digital CMOS process. The highest center frequency measured was 5.7 GHz at 0.20-μm gate length and the maximum repeatably measured Q was 665. 2.4-GHz circuits were also designed and fabricated in 0.40-μm gate length. The all-NMOS-II circuit has superior linearity and signal fidelity, which are robust against process and temperature variations, due to its novel structure. It was used in signal drivers and will be

fabricated in commercial products.

Small-signal analysis was conducted for each of the active-inductor, filter and oscillator circuits, and the calculated performance matches those from simulations. The noise performance of the active inductor, active-inductor filter and oscillator was also analyzed and the calculated results agree with simulations. The difference between simulation and measured results is about 10% due to modeling and parasitic extraction error.

The all-NMOS active-inductor circuit was granted a US patent. The US patent for all-NMOS-II circuit is pending. This research generated three conference papers and two journal papers.

DESIGN OF RADIO-FREQUENCY FILTERS AND OSCILLATORS IN DEEP-SUBMICRON CMOS TECHNOLOGY

by

HAIQIAO XIAO

A dissertation submitted in partial fulfillment of the
requirements for the degree of

DOCTOR OF PHILOSOPHY
in
ELECTRICAL AND COMPUTER ENGINEERING

Portland State University
2008

ACKNOWLEDGMENTS

First of all, I would like to thank my academic advisor, Professor Rolf Schaumann, for his guidance and insight on filter theory, analog circuits, and research. Through my working with him, my research skills, such as critical thinking and problem solving, improved tremendously. I also learnt ways to do a quality and thorough work and be creative.

I would like to thank Professor W. Robert Daasch for his advice and discussions on circuits, layout, technology and device modeling. His enthusiasm about knowledge is very encouraging, and I learnt how to pursue a problem to its root through working with him.

I thank Professor Branimir Pejcinovic for the many discussions on radio-frequency designs and measurements. His microwave course was very useful to my research and interesting by itself.

I would like to thank Professor Xiaoyu Song for his advice and discussions on integrated circuit design and research. His Digital IC Design course helped me greatly on CMOS technology and device physics. I was very much encouraged and affected by his optimism and resourcefulness in solving problems.

I thank Professor Paul Van Halen for his lectures on analog circuit design, which were insightful and helpful to my research.

I thank Philip K. Wong for his help on using the microwave instruments during

IC laboratory characterization.

I thank Professors Charles Balogh and Mara Tableman for their lectures on mathematics. The knowledge is very beneficial to my career and broadened my interests. I appreciate Prof. Charles Balogh's acting as my Graduate Office Representative.

I would like to thank Joseph D. Stenger and Nathan Moyal of Cypress Semiconductors for their support and encouragement on the dissertation, and the opportunity they provided me to advance my research. The help of Jeff Kittle at Cypress on the measurement of phase noise is gratefully acknowledged.

I acknowledge the financial support from the Semiconductor Research Corporation (SRC), ECE Department of Portland State University, and Cypress Semiconductors during my study.

I especially thank my wife, Jing Xia, for her encouragement and patience on my study and research. Without her support, I would not be able to complete the dissertation. I am deeply indebted to her for allowing me to devote so much time and attention to academic pursuit.

I thank my parents and sister for their understanding and encouragement, and for helping me choosing the right career.

I owe special thanks to Hans and Lois Blom, for their encouragement and spiritual inspiration to enable the completion of the dissertation. Lois' proofreading of my dissertation is greatly appreciated.

Finally, I thank Xiangying Ma, Wei Wang, David H. Chiang and Aydin Karsilayan for introducing me to such a great study opportunity.

TABLE OF CONTENTS

page

LIST OF TABLES

Table page

LIST OF FIGURES

Figure page

GLOSSARY

ADC: Analog-to-digital converter/conversion.

ASIC: Application specific integrated circuit.

CMOS: Complementary metal-oxide semiconductor.

DAC: Digital-to-analog converter/conversion.

DSP: Digital signal processing.

Gm: Transconductor, a two-port voltage-to-current converter.

Gyrator: A two-port element that converts its load, Z_L, into $1/Z_L$ at its input port.

IC: Integrated circuit.

IF: Intermediate frequency.

LAN: Local area network.

LNA: Low-noise amplifier.

Opamp: Operational amplifier.

OTA: Operational transconductance amplifier.

PLL: Phase lock loop.

RF: Radio frequency.

TIA: Trans-impedance amplifier.

VCO: Voltage-controlled oscillator.

CHAPTER 1

INTRODUCTION

1.1 The Need for RF Analog Filters and Oscillators

In the last two decades or so, the number of Radio-Frequency (RF) communication integrated circuits (ICs) has seen a dramatic increase, for example, mobile phones, wireless computer peripherals such as cordless mice, wireless routers, inventory information networks, and hobbies. RF communication ICs extensively use oscillators and filters as local oscillators, intermediate frequency (IF) filters, channel-selecting filters and anti-aliasing filters, which span frequencies from about 200 kHz to approximately 5.2 GHz, depending on their location within the radio [1]. Though functionally distinct, the design and theory of filters and oscillators are closely related.

Digital circuits also use oscillators and sometimes filters. As the clock speed reaches several GHz, microprocessors and Application Specific Integrated Circuits (ASICs) are seeing increased use of RF oscillators for clock generation and timing recovery [2]. Filters are widely used in phase locked loops (PLLs) and signal equalization. To be competitive, the ICs must be low-cost. When in mass production, the costs of filters and oscillators are primarily determined by their die area. Thus, reducing die area is a major objective of this work.

Signal filtering and generation can also be done by Digital Signal Processing (DSP) techniques, with high predictability. However, they are generally limited to signal frequencies below 500 MHz. Between 500 MHz and 1 GHz, there are serious tradeoffs between analog processing and DSP in terms of power and cost. To

implement real-time DSP above 1 GHz, the sampling rate and computing circuitry must operate at 10-100 GHz, which is not yet possible, not to mention the tremendous cost due to circuit complexity, silicon area and power dissipation. On the other hand, a properly designed analog circuit can readily process gigahertz signals with moderate power and costs.

The discussion in this work is limited to continuous-time circuits, as some filters, such as switched-capacitor filters, are analog, but not continuous-time. However, "analog" will be used throughout this work for brevity. In the general sense, "radio-frequency" includes all frequencies at which electromagnetic signals can be transmitted, either by line-of-sight propagation and reflections or guided by ionosphere and terrestrial surface, and that starts from approximately 3 kHz [3]. In this work, by "radio frequency", we imply frequencies above 1 GHz, which is also roughly the starting frequency of "microwave" circuits. However, microwave circuits are treated as distributed circuits, while the circuits in this work are designed so that even though they operate at microwave frequency, the distributed effects are negligible and the circuits can be treated as lumped for design and simulation purposes.

1.2 Example Applications

RF oscillators and filters found their first and most popular applications in the wireless communication industry, which includes mobile phones and wireless local connections such as Local Area Networks (LANs) and computer peripherals, understandably, due to the high-frequency requirements. In many cases the baseband signal processing is done by DSP, because of its predicable performance using digital

CMOS process; however, signals above the IF frequency have to be processed by analog RF circuitry. The RF front-end and baseband are interfaced by analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

Shown in Fig. 1-1 is the architecture of a typical wireless communication IC [1]: the antenna and its impedance matching network / band-selecting filter are shared between inbound (Rx) and outbound (Tx) signals by means of an RF switch. Two mixers implement down conversion and up conversion for the Rx and Tx signals, respectively. An RF oscillator phase-locked to a reference frequency from an offchip crystal oscillator provides the signal for the mixers.

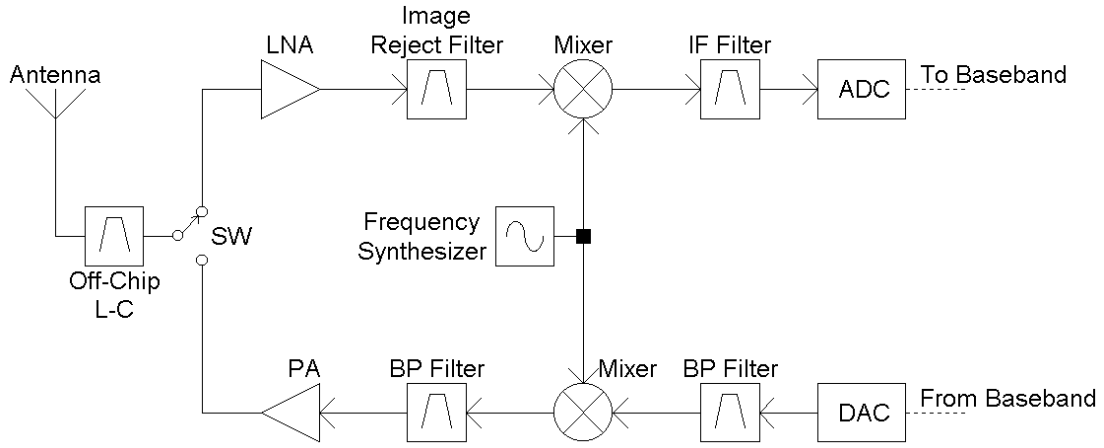


Figure 1-1 The architecture of a wireless communication IC.

Low-to-medium frequency analog filters are needed for IF filtering, ADC anti-aliasing and DAC waveform smoothing. Gigahertz bandpass filters are needed for the band selection, image rejection and Tx spectrum shaping. The band-selection filter rejects out-of-band large interferers and prevents them from saturating the LNA. The image-rejection filter prevents the image frequency from showing up in the down-converted signal band and interfering with the desired signals. The image rejection

filter can be omitted if polyphase (in-phase and quadrature) signal processing is used to the right of the mixers, but that entails quadrature local oscillator and mixers, and doubles the silicon area and power dissipation [1]. The Tx spectrum shaping filter prevents the out-of-band signals from being transmitted, as required by industry regulations.

Gigahertz oscillators are also used in high-speed digital circuits, such as Phase Locked Loops (PLLs), as shown in Fig. 1-2. Different from wireless communication ICs, which require low harmonic distortion sinusoidal signals in the RF section, the output signals in digital circuits are ideally pulses. However, when operated at frequencies above 500 MHz, the signal path bandwidth becomes low compared with the frequency, the signal edges are rounded, and analog techniques must be used.

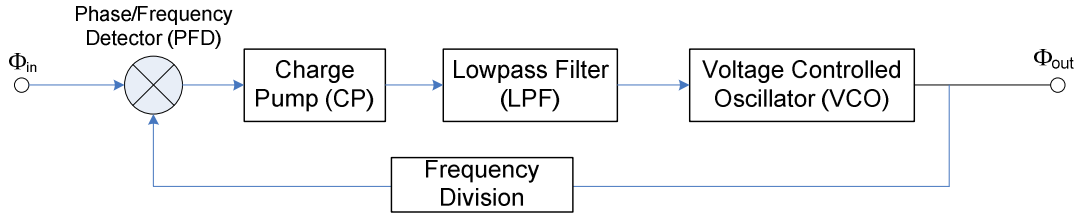


Figure 1-2 Block diagram of a charge-pump PLL.

Inside the PLL, the lowpass loop filter usually operates at a few MHz, while the VCO can be as high as a few GHz.

1.3 Implementation Methods and Literature Survey

The implementation methods of analog filters and oscillators can be categorized into active and (*Q*-enhanced) passive, depending on whether any passive elements such as inductors are involved. In most cases "passive designs" have active circuitry and consumes power in order to enhance the circuit *Q* or realize oscillation, hence they are

more accurately called enhanced passive designs. We classify a circuit as active if only transistors and capacitors are used. The implementation method also depends largely on the operating frequency, because basic electricity laws determine the value of circuit components and there are severe technical limitations on available integrated components, no matter how sophisticated or advanced the fabrication process is. To be sure, transistors are plentiful and cheap (but their power dissipation can be expensive); large capacitors and resistors are expensive and may not be available at all; inductors are expensive and may not be available, and large inductance values (> ~100 nH) are simply impossible.

Active circuits can be used to design oscillators and filters at almost any frequencies, with varied performance and tradeoffs. Below ~100 kHz, filters and oscillators are best designed using opamp-*R*-*C* circuits, likely with a few off-chip capacitors [4]. Between 100 kHz and ~100 MHz, transconductance-*C* (G_M-*C*) is the most popular method and can be fully integrated. The transconductors typically use linearization techniques to improve dynamic range, though the linearization circuits create extra noise. Between 100 MHz and ~500 MHz, G_M-*C* method can still be used, but the requirement on G_M is much higher: they must have minimum parasitic capacitance and phase shift. For frequencies above 500 MHz, the G_Ms are usually reduced to single-transistor or minimum-transistor-count circuits, and the capacitors are very small or completely eliminated, with parasitic capacitance being used to obtain the desired operating frequency.

If passive inductors are available, they can usually be used to design oscillators and filters operating from 500 MHz to 7-10 GHz. For operating frequencies below 500

MHz, the required inductance value is too large and difficult to implement. On the other hand, the self-resonance frequencies of passive inductors are usually around 6-7 GHz, and thus they cannot be used to obtain operating frequencies above that either. Passive inductors have low Qs between 5 and ~ 25, typically around 10. For oscillators, the low Q (and other circuit losses) is compensated by a negative resistance circuit, and the inductor loss only contributes to the oscillator output noise, typically measured in terms of phase noise. To implement narrow-band or high-order lowpass filters, the low Q will have to be "enhanced" by negative resistors [5] or some feedback scheme such as the use of integrated transformers [6].

Oscillators and filters can also be designed using microwave methods, for operating frequencies from ~500 MHz to above 10 GHz. Generally, transmission lines built from metal interconnects are involved. There are two main ways of using transmission lines. Transmission lines of a certain length can generate a specific phase shift at a certain frequency. When used with active circuits in feedback or feed-forward, oscillators and filters can be obtained. Alternatively, terminated (open or ac short-circuit) transmission line stubs can have an inductive or capacitive input impedance of a certain value around a certain frequency, and be used in building oscillators and filters. Note that the transmission line stubs are equivalent to an inductor or a capacitor of desired value only near the design frequency. Therefore, they can only be used to build filters operating over a relative narrow bandwidth. Away from the design frequency, the inductor or capacitor equivalence no longer holds. Computer optimization methods can be used to expand the frequency band of filters designed this way [7].

Finally, oscillators and filters can be implemented using off-chip passive elements, such as crystal and Surface Acoustic Wave (SAW) devices. They utilize some kind of mechanical resonance, and by converting back and forth mechanical movements with electrical signals, implement electrical filters and oscillators. Electrically, the device is equivalent to an *R-L-C* resonator tank, but with extremely high *Q*s up to a few thousands. However, they generally cannot be fabricated on silicon dies or packaged with a die on the same IC, hence, they are expensive to use.

This work focuses on the implementation of oscillators and filters operating above 1 GHz, using transistors and capacitors only.

1.4 Technical Requirements Summary

The targets of this research are:

1. Integrated oscillators and high-*Q* bandpass filters operating at the highest possible frequency as limited by the available technology.
2. Fabricated in the latest deep-submicron standard digital CMOS technology.
3. Operating at 1.8 V or lower.
4. Only transistors and capacitors compatible with digital CMOS are to be used.
5. The circuits are to be designed using minimum device sizes.
6. The circuits need to be robust. No trimming is allowed to overcome process variations, and the high-*Q* filters must be stable when biased with regular commercial components.
7. The oscillators and filters must be electronically tunable to allow for correction of errors from modeling inaccuracies, process variations and environmental

disturbances. The oscillators and filters must provide the appropriate tuning handles for automatic tuning.

Once again, the discussion hereafter is limited to lumped integrated circuits composed primarily of transistors and capacitors, with occasional involvement of passive inductors. Admittedly, above 1 GHz, analog ICs demonstrate distributed effects at times. However, attention has been paid in the circuit design and layout to minimize the distributed effects, for example, by making the layout compact compared with the signal wavelength, always using voltage signals (low R_S, high R_L) or current signals, and increasing the equivalent Z_0 of long signal interconnects by making its inductance per unit length far greater than capacitance per unit length. Without this qualification, some of the statements in this work will not be correct in the strictest sense.

CHAPTER 2

DESIGN OF RF ACTIVE INDUCTOR

2.1 The Need for RF Active Inductor

Inductors (*L*), either passive or simulated using active circuitry, are needed for implementing filters and oscillators. Admittedly, using opamp and *R*-*C* phase shift networks, oscillators such as the Wien-Bridge circuit may be implemented and low-quality-factor (low-*Q*) filters may be obtained using only *R* and *C* [4], but these cases are in the minority and cannot meet the performance requirement of many, if not most, applications. Equivalent (i.e., active) inductors are not always easily detected in active *R*-*C* circuits, especially when the circuit is designed or explained using signal flow, state variables, or other methodologies rather than starting from a passive *L*-*C* prototype. Nonetheless, many oscillators and filters designed using other concepts, such as integrator loops or recursive filtering [8], can almost always be explained by demarcating the circuit elements into active inductor(s), in part, because most filters and oscillators can be equated to prototype *R*-*L*-*C* networks, where the *L* is implemented actively.

To be useful, the active inductor has to have a self-resonance frequency higher than that of the oscillators and filters, and with some margin, because accessory circuits have additional parasitic capacitance, which will lower the operating frequency.

The requirement on active inductor *Q* varies among applications. The *Q*, in principle, does not have to be high in designing oscillators. However, a low-*Q* active

inductor will require a higher-gain feedback circuit, and increase power dissipation and circuit noise. Hence, we are motivated to design a high-Q active inductor for oscillators without introducing undue noise or power dissipation. High-Q bandpass filters and high-order narrow-transition-band lowpass filters also require high-Q inductors.

Low-order lowpass filters do not require high-Q inductors. However, a high-Q inductor will reduce performance errors, such as dc-gain errors, and generally make the design process easier simply because the inductor is closer to an ideal inductor.

2.2 Active-Inductor Design Method

2.2.1 The Gyrator Approach

All active inductors must have at least one capacitor whose voltage lags its current by 90° at ac steady state. Through a properly arranged active circuit, the voltage at the input port of the active inductor can be made to *lead* the input current by 90°. Thus, an inductive input impedance or an equivalent inductor is implemented. Note that the I-V relationship at ac in transistors (excluding their parasitic capacitance) and resistors is always 0° or 180°. Hence, a pure transistor and/or resistor circuit without any capacitor can never generate a 90° I-V relationship to implement an active inductor.

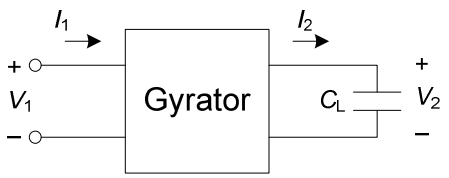


Figure 2-1 Implementing an active inductor using a gyrator.

The conversion is shown in Fig. 2-1. The black box that does the I-V

phase/magnitude translation on the C_{Load} is called a "gyrator", because it inverses the load impedance:

$$Z_{\text{in}} = \frac{R^2}{Z_{\text{L}}} = R^2 sC_{\text{L}} = sL_{\text{eq}} \tag{2.1}$$

where $L_{\text{eq}} = R^2 C_{\text{L}}$ is the equivalent inductance.

The gyrator was proposed by Bernard D. H. Tellegen around 1948 [9], though it is possible that other researchers were working on the same circuit behavior earlier but did not conceptualize and publish it. All active inductor circuits can be analyzed using basic circuit analysis or other methods; but the use of the gyrator concept makes the analysis more concise.

2.2.2 Active Inductor Implementation Methods

Electronic gyrators, and in turn active inductors, can be built with opamps, Operational Transconductance Amplifiers (OTAs), or transistors. The building method largely depends on the desired self-resonance frequency f_{R} of the finished active inductor, since the active inductor will behave as an inductor only at frequencies (well) below f_{R}. An opamp generally can be used to build active inductors with f_{R}s ≤ 1-5% that of its unity-gain frequency f_{u}. For example, an LM741 has an f_{u} of 1.5 MHz, and can be used to build active inductors operating up to about 50 kHz. With frequency and Q pre-distortion [10], we can build active-inductor filters operating slightly above this limit, but the design tradeoffs become severe rapidly. Since the maximum f_{u} of onchip CMOS opamps is about 1 GHz, we could expect to obtain opamp active inductors operating between 10-50 MHz.

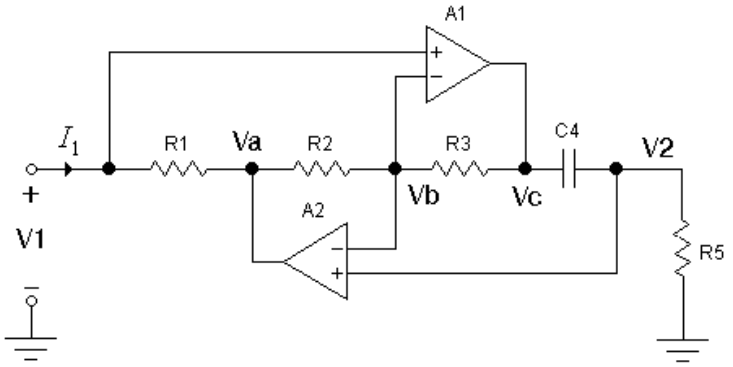


Figure 2-2 Implementing an active inductor using two opamps.

Shown in Fig. 2-2 is an example of implementing an active inductor with opamps. The input impedance is

$$Z_{\text{in}}(s) = \frac{V_1}{I_1} = sC_4 \frac{R_1 R_3 R_5}{R_2} = sL_{\text{eq}} \tag{2.2}$$

and,

$$L_{\text{eq}} = C_4 \frac{R_1 R_3 R_5}{R_2} \tag{2.3}$$

The circuit may not appear to be a gyrator since it is seemingly loaded with a resistor R_5. But if we extract C_4 out of the circuit, and treat V_1-Gnd as Port 1 and V_C-V_2 as Port 2, then between Port 1 and Port 2 the circuit is a gyrator. A drawback of this circuit is that it requires a floating capacitor, which has a sizeable parasitic capacitance on its bottom plate in integrated implementations and will distort the circuit performance.

The phase shifts of the opamps will generate parasitic poles and zeros in $Z_{\text{in}}(s)$ and make the equivalent inductor non-ideal [10]. Nonetheless, at moderate frequencies the circuit is equivalent to an inductor to the first order.

Above 10 MHz, the appropriate way of building active inductors is OTA-*C*, or rather, transconductor-*C* (G_M-*C*) method. The difference between OTA and G_M is obscure. Common understanding is that OTA typically means a transconductor with a differential-pair input, and in most cases, optimized for high R_{OUT} and high dc gain; while G_M is a transconductor with only one or a few transistors, with a particular transconductance value and higher linearity than OTA. This work concentrates on G_M-*C* implementation, though the underlying principles largely the same.

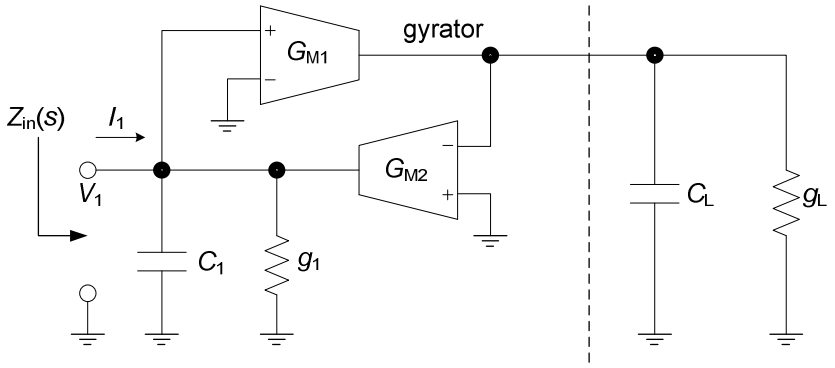


Figure 2-3 Implementing an active inductor using OTAs or G_Ms.

As shown in Fig. 2-3, by connecting an inverting and a noninverting transconductor in a negative feedback loop, a gyrator is derived. When loaded with a capacitor, the input impedance of the gyrator is that of an equivalent inductor. Ignoring C_1, g_1 and g_L for the moment, using simple circuit analysis methods, the input impedance is calculated to be

$$Z_{in}(s) = \frac{V_1}{I_1} = s\frac{C_L}{G_{M1}G_{M2}} = sL_{eq} \tag{2.4}$$

which is an equivalent ideal inductor. Practical G_M cells have non-zero input and output capacitance, C_i and C_o, as well as finite output resistance, R_o, and these are lumped together and modeled as C_1, g_1 and g_L in Fig. 2-3. With these parasitic

elements, the input admittance becomes:

$$Y_{\text{in}} = \frac{1}{Z_{\text{in}}} = \frac{G_{\text{M1}}G_{\text{M2}}}{sC_{\text{L}} + g_{\text{L}}} + sC_1 + g_1 = \frac{1}{s\frac{C_{\text{L}}}{G_{\text{M1}}G_{\text{M2}}} + \frac{g_{\text{L}}}{G_{\text{M1}}G_{\text{M2}}}} + sC_1 + g_1$$
$$= \frac{1}{sL_{\text{eq}} + r_{\text{s}}} + sC_1 + g_1 = \frac{1}{sL_{\text{eq}} + r_{\text{s}}} + sC_{\text{p}} + g_{\text{p}} \tag{2.5}$$

whose equivalent circuit is shown in Fig. 2-4. The equivalent components are

$$L_{\text{eq}} = \frac{C_{\text{L}}}{G_{\text{M1}}G_{\text{M2}}}, \quad r_{\text{s}} = \frac{g_{\text{L}}}{G_{\text{M1}}G_{\text{M2}}}, \quad C_{\text{p}} = C_1, \quad g_{\text{p}} = g_1 \tag{2.6}$$

Incidentally, all real passive inductors have the same equivalent circuit that will be discussed more in the next section.

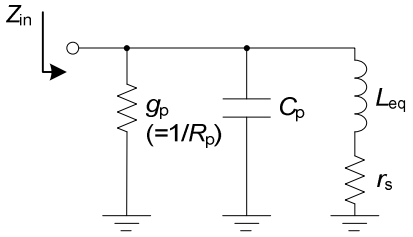


Figure 2-4 Equivalent circuit of a G_{M}-C active inductor.

There are two issues limiting the operating frequency of G_{M}-C active inductors:

(1) When the operating frequency increases, the parasitic capacitance and G_{M} value do not change substantially, thus the required C_{L} becomes smaller and smaller, and eventually negative at some point. It is true that equivalent negative capacitors can be implemented actively; however, in most cases, the active negative capacitor implemented using the same G_{M} cell will have a self-resonance frequency similar to that of the active inductor, hence it will not increase the self-resonance frequency of the entire circuit.

(2) The G_{M} cells have phase shift (usually a phase lag) that increases with

frequency. A small phase shift (< ~10°) will generate an equivalent negative resistive element in Z_{in}, which increases the Q of the inductor and will eventually render it unstable at a certain point. This will be discussed in detail in Section 2.5.

For operation above 500 MHz, the G_M cells in the active inductor circuit must be highly simplified, and highly efficient in terms of a high G_M to C_i, C_o ratio. Linearization circuits will have to be eliminated to reduce the G_M phase lag. Single-transistor or minimum-transistor-count G_M cells have to be used. The load capacitor may be eliminated and only the transistor parasitic capacitance, such as C_{gs} and C_{jd}, is used. There are severe tradeoffs among self-resonance frequency, linearity, noise, power dissipation and layout area.

2.2.3 The Active-Inductor Equivalent Circuit

Equation (2.5) can be further transformed into

$$Z_{in} = \frac{\frac{1}{C_p}\left(s + \frac{r_s}{L_{eq}}\right)}{s^2 + s\left(\frac{r_s}{L_{eq}} + \frac{g_p}{C_1}\right) + \frac{1+g_p r_s}{L_{eq}C_p}} = \frac{\frac{1}{C_p}\left(s + \omega_z\right)}{s^2 + s\frac{\omega_R}{Q_R} + \omega_R^2} \tag{2.7}$$

which is a lowpass function with possibly high peaking when Q_R is very high. The parameters are

$$\begin{aligned} &\omega_z = \frac{r_s}{L_{eq}},\ \omega_R = \sqrt{\frac{1+g_p r_s}{L_{eq}C_p}} \approx \frac{1}{\sqrt{L_{eq}C_p}}, \\ &Q_0 = \frac{\sqrt{\frac{1+g_p r_s}{L_{eq}C_1}}}{\frac{r_s}{L_{eq}} + \frac{g_p}{C_p}} \approx \frac{\sqrt{L_{eq}C_p}}{r_s C_p + g_p L_{eq}} = \frac{R_p\sqrt{\frac{C_p}{L_{eq}}}}{1 + \frac{r_s C_p}{L_{eq} g_p}} = R_p\sqrt{\frac{C_p}{L_{eq}}} \propto R_p, \quad \text{when } r_s = 0 \end{aligned} \tag{2.8}$$

The quality factor of the resonator, Q_R, which is proportional to the shunt resistor R_p, is also the quality factor of the 2nd-order denominator, and it is equal to ω_R divided

by the –3-dB bandwidth of the resulting bandpass filter [10]

$$Q_{\mathrm{R}} = \frac{\omega_{\mathrm{R}}}{BW_{-3\ \mathrm{dB}}} \tag{2.9}$$

The expression is exact only when $\omega_{\mathrm{z}} = 0$, that is, the effect of r_{s} is ignored.

It shall be noted that Q_{R} is different from the inductor Q, which is a function of frequency and is defined as

$$Q_{\mathrm{L}}(\omega) = \frac{\mathrm{Im}(Z_{\mathrm{in}})}{\mathrm{Re}(Z_{\mathrm{in}})} = \frac{\omega L_{\mathrm{eq}}}{r_{\mathrm{s}}} \frac{1 - \frac{\omega_{\mathrm{z}}^2}{\omega_{\mathrm{R}}^2} - \frac{\omega^2}{\omega_{\mathrm{R}}^2}}{1 + g_{\mathrm{p}} r_{\mathrm{s}} + \frac{\omega^2}{\omega_{\mathrm{R}}^2} \frac{g_{\mathrm{p}}}{C_{\mathrm{p}}} \frac{1}{\omega_{\mathrm{z}}}} \approx \frac{\omega L_{\mathrm{eq}}}{r_{\mathrm{s}}}, \tag{2.10}$$

when $\omega_{\mathrm{z}} << \omega_{\mathrm{R}}$, $\omega << \omega_{\mathrm{R}}$, $r_{\mathrm{s}} << R_{\mathrm{p}}$, and $g_{\mathrm{p}}/C_{\mathrm{p}} << \omega_{\mathrm{z}}$.

It should also be noted that

$$Q_{\mathrm{L}}(\omega_{\mathrm{R}}) = \frac{\omega L_{\mathrm{eq}}}{r_{\mathrm{s}}} \frac{-\frac{\omega_{\mathrm{z}}^2}{\omega_{\mathrm{R}}^2}}{1 + g_{\mathrm{p}} r_{\mathrm{s}} + \frac{g_{\mathrm{p}}}{C_{\mathrm{p}}} \frac{1}{\omega_{\mathrm{z}}}}\Bigg|_{g_{\mathrm{p}}=0} = -\frac{r_{\mathrm{s}}}{\omega_{\mathrm{R}} L_{\mathrm{eq}}} \neq Q_{\mathrm{R}} \tag{2.11}$$

Q_{R} is mainly determined by R_{p}, when r_{s} is relatively small; and Q_{L} is primarily determined by r_{s}. To increase Q_{L}, r_{s} should be decreased, and this requires the reduction of load leakage g_{L} per Eq. (2.6). Applying Eq. (2.6) on Eq. (2.8), the expression for Q_{R} becomes

$$Q_{\mathrm{R}} = \frac{\sqrt{G_{\mathrm{M1}} G_{\mathrm{M2}} C_{\mathrm{L}} C_{\mathrm{1}}}}{g_{\mathrm{L}} C_{\mathrm{1}} + g_{\mathrm{1}} C_{\mathrm{L}}} = \frac{\sqrt{G_{\mathrm{M1}} G_{\mathrm{M2}} C_{\mathrm{L}} C_{\mathrm{p}}}}{g_{\mathrm{L}} C_{\mathrm{p}} + g_{\mathrm{p}} C_{\mathrm{L}}} \tag{2.12}$$

When the highest operating frequency is desired and the capacitors are all parasitic capacitors, we have $g_{\mathrm{L}} \approx g_{\mathrm{1}}$ and $C_{\mathrm{1}} \approx C_{\mathrm{L}}$, since they have similar origins. Thus g_{1} and g_{L} have similar contributions to Q_{R}, and increasing Q_{R} becomes a collective effort of reducing both g_{1} and g_{L}, or some other measures may be used.

As we shall see later, g_1 and g_L are not limited to the summation of transistor g_{ds}s; they can be equal to or greater than the values of the two primary transconductors G_{M1} and G_{M2} depending on the particular active-inductor circuit architecture. When g_1 is large, R_p and in turn Q_R will be low, and the inductor is not suitable for designing high-Q bandpass filters. When g_L is large, r_s will be large, and the inductor cannot be used as a good inductor. Per Eq. (2.12), a large g_L will yield a low Q_R, so it cannot be used as a high-Q resonator either.

It should be noted that in many publications, when compensating for the circuit loss to obtain a high Q, it is not stated which loss resistor is targeted: r_s or R_p, even though the compensation methods for them are usually very different. As a rule of thumb, active inductors used in digital (pulse) circuits, such as the input amplifier of fiber optic receivers or to implement wide-band amplifiers, are concerned primarily with r_s; while active inductors used in bandpass and high-order lowpass filters are mainly concerned with R_p. Obtaining high-Q_R circuit to implement narrow-band bandpass filters is one of the targets of this work.

The simulation results of an example are given in Fig. 2-5. Below f_z = 32 MHz, Z_{in} = 10 Ω is a resistor; between f_z and f_0 = 2.25 GHz, Z_{in} is equivalent to a 50 nH inductor, as its magnitude is proportional to ω; above f_0, Z_{in} is equivalent to a 100 fF capacitor, as its magnitude is inversely proportional to ω. The Q_L, defined by $\mathrm{Im}(Z_{in})/\mathrm{Re}(Z_{in})$, is negative when the admittance from C_p is greater than that from L_{eq}. Low-frequency Q is determined by r_s, and high-frequency Q, in particular that at f_R, is determined by R_p. Beyond f_R, the circuit is not of practical use, because it behaves as a

capacitor, but is more complex and consumes power in the case of an active inductor.

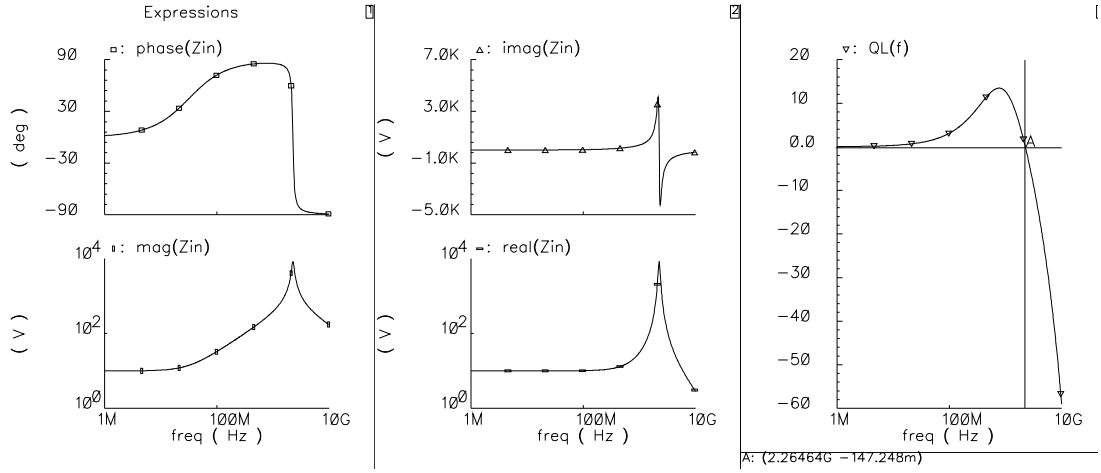


Figure 2-5 Simulation plots of the circuit in Fig. 2-4 with $R_p = 1/g_p = 10$ kΩ, $C_p = 100$ fF, $L_{eq} = 50$ nH, $r_s = 10$ Ω.

2.3 Technology Constraints

A semiconductor fabrication process is a collection of steps (masking, doping, etc.) and technical specifications (topological, electrical, chemical, etc.) that define a production, and consequently, a consortium of devices and interconnects of unique characteristics. Many companies have their own processes, with many more derivations to address different needs in different products, such as high-speed (e.g., data transceivers), low-power (e.g., microprocessors), high-frequency (e.g., RF and microwave ICs), high-density (e.g., memories). As a result, there are probably thousands of processes in the world. However, when categorized by their key masking steps and primary device (transistor) structures, the plethora of processes is reduced to a handful "technologies," with different characteristics.

Bipolar technology was the first technology to be used in the mass production of ICs. Its primary devices are NPN and PNP transistors, with resistors and capacitors

available using extra steps. Bipolar is stable, mature, moderately fast, with good device properties for both digital and analog circuits. Its primary disadvantage is cost, because of its relatively low integration density and extra fabrication steps compared with CMOS (complementary metal oxide semiconductor). Therefore, its product share has been on constant decline over the last few decades, thought its absolute volume has probably been increasing, considering the exponential increase in semiconductor manufacturing. Bipolar Junction Transistors (BJTs) are necessary for implementing bandgap reference and other circuits, and hence are preserved on many CMOS processes. The base current of bipolar transistors is not zero, and this limits their use in memory and other low-power circuits.

CMOS technology is currently the mainstream of the semiconductor industry, mainly because of its low cost. It is the ideal technology for digital circuits: high integration density, nearly zero gate dc currents, and low leakage in the off state. Unfortunately, compared with bipolar technology, it is not the ideal technology for analog circuits because of its higher level of noise and nonlinearity, difficulty of accurate modeling, high threshold voltage (V_{TH}) mismatch, and some functional circuits, such as the bandgap reference, must use bipolar transistors. The long-channel ($L \geq 1$ μm) devices are well modeled by the square-law *I-V* characteristic, which can be used to build analog circuits with good linearity. However, short-channel devices deviate from the square-law significantly because of second-order effects, such as velocity saturation from the horizontal field and mobility degradation from the vertical field, and cannot be modeled accurately across the entire hyperspace of process corners, temperature, biasing voltages and currents, as well as device width and

length. Intermediate-frequency (< ~10 MHz) analog circuit design can dodge this problem by using long-channel devices in deep-submicron CMOS technologies; however, analog circuits operating above 1 GHz, as in this work, have to use minimum or near-minimum device length to reach the required frequency. Consequently, analog CMOS circuits operating above 1 GHz have poor linearity, high noise level and wide performance variation.

Despite the drawbacks, a very sizeable portion of analog designs nowadays are done in CMOS and they have to reside in a hostile environment with devices optimized for digital signals and a high level of interference from digital circuitry being coupled over via the substrate and power supply. The reason is that on most ICs today, the area of digital circuits dominates the die area and determines the IC cost, so the technology selection is mainly based on the requirements of digital circuitry.

The primary devices in CMOS are NFETs and PFETs. Poly/N-Well resistors, metal-insulator-metal (MiM)/poly capacitors, MOS varactors, and passive inductors are available in some processes using extra masking steps. Most standard digital CMOS processes use an epitaxial substrate to reduce its resistivity ρ and in turn the likelihood of latchup, and the only available devices are FETs. An example is the Taiwan Semiconductor Manufacturing Corp (TSMC)'s LOG018 process. Some CMOS processes are modified to accommodate the needs of analog and RF circuits, using non-epitaxial substrate to reduce RF substrate noise coupling; they are called "mixed-signal" process, such as TSMC's MM018 process, to the disadvantage of digital circuitry and at a cost premium. The MM018 process features a thick top metal for spiral inductors, capacitors and poly resistors.

To compensate for the lack of BJTs, some CMOS processes are modified to provide substrate PNPs and/or triple-well NPNs along with FETs; they are referred to as BiCMOS technology. Compared with a pure bipolar technology, the performance of the BJTs is poorer; however, it is still better than MOSFETs for many analog designs. BiCMOS is on the decline and is being replaced by pure CMOS technology in many cases, where analog designs have to be accomplished using MOSFETs only.

Silicon-germanium (SiGe) BiCMOS is an expensive technology, but has seen an increase over the last decade, primarily due to the demand from the mobile phone industry. It combines high-performance heterojunction bipolar transistors (HBTs) with state-of-the-art CMOS technology. A SiGe base with a graded germanium doping profile is sandwiched between the Si collector and Si emitter of the HBT. A built-in electric field is created by making the Ge doping level higher toward the collector, and it accelerates electrons as they travel from the emitter to the collector across the base [11]. Therefore, the transition time of electrons is decreased and the HBTs can operate at a higher frequency than regular BJTs. Together with the availability of passive inductors and capacitors, the technology is suitable for high-performance RF ICs. The available MOSFETs make it possible to implement a small amount of digital circuitry on the same die with moderate costs.

Finally there is the Gallium-Arsenide (GaAs) technology that is primarily used for microwave ICs, though it is also used for very-high-speed digital circuits. By using the GaAs compound instead of silicon as substrate, a higher energy bandgap (1.4 V) and electron mobility (~6x) are obtained compared with silicon, giving it the potential for high-temperature and very-high-speed applications [12]. The transistors in GaAs

technology are metal-semiconductor field-effect-transistors (MESFETs). Instead of the silicon-oxide insulated gate in CMOS, METFET's gate is a Schottky diode whose depletion layer extends into the substrate at reverse biasing and pinch the conduction channel between source and drain. Similar to mixed-signal CMOS and BiCMOS, GaAs technology typically provides passive inductors and capacitors. Due to the high-resistivity of the GaAs substrate, the passive inductors have higher *Q*s than those on CMOS, and microwave structures, such as transmission lines, can be implemented on-chip. These properties make GaAs more popular with RFICs designed with microwave methods.

To eliminate the need for more expensive technologies, this work is done using TSMC's LOG018 standard digital CMOS process. This will also make it possible to integrate RF active inductors directly with standard digital circuits without modifying the fabrication process. However, TSMC's LOG018 process, like most other modern standard digital CMOS processes, comes with a few severe constraints:

1. Only PFETs and NFETs are available, with relatively high threshold voltages that are engineered for digital circuitry to reduce power dissipation and leakage, but limit analog circuit topologies for a given power supply voltage V_{DD}. This precludes the use of many proven linearization methods.
2. Poly capacitors are not available, so ac signal coupling is not possible, as done in many active inductors designed using microwave theory and in GaAs technologies. This requires that the circuit topologies are appropriate for both ac and dc, and restricts design possibilities.

3. Interconnect capacitances are not accurately modeled since the primary application is digital circuits. Due to the high operating frequency, interconnect capacitance is a non-negligible part of circuit design, hence the fabricated circuits may be off the design target or may not function at all.
4. There is no specification on the maximum applicable frequency of the vendor device models. It is estimated to be below 1 GHz. The device modeling is not done using RF methods, which include gate and substrate resistance as well as other parasitic elements that are typically ignored in modeling for analog and digital circuits. The resulting circuit may act differently as simulated.

This work is to obtain operating circuits among the challenges.

2.4 Literature Survey of Active Inductors

In this section, transistor-level active inductors proposed by researchers over the years are reviewed. To expose their fundamental structure, biasing circuits and capacitor ac coupling (popular with microwave ICs, almost never in CMOS ICs) are not shown, but are pointed out when necessary. As we shall see below, all active inductors can be explained by a three-step operation:

1. Converting the port voltage V_{in} into an in-phase (0°) current, more efficiently done by a transconductor, G_m, and less efficiently by a resistor;
2. Applying this current on a capacitor and obtaining a voltage V_{CL} that is –90°;
3. Converting V_{CL} into the input current I_{in}, almost always through a G_m.

The reference directions have to be correct to yield a positive-value inductor with non-negative losses.

Of course, an active inductor can be more complicated than this, e.g., involving more conversions between V_{in} and I_{in} or more parasitic poles in the conversions, but the circuit will be less efficient, and the advantages gained, such as linearity, are rarely worth the degradations in other aspects for GHz designs.

2.4.1 Gate-*R* and Gate-*R*-II Active Inductors

The simplest active inductor is formed by placing a resistor at the gate of a MOSFET or the base of an NPN BJT, as shown in Fig. 2-6 (a) and (c). The circuit is usually called "active inductor" in the literature without a more specific name. For ease of discussion, we name it "gate-*R*," based on its structure.

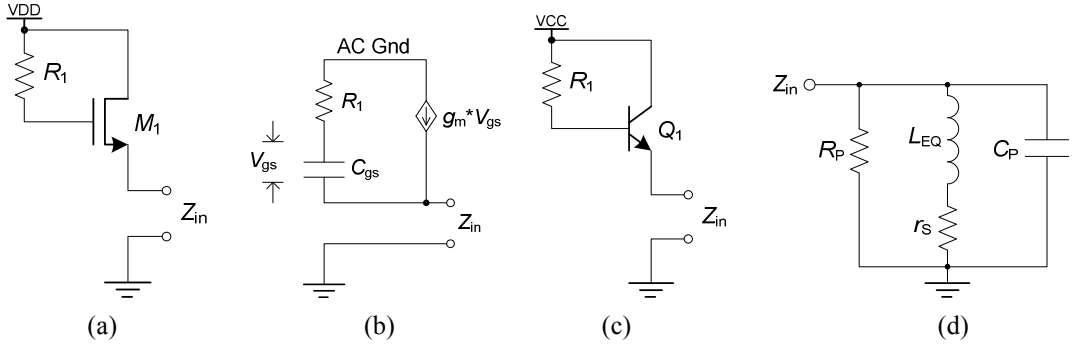


Figure 2-6 (a) CMOS gate-*R* active inductor. (b) Small-signal ac equivalent circuit. (c) Bipolar version of the same circuit. (d) Equivalent circuit showing the inductor.

If R_1 is large compared with $|1/(j\omega C_{gs})|$, the ac voltage v_{gs} can be assumed to be zero, and R_1 will convert V_{in} into an in-phase current which is applied to the gate-source capacitor of M_1, C_{gs}, the first step of inductor formation. For a MOSFET, using a small-signal equivalent circuit and ignoring parasitic components, the voltage across C_{gs} is

$$V_{gs} = V_{in}\frac{1/(sC_{gs})}{R_1 + 1/(sC_{gs})} = V_{in}\frac{1}{sR_1C_{gs}+1} \approx V_{in}\frac{1}{sR_1C_{gs}}\bigg|_{when\ |s|>>\frac{1}{R_1C_{gs}}} \tag{2.13}$$

If R_1 is large, we have $I_{in} \approx -I_{ds1}$. At relatively high frequencies, V_{gs}, and in turn, I_{in}, is going to *lag* V_{in} by 90°, and that is the property of an inductor. It can be easily verified that the reference directions of V_{in} and I_{in} are both correct.

If we remove the high-frequency condition and use small-signal analysis, the input impedance can be calculated as

$$\begin{aligned} Y_{in} &= \frac{g_m + sC_{gs}}{1+sR_1C_{gs}} = \frac{g_mG_1 + sC_{gs}G_1}{G_1 + sC_{gs}} = \frac{1}{R_1} + \frac{g_mG_1 - G_1^2}{G_1 + sC_{gs}} \approx \frac{1}{R_1} + \frac{g_mG_1}{G_1 + sC_{gs}}\bigg|_{G_1<<1} \\ &= \frac{1}{R_1} + \frac{1}{\frac{1}{g_m} + \frac{sC_{gs}R_1}{g_m}} = \frac{1}{R_p} + \frac{1}{r_s + sL_{eq}} \end{aligned} \tag{2.14}$$

where g_m is the transconductance of M_1 and $G_1 = 1/R_1$. The circuit is equivalent to the one in Fig. 2-6(d), and the small-signal equivalent elements are

$$R_p = R_1,\ r_s = \frac{1}{g_m},\ L_{eq} = \frac{R_1C_{gs}}{g_m} \tag{2.15}$$

Due to the parasitic capacitors, there inevitably is an equivalent shunt capacitor C_p, which includes C_{js} of M_1. The inductor Q is

$$Q_L(\omega) = \frac{|j\omega L_{eq}|}{r_s} = \omega R_1C_{gs} \tag{2.16}$$

and the resonance Q, Q_R, is jointly determined by C_p, R_p and L_{eq}.

Comparing this active inductor to the gyrator (Fig. 2-3), the 90° phase shift from V_{in} to V_{cap} is obtained through a resistor, instead of a transconductor, and this conversion is not close to ideal (Eq. 2.13). This contributes to its very low Q_R.

This active inductor exists at the output of a source or emitter follower, causing undesirable signal peaking. However, it has been widely used in the Trans-Impedance Amplifier (TIA) and limiting amplifier of fiber optic receivers in the last two decades [13-15], for "shunt peaking" [16, 17], that is, improving the sharpness of pulse signal edges by partially "canceling out" the load capacitance. In fact, any wide-band pulse-signal processing circuits, such as amplifiers and mixers, can benefit from it for the added bandwidth. It is also used in oscillators [18-20], even though due to its very low Q_R (around 2) [19], the negative resistor has to be very large to make the oscillator work and hence consumes a high current.

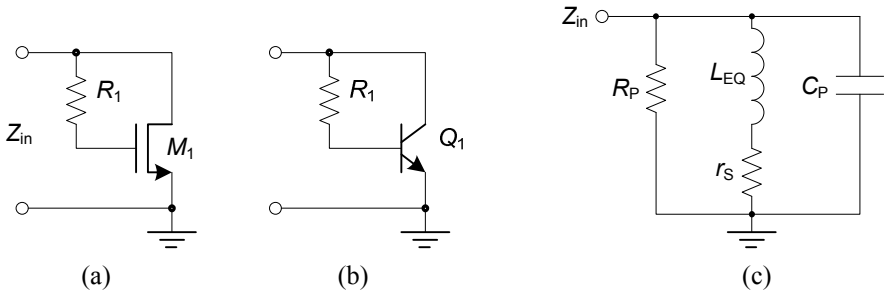


Figure 2-7 Gate-*R*-II active inductors and their small-signal equivalent circuit.

A slight connection variation in gate-*R* active inductor results in another active inductor, as shown in Fig. 2-7, and is named "gate-*R*-II". For the MOSFET version, ignoring parasitic components and using the small-signal equivalent circuit, Z_{in} is calculated as

$$Y_{in} = \frac{sC_{gs} + g_m}{1 + sR_1C_{gs}} = \frac{1}{R_1} + \frac{1}{\frac{1}{g_m - \frac{1}{R_1}} + s\frac{R_1C_{gs}}{g_m - \frac{1}{R_1}}} \approx \frac{1}{R_1} + \frac{1}{\frac{1}{g_m} + s\frac{R_1C_{gs}}{g_m}}\Bigg|_{when\ g_m >> 1/R_1} \tag{2.17}$$

$$= \frac{1}{R_p} + \frac{1}{r_s + sL_{eq}}$$

where C_{gs} and g_m are the gate-source capacitance and transconductance of M_1, respectively, and the equivalent elements are

$$R_p = R_1,\ r_s = \frac{1}{g_m},\ L_{eq} = \frac{R_1 C_{gs}}{g_m} \tag{2.18}$$

$Q_L(\omega)$ and Q_R have the same expression as that of the gate-R active inductor.

Interestingly, the gate-R-II and gate-R active inductors have identical input impedances. Nonetheless, M_1 in gate-R-II circuit is not subject to the body effect, which increases V_{th} and affects the effective g_m of the transistor. The dc voltages at the input terminal of the two circuits are also different, one $V_{gs,n}$ down from V_{DD} and one $V_{gs,n}$ up from ground, respectively, and may fit different applications. Similar to the gate-*R* active inductor, the gate-*R*-II also has very low Q_R, which may or may not be an issue depending on the application.

The Gate-*R*-II circuit also found its most popular use in limiting amplifiers for optical receivers [21, 22]. It has also been used in LNA design [23], in which BJTs were used to reduce the noise level.

In some works [14, 19, 21, 22], instead of a poly or diffusion resistor, the *R* is implemented by a MOSFET operating in the linear region, as shown in Fig. 2-8.

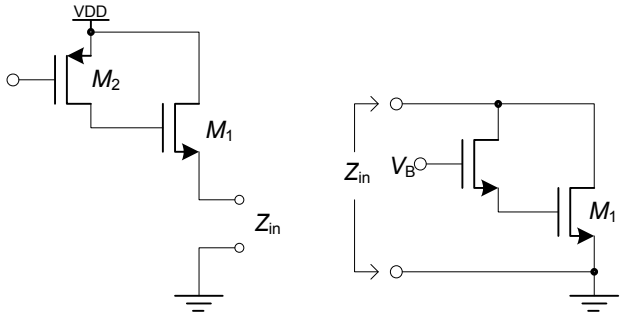
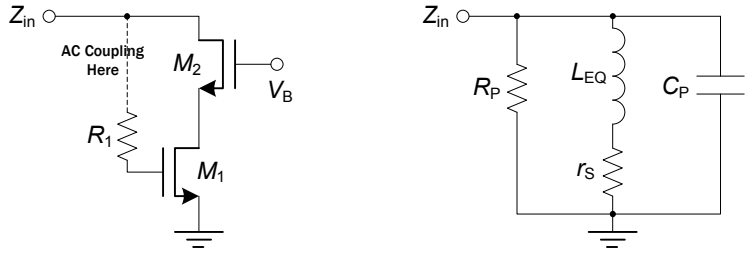


Figure 2-8 Gate-*R* (a) and Gate-*R*-II (b) active inductors using a linear-region FET as gate resistor.

2.4.2 Cascode Gate-*R* Active Inductors

Real transistors have limited R_{out}, or non-zero g_{ds} in the case of CMOS, and it is in parallel with R_P in gate-*R* and gate-*R*-II circuits, reducing Q_R and Q_L. In an effort to increase R_{out} and improve Q, cascode is introduced to M_1 in Fig. 2-7, resulting in the cascode gate-*R*-II circuit in Fig. 2-9(a).



(a) (b)

Figure 2-9 Cascode gate-*R*-II active inductor (Shinji Hara, 1988). (a) Primary circuit with ac coupling shown; (b) Equivalent circuit showing the inductor.

The circuit was proposed by Shinji Hara et al. in 1988 using an off-chip resistor [24, 25] and has seen many variations over the years, mostly in microwave circuits. Small-signal analysis yields [24, 25]

$$L_{eq} = \frac{R_1 C_{gs}}{g_m},\ r_s = \frac{1}{g_m},\ C_P \approx \left(\frac{\omega C_{gs}}{g_m}\right)^2 C_{gs} \tag{2.19}$$

The improvement in Q_L is paltry, because r_s does not change. Q_R, which is determined mainly by R_P, can be improved, however, not due to the improvement of transistor R_{out} from the use of cascode, as believed by many researchers, but from the C_{gs} of the cascode FET M_2 [26, 27]. The C_{gs} of M_2 introduces a parasitic pole to the circuit at its source, and this generates a phase lag in the gyrator loop. As we shall examine more closely in Section 2.5.3, a phase lag within the gyrator loop has the effect of improving Q_R, and can even render the circuit unstable.

Other efforts in compensating the loss and improving Q include replacing the R on the gate with another gate-R active inductor (recursive topology) [28-30], as shown in Fig. 2-10.

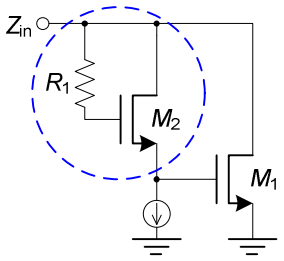


Figure 2-10 Recursive Gate-R-II active inductor.

The cascode gate-R active inductors were used in optical receivers for wide-band pulse amplification [31], but also found use in RF filters [32-35] due to their potential for higher Q_R, through the use of cascode and, more commonly, additional loss-compensating circuitry.

2.4.3 CG-CS Active Inductors

As mentioned, many gate-R active inductors are implemented by replacing the gate resistor with a linear-region MOSFET [14, 19, 21, 22], especially in optical receivers, where the prevalent technology is CMOS and usually does not allow resistors and large-value capacitors (for ac coupling) on chip. Another active inductor can be obtained by making the same gate-FET operating in the forward-active region in common-gate (CG) mode, as shown by Fig. 2-11, with a structure similar to that of the cascode gate-R-II circuit. Note that if only signal-path transistors are shown, it is not possible to tell whether the gate-FET M_2 is acting as a resistor or a CG transistor, and unfortunately, some papers do not include this information directly. One way to tell

the operating region of the gate-FET is to observe the biasing. If there is a biasing current source connecting to the M_1 gate, M_2 is likely to be operating in CG mode; otherwise it has to be a resistor, because it has no dc biasing current path.

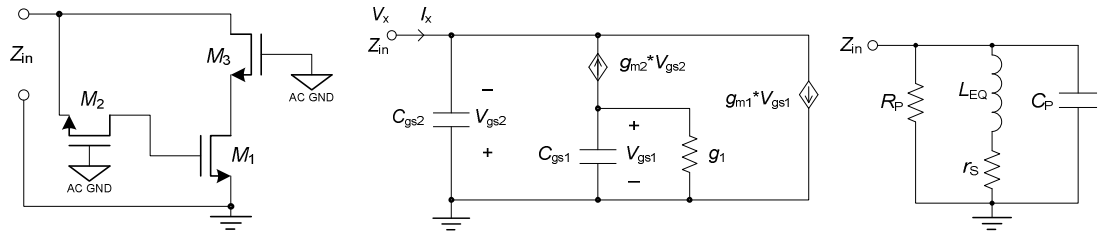


Figure 2-11 (a) CG-CS active inductor (Shinji Hara, 1989). (b) Small-signal ac circuit. g_1 is mainly from the g_{ds} of the biasing transistor (not shown) for M_2. (c) Equivalent circuit.

Shinji Hara et al. began their active inductor research [24, 25] with the gate-*R* circuit and then replaced the external resistor with a common-gate MOSFET M_2 [36], as shown in Fig. 2-11. This circuit is named "CG-CS" active inductor because the two transistors along the signal path operate in common-gate (M_2) and common-source (M_1), respectively. The original motive was to eliminate the off-chip resistor in the gate-*R* cirucit and fully integrate it; however, this circuit is very remotely related to the gate-*R* active inductor.

M_2 is a noninverting G_M between V_{in} and C_{gs1}, and $M_{1,3}$ forms an inverting G_M from C_{gs1} back to V_{in}. Note that M_3 is optional and its main function is to increase the resistance looking into the M_1 drain. Using the small-signal ac equivalent circuit in Fig. 2-11(b), the circuit input impedance is calculated as

$$Y_{in} = g_{m2} + sC_{gs2} + \frac{g_{m1}g_{m2}}{sC_{gs1} + g_1} = g_{m2} + sC_{gs2} + \frac{1}{s\dfrac{C_{gs1}}{g_{m1}g_{m2}} + \dfrac{g_1}{g_{m1}g_{m2}}} \tag{2.20}$$

which can be represented by the equivalent circuit in Fig. 2-11(c), with elements being

$$R_{\mathrm{p}} = \frac{1}{g_{\mathrm{m2}}},\ C_{\mathrm{p}} = C_{\mathrm{gs2}},\ L_{\mathrm{eq}} = \frac{C_{\mathrm{gs2}}}{g_{\mathrm{m1}} g_{\mathrm{m2}}},\ r_{\mathrm{s}} = \frac{g_1}{g_{\mathrm{m1}} g_{\mathrm{m2}}} \tag{2.21}$$

The quality factors are

$$Q_{\mathrm{R}} = R_{\mathrm{p}} \sqrt{\frac{C_{\mathrm{p}}}{L_{\mathrm{eq}}}} = \sqrt{\frac{g_{\mathrm{m1}}}{g_{\mathrm{m2}}}},\ Q_{\mathrm{L}}(\omega) = \frac{\omega L_{\mathrm{eq}}}{r_{\mathrm{s}}} = \frac{\omega C_{\mathrm{gs2}}}{g_1} \tag{2.22}$$

The circuit is a very-low-Q_{R} (≈ 1 if $g_{\mathrm{m1}} \approx g_{\mathrm{m2}}$) active inductor due to $R_{\mathrm{p}} = 1/g_{\mathrm{m2}}$. Another way to look at this is that the source of M_2 is connected to the inductor port and the resistance looking into the M_2 source is $1/g_{\mathrm{m2}}$, a small number compared with other equivalent elements. Therefore, the claim of "lossless" for this circuit [36] is not quite true, as confirmed by the low Q_{R} of about 2 at 3 GHz [36].

On the other hand, if g_1 is sufficiently low, r_{s} can be low, too. And Q_{L} is larger than that of the gate-R and its derivatives, because g_1 generally is much lower than $1/R_1$ in the gate-R circuits. So this circuit could implement an inductor with low series resistance r_{s}. However, there is no easy way of improving Q_{L} besides reducing g_1.

The circuit's main drawback is that for the MMIC implementation proposed by the authors, multiple resistors and capacitors are needed to bias the transistors and complete the signal path, increasing parasitic components and making the circuit expensive.

Six months later, the authors reported the results of the same active inductor, with a cascode NMOS inserted to the drain of M2 in Fig. 2-11(a) in an effort to overcome g_{ds}-limitations and increase Q_{L} [37, 38]. This over-compensated the circuit loss (mainly because of the extra phase shift from the parasitic poles of the two G_{M}s that are now both cascoded, see Section 2.5.3) and yielded a negative resistor element

in the equivalent circuit. The authors then put a resistor in shunt with the input port to cancel out the negative resistor and obtained a Q_R as high as 65 at 8 GHz [37, 38]. This method of over-compensating the loss and then introducing another loss element is inefficient in terms of reducing circuit noise and power dissipation.

In 1996, H. Hayashi el al. introduced a similar scheme [26, 27] that over-compensates the circuit loss through the parasitic pole of the cascode transistor M_3, and then added a series, instead of shunt, resistor to the circuit to compensate the negative equivalent resistor and obtain a high Q_L. W. Li et al. proposed a similar method of improving Q [39], using instead an R-C network on the gate of the cascode FET M_3, and demonstrated a simulated Q near 8000, which is of little significance in practical applications due to the ultra-high circuit sensitivities, which are proportional to Q.

2.4.4 Cascode CG-CS Active Inductors

One way of implementing the CG-CS active inductor is shown in Fig. 2-12(a), including the biasing circuit, with M_1 and M_2 configured as CG and CS, respectively. Since I_2 and I_3 are connected to the same node, I_3 can be omitted. Then if $I_{DS1} = I_{DS2}$, I_2 can also be omitted. The result is the Cascode CG-CS active inductor. This concept was proposed by Yang et al. using BJTs in 1997 [40] (Fig. 2-12(b)), and then by Wu and Ismail in CMOS technology [41-45] (Fig. 2-12(c)). The equivalent circuit is shown in Fig. 2-12(d).

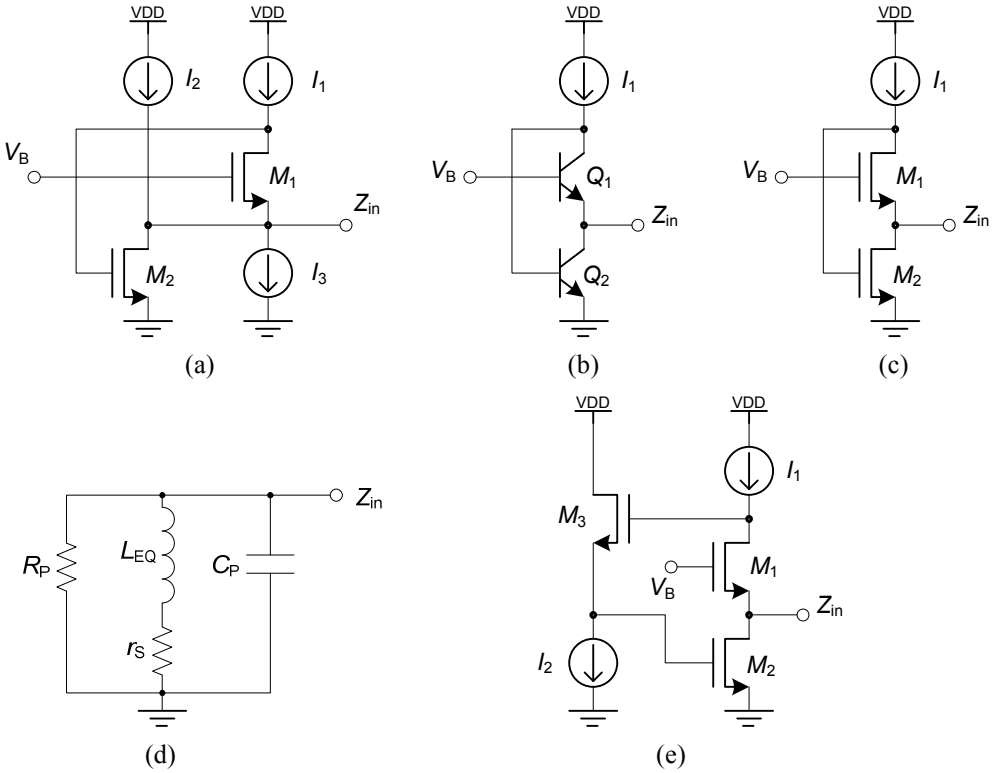


Figure 2-12 Derivation of the cascode CG-CS active inductor. (a) Circuit derived from signal flow. (b) BJT version. (c) CMOS version. (d) Equivalent circuit. (e) Modified cascode CG-CS.

Aside from a low Q_R that is determined by its CG-CS structure, the circuit's main limitation is the dc biasing. In the CMOS case, we have $V_{GS2} = V_{T,n} + V_{OD} = V_{DS1} + V_{DS2}$. Typically $V_{T,n} \approx 0.4$-0.6 V, and V_{DS} has to be greater than $V_{OD} + 100$ mV ≈ 0.3 V, hence the V_{DS} margins are very limited since V_{GS2} is not large, and the circuit may not work across process and temperature corners. A voltage level shifter, which adds parasitic poles and noise, is often used on this circuit to make $V_{DS1} + V_{DS2} = V_{GS2} + \Delta V$. A voltage level shifter implemented by a source follower is shown in Figure 2-12(e) [46]. Wu and Ismail instead inject extra current to M_2 through a second current source I_2 to greatly increase V_{OD2} and in turn V_{GS2}, without increasing V_{OD1} and in turn the requirement on V_{DS1} (Fig. 2-13). Part of I_2 is the "recycled" current used by the negative resistor (cross-connected differential pair) for Q_R improvement [45]. I_2

cannot be totally derived from the negative resistor, in order to obtain separate tuning for Q_R and L_{eq} (frequency).

The active inductor's signal swing is limited by the low V_{DS} of the FETs. A simple analysis will reveal that similar problem exists in the bipolar case without the use of a level shifter.

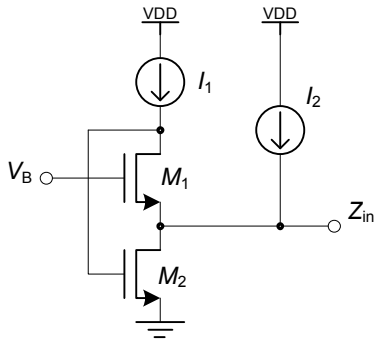
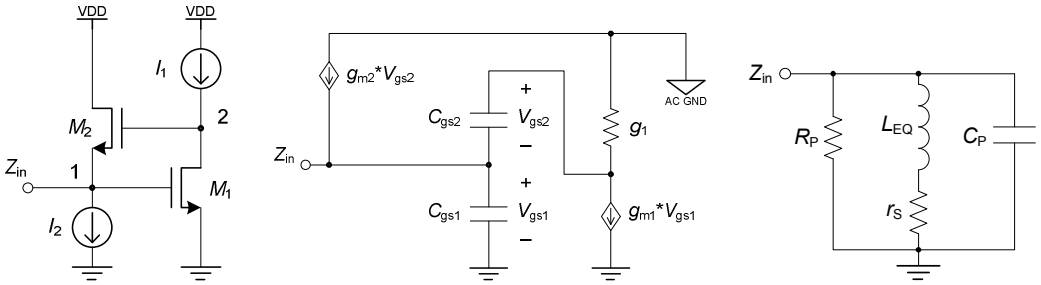


Figure 2-13 Wu and Ismail's solution to dc biasing difficulty: injecting extra current I_2 into M_2 to raise V_{GS2} without increasing V_{GS1}, which will increase the V_{DS1} requirement and defeat the margin gained through the increase in V_{GS2}.

2.4.5 CS-CD Active Inductor and Q Enhancement using R_f

The Common-source common-drain (CS-CD) active inductor [47] is shown in Fig. 2-14(a). It is fundamental to a popular class of active inductors called "cascode" and "regulated cascode" active inductors. Along the signal path, M_1 and M_2 are in CS and CD configuration, respectively, hence its name. It can be roughly explained using the gyrator principle, with M_1 being the inverting G_M and M_2 being the noninverting G_M, though the load capacitor C_{gs2} is connected across the two nodes of gyrator instead of grounded.



(a) (b) (c)

Figure 2-14 Common-Source Common-Drain (CS-CD) active inductor. (a) The circuit. (b) Small-signal ac equivalent circuit. g_1 is $g_{ds1} + g_{ds,I_1}$. (c) Equivalent circuit showing the inductor.

Small-signal ac analysis reveals that its input impedance is

$$\begin{aligned} Y_{in} &= sC_{gs1} + \frac{(g_{m1}+g_1)(g_{m2}+sC_{gs2})}{g_1+sC_{gs2}} \approx sC_{gs1} + \frac{g_{m1}(g_{m2}+sC_{gs2})}{g_1+sC_{gs2}} \\ &= sC_{gs1} + g_{m1} + \frac{g_{m1}g_{m2}-g_{m1}g_1}{g_1+sC_{gs2}} \approx sC_{gs1} + g_{m1} + \frac{g_{m1}g_{m2}}{g_1+sC_{gs2}} \\ &= sC_{gs1} + g_{m1} + \frac{1}{\frac{g_1}{g_{m1}g_{m2}} + s\frac{C_{gs2}}{g_{m1}g_{m2}}} \end{aligned} \tag{2.23}$$

which can be represented by the equivalent circuit shown in Fig. 2-14(c). The equivalent elements are

$$R_p = \frac{1}{g_{m1}},\ C_p = C_{gs1},\ L_{eq} = \frac{C_{gs2}}{g_{m1}g_{m2}},\ r_s = \frac{g_1}{g_{m1}g_{m2}} \tag{2.24}$$

If g_1 is low, r_s can be very low; however, $R_p = 1/g_{m1}$ is a low shunt resistance, and consequently, the CS-CD active inductor has an average Q_L but very low Q_R. Nonetheless, this circuit is readily biased, with a low V_{DD} requirement and a decent maximum signal swing.

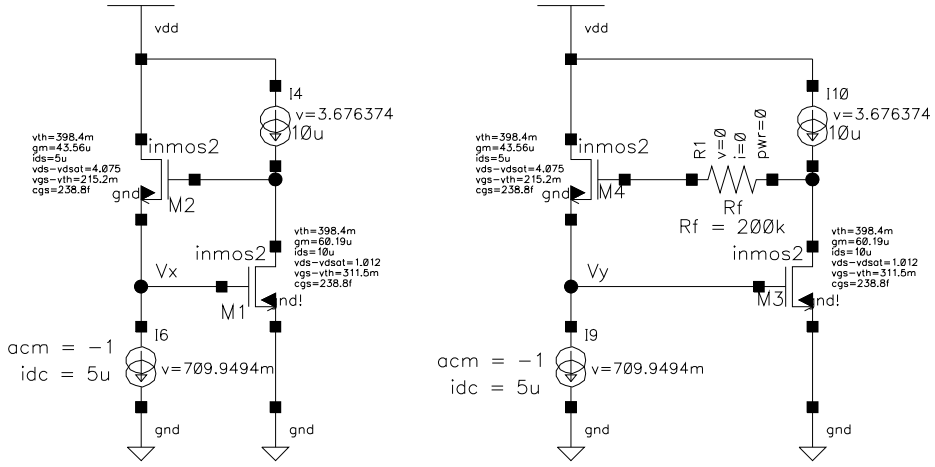
It can be shown that the CS-CD circuit exhibits a low-Q lowpass filter characteristic from Node 1 to Node 2 in Fig. 2-14(a). The input impedance is low (= $1/g_{m1}$) and can be 50 Ω when properly designed. These two characteristics make CS-

CD as well as its derivatives, cascode and regulated cascode active inductors, suitable for the low-noise amplifiers (LNAs) in broadband wireless communications [47-50], even though the "low-noise" designation is not entirely true, if compared with LNAs designed with passive inductors. The transfer function is a broadband lowpass; in contrast LNAs using passive inductors are always narrow-band bandpass. The broadband property also allows more noise at different frequencies pass through, so it should be used judiciously.

A common method of enhancing the low Q_R is to insert a resistor R_f in the signal loop [51-53], as shown in Fig. 2-15(b). We can include R_f in the equivalent circuit in Fig. 2-14(b) and reveal its effect through circuit analysis; however, a quicker way to understand the function is to recognize that R_f, together with C_{gs2}, creates a phase lag in V_{gs2} and in turn in I_{d2}. As we shall see later in Section 2.5.3, a phase lag in the gyrator loop has the effect of increasing Q_R. However, there are two issues associated with this:

(1) Not all processes have large-value resistors available.

(2) Since C_{gs2} is very small, to create an appreciable phase lag (~5-15°), a resistor on the order of a few hundred kΩ may be needed, and this means a large layout area. In reality, however, the required value of R_f is usually a little lower, because the poly resistors have distributed R and C, and create extra phase lag.



(a) (b)

Figure 2-15 (a) A CS-CD active inductor simulation circuit. g_{ds1} = 0.597 pS. (b) With a Q-enhancing resistor R_f.

The circuits in Fig. 2-15 were simulated and their R_p are shown in Fig. 2-16. For the circuit in Fig. 2-15(a), using Eq. (2.24) and the simulated operating points shown, we can calculate R_p = 16.6 kΩ, L_{eq} = 91 μH, and r_s = 0.23 mΩ; these numbers are close to the simulated results, which are R_p = 16.7 kΩ, L_{eq} = 97.7 μH, and r_s = 0.63 mΩ.

Comparing the simulation results we find that R_f does improve Q, as measured by the R_p increase from 16.8 kΩ (cursor A) to 22.4 kΩ (cursor B). Since Q_R is proportional to R_P to the first order (Eq. 2.8), Q_R will increase by about 35%. R_f does not change the value of L_{eq} to the first order.

This method of creating a phase lag by inserting R_f to enhance Q_R is also used in cascode and regulated cascode, as well as differential active inductors, as we shall see later.

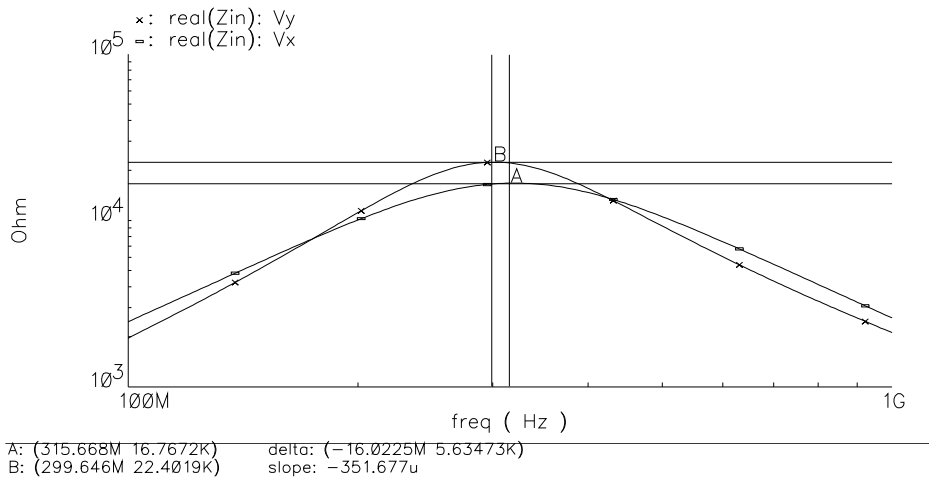


Figure 2-16 Simulated R_p of the circuits in Fig. 2-15. V_x and V_y are from the circuits in Fig. 2-15(a) and (b), respectively.

2.4.6 Cascode and Regulated-Cascode Active Inductors

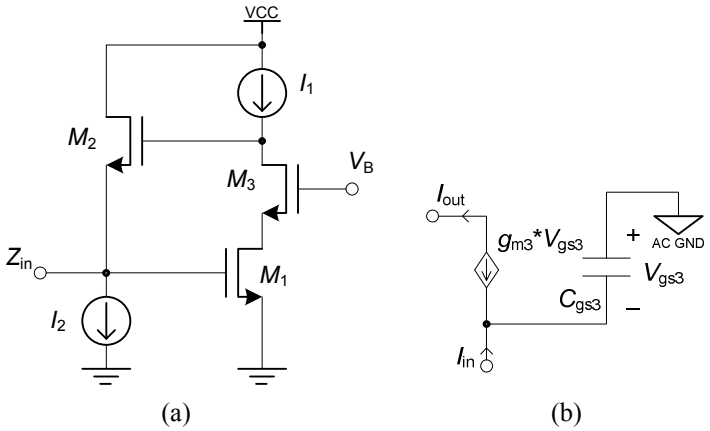


Figure 2-17 (a) Cascode active inductor. (b) small-signal equivalent circuit of M_3.

As seen from Eq. (2.24), to reduce the series resistor r_s of the CS-CD circuit we need to reduce g_1. In an effort to reduce g_1, in many designs [51, 53-59] a cascode transistor is introduced to the drain of M_1 of the CS-CD active inductor, resulting in the cascode active inductor as shown in Fig. 2-17(a). The common understanding is that the cascode NFET increases R_{out} looking into the M_1 drain and hence increases Q_L and Q_R. However, there are two apparent paradoxes to this claim:

1. The PFET implementing the biasing current I_1 is usually not cascoded, limiting g_1 by the PFET's g_{ds}. The introduction of the cascode NFET M_3 will therefore reduce g_1 by a maximum of about 50%.
2. Per Eq. (2.24), g_1 is only related to the series resistance r_S. Reducing g_1 does not affect the low-value parallel resistor R_p [57], which limits the Q_R to a low value.

Nonetheless, the cascode scheme does improve Q_R and compensates for the parallel resistance R_p, as verified in many papers. The true reason is that the cascode transistor M_3 creates a phase lag between its input and output current. Using the small-signal ac circuit in Fig. 2-17(b), the relationship is

$$\frac{I_{out}}{I_{in}} = \frac{1}{1 + sC_{gs3}/g_{m3}} \tag{2.25}$$

The active inductor f_R is usually 5-40% that of g_m/C_{gs} of the FETs used, hence the cascode FET current transfer function pole frequency is conveniently located at a frequency of 2-20 times that of f_R, with a phase lag of 3-20° at f_R. As we will see later in Section 2.5.3, this is the right amount of phase lag for Q_R compensation. Therefore, cascode is an effective way of improving the CS-CD active-inductor Q_R, not because that it increases R_{out} of the G_m cell, but because of its phase lag from the high-frequency parasitic pole. Note that the cascode FET does not significantly reduce r_s and improve Q_L, as it cannot reduce g_1 much without inserting a cascode PFET to the current source I_1, which will increase the minimum V_{DD} requirement.

J. Yang et al. insert a gate-biasing resistor R_B (of unknown value) to the cascode circuit (Fig. 2-18(a)) and augment C_{gs3} by putting a capacitor between M_3's gate and source, and claim that this compensates the device losses [58]. Using the ac small-

signal equivalent circuit of M_3 in Fig. 2-18(b), we have

$$\begin{aligned} &\left(I_{\text{in}} - I_{\text{out}}\right)\frac{1}{sC_{\text{gs3}}}g_{\text{m3}} = I_{\text{out}}, \quad \text{and} \\ &\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{g_{\text{m3}}}{sC_{\text{gs3}} + g_{\text{m3}}} \end{aligned} \tag{2.26}$$

Comparing Eqs. (2.25) and (2.26), we find that R_{b} has no direct effect on the current transfer function of M_3, and therefore the circuit performance is not significantly different from that in Fig. 2-17. R_{b} only works through the 2nd-order effect from the g_{ds} of M_3. Nonetheless, R_{b} exists on most real circuits because the output resistance of biasing circuits is limited.

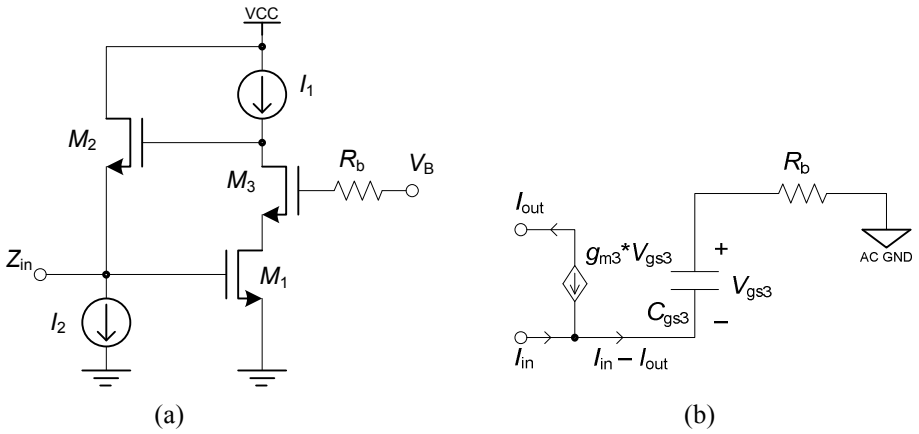


Figure 2-18 (a) Adding R_{b} to the cascode active inductor. (b) Small-signal equivalent circuit of M_3 and R_{b}.

To examine the Q enhancement of the cascode FET, a comparison simulation is performed on the circuits in Fig. 2-19. Note that ideal current sources are used, and the r_{s} reduction from the use of cascode is exaggerated because there is no current source leakage to dilute the Q enhancement. The simulation results in Fig. 2-20 show that R_{p} is increased by ~ 5.5x (R_{P} ratio = 92.5 kΩ/16.8 kΩ).

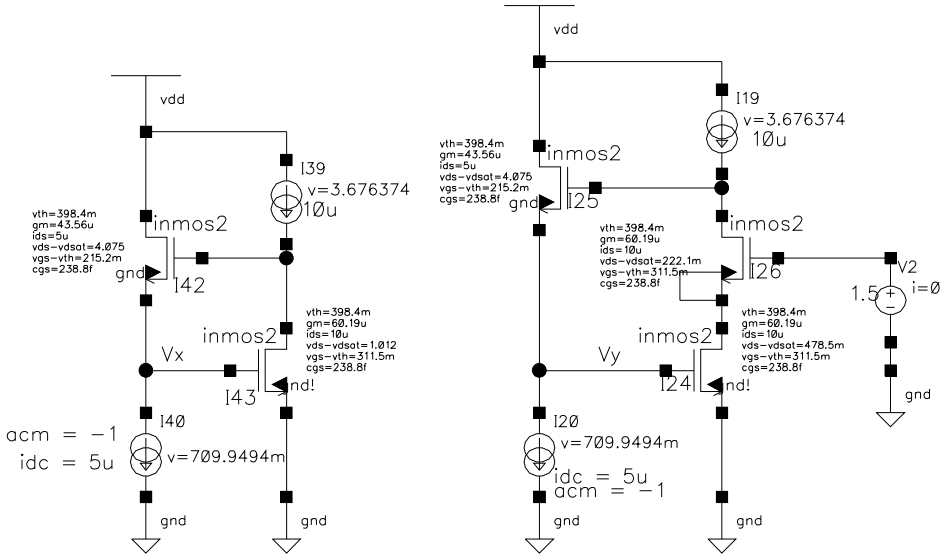


Figure 2-19 Simulation circuits to show the *Q* enhancement achieved by cascode. (a) CS-CD active inductor; (b) Cascode active inductor.

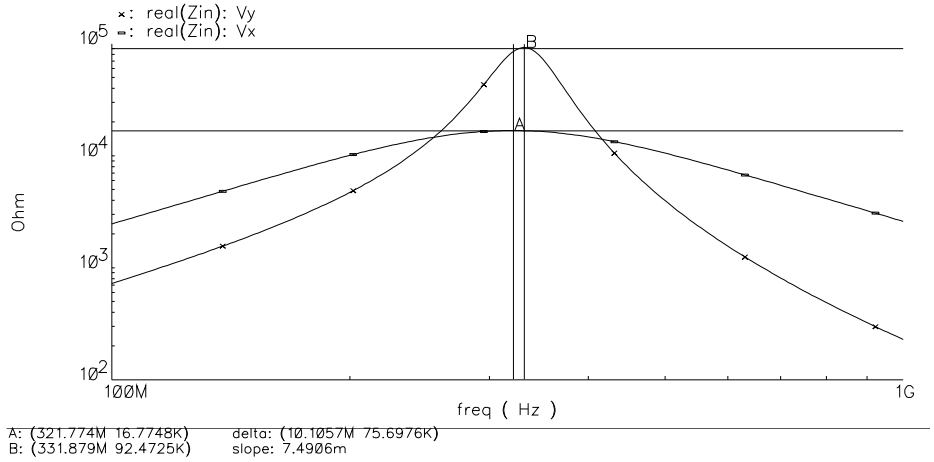


Figure 2-20 Simulated R_p of the circuits in Fig. 2-19. Cursor A and B are for circuit (a) and (b), respectively.

Finally, by introducing M_4 and I_3 to regulate the M_3 gate voltage, the regulated cascode active inductor can be derived [53, 55, 60], as shown in Fig. 2-21. M_4 is biased at a fixed $I_{DS4} = I_3$, thus V_{GS4}, and in turn, V_{DS1}, is constant, increasing the resistance looking into the M_1 drain. The cascode FET M_3 further amplifies the resistance looking into the drain of M_3. The voltage regulation through M_4 only makes M_3 more effective.

The regulated cascode active inductor can be understood as a CS-CD active inductor + g_1 reduction through cascode + further g_1 reduction from voltage regulation. Note that g_1 is limited by the biasing current I_1 in Fig. 2-17(a) when the resistance looking down into the cascode FET is very high, therefore, the improvement from voltage regulation will be negligible if the cascode active inductor is designed properly in the first place. The efficacy in improving Q_R researchers are seeing from the use of voltage regulation is more likely due to the extra current-transfer-function delay in the cascode FET from the voltage regulation, rather than due to the g_1 reduction from the use of voltage regulation.

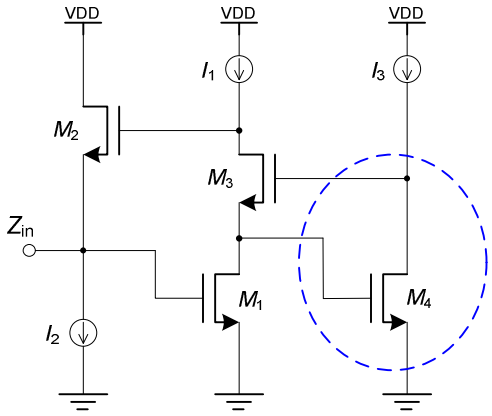


Figure 2-21 Regulated cascode active inductor circuit.

2.4.7 Differential-Pair Active Inductor

The differential-pair active inductor [61-64] is shown in Fig. 2-22(a). The differential pair is the simplest differential G_M, and using the G_M symbol, the circuit is redrawn in Fig. 2-22(b). The circuit is recognized as a gyrator, with C_1 and C_2 being the parasitic capacitance (mainly C_{gs}) across the drains of $M_{1,2}$ and $M_{3,4}$, respectively. The noninverting G_M is conveniently obtained by a cross connecting of one of the G_M

cells.

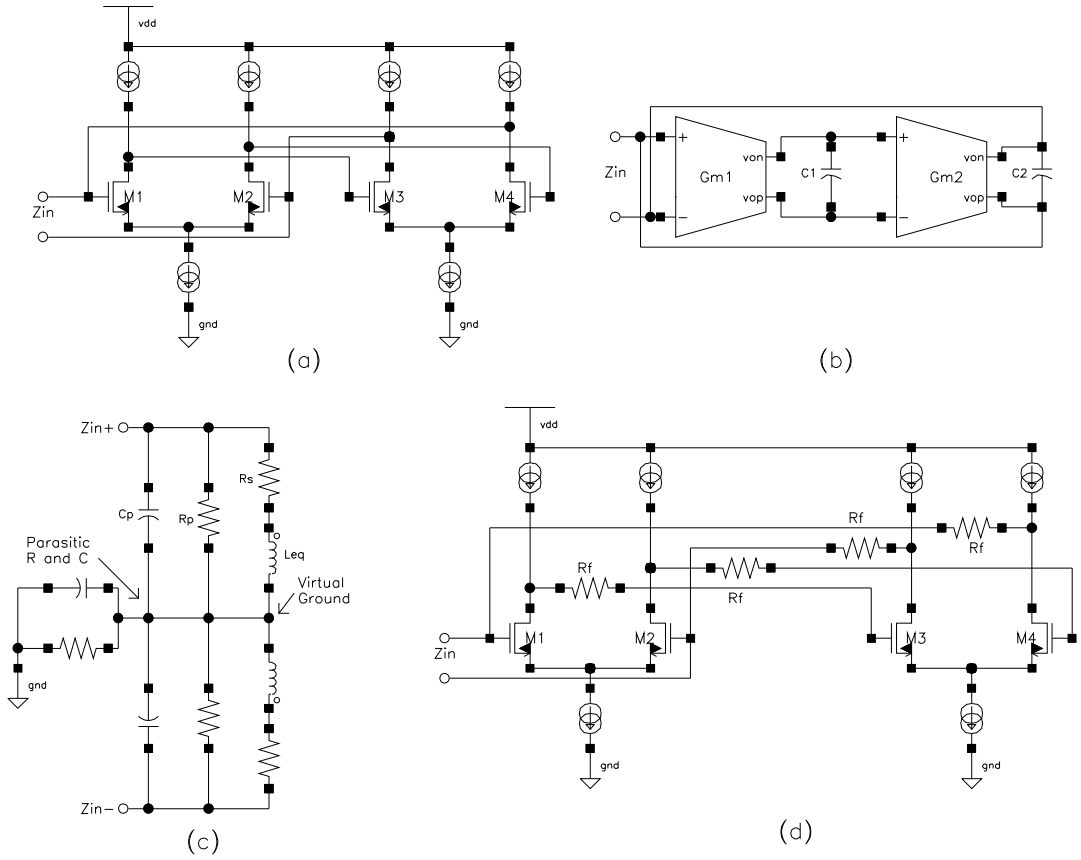


Figure 2-22 The differential-pair active inductor.

The circuit shall not be erroneously interpreted as a floating inductor, even though it may roughly operate as one. There is a virtual ground node between the two input terminals, as shown in Fig. 2-22(c), if the circuit is treated as a floating inductor, the virtual ground node will become a signal node, with a parasitic capacitor, so it will not be a good floating inductor.

The differential-pair active inductor does not have a low-impedance node in its gyrator loop, hence it can achieve a reasonably high Q_R without compensation. To further compensate for the device losses, a negative resistor made with a cross-connected differential pair can be introduced to the circuit [64]. However, very often

the circuit is overly compensated and becomes unstable, because its g_1 and g_L are both from g_{ds}s, which are orders of magnitude smaller than g_m. A more common method is to add some feedback resistors in series with the gates [61-63], as shown in Fig. 2-22(d). R_f, together with the C_{gs} it connects to, creates a phase lag in the gyrator loop. As we shall see later in Section 2.5.3, a phase lag in the gyrator loop has the effect of increasing Q_R.

The major drawback of this circuit is the difficulty of dc biasing, because it has positive feedback for common-mode voltages with loop gain much greater than 1. It can be found from Fig. 2-22(a) that the common-mode signal path consists of two inverters in a loop, which has a large positive gain. Special measures such as biasing resistors must be used to stabilize the dc biasing, which as a result, degrade the circuit's performance.

2.4.8 Karsilayan's Active Inductor

During the design of a floating tunable voltage source for high-linearity G_M cells, Karsilayan and Schaumann [65] discovered that the circuit shown in Fig. 2-23(a) is in fact a high-Q active inductor. The circuit is easily understood using the gyrator principle. The differential pair formed by M_1 and M_2 is a noninverting G_M cell with input voltage at node 1 and output current at node 3, and M_3 is an inverting G_M with input voltage at node 3 and output current at node 1. The parasitic capacitance, mainly C_{gs3}, is thus gyrated into an equivalent inductor at node 1. Due to the inevitable parasitic capacitance at node 1 and the circuit losses, the equivalent circuit is a resonator, as shown in Fig. 2-23(b). The series resistor originates from the load loss g_L

at node 3.

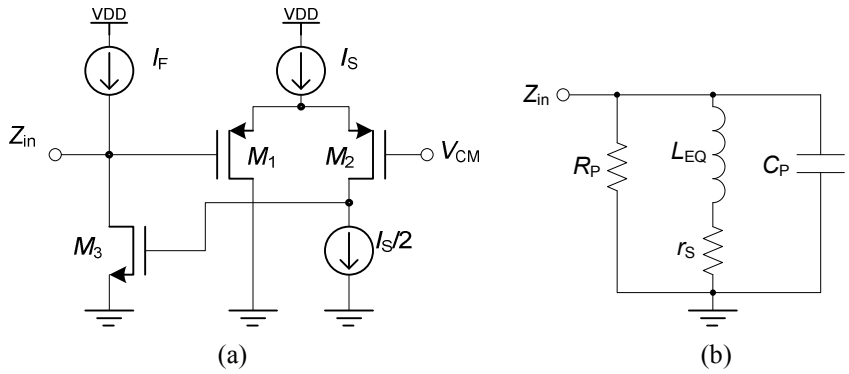


Figure 2-23 (a) Karsilayan's active inductor circuit. V_{CM} is a dc voltage that sets the circuit's common-mode voltage. (b) Small-signal ac equivalent circuit.

Karsilayan's circuit, like the regulated cascode circuit, is readily biased, with low V_{DD} requirement ($2V_{DS} + V_{GS}$). Unlike the regulated cascode circuit and many other active inductors, the two nodes in the gyrator loop are both high-resistance, and consequently, the circuit has an intrinsically high Q_R. It was also proved that the unavoidable device losses are readily compensated by tuning the parasitic capacitance at node 2, C_2, via a varactor [65]. When C_2 increases, the phase lag of M_1-M_2 differential-pair G_M cell increases, and this has the effect of increasing the Q_R.

It can be shown that if node 1 is driven by a current source, I_{in}, the output voltage at node 3 has lowpass characteristic. If the output is taken instead at node 1, a bandpass function, $V_{out} = I_{in}Z_{in}$, is obtained. Alternatively, if the input voltage signal is injected at node V_{CM} together with a dc-voltage V_{CM}, a lowpass voltage output can be derived at node 1 [66]. The active inductor circuit has also been used to design sinusoidal RF oscillators [67].

2.4.9 Other Active Inductors

There are many other active inductor circuits [68-79] that are variations of the basic topologies shown above, for example, by exchanging NFET with PFET in part or all of the circuits, combining the Q-enhancement techniques, etc. However, they can almost always be simplified down to the gyrator equivalent circuit shown in Fig. 2-3. The actual circuit can have more equivalent devices than that; however, the benefits from the extra devices rarely leverage the entailed disadvantages, such as lower f_R from extra parasitic capacitance, more parasitic poles/zeros from extra circuit nodes, higher noise, and more power dissipation.

2.5 Methods of Increasing Q_R

There are three approaches for increasing Q_R: reducing g_1 and/or g_L in the gyrator equivalent circuit; introducing a negative resistor; and generating phase lag. It shall be noted that per Eq. (2.6), r_S is determined by g_L, which is the loss at the load node, and the only way to reduce r_S and increase Q_L is to reduce g_L. Phase lag in the gyrator loop will not reduce r_S and improve Q_L.

2.5.1 Reducing g_1 and/or g_L in Gyrator Equivalent Circuit

From Eqs. (2.6) and (2.10) we have

$$Q_L(\omega) \approx \frac{\omega L_{eq}}{r_s} = \frac{\omega C_L / (G_{M1} G_{M2})}{g_L / (G_{M1} G_{M2})} = \frac{\omega C_L}{g_L} \tag{2.27}$$

that is, to increase Q_L at a certain frequency we must increase C_L/g_L. Usually, the value of C_L is kept the same, but through circuit techniques g_L is reduced. Note that all

circuits can be scaled up and down, but it is the ratio that matters. This is a very common method for enhancing Q in many circuits, such as in the cascode active inductor. Note that reducing g_L alone is sufficient to enhance Q_L, because as an inductor the circuit operates at a lower frequency than as a resonator, and the effect of g_L dominates that of g_1 in determining Q_L.

On the other hand, reducing g_L is necessary, but not sufficient to obtain a high Q_R, that is, a high-Q resonator, to implement designs such as narrow-band bandpass filters. From Eqs. (2.6) and (2.8) we have

$$Q_R = \frac{\sqrt{\frac{1+g_1 r_s}{L_{eq} C_1}}}{\frac{r_s}{L_{eq}} + \frac{g_1}{C_1}} \approx \frac{\sqrt{L_{eq} C_1}}{r_s C_1 + g_1 L_{eq}} = \frac{\sqrt{\frac{G_{M1} G_{M2}}{C_1 C_L}}}{\frac{g_L}{C_L} + \frac{g_1}{C_1}} = \frac{\omega_0}{\frac{g_L}{C_L} + \frac{g_1}{C_1}} \tag{2.28}$$

Q_R is jointly determined by g_L and g_1. To enhance Q_R, both g_L and g_1 must be reduced, a simple requirement, but not always easy to realize.

2.5.2 Negative Resistors

Many designers use negative resistors, such as cross-connected differential pairs, to cancel out the effect of g_1 or g_L, or both, to improve Q. There are too many references to be included here. One example is [45]. Negative resistors consume power and introduce nonlinearities and noise; however, this method is easy to implement, and for some circuit structures, is the only option.

2.5.3 Phase Lag in the Gyrator Loop

Another way to enhance Q_R is to introduce a phase lag into the gyrator loop. This is a widely used method, but not always so realized by designers. For example, many

papers attribute the higher Q_R of the cascode-active inductor solely to the R_{out} enhancement of the cascode FET [57], and some researchers believe that the phase lag decreases Q and hence is undesirable [59]. The following discussion will show that the opposite is true.

Figure 2-3 assumes that both G_{M1} and G_{M2} have zero phase shift at all frequencies concerned. This is not true in practice. The inverting G_M can be implemented by a single common-source FET and has almost zero phase shift; however, due to transistor (either FET or BJT) properties, a noninverting G_M has to be a common-gate (cascode) FET, which yields low-Q circuits, or a differential pair [65] (= folded cascode), and has inevitably a phase lag due to the parasitic pole(s). Note that a single CS FET may have a *phase advance* at high frequencies due to C_{gd}.

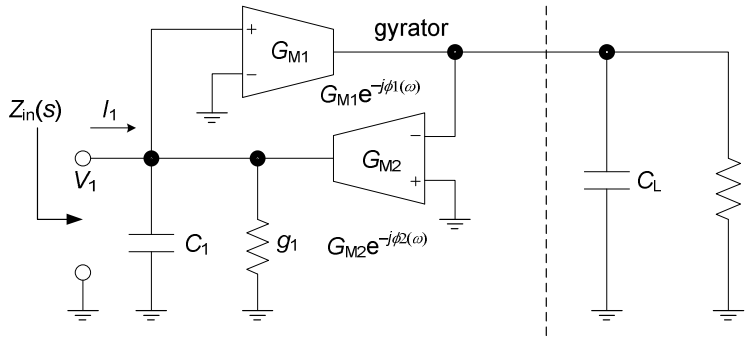


Figure 2-24 The gyrator equivalent circuit of an active inductor. The phase lags of the G_M cells are shown to analyze their effect on Q.

The gyrator equivalent circuit including the G_M phase shifts is shown in Fig. 2-24, where each G_M cell has a frequency-dependent phase lag. The expression for input admittance is

$$Y_{in} = sC_1 + g_1 + \frac{G_{M1}e^{-j\phi_1(\omega)}G_{M2}e^{-j\phi_2(\omega)}}{g_L + sC_L} = sC_1 + g_1 + \frac{G_{M1}G_{M2}e^{-j\phi(\omega)}}{g_L + sC_L} \qquad (2.29)$$

where

$$\phi(\omega) = \phi_1(\omega) + \phi_2(\omega) \tag{2.30}$$

We first concentrate on the last term of Y_{in} and name it $Y'_{in} = 1/Z'_{in}$,

$$\begin{aligned} Z_{in}' &= \frac{g_L + sC_L}{G_{M1}G_{M2}e^{-j\phi(\omega)}} = \frac{g_L + sC_L}{G_{M1}G_{M2}\left[\cos\phi(\omega) - j\sin\phi(\omega)\right]} \\ &= \frac{\left(g_L + j\omega C_L\right)\left[\cos\phi(\omega) + j\sin\phi(\omega)\right]}{G_{M1}G_{M2}} \\ &= \frac{j\omega\left(C_L\cos\phi + \frac{g_L\sin\phi}{\omega}\right) + g_L\cos\phi - \omega C_L\sin\phi}{G_{M1}G_{M2}} \\ &= j\omega L_{eq} + r_s \end{aligned} \tag{2.31}$$

where

$$L_{eq} = \frac{C_L\cos\phi(\omega) + \frac{g_L\sin\phi(\omega)}{\omega}}{G_{M1}G_{M2}}, \quad r_s = \frac{g_L\cos\phi(\omega) - \omega C_L\sin\phi(\omega)}{G_{M1}G_{M2}} \tag{2.32}$$

Therefore the circuit is equivalent to that in Fig. 2-23(b) with $C_P = C_1$, $R_P = 1/g_1$, and L_{eq} and r_S given in Eq. (2.32).

The inductor Q is

$$Q_L(\omega) = \frac{j\omega L_{eq}}{r_s} = j\omega\frac{C_L\cos\phi(\omega) + \frac{g_L\sin\phi(\omega)}{\omega}}{g_L\cos\phi(\omega) - \omega C_L\sin\phi(\omega)} \tag{2.33}$$

When $\phi = 0$, Q_L is identical to that in Eq. (2.27). As ϕ gradually increases, Q_L will increase, too, because of the cancellation in the denominator. When

$$\phi(\omega) = \tan^{-1}\frac{g_L}{\omega C_L} \tag{2.34}$$

$Q_L = \infty$. This conclusion is contrary to that in [59], which states that the phase lag will reduce Q. On the other hand, $\phi(\omega)$ is generally derived from poles, and rarely matches

the $\tan^{-1}(1/\omega)$ curve. So this compensation scheme for active inductors when used as inductors can only work over a narrow frequency range.

The input impedance can also be written as

$$\begin{aligned} Z_{\text{in}} &= \frac{1}{g_1 + sC_1 + \frac{G_{\text{M1}}G_{\text{M2}}e^{-j\phi(\omega)}}{g_{\text{L}}+sC_{\text{L}}}} \\ &= \frac{g_{\text{L}} + sC_{\text{L}}}{s^2C_1C_{\text{L}} + s\left(C_{\text{L}}g_1 + C_1g_{\text{L}} - \frac{G_{\text{M1}}G_{\text{M2}}\sin\phi}{\omega}\right) + g_1g_{\text{L}} + G_{\text{M1}}G_{\text{M2}}\cos\phi} \\ &= \frac{\frac{s}{C_1} + \frac{g_{\text{L}}}{C_1C_{\text{L}}}}{s^2 + s\left(\frac{g_1}{C_1} + \frac{g_{\text{L}}}{C_{\text{L}}} - \frac{G_{\text{M1}}G_{\text{M2}}\sin\phi}{\omega C_1C_{\text{L}}}\right) + \frac{g_1g_{\text{L}}+G_{\text{M1}}G_{\text{M2}}\cos\phi}{C_1C_{\text{L}}}} = \frac{\frac{s}{C_1} + \frac{g_{\text{L}}}{C_1C_{\text{L}}}}{s^2 + s\frac{\omega_{\text{R}}}{Q_{\text{R}}} + \omega_{\text{R}}^2} \end{aligned} \tag{2.35}$$

with

$$\omega_{\text{R}} = \sqrt{\frac{g_1g_{\text{L}} + G_{\text{M1}}G_{\text{M2}}\cos\phi}{C_1C_{\text{L}}}} \approx \sqrt{\frac{G_{\text{M1}}G_{\text{M2}}\cos\phi}{C_1C_{\text{L}}}} \tag{2.36}$$

$$Q_{\text{R}} = \frac{\omega_{\text{R}}}{\frac{g_1}{C_1} + \frac{g_{\text{L}}}{C_{\text{L}}} - \frac{G_{\text{M1}}G_{\text{M2}}\sin\phi(\omega_{\text{R}})}{\omega_{\text{R}}C_1C_{\text{L}}}} \approx \frac{\omega_{\text{R}}}{\frac{g_1}{C_1} + \frac{g_{\text{L}}}{C_{\text{L}}} - \omega_{\text{R}}\tan\phi(\omega_{\text{R}})} = \frac{\omega_{\text{R}}}{a-b} \tag{2.37}$$

where

$$a = \frac{g_1}{C_1} + \frac{g_{\text{L}}}{C_{\text{L}}}, \quad b = \omega_{\text{R}}\tan\phi(\omega_{\text{R}}) \tag{2.38}$$

The terms a and b represent the intrinsic circuit loss and the compensation effect through the total loop phase lag, respectively. There are a few observations:

1. As ϕ increases from 0 to $\leq \pi/2$, Q_{R} will increase. By our notation, $\phi > 0$ represents a phase lag.
2. The ϕ value near ω_{R} determines Q_{R}. ϕ values at other frequencies have no direct effect on Q_{R}.

3. Only the total phase lag $\phi = \phi_1 + \phi_2$ matters. The ϕ distribution between G_{M1} and G_{M2} does not matter.

4. ϕ compensates both g_1 and g_L for Q_R.

When

$$\phi(\omega_R) \geq \sin^{-1} \frac{\left(\frac{g_1}{C_1} + \frac{g_L}{C_L}\right)\omega_R C_1 C_L}{G_{M1} G_{M2}} \tag{2.39}$$

Q_R will be ∞ or negative, an inadvisable situation, as the implemented circuit will be unstable and self oscillate. Nonetheless, this indicates that ϕ can fully compensate losses contributed by g_1 and g_L at ω_R.

The phase lag in the gyrator loop can be created through the use of a cascode transistor, a resistor to create *R*-*C* delay, or a tunable capacitor. These methods are discussed in the survey of active inductors above.

2.5.4 Q_R Sensitivities

Using Eq. (2.37) we can calculate the Q_R sensitivities with respect to a and b as

$$S_a^{Q_R} = \frac{a}{Q_R}\frac{\partial Q_R}{\partial a} = -Q_R \frac{a}{\omega_R} \tag{2.40a}$$

$$S_b^{Q_R} = \frac{b}{Q_R}\frac{\partial Q_R}{\partial b} = Q_R \frac{b}{\omega_R} \tag{2.40b}$$

which are both proportional to Q_R, and restrict the maximum realizable Q_R in practice. a and b are both related to circuit biasing and temperature. If Q_R is designed overly high, e.g., at 400, it is going to be highly sensitive to circuit variations and disturbances, and a very small change may push Q_R to thousands or negative

(unstable), or down to 200s. This is not surprising, since a high Q_R is derived from a delicate and measured cancellation between the effects of intrinsic circuit losses and Q_R compensation, that is, Q_R = 1/(large[1] number – large number). When the two numbers are close, a small error in either will dramatically change Q_R. This is the well-known problem entailed by setting a critical circuit parameter, here Q, via the measured coordination of different effects. If the parameter is set by the coordination of the same effect, for example, Q by a capacitor ratio, then the parameter will be very insensitive to circuit errors [10].

2.6 Noise of Gyrator-Based Active Inductors

Inevitably, all active inductors are noisy, since they are build with transistors (and resistors in some circuits), which generate noise. In most cases, noise is an undesirable attribute, and we would like to understand the generation mechanism and the fundamental limits, and reduce it if possible. The noise of active inductors can be represented as an equivalent shunt noise current, i_n^2 in Fig. 2-25. The noise current i_n^2 has a unit of A^2/Hz, and is generally a function of frequency, i.e., $i_n^2(f)$. This is sufficient in the noise analysis of typical active inductor applications, limiting/low-noise amplifiers, oscillators, and bandpass filters, and is more convenient than a series noise voltage, since in these applications, the active inductor is used as a shunt element rather than a series element.

[1] "Large" is relative to the difference between the two numbers.

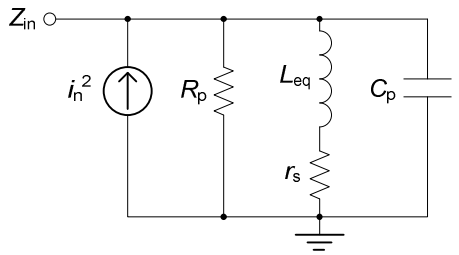


Figure 2-25 The noise model of an active inductor.

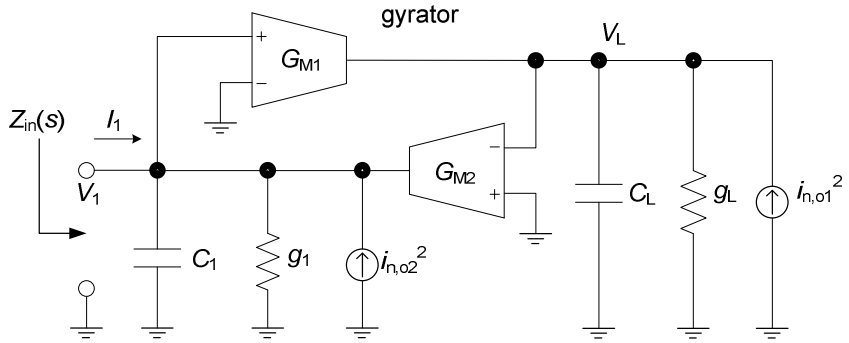


Figure 2-26 A gyrator-based active inductor showing noise elements.

The active inductor based on a gyrator is shown again in Fig. 2-26, including the noise elements from the transconductors. The noise of transconductors can be modeled as an equivalent input noise voltage, $v_{n,i}^2$ (V^2/Hz), in series with the input port or an equivalent shunt noise current, $i_{n,o}^2$, at the output, and they are related by

$$i_{n,o}^2 = G_M^2 v_{n,i}^2 \tag{2.41}$$

The noise voltage $v_{n,i}^2$ has a unit of V^2/Hz, and generally is a function of frequency, too. We choose to use the equivalent current. A higher value G_M will have higher noise level; however, a complicated circuit structure may also yield a higher noise level. A measure of transconductor noise level is herein defined as noise-factor coefficient, by dividing its squared noise to that of a resistor of equal value,

$$K_{NF} = \frac{i_{n,o}^2}{4kTG_M} \tag{2.42}$$

It can be shown that K_{NF} is unitless, and for a resistor, $K_{NF} = 1$. Note that a high K_{NF} may be a byproduct of other desirable features, such as high linearity. The conductors g_1 and g_L represent transconductor output losses; they are not physical resistors and their noise contributions have been included in $i_{n,o1}$ and $i_{n,o2}$ (both in $A/Hz^{1/2}$), hence their noises are not shown separately in the circuit.

Next we use node equations to derive the equivalent noise of the active inductor. From the node equation at V_L,

$$V_L\left(sC_L + g_L\right) = G_{M1}V_1 + i_{n,o1} \tag{2.43}$$

we have

$$V_L = \frac{G_{M1}}{sC_L + g_L}V_1 + \frac{i_{n,o1}}{sC_L + g_L} \tag{2.44}$$

Note that the node voltages V_L and V_1 are actually noise voltages, since we are using node equations for noise analysis, and have a unit of $V/Hz^{1/2}$. The same is true for the voltage and current signals in other noise analysis equations. Plugging this into the node equation at V_1,

$$V_1\left(sC_1 + g_1\right) + G_{M2}V_L = i_{n,o2} \tag{2.45}$$

we have

$$V_1\left(sC_1 + g_1\right) + \frac{1}{\left(sC_L + g_L\right)/\left(G_{M1}G_{M2}\right)}V_1 + \frac{G_{M2}}{sC_L + g_L}i_{n,o1} = i_{n,o2} \tag{2.46}$$

where $(sC_L + g_L)/(G_{M1}G_{M2})$ is recognized as the lossy inductor converted from the load by the gyrator, and the third term is an equivalent shunt noise current. In other words, the effect of noise source $i_{n,o1}$ can be moved to the output of G_{M2} by a transfer

function, despite the existence of a feedback loop formed by G_{M1} and G_{M2}. Thus, the total equivalent noise current in shunt with the input port of the active inductor is

$$i_n^2 = i_{n,o2}^2 + \frac{G_{M2}^2}{\omega^2 C_L^2 + g_L^2} i_{n,o1}^2 = i_{n,o2}^2 + \left|T_{N1}(\omega)\right|^2 i_{n,o1}^2 \tag{2.47}$$

where $T_{N1}(\omega)$ is the noise transfer function for $i_{n,o1}$.

Therefore, the noise contribution from $i_{n,o1}$ has been shaped by a low pass transfer function. As a special but representative case, consider $G_{M1} = G_{M2}$, $C_1 = C_L$, and ignore the effects of g_1 and g_L, at the frequency $\omega = \omega_R = G_{M1}/C_1$, we have

$$i_n^2 = i_{n,o2}^2 + \frac{G_{M1}^2}{\left(G_{M1}/C_1\right)^2 C_1^2 + 0} i_{n,o1}^2 = i_{n,o2}^2 + 1 \cdot i_{n,o1}^2 \tag{2.48}$$

i.e., the noise transfer function for $i_{n,o1}$ is 1. For frequencies $\omega < \omega_R$, the magnitude of the noise transfer function for $i_{n,o1}$ will be greater than 1:

$$\left|T_{N1}(\omega)\right|^2 = \frac{G_{M2}^2}{\omega^2 C_L^2 + g_L^2} \approx \frac{G_{M2}^2 / C_L^2}{\omega^2} \approx \frac{\omega_R^2}{\omega^2} > 1 \tag{2.49}$$

Using the definition of Eq. (2.42), we have

$$i_n^2 = i_{n,o2}^2 + \frac{\omega_R^2}{\omega^2} i_{n,o1}^2 = 4kT\left(K_{NF2} G_{M2} + \frac{\omega_R^2}{\omega^2} K_{NF1} G_{M1}\right) \tag{2.50}$$

Therefore, for a given ω_R and ω ($< \omega_R$), to reduce overall equivalent noise, we should reduce $i_{n,o1}$; whether this means G_{M1} should be less than G_{M2} depends on the G_M structure's noise factors K_{NF1} and K_{NF2}. Note that for practical circuits, the G_{M1} and G_{M2} values cannot be too different, for example, more than an order of magnitude, because the parasitic effects (e.g. C_{in}, C_{out}, phase shift) of the larger G_M cell can overwhelm the smaller G_M cell.

Similarly, in the case of $K_{NF1} = K_{NF2}$, we cannot make $G_{M1} = 0$ to minimize the overall noise. In other words, depending on the particular circuits, a G_{M1} to G_{M2} ratio optimum for low noise is likely to be outside of practicality.

Per Fig. 2-26, when the active inductor port is floating, the equivalent output noise voltage, $v_{n,o}$ (V/Hz$^{1/2}$), on the port will be

$$v_{n,o}^2(\omega) = \left|Z_{in}(\omega)\right|^2 i_{n,o}^2(\omega) \quad \text{or} \quad v_{n,o}(\omega) = \left|Z_{in}(\omega)\right| i_{n,o}(\omega) \tag{2.51}$$

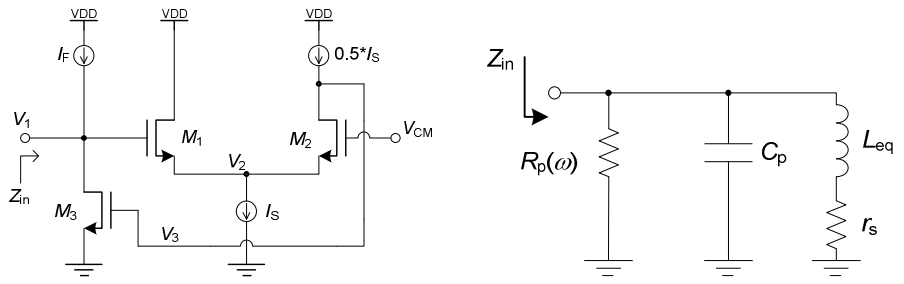
which is the equivalent shunt noise current shaped by the active inductor Z_{in} profile.

2.7 The All-NMOS Active Inductor (New in This Work)

2.7.1 The All-NMOS Active-Inductor Circuit

This circuit is developed from Karsilayan's circuit (Fig. 2-23) and is shown in Fig. 2-27 [80-82]. Its Z_{in} is equivalent to that of a grounded inductor. It is new in this work, and the main difference from Karsilayan's circuit is that the noninverting G_M is implemented using an NMOS differential pair rather than a PMOS differential pair. The inverting G_M is not changed. NFETs have higher mobility than PFETs and thus the active inductor has higher self-resonance frequency f_R due to its all-NMOS signal path. The frequency improvement is about 30%[2].

[2] f_R of the all-NMOS active inductor is measured to be 5.7 GHz at 0.2-μm gate length, while in Karsilayan's circuit f_R was measured to be 4.1 GHz for the same technology and gate length. Results of the latter are unpublished.



(a) (b)

Figure 2-27 (a) The all-NMOS signal-path active-inductor circuit. (b) Equivalent circuit.

The circuit's operation can be understood by tracing the signal flow. Transistors M_1 and M_2 implement a noninverting G_M, labeled G_{M1} (= $0.5g_{m1}$, if $g_{m1} = g_{m2}$ and the loss at node 2, g_2, is zero), with input voltage V_1 and output current at V_3. M_3 is an inverting transconductor, labeled $-G_{M2}$ (= $-g_{m3}$), with input voltage V_3 and output current at V_1. Thus, G_{M1} and $-G_{M2}$ form a gyrator, and convert the parasitic capacitor C_3 at Node 3 into a grounded inductor, $L_{eq} = C_3/(G_{M1}G_{M2})$, at node 1. The signal path consists of only NMOS transistors to take advantage of their higher mobility for the same device geometry. Therefore, the circuit can operate at a higher frequency [80, 81] than those built with a CMOS signal path [65-67]. The minimum V_{DD} is $V_{DS,p} + V_{GS,n} + V_{DS,n}$, which is around 1 V depending on the IC process and biasing conditions. For comparison, the minimum V_{DD} requirement of Karsilayan's circuit is $V_{DS,p} + V_{GS,p} + V_{DS,n}$. The difference in V_{DD} requirement of the two circuit is $V_{T,n} - V_{T,p}$, which is determined by the process, when the transistors have the same overdrive voltages.

2.7.2 Small-Signal Analysis

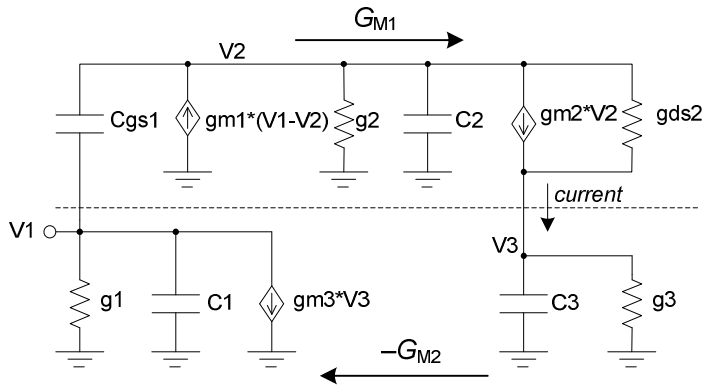


Figure 2-28 Small-signal equivalent circuit of the active inductor in Fig. 2-27(a). $g_{m1\text{-}3}$ are the transconductances of $M_{1\text{-}3}$, and $C_{1\text{-}3}$ and $g_{1\text{-}3}$ are the total parasitic capacitances/conductances at nodes 1-3, respectively. C_2 also includes the capacitance from a small varactor for Q tuning.

The input impedance Z_{in} can be derived from an analysis of the small-signal ac equivalent circuit in Fig. 2-28. A mathematically accurate expression including all terms can of course be obtained; however, to provide designers with better insight, a few small parasitic terms are neglected when summed with dominant terms. The approximate expression is

$$Z_{in}(s) \approx \frac{\frac{s}{C_1}+\frac{g_3}{C_1C_3}}{s^2+s\left(\frac{g_1}{C_1}+\frac{g_3}{C_3}+\frac{g_1g_3C_2}{C_1C_3G}-\omega^2\frac{C_2}{G}\right)+\frac{g_{m2}}{G}\frac{g_{m1}g_{m3}}{C_1C_3}} \tag{2.52}$$

where $G = g_{m1} + g_{m2} + g_2$, and the equivalence $s^3 = -\omega^2 s$ has been used, because the effect of the negative real pole from the s^3 term is not dominant, compared with that of the dominant conjugate complex poles. The format of Z_{in} shows that it is equivalent to an *RLC* network, as shown in Fig. 2-27(b): the denominator together with the s term in the numerator indicates an *LC* resonance with limited Q, and the real term in the numerator indicates a resistor in series with the inductor. The element values can be determined from Z_{in} as follows. At dc ($s = 0$),

$$Z_{\text{in}}(0)=\frac{g_3 G}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}=\frac{g_3\left(g_{\text{m1}}+g_{\text{m2}}+g_2\right)}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}=\frac{g_3\left(g_{\text{m1}}/g_{\text{m2}}+1+g_2/g_{\text{m2}}\right)}{g_{\text{m1}}g_{\text{m3}}}$$
$$\approx\frac{g_3}{0.5g_{\text{m1}}g_{\text{m3}}}=r_{\text{s}},\ \text{when } g_{\text{m1}}\approx g_{\text{m2}}\ \text{and } g_2<<g_{\text{m1}},\ g_{\text{m2}} \tag{2.53}$$

where r_{s} is the resistor in series with L_{eq}; it dominates $R_{\text{p}}(\omega)$ at dc. At very high frequencies, $Z_{\text{in}} \propto 1/(sC_1)$, hence the parallel capacitor is

$$C_{\text{p}}=C_1 \tag{2.54}$$

The resonance frequency is

$$\omega_{\text{R}}=\sqrt{\frac{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}{GC_1C_3}}\approx\sqrt{\frac{0.5g_{\text{m1}}g_{\text{m3}}}{C_1C_3}}=\frac{1}{\sqrt{L_{\text{eq}}C_1}} \tag{2.55}$$

At intermediate frequencies between g_3/C_3 and ω_{R}, $Z_{\text{in}}(s)$ can be transformed into

$$Z_{\text{in}}(s)=\frac{\frac{sGC_3}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}\left(1+\frac{g_3/C_3}{s}\right)}{\frac{s^2}{\omega_{\text{R}}^2}+\frac{s}{\omega_{\text{R}}^2}\left(\frac{g_1}{C_1}+\frac{g_3}{C_3}+\frac{g_1g_3C_2}{C_1C_3G}-\omega^2\frac{C_2}{G}\right)+1}\approx\frac{\frac{sGC_3}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}(1+0)}{0+0+1}$$
$$=s\frac{GC_3}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}=sL_{\text{eq}},\qquad \text{when } \frac{g_3}{C_3}<<|s|<<\omega_{\text{R}} \tag{2.56}$$

which represents an inductor. L_{eq} can also be derived from Eqs. (2.54) and (2.55),

$$L_{\text{eq}}=\frac{GC_3}{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}\approx\frac{C_3}{0.5g_{\text{m1}}g_{\text{m3}}},\ \text{when } g_{\text{m1}}\approx g_{\text{m2}}\ \text{and } g_2<<g_{\text{m1}},\ g_{\text{m2}} \tag{2.57}$$

The quality factor at ω_{R} is

$$Q_{\text{R}}=Q(\omega_{\text{R}})=\frac{\sqrt{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}/\left(GC_1C_3\right)}}{\frac{g_1}{C_1}+\frac{g_3}{C_3}-\frac{C_2}{G}\left(\omega_{\text{R}}^2-\frac{g_1g_3}{C_1C_3}\right)}=\frac{\omega_{\text{R}}}{a-b} \tag{2.58}$$

where a and b are

$$a = \frac{g_1}{C_1} + \frac{g_3}{C_3},\ b = \frac{C_2}{G}\left(\omega_R^2 - \frac{g_1 g_3}{C_1 C_3}\right) \tag{2.59}$$

a represents again the intrinsic loss of the circuit and b represents the compensation effected through C_2. C_2 is at the internal node of the noninverting G_M. A larger C_2 will yield a larger phase lag ϕ in the noninverting G_M and hence a larger Q_R, per Eq. (2.37). Since $g_i << g_{mi}$, $i = 1, 3$, we always have

$$\omega_R^2 - \frac{g_1 g_3}{C_1 C_3} = \frac{1}{C_1 C_3}\left(\frac{g_{m1} g_{m2} g_{m3}}{G} - g_1 g_3\right) \approx \frac{1}{C_1 C_3}\left(\frac{g_{m1} g_{m3}}{2} - g_1 g_3\right) > 0 \tag{2.60}$$

hence the loss compensation through C_2 is guaranteed. When

$$C_2 = \left(\frac{g_1}{C_1} + \frac{g_3}{C_3}\right)\frac{G}{\omega_R^2 - g_1 g_3 / (C_1 C_3)} \approx \left(\frac{g_1}{C_1} + \frac{g_3}{C_3}\right)\frac{G}{\omega_R^2} \tag{2.61}$$

Q_R will be infinite. Although $Q_R = \infty$ is not advisable in practice since the circuit will oscillate, it nevertheless indicates that there is no upper limit on Q_R with this active-inductor structure because C_2 can compensate the effects of g_1, g_2, and g_3, that is, of all losses in the circuit, around f_R. But observe the potentially huge sensitivities in Eq. (2.40) as Q_R increases.

The shunt equivalent resistor R_p can be derived from Eq. (2.8),

$$R_p = Q_R\sqrt{\frac{L_{eq}}{C_p}} = \frac{1}{g_1 + g_3\dfrac{C_1}{C_3} - \dfrac{C_1 C_2}{G}\left(\omega_R^2 - \dfrac{g_1 g_3}{C_1 C_3}\right)} \tag{2.62}$$

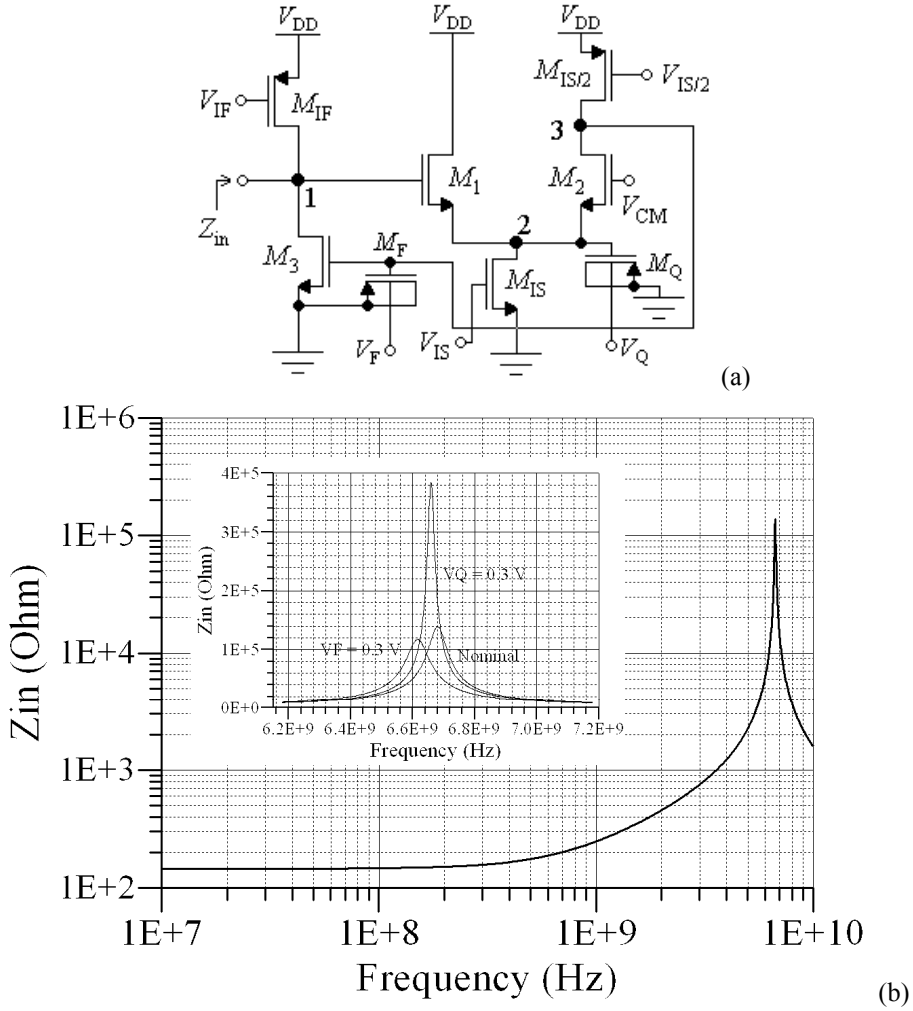


Figure 2-29 Example simulations of the all-NMOS signal-path active inductor in a pseudo-differential structure. (a) The active inductor circuit with biasing and tuning components shown. (b) The magnitude of Z_{in} as simulated in the TSMC 0.18-μm standard digital CMOS process. Transistor sizes (W/L in μm) and nominal bias values are: $M_{1,\,2,\,3}$ 3/0.2, $M_{IF,\,IS/2}$ 6/0.2, M_{IS} 8.4/0.2, M_F 1.5/0.4, M_Q 3/0.4, $I_{M_{IF}} = I_{M_{IS}} = 250$ μA, $V_F = V_Q = 0.6$ V, $V_{CM} = 1.325$ V, $V_{DD} = 1.8$ V, $f_R = 6.68$ GHz, $Q_R = 106$. Shown in the insert are the ("Nominal") plot of Z_{in} "zoomed-in" around f_R at the above biasing conditions, and two others showing f_R and Q_R tuning. When V_F is reduced to 0.3 V, $f_R = 6.613$ GHz, and Q_R becomes 87; when V_Q is reduced to 0.3 V, $Q_R = 289$ and f_R becomes 6.658 GHz. Other conditions remain the same in both cases.

The Q_R enhancement and tuning are achieved solely through the capacitor C_2 (tuned by the varactor M_Q, see Fig. 2-29), whose major portion is already in the circuit as a parasitic component; no additional loss-compensation circuitry, such as negative

resistors, is used. Hence, there is no power and only a small frequency penalty[3] for obtaining a large Q_R, and the circuit structure is very concise and efficient.

The complete circuit is shown in Fig. 2-29(a) and some representative simulation results are contained in Fig. 2-29(b). Two varactors, M_F and M_Q, are added for tuning f_R and Q_R, respectively. Tuning of f_R and Q_R via varactors is relatively independent within a moderate tuning range; hence there will be little or no need for tuning iterations. Note that single-transistor current sources can be used because their higher output losses are readily compensated by the choice of C_2. This saves devices, power and makes the active inductor/resonator suitable for low-voltage designs. As seen from Eqs. (2.55) and (2.58), f_R and Q_R are also tunable via the bias currents I_F and I_S over a wider range, since they change the values of g_m and g_{ds}.

To verify the equations, the circuit was simulated. As shown in Fig. 2-29(b), below 40 MHz, Z_{in} is roughly equal to a 146-Ω resistor; between 500 MHz and 4 GHz, $|Z_{in}| \propto \omega$ and is equivalent to an inductor of 31 nH in series with the 146-Ω resistor; above 12 GHz, $|Z_{in}| \propto 1/\omega$: it behaves like a capacitor of 16.8 fF. All frequency ranges are approximate as there is no clear cutoff between the regions. Its resonance frequency is f_R = 6.68 GHz, and Q_R = 106.

The small-signal parameters, g_{m1} = 1.15 mS, g_{m2} = 1.14 mS, g_{m3} = 1.15 mS, C_1 = 16.8 fF, C_2 = 16.4 fF, C_3 = 20.4 fF, g_1 = 132 μS, g_3 = 91 μS, and G = 2.44 mS are found from the operating points. Using these parameters in the equations, the circuit

[3] Unlike C_1 and C_3, C_2 has only a second-order effect on f_R, as shown by Eq. (2.55). However, as expected, increasing C_2 does reduce f_R by a relatively small amount due to second- and higher-order effects through the parasitic elements in the equivalent circuit (Fig. 2.28).

parameters, L_{eq}, r_s, f_R, Q_R and R_p can be calculated, as shown in Table 2-1. The calculated parameters are very close to the simulation results. Nevertheless, it is noted again that due to the potential high circuit sensitivities when Q_R is high and the approximation made in the small-signal circuit, the equations are not given for obtaining precise circuit performance, but to provide insight into the circuit's operation and to facilitate an informed design process. More accurate circuit performance in design should be obtained from circuit simulations, based on accurate device modeling and layout parasitics extraction.

Table 2-1 Calculated versus Simulated Results for the All-NMOS Active Inductor

Parameter	Unit	Sims	Calc'ed	Equation
g_{m1}	mS	1.15		
g_{m2}	mS	1.14		
g_{m3}	mS	1.15		
C_1	fF	16.8		
C_2	fF	16.4		
C_3	fF	20.4		
g_1	uS	132		
g_3	uS	91		
G	mS	2.44		
L_{eq}	nH	**31**	**33.0**	(2.57)
r_s	Ohm	**146**	**147.3**	(2.53)
f_R	GHz	**6.68**	**6.76**	(2.55)
ω_R	Grad/s		42.5	(2.55)
Q_R		**106**	**97**	(2.58)
R_p	kOhm	**140**	**137**	(2.62)

2.7.3 Noise Analysis

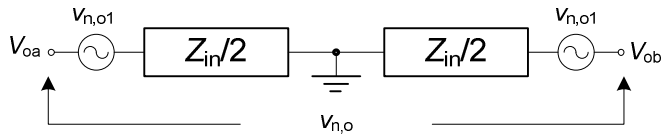


Figure 2-30 The noise model of a pseudo-differential active inductor.

The noise model of the pseudo-differential inductor is shown in Fig. 2-30. From

$$v_{\mathrm{n,o}}^2 = v_{\mathrm{n,o1}}^2 + v_{\mathrm{n,o1}}^2 = 2 \cdot v_{\mathrm{n,o1}}^2 \tag{2.63}$$

we have

$$v_{\mathrm{n,o1}} = \frac{v_{\mathrm{n,o}}}{\sqrt{2}} \tag{2.64}$$

Thus, the equivalent shunt noise current for each half of the active inductor is

$$i_{\mathrm{n,o1}} = \frac{v_{\mathrm{n,o1}}}{|Z_{\mathrm{in}}/2|} = \sqrt{2}\,\frac{v_{\mathrm{n,o}}}{|Z_{\mathrm{in}}|} = \sqrt{2} i_{\mathrm{n,o}} \tag{2.65}$$

This is verified by circuit simulation results shown in Fig. 2-31, as $i_{\mathrm{n,o1}}$ = 10.51 pA/Hz$^{1/2}$ at 6.68 GHz, while $\sqrt{2} i_{\mathrm{n,o}} = 9.73$ pA/Hz$^{1/2}$ per Fig. 2-31. The difference is about 7.4%.

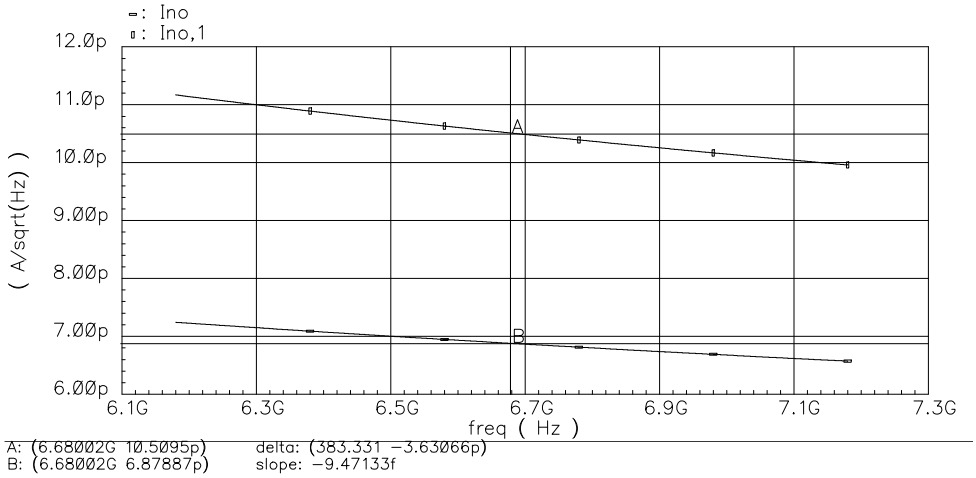


Figure 2-31 The equivalent output noise currents of the all-NMOS active inductor. The biasing conditions are the same as those in Fig. 2-29.

Next we will use the theory in Section 2.6 to derive the noise equations for the two G_{M} cells in the all-NMOS active inductor. For an NFET and a PFET carrying the same I_{D}, for example, M_3 and M_{IF}, we typically choose the similar gate overdrive voltage, to even the dynamic-range limiting and as a recommended circuit design

practice, that is

$$\frac{V_{\text{od,p}}}{V_{\text{od,n}}} = \sqrt{\frac{2I_{\text{D}}}{\mu_{\text{p}}C_{\text{ox,p}}\left(\frac{W}{L}\right)_{\text{p}}}} \Bigg/ \sqrt{\frac{2I_{\text{D}}}{\mu_{\text{n}}C_{\text{ox,n}}\left(\frac{W}{L}\right)_{\text{n}}}} = \sqrt{\frac{\mu_{\text{n}}C_{\text{ox,n}}\left(\frac{W}{L}\right)_{\text{n}}}{\mu_{\text{p}}C_{\text{ox,p}}\left(\frac{W}{L}\right)_{\text{p}}}} \approx 1 \tag{2.66}$$

Thus we have

$$\frac{g_{\text{m,p}}}{g_{\text{m,n}}} = \sqrt{\frac{2I_{\text{D}}\mu_{\text{p}}C_{\text{ox,p}}\left(\frac{W}{L}\right)_{\text{p}}}{2I_{\text{D}}\mu_{\text{n}}C_{\text{ox,n}}\left(\frac{W}{L}\right)_{\text{n}}}} = 1, \text{ when } I_{\text{D,p}} = I_{\text{D,n}} \tag{2.67}$$

Therefore, for G_{M1} (M_1 and M_2 in Fig. 2-29(a)), assuming $g_{\text{m1}} = g_{\text{m2}} = 0.5g_{\text{m,IS}}$ (because they have the same V_{OD}) and ignoring flicker noise and the effect of C_2 at node 2, we have

$$\begin{aligned} i_{\text{no,gm1}}^2 &\approx \left(i_{\text{n,M1}}^2 + i_{\text{n,M2}}^2 + i_{\text{n,MIS}}^2\right)\left(\frac{1}{g_{\text{m1}} + g_{\text{m2}}}\right)^2 g_{\text{m2}}^2 + i_{\text{n,MIS/2}}^2 \\ &\approx \left[4kT\Gamma_{\text{n}}g_{\text{m1}} + 4kT\Gamma_{\text{n}}g_{\text{m2}} + 4kT\Gamma_{\text{n}}\left(2g_{\text{m2}}\right)\right]\left(\frac{1}{2g_{\text{m2}}}\right)^2 g_{\text{m2}}^2 + 4kT\Gamma_{\text{p}}g_{\text{m2}} \\ &\approx 4kT\Gamma_{\text{n}} \cdot 4g_{\text{m1}} \cdot \frac{1}{4} + 4kT\Gamma_{\text{p}}g_{\text{m1}} = 4kT\left(\Gamma_{\text{n}} + \Gamma_{\text{p}}\right)g_{\text{m1}} \end{aligned} \tag{2.68}$$

where Γ_{n} and Γ_{p} are approximately 2/3 for long-channel ($L \geq 1.0$ μm) devices, but could be 1-2 in short-channel devices. Since $G_{\text{M1}} \approx 0.5g_{\text{m1}}$, the noise factor coefficient, $K_{\text{NF,1}}$, is calculated per Eq. (2.42)

$$K_{\text{NF,1}} = \frac{4kT\left(\Gamma_{\text{n}} + \Gamma_{\text{p}}\right)g_{\text{m1}}}{4kT0.5g_{\text{m1}}} = 2\left(\Gamma_{\text{n}} + \Gamma_{\text{p}}\right) \tag{2.69}$$

Similarly, for G_{M2} (M_3 in Fig. 2-29(a)), using the conclusion from Eq. (2.67), we have

$$i_{\text{no,gm2}}^2 = i_{\text{n,M3}}^2 + i_{\text{n,MIF}}^2 = 4kT\Gamma_{\text{n}}g_{\text{m3}} + 4kT\Gamma_{\text{p}}g_{\text{mIF}} \approx 4kT\left(\Gamma_{\text{n}} + \Gamma_{\text{p}}\right)g_{\text{m3}} \tag{2.70}$$

Since $G_{M2} = -g_{m3}$, we have

$$K_{NF,2} = \frac{4kT\left(\Gamma_n + \Gamma_p\right)g_{m3}}{4kTg_{m3}} = \Gamma_n + \Gamma_p \tag{2.71}$$

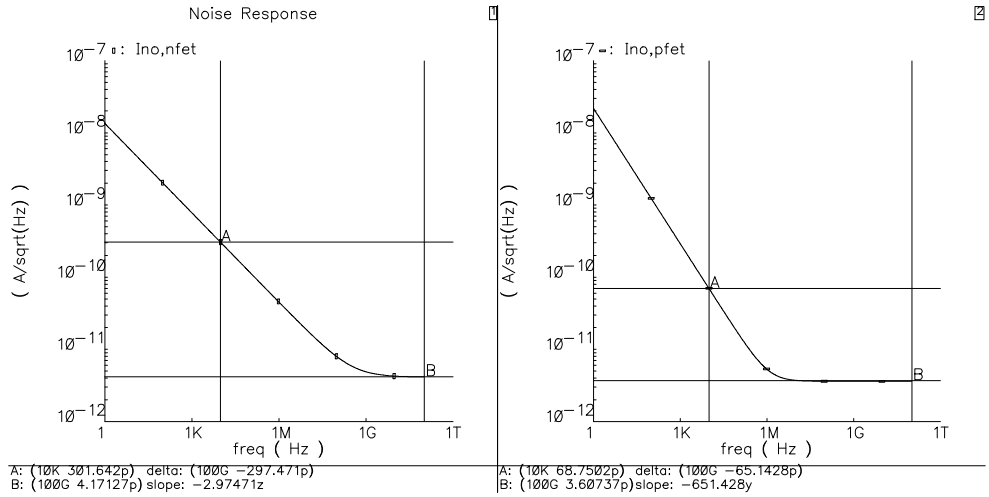


Figure 2-32 The output noise currents of an NFET and a PFET in TSMC 0.18-μm CMOS. Cursor A rests on 1/*f* noise region; cursor B rests on thermal noise region.

To use the above results, we need to know the noise parameters of the MOSFETs used in the all-NMOS active inductor. The TSMC device BSIM3 models have noise parameters available, of course; however, the equations for calculating noise using them are very complex, and we need something simpler for hand calculation. Therefore, we will extract simple noise model parameters from simulations. Figure 2-32 shows the output noise current of a 3.0/0.2 μm NFET and 6.0/0.2 μm PFET, which are used in the active-inductor circuit (varactor noise is not considered). Using the following MOSFET noise model [46],

$$\frac{i_{dn}^2}{\Delta f} = \frac{K_g}{W \cdot L \cdot f^t} g_m^2 + 4kT\Gamma g_m \tag{2.72}$$

the noise model parameters can be extracted from simulation results:

$$
\begin{aligned}
i_{\text{dn,nfet}}^2 &= \frac{7.622\times10^{-23}}{W\cdot L\cdot f^{0.825}}g_{\text{m,n}}^2 + 4kT\cdot 0.8786\cdot g_{\text{m,n}},\ \text{extracted on}\ 3.0/0.2\,\mu\ \text{NFET} \\
i_{\text{dn,pfet}}^2 &= \frac{8.599\times10^{-22}}{W\cdot L\cdot f^{1.25}}g_{\text{m,p}}^2 + 4kT\cdot 0.9685\cdot g_{\text{m,p}},\ \text{extracted on}\ 6.0/0.2\,\mu\ \text{PFET}
\end{aligned}
\tag{2.73}
$$

The flicker noise corner frequencies are 318 MHz and 1.1 MHz for the NFET and PFET at the above W/Ls, respectively. Ignoring the effect of flicker noise, the noise factor coefficients for G_{M1} and G_{M2} are calculated to be K_{NF1} = 3.6942 and K_{NF2} = 1.8471, respectively. Plugging in $G_{\text{M1}} \approx g_{\text{m2}}$ = 1.1 mS, $G_{\text{M2}} \approx g_{\text{m3}}$ = 1.2 mS, we expect their output noise currents being

$$
\begin{aligned}
i_{\text{no,gm1}} &= \sqrt{4kTG_{\text{M1}}K_{\text{NF1}}} = 8.20\ \text{pA}/\sqrt{\text{Hz}} \\
i_{\text{no,gm2}} &= \sqrt{4kTG_{\text{M2}}K_{\text{NF1}}} = 6.06\ \text{pA}/\sqrt{\text{Hz}}
\end{aligned}
\tag{2.74}
$$

which are close to the simulation results of 6.47 pA/Hz$^{1/2}$ and 5.89 pA/Hz$^{1/2}$ shown in Fig. 2-33. The difference for $i_{\text{no,gm1}}$ is mainly because the lowpass filtering effect of C_2 at node 2 is ignored in the above analysis. C_2 will reduce the noise appearing at the output of G_{M1}.

The noise of the active inductor in Fig. 2-29(a) built in a pseudo-differential structure was simulated and extracted for half of the circuit, as shown in Fig. 2-32. $I_{\text{no,gm1}}$ and $i_{\text{no,gm2}}$ are the equivalent output noise current of G_{M1}(M_1 and M_2 in Fig. 2-29(a)) and G_{M2}(M_3 in Fig. 2-29(a)), respectively, and can be approximately obtained by ac grounding the input node and placing a current probe with correct dc voltage at the output node. Also shown is the single-ended output noise current $i_{\text{n,o1}}$ (panel 2).

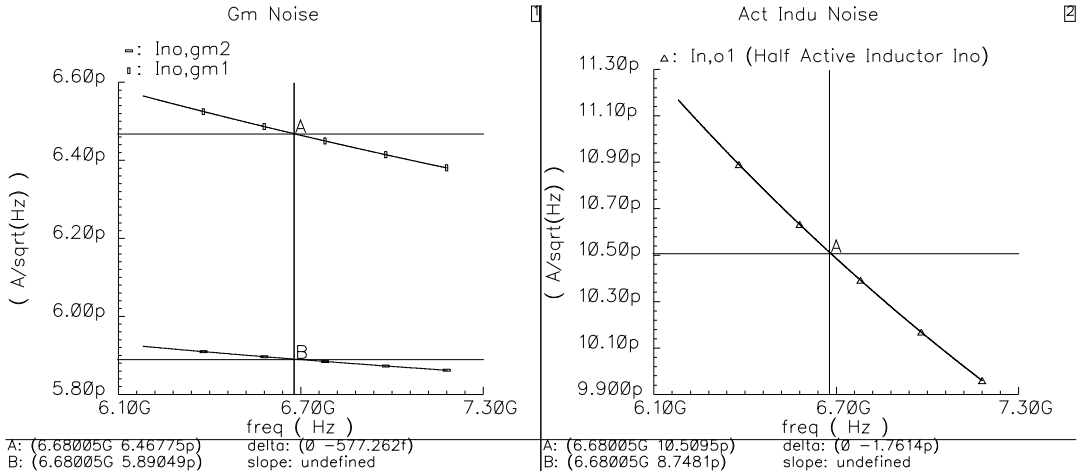


Figure 2-33 Noise simulation results of the G_M cells in the active inductor in Fig. 2-29(a). The biasing conditions are given in Fig. 2-29. Panel 1 shows the output noise current of G_{M1} and G_{M2}, respectively. Panel 2 shows the output noise current of the active inductor. All data are extracted from half of the circuit in a pseudo-differential structure.

Using Eq. (2.50) in Section 2.6, the equivalent shunt noise current of the active inductor at f_R is expected to be

$$i_n = \sqrt{4kT\left(K_{NF2}G_{M2} + \frac{\omega_R^2}{\omega_R^2}K_{NF1}G_{M1}\right)} = 10.2 \text{ pA}/\sqrt{\text{Hz}} \tag{2.75}$$

very close to the simulation results of 10.51 pA/Hz$^{1/2}$ shown in Fig. 2-33 (Panel 2).

Per Eq. (2.51), the noise voltage across the active inductor port is the equivalent shunt noise current times the port impedance. This is confirmed by the noise simulation results of the prototype active inductor shown in Fig. 2-34. $i_{n,o}$ (A/Hz$^{1/2}$) is the equivalent shunt noise current measured across the two terminals, V_{oa} and V_{ob}, using a current probe. Mag(Z_{in}) is the magnitude of Z_{in} measured across terminals V_{oa} and V_{ob}. It is found that the equivalent output noise voltage, $v_{n,o}$ (V/Hz$^{1/2}$), completely overlays the product of mag(Z_{in}) and $i_{n,o}$, as predicted by Eq. (2.51).

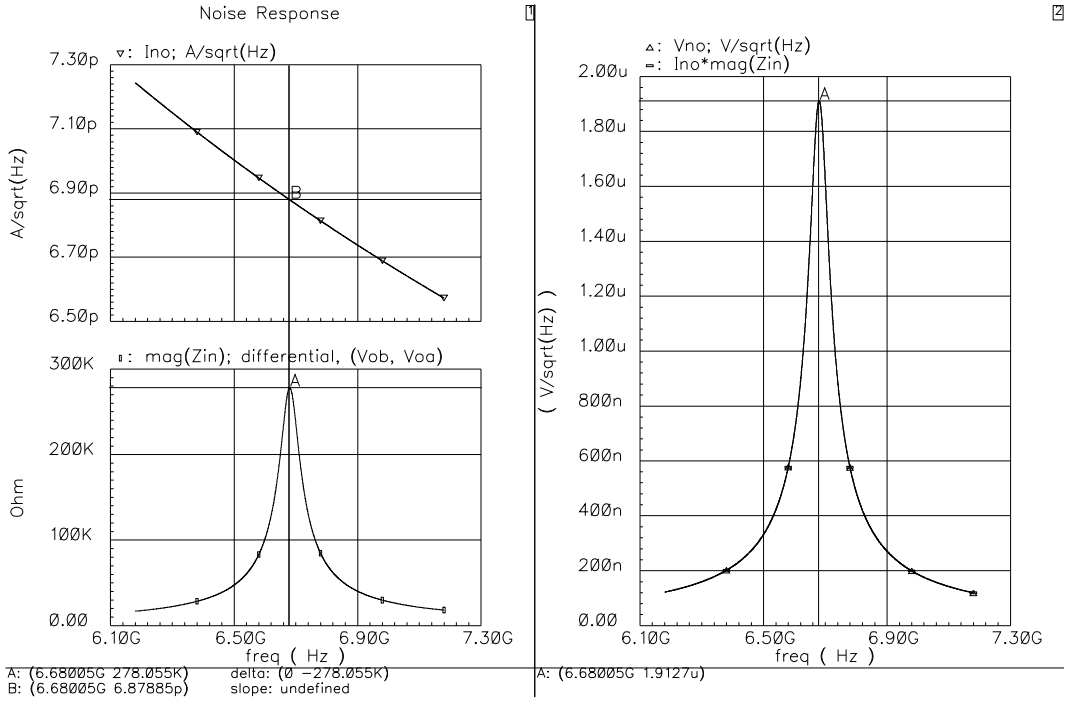


Figure 2-34 The noise of the active inductor shown in Fig. 2-29.

Table 2-2 All-NMOS active inductor noise summary

Parameter	Unit	Sims	Calc'ed	Equation
GammaN		0.8786		(2.73)
GammaP		0.9685		(2.73)
KNF1		3.6942		(2.69)
KNF2		1.8471		(2.71)
G_{M1}	mS	1.14		Tab(2.1)
G_{M2}	mS	1.15		Tab(2.1)
$i_{no,gm1}$	pA/sqrt(Hz)	6.47	7.82	(2.74)
$i_{no,gm2}$	pA/sqrt(Hz)	5.89	5.53	(2.74)
$i_{n,o1}$	pA/sqrt(Hz)	10.51	10.24	(2.75)
$i_{n,o}$	pA/sqrt(Hz)	6.88	7.24	(2.65)
Z_{in} (between Voa and Vob)	kOhm	278.0	273.3	(2.62)
$v_{n,o}$	uV/sqrt(Hz)	1.91	1.98	(2.51)
All at f_R = 6.68 GHz				

Table 2-2 summarizes the all-NMOS active-inductor noise simulation and calculated results. The Z_{in} is about twice that of the value in Table 2-1, because it is taken differentially here between V_{oa} and V_{ob}. The calculated results match the

simulation results.

2.8 All-NMOS-II Active-Inductor Circuit (New in This Work)

This circuit was initially developed as a precision analog signal driver, with a constant unity gain and very high linearity. But when configured differently, it can be an active inductor with an all-NMOS signal path and hence was designated "all-NMOS-II active inductor". It has the same high-frequency capability of the previous circuit with a 1.414 times improvement in f_R.

2.8.1 The Circuit as a Precision Analog Signal Driver

The primary circuit is shown in Fig. 2-35. $M_{B1\text{-}3}$ are biasing transistors acting as current sources. M_{B1} and M_{B2} are matched, and M_{B3} can be different depending on the application requirement. For reasons we will see below, M_{B1} and M_{B2} have almost identical V_{ds}s with low dynamic variation, hence cascode is not necessary to ensure their I_{DS} match. And we will find that the g_{ds} of M_{B3} does not affect the circuit's performance and hence cascode is not necessary on M_{B3} either. M_1 and M_2 have identical aspect ratios and their W and L are chosen based on the requirements on the maximum operating frequency and V_{IN}-V_{OUT} dc mismatch.

M_3 and M_4 have identical length, which is chosen based on frequency requirement and process variation, and their widths are chosen according to

$$\frac{W_{M4}}{W_{M3}} = \frac{I_1 + I_2}{I_3} = \frac{2I_1}{I_3} \tag{2.76}$$

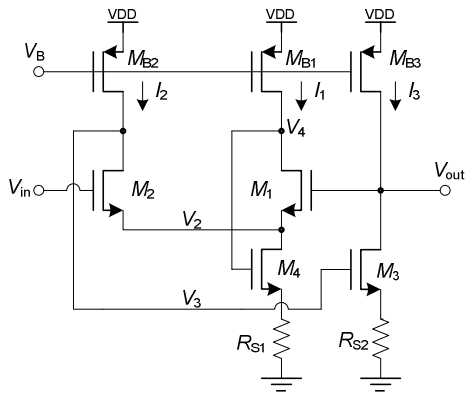


Figure 2-35 The all-NMOS-II circuit configured as a precision analog signal driver.

The source degeneration resistors R_{S1} and R_{S2} are optional, and merely create an extra degree of freedom in the circuit design. R_{S1} raises the source voltage of M_4 by a fixed amount, and R_{S2} degenerates M_3 and reduces the capacitance looking into the M_3 gate. Their values are chosen to satisfy

$$R_{S1}\left(I_1 + I_2\right) = R_{S2} I_3 \quad \text{or} \quad V_{S4} = V_{S3} \tag{2.77}$$

Therefore,

$$V_3 = V_{gs3} + V_{S3} = V_{gs4} + V_{S4} = V_4 \tag{2.78}$$

Since M_1 and M_2's sources are connected to the same node V_2, we have two desired outcomes at the same time:

$$V_{ds1} = V_{ds2} \quad \text{and} \quad V_{ds,MB1} = V_{ds,MB2} \tag{2.79}$$

The latter fulfills our identical V_{ds} assumption on M_{B1} and M_{B2} above and makes $I_1 = I_2$, since M_{B1} and M_{B2} have the same geometry and V_{GS}. The former, together with

$$I_{d,M1} = I_{d,M2},\ V_{t,M1} = V_{t,M2},\ W_{M1} = W_{M2},\ L_{M1} = L_{M2} \tag{2.80}$$

yields

$$V_{gs,M1} = V_{gs,M2},\ \text{or}\ V_{gs1} = V_{gs2} \tag{2.81}$$

after simplifying the notation. This is guaranteed by the feedbacks within the circuit, of course, since V_{gs} controls I_d and I_d does not control V_{gs}. Since

$$V_{in} - V_2 = V_{gs2}, \quad V_{out} - V_2 = V_{gs1} \tag{2.82}$$

we have

$$V_{in} = V_{out} \tag{2.83}$$

and this is enforced by the feedback through M_3.

Assuming that when the circuit is in dynamic operation, V_{in} increases by ΔV_{in} (> 0), and consequently V_{out} and V_2 both increase by (approximately) ΔV_{in}. Using the MOSFET I-V equation, when their I_{DS}'s are constant[4], the V_{gs} change of M_3 and M_4 from their V_{ds} change through the channel-length modulation effect is solved as

$$\frac{dV_{gs}}{dV_{ds}} = \frac{d\left(V_T + V_{od}\right)}{dV_{ds}} = -\frac{\lambda V_{od}}{2\left(1+\lambda V_{ds}\right)} \approx -\frac{\lambda V_{od}}{2} = -\frac{g_{ds}V_{od}}{2I_{ds}} \tag{2.84}$$

Note that λ is a very small number, and hence dV_{gs}/dV_{ds} is very small. Since M_3 and M_4 have identical V_{od} and λ, they have the identical V_{gs} change of

$$\Delta V_{gs3,4} = \Delta V_3 = \Delta V_4 \approx -\frac{\lambda V_{od3}}{2}\Delta V_{in} \tag{2.85}$$

again, a very small number. The V_{ds} changes for M_1 and M_2 will be

$$\begin{aligned} \Delta V_{ds1} &= \Delta V_4 - \Delta V_2 \approx -\frac{\lambda V_{od4}}{2}\Delta V_{in} - \Delta V_{in} = -\Delta V_{in}\left(1+\frac{\lambda V_{od4}}{2}\right) \\ \Delta V_{ds2} &= \Delta V_3 - \Delta V_2 \approx -\frac{\lambda V_{od3}}{2}\Delta V_{in} - \Delta V_{in} = -\Delta V_{in}\left(1+\frac{\lambda V_{od3}}{2}\right) = \Delta V_{ds1} \end{aligned} \tag{2.86}$$

[4] The I_{DS}'s of M_3 and M_4 will change slightly due to the channel-length modulation effect on $M_{B1\text{-}3}$ that is determined by the solution of the next few equations. This has very little effect and is neglected to simplify the discussion.

ΔV_3 and ΔV_4, both < 0, will increase I_1 and I_2 slightly by the same amount through the channel-length modulation of M_{B1} and M_{B2}, and ΔV_{ds1} and ΔV_{ds2}, both <0, will increase V_{gs1} and V_{gs2} slightly by the same amount. Per Eq. (2.82),

$$\begin{aligned}\Delta\left(V_{out}-V_{in}\right)&=\Delta\left[\left(V_2+V_{gs1}\right)-\left(V_2+V_{gs2}\right)\right]=\Delta\left(V_{gs1}-V_{gs2}\right)\\&=\Delta\left(\Delta V_{gs1}-\Delta V_{gs2}\right)=0\end{aligned} \tag{2.87}$$

Hence, the 2nd-order effects of MOSFETs have no direct effect on $\Delta(V_{out} - V_{in})$. The 2nd-order effects are repeatedly subtracted from each other before they reach $\Delta(V_{out} - V_{in})$, that is

$$A_V=\frac{dV_{out}}{dV_{in}}=\frac{d}{dV_{in}}\left(V_{gs1}-V_{gs2}+V_{in}\right)=\frac{d}{dV_{in}}\left(V_{gs1}-V_{gs2}\right)+1=1 \tag{2.88}$$

Therefore, we have $V_{out} = V_{in}$ and $\Delta V_{out} = \Delta V_{in}$, and three interesting results ensue:

1. The dc (or common-mode) voltages V_{OUT} and V_{IN} are the same, less the V_T mismatch between M_1 and M_2.
2. $\Delta V_{out} = \Delta V_{in}$ and the gain is equal to 1.0. V_T mismatches have no direct impact on the gain (Eq. 2.85) and consequently the gain is constant across process-temperature corners.
3. Since V_{out} follows V_{in} exactly, the small-signal linearity (*IIP3*) is high and the linearity is preserved over a wide input signal range.

2.8.2 Analysis using Feedback Theory

The constant gain and high linearity of the circuit may also be explained using the

feedback theory. Considering small signals only, the drain current of M_1 is $g_{m1}(V_{out} - V_2)$, and it is converted into voltage V_4 by multiplying the total conductance looking into node V_4, g_4. V_4 is further transferred to V_2 by $g_{m4}/(g_{m1}+g_{m2})$, as shown by the block diagram in Fig. 2-36:

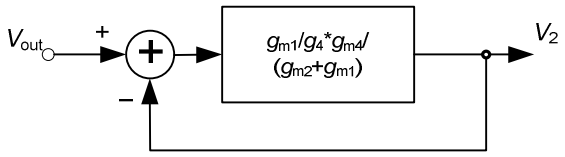


Figure 2-36 The local feedback loop within the circuit.

The transfer function is

$$\frac{V_2}{V_{out}} = \left.\frac{\frac{g_{m1}}{g_4}\frac{g_{m4}}{g_{m1}+g_{m2}}}{1+\frac{g_{m1}}{g_4}\frac{g_{m4}}{g_{m1}+g_{m2}}}\right|_{V_{od1}=V_{od2}\approx V_{od4}\text{, and Eq(2.67)}} \approx \frac{\frac{g_{m1}}{g_4}\frac{2g_{m1}}{g_{m1}+g_{m1}}}{1+\frac{g_{m1}}{g_4}\frac{2g_{m1}}{g_{m1}+g_{m1}}} = \left.\frac{\frac{g_{m1}}{g_4}\cdot 1}{1+\frac{g_{m1}}{g_4}\cdot 1}\right|_{g_{m1}/g_4>>1} \approx 1 \quad (2.89)$$

Next V_{in} and V_2 are subtracted by M_2, whose drain current is converted into the voltage V_3 by the total conductance looking into node V_3, g_3, and V_3 is transferred to V_{out} by g'_{m3}/g_{out} ($g'_{m3} = g_{m3}/(1+ g_{m3}R_{S2})$ is g_{m3} with the degeneration effect of R_{S2}). g_{out} is the total conductance looking into node V_{out}. This process can be represented by the diagram in Fig. 2-37:

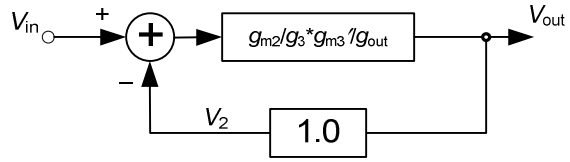


Figure 2-37 The main feedback loop within the circuit.

Its transfer function is

$$A_V = \left.\frac{g_{m2}g'_{m3}/(g_3 g_{out})}{1+1\cdot g_{m2}g'_{m3}/(g_3 g_{out})}\right|_{\frac{g_{m2}g'_{m3}}{g_3 g_{out}}>>1} \approx 1 \quad (2.90)$$

The loop gain of the main feedback is $\propto (g_m/g_{ds})^2$, that is, very high; the local feedback loop gain is $\propto (g_m/g_{ds})$ and lower, but sufficient. The voltage gain of the circuit is 1 because the feedback factors of the two loops are both 1, determined by the circuit architecture, not by component matching, and the high loop gain ensures that the voltage gain is constant with process, temperature variations, and device mismatches.

2.8.3 AC Small-Signal Analysis

For this circuit, we may of course draw the entire ac equivalent circuit and conduct a symbolic circuit analysis. However, due to the high number of parasitic capacitors, the transfer function will be high-order and the mathematics will be too complex to bring any design insights. Therefore, we will break the circuit into functional blocks with unilateral signal transfer functions, and judiciously neglect parasitic terms in the circuit equations.

The circuit is decomposed into three blocks: voltage transfer block from V_{out} to V_2; M_2 as a noninverting transconductor with input being V_2 and output at V_3; M_3 as a source-degenerated inverting transconductor with input being V_3 and output at V_{out}. The ac small-signal equivalent circuit of the voltage transfer block is shown in Fig. 2-38, where $1/g_{m2}$ is the resistance looking into the M_2 source and is the load of the block, g_4 and C_4 are the parasitic conductance and capacitance at V_4, respectively. From the node equations for V_4 and V_2, we solve the transfer function as[5]

[5] The circuit is assumed to be driven by a voltage source with zero source impedance, a reasonable and acceptable assumption for this circuit, since the capacitive loading effect of the M_2 gate to the M_3 drain is considered in the following analysis.

$$T(s)=\frac{V_2}{V_{\text{out}}}=\frac{s^2+s\frac{g_{\text{m1}}}{C_{\text{gs1}}}+\frac{g_{\text{m1}}g_{\text{m4}}}{C_{\text{gs1}}C_4}}{s^2+s\frac{2g_{\text{m1}}}{C_{\text{gs1}}}+\frac{g_{\text{m1}}g_{\text{m4}}}{C_{\text{gs1}}C_4}} \tag{2.91}$$

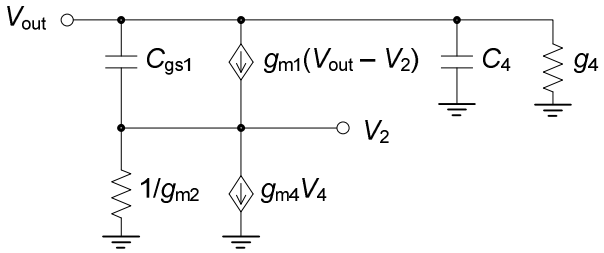


Figure 2-38 Small-signal equivalent circuit from V_{out} to V_2.

Its pole frequency and Qs are

$$\omega_{\text{p1}}=\sqrt{\frac{g_{\text{m1}}g_{\text{m4}}}{C_{\text{gs1}}C_4}},\quad Q_{\text{p1}}=\frac{1}{2}\sqrt{\frac{g_{\text{m4}}C_{\text{gs1}}}{g_{\text{m1}}C_4}},\quad Q_{\text{z1}}=\sqrt{\frac{g_{\text{m4}}C_{\text{gs1}}}{g_{\text{m1}}C_4}}=2Q_{\text{p1}} \tag{2.92}$$

ω_{p1} is the ratio of transistor g_{m} to parasitic capacitor, and as we shall see later, is much larger than the pole frequency of the whole circuit, which contains the large load capacitor at V_{out}. Q_{p1} and Q_{z1} are both fairly low for practical circuits ($Q_{\text{p1}} \approx 1$ in most cases). Therefore, within the frequency range of interest, it operates almost like a unity-gain filter, that is

$$T(s)=\frac{V_2}{V_{\text{out}}}=\frac{s^2+s\frac{g_{\text{m1}}}{C_{\text{gs1}}}+\frac{g_{\text{m1}}g_{\text{m4}}}{C_{\text{gs1}}C_4}}{s^2+s\frac{2g_{\text{m1}}}{C_{\text{gs1}}}+\frac{g_{\text{m1}}g_{\text{m4}}}{C_{\text{gs1}}C_4}}\approx 1,\ \text{or } V_2=V_{\text{out}} \tag{2.93}$$

The Q_{p1} and Q_{z1} difference of a factor of 2 will distort the frequency profile a little bit, but will have little effect since ω_{p1} is much higher than the circuit's operating frequency and Q_{p1} and Q_{z1} are both low.

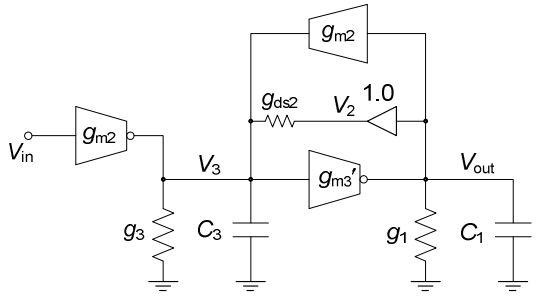


Figure 2-39 Small-signal equivalent circuit of the entire circuit.

Using this result, the small-signal equivalent of the entire circuit is drawn in Fig. 2-39. g_{m2} is the g_m of M_2 and g'_{m3} is the g_m of M_3 degenerated by R_{S2}:

$$g_{m3}' = \frac{g_{m3}}{1 + g_{m3}R_{S2}} \tag{2.94}$$

The unity-gain buffer on g_{ds2} in the figure is from the unilateral isolation effect of M_1 and M_4 for V_{out}, that is, V_2 ($\approx V_{out}$) can generate current into V_3 through g_{ds2}, but the current generated by V_3 through g_{ds2} into V_2 is totally sunk without affecting V_2 since V_2 is low-impedance.

Since the impedance looking into the M_3 gate is very high and g_{ds2} has been taken into account separately, we have

$$g_3 \approx g_{ds,MB2} \tag{2.95}$$

Using a simple small-signal analysis, the capacitance looking into M_3 gate with source-degeneration resistor R_{S2} is

$$C_{gs3}' = \frac{C_{gs3}}{1 + R_{S2}\left(sC_{gs3} + g_{m3}\right)} \approx \frac{C_{gs3}}{1 + R_{S2}g_{m3}} \tag{2.96}$$

because at the circuit's pole frequency, $|sC_{gs3}| << g_{m3}$, typically at about 1%.

C_3, the total capacitance at node V_3, is the sum of junction capacitance and C_{gs3}',

$$C_3 = C_{\text{jd,MB2}} + C_{\text{jd2}} + \frac{C_{\text{gs3}}}{1 + R_{\text{S2}} g_{\text{m3}}} \tag{2.97}$$

C_1 and g_1 are the total capacitance (mostly the load capacitor) and conductance at node V_{out}, and they are

$$C_1 = C_{\text{L}} + C_{\text{jd3}} + C_{\text{jd,MB3}}, \quad g_1 = g_{\text{ds,MB3}} + \frac{1}{R_{\text{S2}} + \left(1 + g_{\text{m3}} R_{\text{S2}}\right) / g_{\text{ds3}}} \tag{2.98}$$

Using node analysis, the transfer function of the circuit can be solved as

$$T(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{g_{\text{m2}} g'_{\text{m3}}}{C_1 C_3}}{s^2 + s\left(\frac{g_1}{C_1} + \frac{g_3 + g_{\text{ds2}}}{C_3}\right) + \frac{(g_{\text{m2}} + g_{\text{ds2}}) g'_{\text{m3}} + g_1 (g_3 + g_{\text{ds2}})}{C_1 C_3}} \tag{2.99}$$

$T(s)$ is recognized as a lowpass function, with pole frequency, pole Q, and dc gain being

$$\omega_{\text{p}} = \sqrt{\frac{(g_{\text{m2}} + g_{\text{ds2}}) g'_{\text{m3}} + g_1 (g_3 + g_{\text{ds2}})}{C_1 C_3}} \approx \sqrt{\frac{g_{\text{m2}} g'_{\text{m3}}}{C_1 C_3}}, \quad Q_{\text{p}} = \frac{\omega_{\text{p}}}{\frac{g_1}{C_1} + \frac{g_3 + g_{\text{ds2}}}{C_3}},$$
$$H_0 = \frac{g_{\text{m2}} g'_{\text{m3}}}{(g_{\text{m2}} + g_{\text{ds2}}) g'_{\text{m3}} + g_1 (g_3 + g_{\text{ds2}})} \approx \frac{g_{\text{m2}} g'_{\text{m3}}}{g_{\text{m2}} g'_{\text{m3}}} = 1 \tag{2.100}$$

2.8.4 Design Example

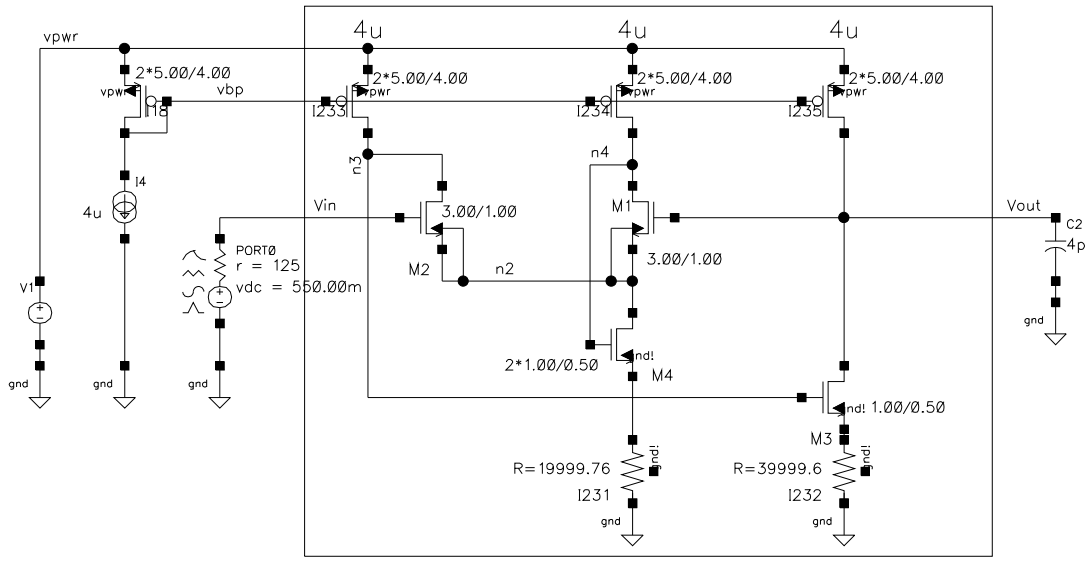


Figure 2-40 Example of All-NMOS-II circuit configured as an analog signal driver.

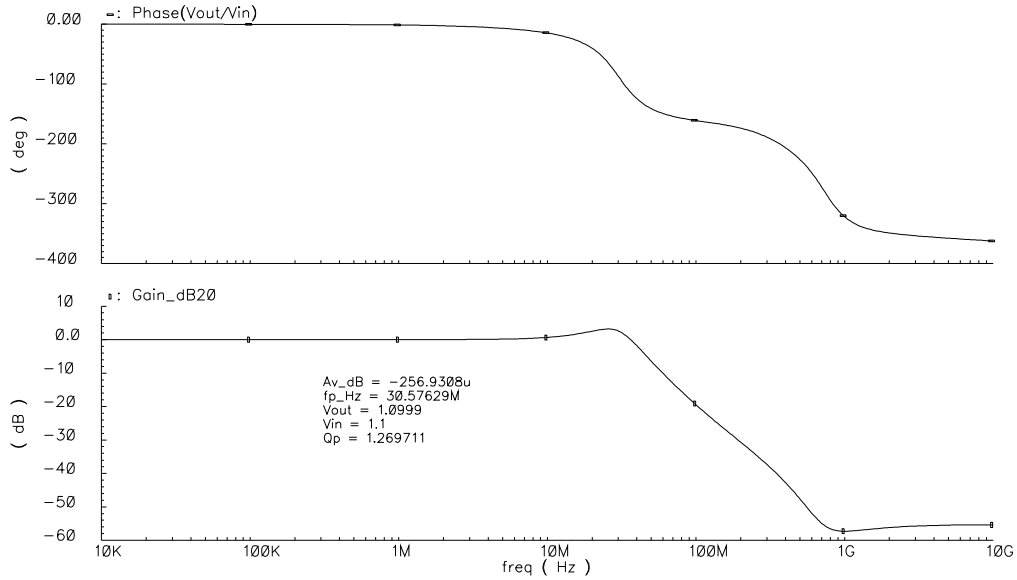


Figure 2-41 The frequency response of the analog signal driver.

Figure 2-40 shows an example of the circuit as an analog signal driver, designed in a submicron CMOS process. As expected, V_{IN} and V_{OUT} are identical. The gain is –0.26 mdB, and the pole frequency and Q are 30.6 MHz and 1.27, respectively, at a 4-pF load. To verify the circuit equations, equivalent-circuit-component parameters are

obtained from the operating points: g_{m2} = 65.32 μS, g_{m3} = 51.96 μS, C_1 = 4.003 pF, C_3 = 8 fF, g_{ds2} = 1.11 μS, $g_{ds,MB2}$ = 80 nS, $g_{ds,MB3}$ = 90 nS, g_{ds3} = 0.48 μS, R_{S2} = 40 kΩ. Using these, we can calculate g_1 = 0.245 μS, g_3 = 80 nS, g_{m3}' = 16.88 μS. Plugging these into Eq. (2.95), we get f_p = 29.8 MHz, Q_p = 1.26, H_0 = 0.98, very close to the simulation results. H_0 is more pessimistic because the cancellation of MOSFET second-order effects discussed in Section 2.8.1 is not included in the small-signal circuit model in Fig. 2-37 for simplicity. The simulation and calculated results are summarized in Table 2-3.

Table 2-3 Calculated versus simulated results for the All-NMOS-II circuit when used an analog signal driver or lowpass filter

Parameter	Unit	Value	Equation	Parameter	Unit	Sims	Calc'ed	Equation
g_{m1}	uS	65.31		f_p	MHz	**30.58**	**29.8**	(2.98)
g_{m2}	uS	**65.32**		Q_p		**1.27**	**1.26**	(2.98)
g_{m3}	uS	**51.96**		H_0		**1.00**	**0.98**	(2.98)
C_1	pF	**4.003**	(2.98)					
C_3	fF	**8**	(2.97)	V_{DD}	V	**1.8**		
g_{ds2}	uS	**1.11**		ΔV_{in} (gain varies by 1%)	mV	**570**		
$g_{ds,MB1}$	nS	80		IIP3	Vp	**39.5**		
$g_{ds,MB2}$	nS	80						
$g_{ds,MB3}$	nS	90						
g_{ds3}	uS	0.48						
R_{S2}	kOhm	40						
g_1	uS	**0.245**	(2.98)					
g_3	nS	**80**	(2.95)					
g'_{m3}	uS	**16.88**	(2.94)					

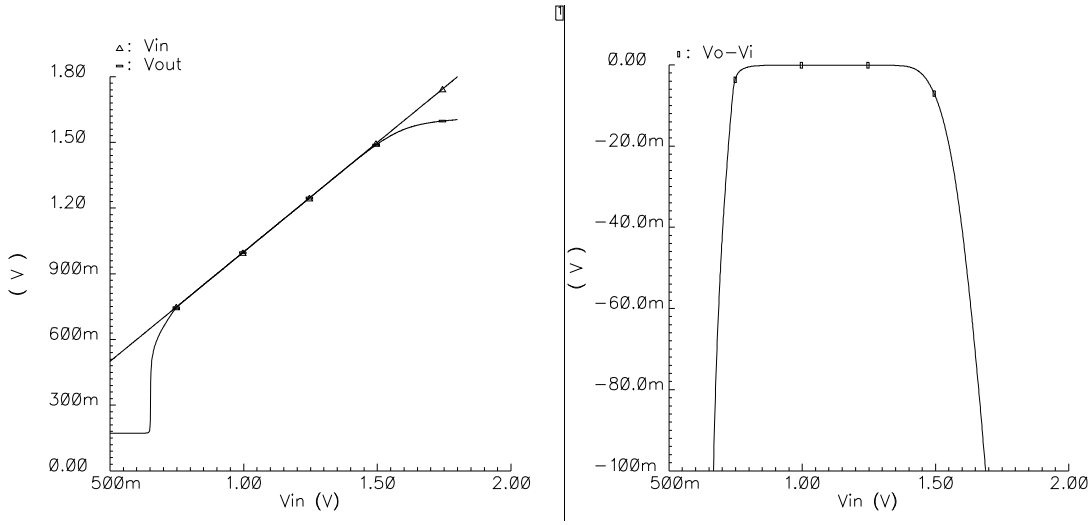


Figure 2-42 dc characteristics of the analog signal driver.

Figure 2-42 shows the dc characteristics of the circuit. The 1% dc gain-variation range is about 570 mV at 1.8-V supply, and V_{out} tracks V_{in} closely. To examine the linearity from another aspect, Fig. 2-43 shows the IIP3 of the circuit, which is 32 dBVp or 39.5 Vp, a very high number for a CMOS circuit at 1.8 V.

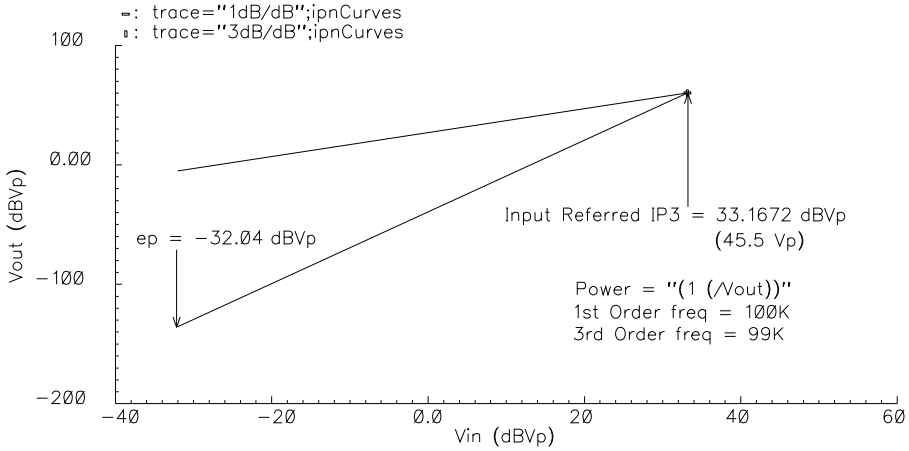


Figure 2-43 The IIP3 of the circuit is 33 dBVp or 45.5 Vp, at 1.8 V power supply, single-ended.

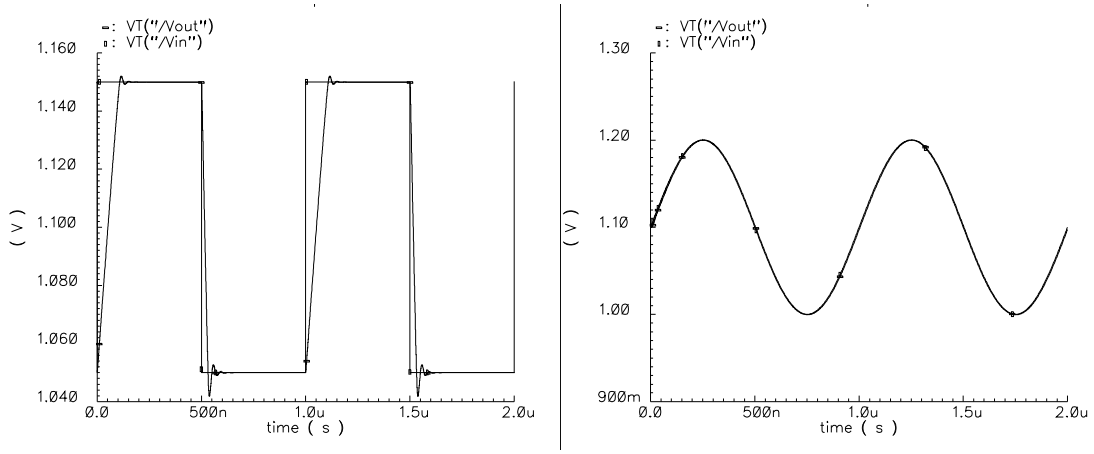


Figure 2-44 Transient simulation of the circuit, sinusoidal and pulse input.

Figure 2-44 shows the transient simulations of the circuit, for a sinusoidal input and a pulse input, both at 1 MHz. The sinusoidal output is almost an exact replica of the input; the rise time of the pulse output, however, is limited by the circuit's slew rate,

$$SR_{\text{rising}} = \frac{dV_{\text{out}}}{dt} = \frac{I_3}{C_{\text{L}}} \tag{2.101}$$

The slew rate can be increased by increasing I_3 for a given load. I_1 (= I_2) can be kept unchanged to be more power efficient. The fall-time slew rate is primarily determined by the source-degeneration resistor R_{S2}, and unlike SR_{rising}, is not constant with respect to V_{out},

$$SR_{\text{falling}} = \frac{dV_{\text{out}}}{dt} \approx \frac{V_{\text{out}}/R_{\text{S2}}}{C_{\text{L}}} = \frac{V_{\text{out}}}{R_{\text{S2}}C_{\text{L}}} \tag{2.102}$$

The equation is exact when $V_{\text{out}} = V_{\text{OUT}}$. When $R_{\text{S2}} = 0$, SR_{falling} is indeed only limited by the intrinsic R_{S} and R_{D} of M_3 and could be very large. The sinusoidal signal is also subject to the slew rate limitation, of course, albeit at a higher amplitude.

To verify the circuit's robustness, Monte Carlo simulation results are shown in

Fig. 2-45. The 6-σ gain variation range is only about 1.8 mdB, due to the dual feedback loops discussed above. The dc voltage mismatch, $V_{OUT} - V_{IN}$, is larger, with a 6-σ range of 19 mV, i.e., V_{OUT} could deviate as far as $V_{IN} \pm 9.5$ mV, due to the V_{TH} mismatch in M_1 and M_2, which differs from process to process. The mismatch can be reduced by increasing M_1 and M_2's W and L proportionally, with low impact to circuit f_p, since f_p is mainly limited by C_L, not the parasitic capacitors. The 6-σ variation range of f_p is 30.6 MHz ± 0.57 MHz, or 3.7% of f_p. The frequency profile of the gain is stable against process variations.

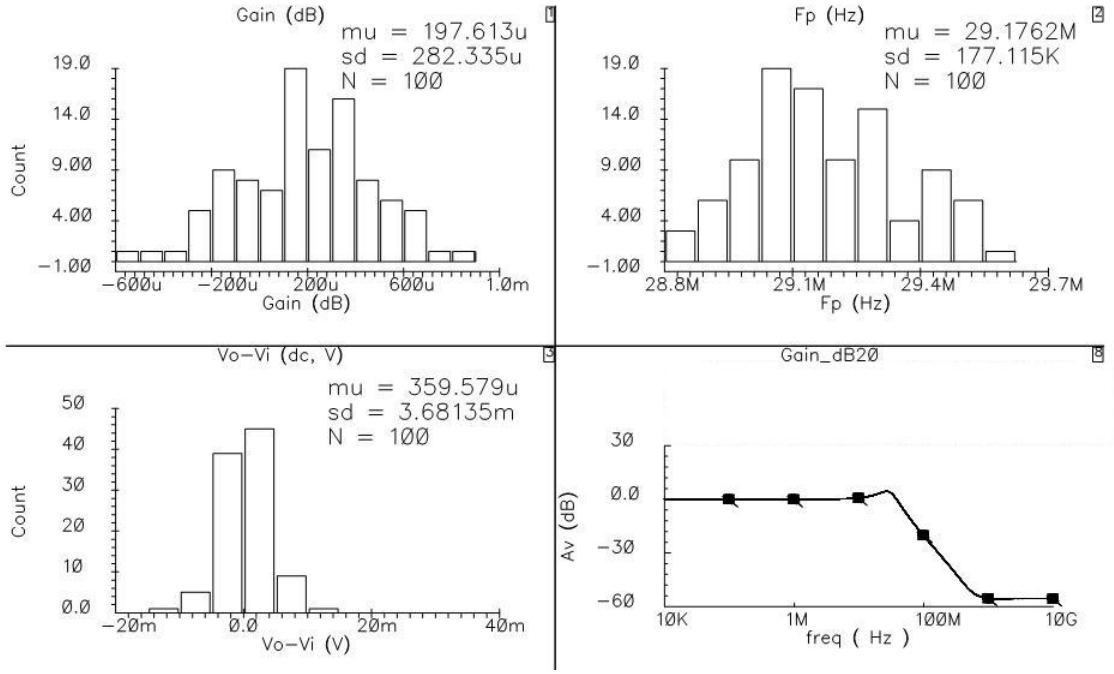


Figure 2-45 Monte Carlo simulation results.

2.8.5 The all-NMOS-II Circuit Configured as an Active Inductor

The all-NMOS-II circuit can be configured as an active inductor, as shown in Fig. 2-46, by connecting the gate of M_2 to a common-mode voltage V_{CM}, and using V_1 as

input port. Per the previous analysis, V_2 replicates V_1, thus M_2 becomes a non-inverting G_M, with input at V_2 and output at V_3. M_3, degenerated by the optional R_{S2}, is an inverting G_M, with input at V_3 and output at V_1. Thus a gyrator is obtained, converting the parasitic capacitor C_3 at node V_3 into an equivalent inductor at V_1, as shown by Fig. 2-47.

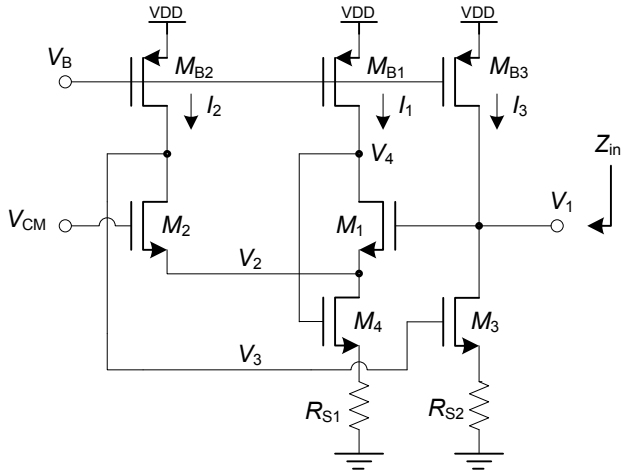


Figure 2-46 The all-NMOS-II circuit configured as an active inductor.

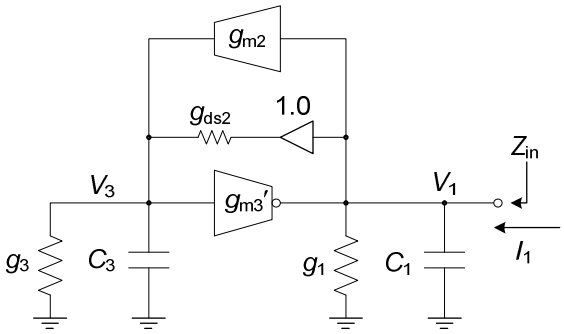


Figure 2-47 Small-signal equivalent circuit of the all-NMOS-II active inductor.

The small-signal elements are the same as in the above analysis. The input impedance Z_{in} can be obtained through circuit analysis:

$$Z_{in}(s)=\frac{V_1}{V_1}=\frac{\frac{s}{C_1}+\frac{g_3+g_{ds2}}{C_1C_3}}{s^2+s\left(\frac{g_1}{C_1}+\frac{g_{ds2}+g_3}{C_3}\right)+\frac{(g_{m2}+g_{ds2})g_{m3}'+g_1(g_{ds2}+g_3)}{C_1C_3}} \tag{2.103}$$

Compared with the format of Eq. (2.7), Z_{in} is recognized as the input impedance

of an *R*-*L*-*C* network, as shown in Fig. 2-27(b). At dc ($s = 0$), we have

$$r_s = \frac{g_3 + g_{ds2}}{(g_{m2} + g_{ds2})g_{m3}' + g_1(g_{ds2} + g_3)} \approx \frac{g_3 + g_{ds2}}{g_{m2}g_{m3}'} \tag{2.104}$$

As $s \to \infty$, we have

$$\lim_{s\to\infty} Z_{in}(s) = \frac{1}{sC_1} \tag{2.105}$$

Hence the shunt capacitor is

$$C_P = C_1 \tag{2.106}$$

Using the pole (self-resonance) frequency,

$$\omega_R = \sqrt{\frac{(g_{m2} + g_{ds2})g_{m3}' + g_1(g_{ds2} + g_3)}{C_1C_3}} \approx \sqrt{\frac{g_{m2}g_{m3}'}{C_1C_3}} \tag{2.107}$$

the equivalent inductor can be calculated as

$$L_{eq} = \frac{1}{\omega_R^2 C_1} = \frac{C_3}{(g_{m2} + g_{ds2})g_{m3}' + g_1(g_{ds2} + g_3)} \approx \frac{C_3}{g_{m2}g_{m3}'} \tag{2.108}$$

The quality factor at ω_R is

$$Q_R = \frac{\omega_R}{\frac{g_1}{C_1} + \frac{g_{ds2}+g_3}{C_3}} \tag{2.109}$$

Using Eq. (2.8), the shunt resistance is calculated as

$$R_p \approx \frac{1}{g_1 + \frac{C_1}{C_3}(g_{ds2} + g_3)} \tag{2.110}$$

To appreciate the higher ω_R of the all-NMOS-II active inductor, we compare Eqs. (2.107) and (2.55), and find that the all-NMOS-II circuit's f_R is 1.414 times that of the all-NMOS circuit. The reason is that due to the local feedback introduced by M_4

in Fig. 2-45, V_2 is no longer approximately $0.5V_1$, but equal to V_1. Thus, the noninverting transconductor, G_{M1}, implemented by M_2, is doubled. Note that this frequency enhancement does not increase the circuit's power dissipation, because M_4 will exist as a biasing FET in the circuit anyway. The insertion of M_{B1} does not require extra current or a V_{dd} increase; it merely shares part of the more than sufficient V_{ds} of M_1 in the all-NMOS circuit.

This voltage segmentation technique is sometimes dubbed "current recycling" in the industry. From another aspect, V_{DD} and I_{DD} are both resources, and can be broken down into a matrix, as shown in Fig. 2-48. The more devices we can fit into a given dimension set by V_{DD} and I_{DD}, the more functionality and/or performance we can potentially obtain. The vertical size of the matrix is determined by V_{DD} and device V_{TH}s. The horizontal size is determined by I_{DD} and specific technology. The current per column cannot be infinitely reduced, when technology constraints, parasitic capacitance, and device matching are considered. Of course, we should not add a device just to "patch a hole" in the matrix without serving a useful purpose, as it is going to introduce parasitic elements and degrade the circuit performance. However, by inspecting a circuit for "holes" in the matrix, we can quickly locate places where a device may be introduced without increasing I_{DD}.

As a very important side benefit obtained from the insertion of M_{B1}, the drain voltages of M_1 and M_2 are now equal, and this is the key reason for the high linearity of the circuit when used as an analog signal driver.

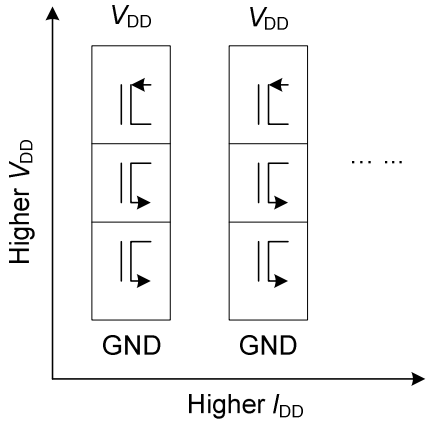


Figure 2-48 Lateral and vertical development of analog circuits.

2.8.6 Example of the all-NMOS-II Active Inductor Circuit

An all-NMOS-II active inductor example is shown in Fig. 2-49. All MOSFETs are kept at the same operating point, but the 4-pF load capacitor is separated into two parts at V_1 and V_3. The ac simulation results are shown in Fig. 2-50.

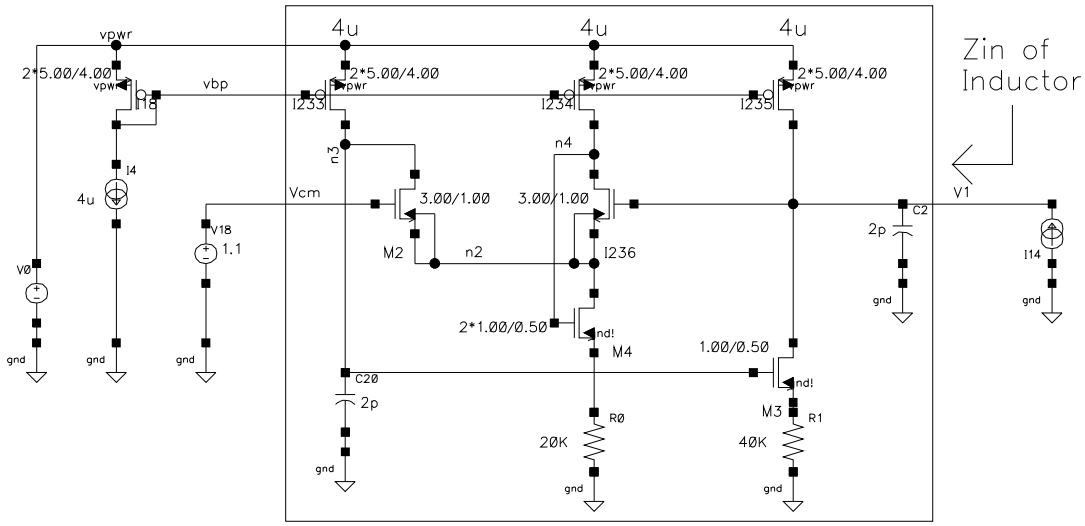


Figure 2-49 The all-NMOS-II circuit configured as an active inductor.

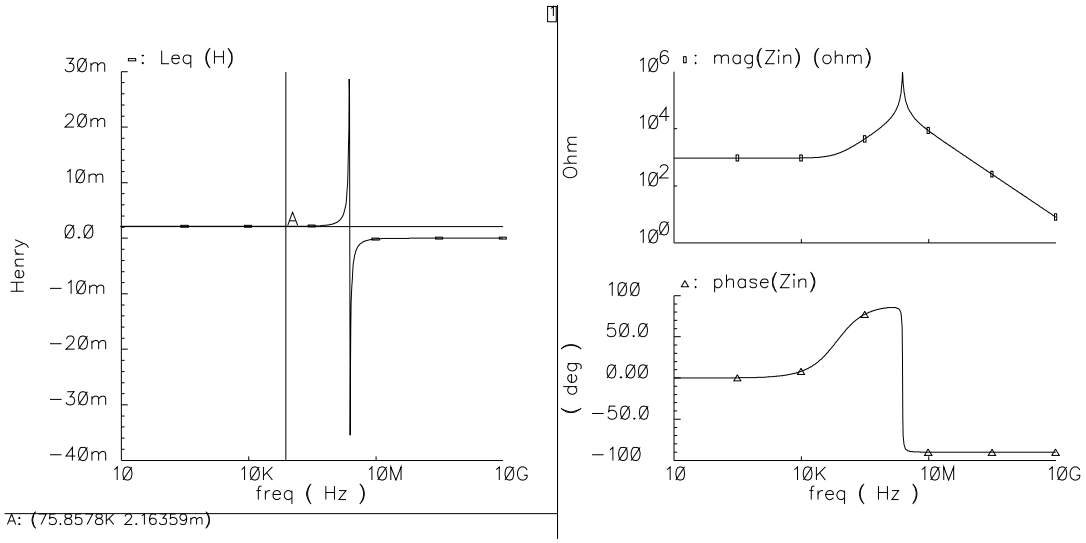


Figure 2-50 Example ac simulation results of the all-NMOS-II active inductor.

The component values of the equivalent circuit are extracted from the operating point: g_{m2} = 65.32 μS, g_{m3} = 51.96 μS, C_1 = 2.017 pF, C_3 = 2.007 pF, g_{ds2} = 1.11 μS, g_3 = 80 nS, g_1 = 0.245 μS, R_{S2} = 40 kΩ. Using the above equations, the circuit parameters are calculated as f_R = 2.65 MHz, Q_R = 23.3, L_{eq} = 1.79 mH, r_s = 1.06 kΩ, very close to the simulated results shown in Fig. 2-50. The results are summarized in Table 2-4.

It is noted that when C_1 and C_3 are reduced to the parasitic capacitance of the devices and layout in order to obtain very high operating frequencies, the design for a certain Q_R becomes less straightforward than the above equations appear to indicate, because the parasitic pole and zero frequencies of the $V_1 \rightarrow V_2$ transfer function of the M_4 and M_1 local feedback loop, as given by Eq. (2.91), become close to the circuit f_R, and the phase shift of the noninverting G_M formed by M_2-M_1-M_4 modifies Q_R per section 2.5.3, Eq. (2.37).

Table 2-4 Calculated versus Simulated Results for the All-NMOS-II circuit when used as an active inductor

Parameter	Unit	Value	Equation	Parameter	Unit	Sims	Calc'ed	Equation
g_{m1}	uS	65.31		f_R	MHz	**2.42**	**2.65**	(2.107)
g_{m2}	uS	**65.32**		Q_R		**22.00**	**23.30**	(2.109)
g_{m3}	uS	**51.96**		L_{eq}	mH	**2.16**	**1.79**	(2.108)
C_1	pF	**2.017**	(2.98)	r_s	kOhm	**0.940**	**1.061**	(2.104)
C_3	pF	**2.007**	(2.97)	R_p	MOhm	**0.759**	**0.694**	(2.110)
g_{ds2}	uS	**1.11**						
$g_{ds,MB1}$	nS	80						
$g_{ds,MB2}$	nS	80						
$g_{ds,MB3}$	nS	90						
g_{ds3}	uS	0.48						
R_{S2}	kOhm	40						
g_1	uS	**0.245**	(2.98)					
g_3	nS	**80**	(2.95)					
g_{m3}'	uS	**16.88**	(2.94)					

2.9 Summary of the Active-Inductor Circuits

The active-inductor circuits discussed in this chapter are summarized in Table 2-5. The circuits can be classified into two types: those that are best used as an inductor, such as the load of the limiting amplifier in optic receivers; and those that are best used as a resonator, in obtaining high-Q bandpass filters or oscillators.

It shall be noted that in designing GHz filters, the circuits are not used to directly replace the inductors in prototype L-C filters, as this method cannot fully exploit the high-frequency potential of the active-inductor circuits, but rather directly or indirectly as a filter, after adding the necessary circuitry. This will be discussed in more detail in Chapter 3. When used as inductors, the active-inductor circuits are typically used as a load in wide-band pulse amplifiers and oscillators to mimic passive inductors.

Table 2-5 Summary of active-inductor circuits

Active Inductor	Section	Q_L	Q_R	Good for inductor	Good for resonator	typical application	Note
Gate-R and Gate-R-II	2.4.1	low to moderate	low	yes	no	wideband pulse amplifier	
Cascode Gate-R	2.4.2	low to moderate	low	yes	no	wideband pulse amplifier	
CG-CS	2.4.3	moderate to high	low	yes	no	wideband pulse amplifier	easy to bias
Cascode CG-CS	2.4.4	moderate to high	low	yes	no	wideband pulse amplifier	derived from CG-CS
CS-CD	2.4.5	moderate to high	low	yes	no	wideband/"low-noise" amplifier	
Cascode and Regulated Cascode	2.4.6	moderate to high	low	yes	no	wideband/"low-noise" amplifier	Derived from CS-CD, easy to bias
Differential-Pair	2.4.7	moderate to high	low	yes	yes	bandpass filters	very difficult to bias
Karsilayan's	2.4.8	moderate to high	high	yes	yes	bandpass/lowpass filters	easy to bias
All-NMOS (new in this work)	2.7	moderate to high	high	yes	yes	bandpass/lowpass filters	all-NMOS signal path, high f_R, easy to bias
all-NMOS-II (new in this work)	2.8	moderate to high	high	yes	yes	analog signal driver, voltage follower, lowpass filter	very high linearity

CHAPTER 3

DESIGN OF RF ANALOG FILTERS

3.1 Designing RF Analog Filters with Active Inductors

Analog filters can be constructed using active inductors and capacitors in ladder structures [10]. Since the active inductors are used as inductors, the filters will have to operate at frequencies well below (1-10%) the inductor self-resonance frequency f_R, so that the active inductors will behave as inductors rather than resonators. To obtain RF filters that operate near or at f_R, we will have to treat the active inductor as a resonator and use different methods.

3.1.1 Bandpass Filters

If floating active inductors are available, bandpass filters can be obtained by replacing the passive inductors in an *L-C* ladder bandpass filter with active inductors [10]. However, the bandpass filter's center frequency f_0 has to be much lower than the active inductors' self-resonance frequency f_R, because the active inductor will behave like an inductor only at frequencies much lower than f_R. To obtain the highest possible f_0, we may use the active inductor as a resonator, as shown in Fig. 3-1, where the *R-L-C* network is the equivalent circuit of an active inductor.

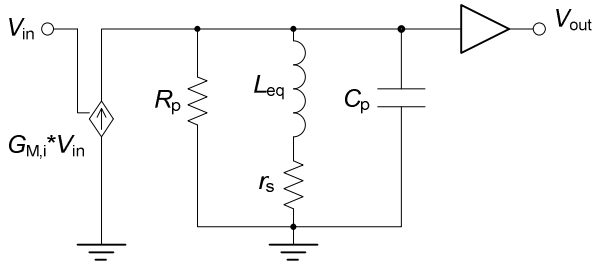


Figure 3-1 Constructing an HF active-inductor bandpass filter.

From Section 2.2 we know that the input impedance Z_{in} of an active inductor has a bandpass profile when Q_R is high (> 2) and r_s's effect at dc is ignored. Thus, when an input current is applied to Z_{in}, the voltage across the Z_{in} port will have a bandpass profile, too. A transconductor $G_{M,i}$ can be used to convert V_{in} into a current. A voltage follower is needed at the output to drive the resistive/capacitive load, preventing it from reducing the active inductor's f_R and/or Q_R. Real transconductors inevitably have an output capacitance C_o and leakage g_o, and the voltage follower has an input capacitance C_i. C_i and C_o can be absorbed by C_p, reducing f_R slightly, and g_o can be absorbed by R_p, reducing Q_R. Therefore, the parasitic elements of $G_{M,i}$ and the output buffer do not change the order or the function format of Z_{in}, but merely change its parameters to some extent. If the active inductor is designed with these parasitic elements included, the desired frequency and Q can be obtained.

Assuming that f_R becomes f_0 and Q_R becomes Q_0 after taking into account the parasitic elements, the bandpass filter transfer function is

$$T(s) = \frac{V_{out}}{V_{in}} = G_{M,i} Z_{in} = \frac{G_{M,i}\omega_0^2}{s^2 + s\frac{\omega_0}{Q_0} + \omega_0^2} \tag{3.1}$$

where the effect of r_s has been neglected. Including r_s, $T(0) = G_{M,i}*r_s \neq 0$, which can be neglected when Q_R is very high. The mid-band gain of the bandpass filter is

$$H_{\mathrm{M}} = G_{\mathrm{M,i}} \left(R_{\mathrm{p}} \parallel g_{\mathrm{o}} \right) \tag{3.2}$$

In practice, $G_{\mathrm{M,i}}$ may be implemented by a single FET or a differential pair; and the output buffer may be implemented by a source follower.

High-order filters may be constructed by cascading several of the 2nd-order bandpass filters shown in Fig. 3-1. For example, by tuning the f_0 and Q_0 of three filters properly, a maximally flat passband may be obtained. However, there are two issues limiting its practicality:

1. Tuning f_0 and Q_0 of several filters together is difficult at a few GHz, if possible at all;
2. Due to the feed-through capacitances, such as C_{gd} of $G_{\mathrm{M,i}}$, as well as substrate coupling at several GHz, the maximum stopband attenuation is going to be limited to 30-50 dB, depending on the particular design and operating frequency. Thus, the higher stopband attenuation benefit of a higher-order filter will be defeated.

It may be possible to design a flat passband with cascaded low-Q bandpass filters and at low frequencies (e.g., < 100 MHz). The resulting filter cannot be narrow-band, of course.

3.1.2 Lowpass Filters

Similar to the bandpass filter, if floating active inductors are available lowpass filters can be constructed by replacing the passive inductors in an L-C lowpass filter with active inductors. The lowpass filter's cutoff frequency f_{c} ($\approx f_{\mathrm{p}}$) must be much less than

f_R of the active inductors. To obtain a lowpass filter with the highest possible f_p, we must use the active inductor directly.

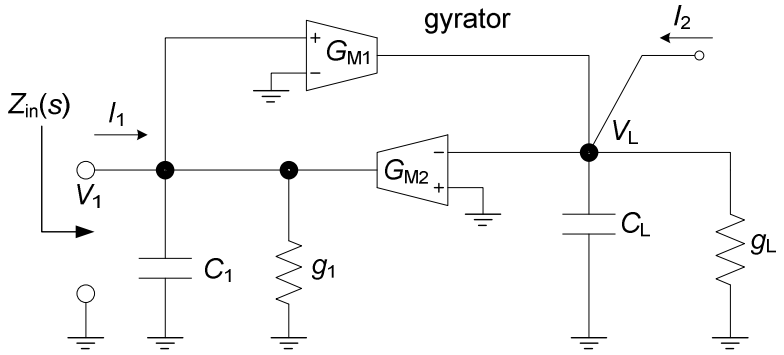


Figure 3-2 Implementing a lowpass filter using the active inductor.

The lowpass function is in fact already provided by the gyrator used to implement the active inductor, as shown in Fig. 3-2. This will be obvious after the following discussion. For the circuit in Fig. 3-2, if $I_2 = 0$, and an input current I_1 is injected into node V_1, using circuit analysis methods, the trans-impedance transfer function may be obtained as

$$T(s) = \frac{V_L}{I_1} = \frac{\frac{G_{M1}}{C_1 C_L}}{s^2 + s\left(\frac{g_L}{C_L} + \frac{g_1}{C_1}\right) + \frac{G_{M1}G_{M2} + g_1 g_L}{C_1 C_L}} = \frac{H_0 \omega_p^2}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \tag{3.3}$$

which is a lowpass function. The transfer function parameters are

$$H_0 = \frac{G_{M1}}{G_{M1}G_{M2} + g_1 g_L} \approx \frac{1}{G_{M2}}, \quad \omega_p = \sqrt{\frac{G_{M1}G_{M2} + g_1 g_L}{C_1 C_L}} \approx \sqrt{\frac{G_{M1}G_{M2}}{C_1 C_L}} = \omega_R$$
$$Q_p = \frac{\omega_p}{\frac{g_L}{C_L} + \frac{g_1}{C_1}} = Q_R \tag{3.4}$$

In other words, the pole frequency f_p and Q_p of the lowpass filter are the same as the self-resonance frequency f_R and Q_R of the active inductor. $T(s)$ is recognized as a 2nd-order function with conjugate poles, and has the advantage of wider bandwidth

with an appropriate Q_p (e.g., between 0.707 and 2) compared with a 1st-order filter or a cascade of 1st-order sections. This is equivalent to the "shunt peaking" bandwidth enhancement technique [16, 83] when a transistor is loaded with a capacitor, without the need for a passive inductor.

Alternatively, if $I_1 = 0$, and I_2 is the input current, it can be found that the trans-impedance transfer function

$$T(s) = \frac{V_1}{I_2} = \frac{-\frac{G_{M2}}{C_1 C_L}}{s^2 + s\left(\frac{g_L}{C_L} + \frac{g_1}{C_1}\right) + \frac{G_{M1}G_{M2} + g_1 g_L}{C_1 C_L}} = \frac{H_0 \omega_p^2}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \tag{3.5}$$

is also a lowpass function, but with inverting gain. The transfer function parameters are

$$H_0 = \frac{-G_{M2}}{G_{M1}G_{M2} + g_1 g_L} \approx -\frac{1}{G_{M1}}, \quad \omega_p = \sqrt{\frac{G_{M1}G_{M2} + g_1 g_L}{C_1 C_L}} \approx \sqrt{\frac{G_{M1}G_{M2}}{C_1 C_L}} = \omega_R$$
$$Q_p = \frac{\omega_p}{\frac{g_L}{C_L} + \frac{g_1}{C_1}} = Q_R \tag{3.6}$$

The two lowpass functions are dual functions of each other, and there is no reason to favor one over the other.

To utilize the lowpass trans-impedance functions, we may expect the need of an input transconductor to convert the input voltage into a current. However, in many cases, during transistor-level circuit design, by some clever circuit techniques, it is possible to free one of the grounded terminals of G_{M1} or G_{M2} in Fig. 3-2 and use it as the input terminal, thus eliminate the need for an input G_M. An example is shown in Fig. 3-3. The transfer function is

$$T(s)=\frac{V_1}{V_{in}}=\frac{\frac{G_{M1}G_{M2}}{C_1C_L}}{s^2+s\left(\frac{g_L}{C_L}+\frac{g_1}{C_1}\right)+\frac{G_{M1}G_{M2}+g_1g_L}{C_1C_L}}=\frac{H_0\omega_p^2}{s^2+s\frac{\omega_p}{Q_p}+\omega_p^2} \tag{3.7}$$

with transfer function parameters being

$$H_0=\frac{G_{M1}G_{M2}}{G_{M1}G_{M2}+g_1g_L}\approx 1,\quad \omega_p=\sqrt{\frac{G_{M1}G_{M2}+g_1g_L}{C_1C_L}}\approx\sqrt{\frac{G_{M1}G_{M2}}{C_1C_L}}=\omega_R$$
$$Q_p=\frac{\omega_p}{\frac{g_L}{C_L}+\frac{g_1}{C_1}}=Q_R \tag{3.8}$$

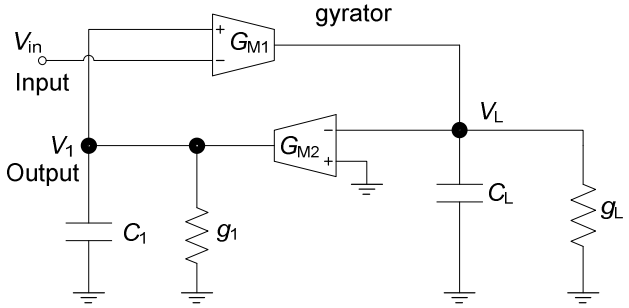


Figure 3-3 Reusing G_{M1} as input G_M to implement a lowpass filter.

This is a very efficient circuit structure, which has been used in the all-NMOS-II analog signal driver circuit in Chapter 2.

3.2 The RF Bandpass Filter in this Work

3.2.1 The Bandpass Filter Circuit

The high-Q bandpass filter circuit is shown in Fig. 3-4. The right half side is recognized as the active-inductor circuit, whose input impedance has a bandpass frequency profile. Transistor M_i converts the input voltage, V_{in}, into a current, and applies it to the inductor port. The output voltage is taken from that port as V_{out}. A very-small-size source follower connects to V_{out}, to isolate the load and reduce the stray capacitance from interconnects.

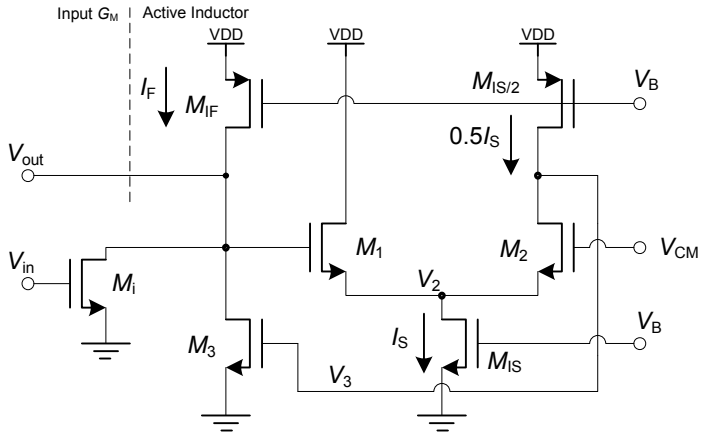


Figure 3-4 The bandpass filter circuit.

The transfer function is derived by multiplying the transconductance of M_i, $G_{M,i}$, with Z_{in} of the active inductor (Eq. 2.52)

$$T(s)=\frac{G_{M,i}\left(\frac{s}{C_1}+\frac{g_3}{C_1C_3}\right)}{s^2+s\left(\frac{g_1}{C_1}+\frac{g_3}{C_3}+\frac{g_1g_3C_2}{C_1C_3G}-\omega^2\frac{C_2}{G}\right)+\frac{g_{m2}}{G}\frac{g_{m1}g_{m3}}{C_1C_3}} \tag{3.9}$$

The transfer-function parameters are

$$H_M=\frac{G_{M,i}}{g_1+\frac{C_1}{C_3}g_3+\frac{C_2g_1g_3}{C_3G}-\omega^2\frac{C_1C_2}{G}}\approx G_{M,i}R_p,\quad \omega_0=\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{GC_1C_3}}\approx\sqrt{\frac{0.5g_{m1}g_{m3}}{C_1C_3}} \tag{3.10}$$

$$Q_0=\frac{\sqrt{g_{m1}g_{m2}g_{m3}/(GC_1C_3)}}{\frac{g_1}{C_1}+\frac{g_3}{C_3}-\frac{C_2}{G}\left(\omega_0^2-\frac{g_1g_3}{C_1C_3}\right)}=\frac{\omega_0}{\frac{g_1}{C_1}+\frac{g_3}{C_3}-\frac{C_2}{G}\left(\omega_0^2-\frac{g_1g_3}{C_1C_3}\right)} \tag{3.11}$$

$$H_0=T(0)=\frac{G_{M,i}g_3G}{g_{m1}g_{m2}g_{m3}}\approx\frac{G_{M,i}g_3}{0.5g_{m1}g_{m3}}\neq 0$$

Note that C_1 and g_1 should be adjusted to reflect the additional parasitic capacitance and conductance from M_i and the output buffer. Different from an ideal bandpass filter, the filter attenuation at dc is not infinity, but determined by the circuit loss g_3, which is transformed into the equivalent series resistor r_s.

Transistor M_i draws current out of the active-inductor circuit for its own biasing,

and M_{IF} needs to be augmented to allow this. The final circuit is designed in pseudo-differential form, and M_i together with its dual component becomes a common-source differential pair.

3.2.2 Noise Analysis of the Bandpass Filter

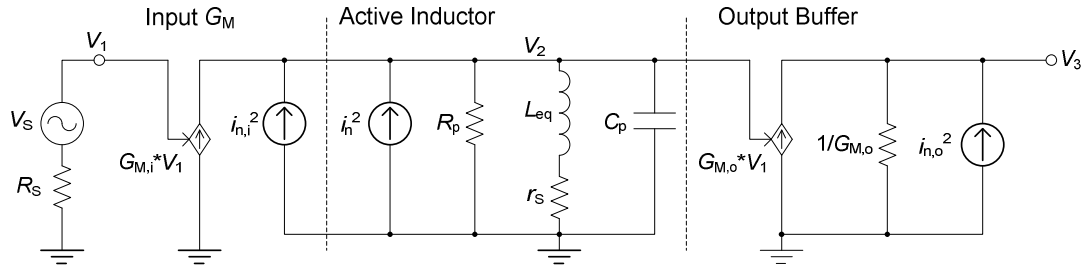


Figure 3-5 Small-signal equivalent circuit of the bandpass filter with noise elements.

Figure 3-5 shows the small-signal equivalent circuit of the bandpass filter with noise elements, where $i_{n,i}^2$ and $i_{n,o}^2$ represent the noise currents from the input G_M and output buffer, respectively, and i_n^2 is the equivalent noise current of the active inductor (Section 2.6). It would be easy to assume that $i_{n,i}^2$ is $4kT\Gamma_n G_{M,i}$; however, we shall remember that by hooking M_i to the active inductor in Fig. 3-4, we have to increase M_{IF} accordingly so that the active inductor's biasing currents are not changed. In addition, per Eq. (2.67), for equal V_{od}, a PFET and a NFET have the same g_m value when I_D is the same. Therefore, we have

$$i_{n,i}^2 \approx 4kT\Gamma_n G_{M,i} + 4kT\Gamma_p G_{M,i} = 4kT\left(\Gamma_n + \Gamma_p\right)G_{M,i} \tag{3.12}$$

The output buffer is modeled as $G_{M,o}$ driving a resistor of $1/G_{M,o}$. The load capacitor at V_3 is ignored since the pole frequency of the output buffer is assumed to be much greater than the filter's f_0. Similarly, the noise current of the output buffer is twice that of the main FET due to the load current source, assuming V_{od} is the same for

both,

$$i_{\mathrm{n,o}}^2 \approx 4kT\Gamma_{\mathrm{n}}G_{\mathrm{M,o}} + 4kT\Gamma_{\mathrm{n}}G_{\mathrm{M,o}} = 8kT\Gamma_{\mathrm{n}}G_{\mathrm{M,o}} \tag{3.13}$$

At f_0, $j\omega L_{\mathrm{eq}}$ cancels $1/(\omega C_{\mathrm{p}})$. Ignoring r_{s}, the filter gain is

$$\left|T\left(\omega_0\right)\right| = G_{\mathrm{M,i}}R_{\mathrm{p}} \tag{3.14}$$

When the filter is driven by a port element of resistance R_{S}, using Eq. (2.50), the total output noise voltage at f_0 is

$$\begin{aligned} v_{\mathrm{n,o}}^2 &= \left[\left(4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2 + i_{\mathrm{n,i}}^2 + i_{\mathrm{n}}^2\right)R_{\mathrm{p}}^2G_{\mathrm{M,o}}^2 + i_{\mathrm{n,o}}^2\right]\frac{1}{G_{\mathrm{M,o}}^2} \\ &= \left[4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2 + 4kT\left(\Gamma_{\mathrm{n}} + \Gamma_{\mathrm{p}}\right)G_{\mathrm{M,i}} + 4kT\left(K_{\mathrm{NF1}}G_{\mathrm{M1}} + K_{\mathrm{NF2}}G_{\mathrm{M2}}\right)\right]R_{\mathrm{p}}^2 + \frac{8kT\Gamma_{\mathrm{n}}}{G_{\mathrm{M,o}}} \end{aligned} \tag{3.15}$$

If only the noise from R_{S} is considered, the output noise becomes

$$v_{\mathrm{n,o,Rs\ only}}^2 = 4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2R_{\mathrm{p}}^2G_{\mathrm{M,o}}^2\frac{1}{G_{\mathrm{M,o}}^2} = 4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2R_{\mathrm{p}}^2 \tag{3.16}$$

Thus, the noise factor is

$$\begin{aligned} NF &= \frac{v_{\mathrm{n,o}}^2}{v_{\mathrm{n,o,Rs\ only}}^2} = \frac{\left[4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2 + 4kT\left(\Gamma_{\mathrm{n}} + \Gamma_{\mathrm{p}}\right)G_{\mathrm{M,i}} + 4kT\left(K_{\mathrm{NF1}}G_{\mathrm{M1}} + K_{\mathrm{NF2}}G_{\mathrm{M2}}\right)\right]R_{\mathrm{p}}^2 + \frac{8kT\Gamma_{\mathrm{n}}}{G_{\mathrm{M,o}}}}{4kTR_{\mathrm{S}}G_{\mathrm{M,i}}^2R_{\mathrm{p}}^2} \\ &= 1 + \frac{\left(\Gamma_{\mathrm{n}} + \Gamma_{\mathrm{p}}\right)G_{\mathrm{M,i}} + \left(K_{\mathrm{NF1}}G_{\mathrm{M1}} + K_{\mathrm{NF2}}G_{\mathrm{M2}}\right) + \frac{2\Gamma_{\mathrm{n}}}{G_{\mathrm{M,o}}R_{\mathrm{p}}^2}}{R_{\mathrm{S}}G_{\mathrm{M,i}}^2} \end{aligned} \tag{3.17}$$

For a given active inductor, increasing $G_{\mathrm{M,i}}$ can reduce NF, at the cost of reducing the maximum input signal level, since $H_{\mathrm{M}} = G_{\mathrm{M,i}}R_{\mathrm{p}}$.

Equation (3.17) is derived for a single-ended circuit. If the BPF circuit in Fig. 3-5 is built in a pseudo-differential structure, and R_{S} connects to the filter through a balun, the NF will be 3 dB higher than the single-ended circuit, since every squared

noise source within the circuit is doubled (see also Section 2.7.3).

3.2.3 Bandpass Filter Example

Using Fig. 3-4, a BPF example is built based on the all-NMOS active inductor presented in Section 2.7, in a pseudo-differential structure, as shown in Fig. 3-6. A differential-pair input transconductor $G_{M,i}$ and a pair of source followers are added to form a bandpass filter per the previous discussion. The biasing conditions are identical to those of the active inductor shown in Fig. 2.29: $I_{M_{IF}} = I_{M_{IS}} = 250$ μA, $V_F = V_Q = 0.6$ V, $V_{CM} = 1.325$ V, $V_{DD} = 1.8$ V, and $I_B = 7$ μA. The circuit simulation results are: $f_0 =$ 6.4 GHz, $Q_0 = 90$, $H_{M,lf2} = 1.868$, $H_{M,lf3} = 1.362$.

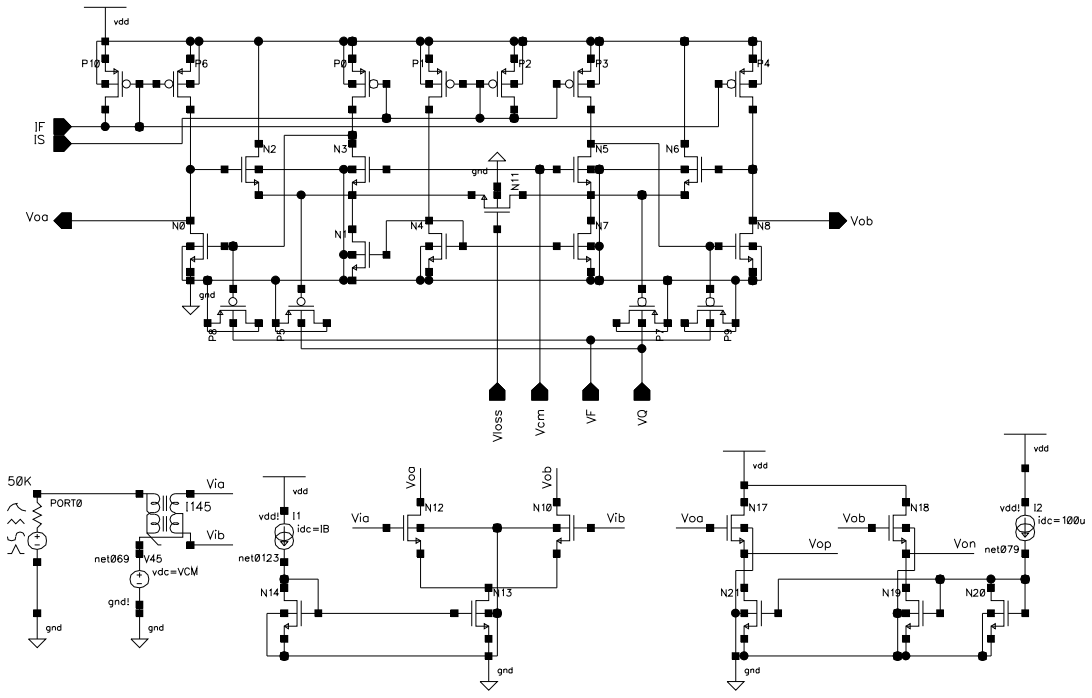


Figure 3-6 Active-inductor bandpass filter example.

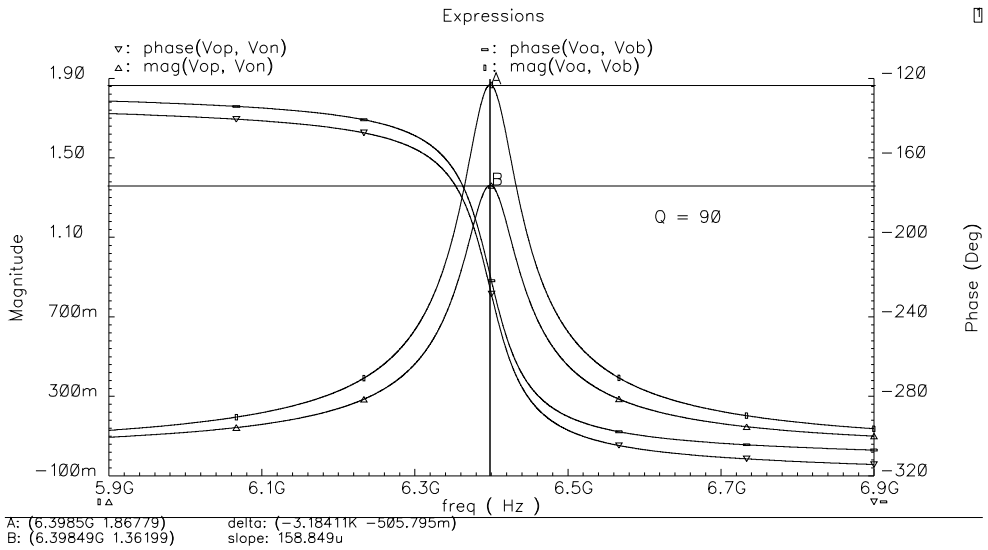


Figure 3-7 Transfer function from ac simulations (pseudo-differential).

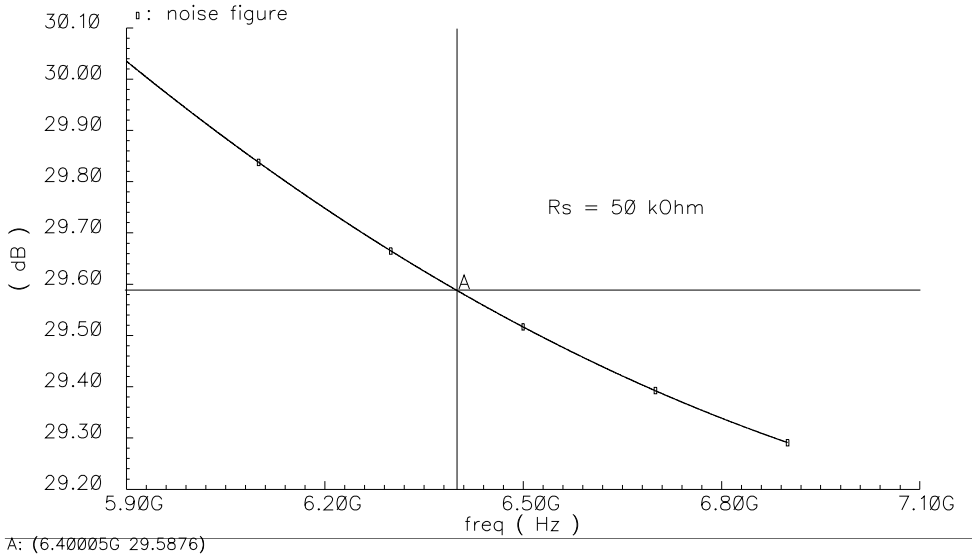


Figure 3-8 Noise simulation results, pseudo-differential, outputs taken at the source-follower output.

The small-signal parameters are found from the circuit's operating points: g_{m1} = 1.2 mS, g_{m2} = 1.1 mS, g_{m3} = 1.2 mS, C_1 = 21 fF, C_2 = 18 fF, C_3 = 19 fF, g_1 = 132 μS, g_3 = 112 μS, $G = g_{m1} + g_{m2} + g_2$ = 2.44 mS, $G_{M,i}$ = 17.25 μS, $G_{M,o}$ = 481.2 μS, $G_{M,o,load}$ = 632.2 μS. The only parameters changed from the active inductor circuit are g_1 and C_1, due to the parasitic capacitance and leakage from the input G_M and output source

follower. The circuit's performances are calculated using a spreadsheet using the equations in this work, as shown in Table 3-1. The calculated results match the simulation results very closely.

Table 3-1 Calculation of Active-Inductor Bandpass Performances

Para-meter	Unit	Sims	Calc-'ed	Equ-ation	Para-meter	Unit	Sims	Calc-'ed	Equ-ation
g_{m1}	mS	1.2			GammaN		0.8786		(2.73)
g_{m2}	mS	1.1			GammaP		0.9685		(2.73)
g_{m3}	mS	1.2			KNF1		3.6942		(2.69)
C_1	fF	21			KNF2		1.8471		(2.71)
C_2	fF	18							
C_3	fF	19			Rs	Mohm	0.05		
g_1	uS	132							
g_3	uS	112							
G	mS	2.44							
$G_{M,i}$	uS	17.25							
$G_{M,o}$	uS	481.2							
$G_{Mo,load}$	uS	632.15							
f_0	GHz	**6.4**	**6.420**	(3.10)	NF			450.08	(3.17)
ω_0	Grad/s		40.34	(3.10)	NF	dB	**29.59**	26.53	(3.17)
Q_0		**90**	**89.4**	(3.11)	NF+3 dB	dB		**29.54**	(3.17)
$H_{M,V2}$		**1.87**	**1.82**	(3.11)					
$H_{M,V3}$		**1.36**	**1.39**	(3.11)					
R_p	MOhm		0.106	(3.10)					

3.3 The RF Lowpass Filters in this Work

3.3.1 All-NMOS-II Active Inductor Lowpass Filter

The all-NMOS-II active inductor circuit, when configured as an analog signal driver, has the characteristics of a lowpass filter. Details were discussions in Section 2.8.3. The gate of the non-inverting transconductor in the all-NMOS-II circuit is freed from ac ground and used as a voltage input, and per Section 3.1.2, it will behave as a lowpass filter. Incidentally, due to the special circuit architecture, the lowpass filter has very high linearity.

3.3.2 All-NMOS Active Inductor Lowpass Filter

The all-NMOS active inductor circuit can be readily converted into a lowpass filter by using the V_{CM} terminal on the M_2 gate as input and taking the output voltage on the drain of M_3, as shown in Fig. 3-9. It uses the principle shown in Fig. 3-2, by converting V_{in} into a current into node V_L and using V_1 as output voltage. Similar to the bandpass filter, V_{out} needs to be buffered, to prevent the load and interconnect capacitance and conductance from loading the active inductor core. The circuit has similar properties as the all-NMOS-II analog signal driver, such as $V_{IN} = V_{OUT}$. However, since M_1 and M_2 have different voltage V_{ds}, V_{out} does not exactly follow V_{in} in dynamic operation: as a result, the circuit's linearity is not as good, and $V_{IN} \approx V_{OUT}$ instead of being exactly equal.

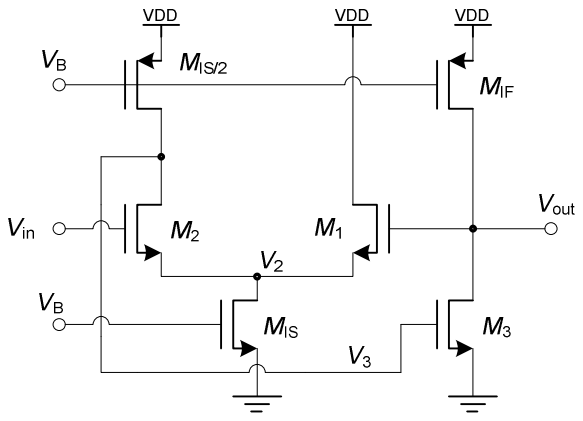


Figure 3-9 Implementing a lowpass filter using the all-NMOS active inductor.

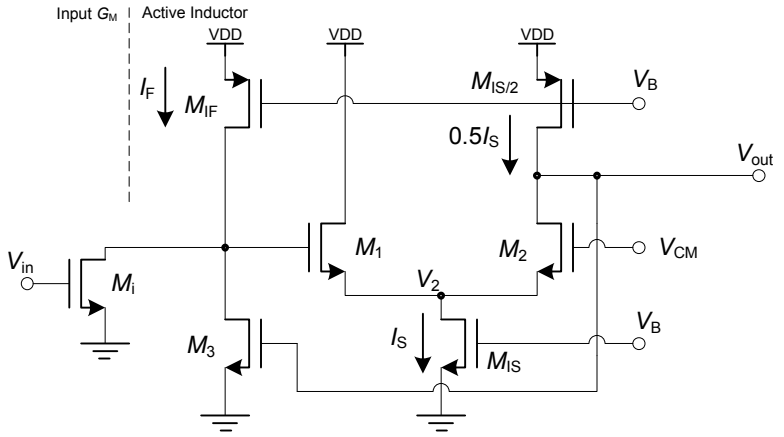


Figure 3-10 Another method of implementing a lowpass filter using the all-NMOS active inductor.

Another method of implementing a lowpass filter is shown in Fig. 3-10, where M_i converts V_{in} into a current on node V_1, and V_{out} is taken from the "load" node of the gyrator, as described in Fig. 3-2. This method allows the common-mode of V_{in} and V_{out} to be different, especially when M_i is implemented as a differential pair, at the cost of adding the M_i circuitry and slightly higher power dissipation and noise.

3.4 Conclusion

Bandpass and lowpass filters can be readily implemented with active inductors. To obtain high operating frequency, the filter function must be incorporated into the active-inductor circuit itself, rather than treating the active inductor as a pure inductor. For an arbitrarily given active-inductor circuit, by locating the two nodes of the gyrator, lowpass filters can be readily obtained using the principles given in this chapter.

The all-NMOS active-inductor bandpass filter is discussed in detail, and the performance equations are verified by simulation results.

CHAPTER 4

DESIGN OF RF ANALOG OSCILLATORS

4.1 Designing RF Oscillators with Active Inductors

4.1.1 A Passive *L*-*C* Oscillator

There are two types of oscillators operating at several GHz: ring oscillators and *L*-*C* oscillators. A ring oscillator is a loop of an odd number of inverters, and each inverter can be a CMOS inverter or a resistor-loaded differential amplifier [84]. The inverter acts as both the gain- and amplitude-limiting element, thus its output voltage has high harmonic distortion and appears typically as rounded pulses. This is not an issue for digital circuitry since their clocks are pulses; however, for many other applications, such as modulation/demodulation, sinusoidal signals are required with low output harmonics and low phase noise, and this is almost always done with oscillators based on passive *L*-*C* elements, labeled here simply as passive *L*-*C* oscillators.

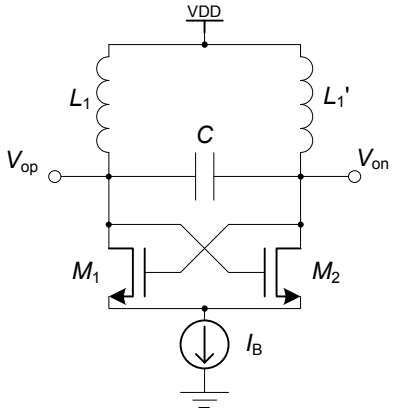


Figure 4-1 A passive *L*-*C* oscillator.

Figure 4-1 shows a typical passive *L*-*C* oscillator for operations between 1-10 GHz. The passive inductors L_1 and L_1' are symmetrical and contained within one single spiral inductor. *C* is usually a pair of varactors connected back to back to

facilitate frequency tuning. To obtain a certain frequency tuning range, C has to vary between C_{max} and C_{min} and cannot be zero, and this limits the oscillation frequency from approaching the self-resonance frequency of the inductors. M_1, M_2 and I_B implement a negative resistor, providing the gain for the oscillation to start and continue. M_1 and M_2 also limit the oscillation amplitude. The output voltage (power) is available through the V_{op} and V_{on} terminals. The oscillator can only be differential due to the cross connection of M_1 and M_2, and this happens to be desirable and not an issue for most applications. Depending on the particular design, the oscillation may be current- or voltage-limited:

1. Current limited. The voltage amplitudes on V_{op} and V_{on} can fully turn on and off M_1 and M_2 and make them operating in switching mode, but is smaller than V_{DD}. The biasing current I_B is alternated between L_1 and L_1'. I_B and the "tank" loss determine the voltage amplitude.
2. Voltage limited. The voltage amplitudes on V_{op} and V_{on} are so high that they are reaching ~ $2 \cdot V_{DD}$ at their high points and turning off M_1 and M_2 at low points.

4.1.2 An Active-Inductor Oscillator

Active inductors can be used to replace the passive inductors in Fig. 4-1 to implement oscillators. The varactor C is not needed, since the active inductor is tunable, and its f_R determines the oscillation frequency f_0. The circuit is shown in Fig. 4-2 where each active inductor is represented by its equivalent circuit. Since the active-inductor circuit can be designed differentially or pseudo-differentially, it naturally provides a dual R-L-C tank for the differential structure. The output voltages are obtained from the

inductor port, and just like the active-inductor filters, a voltage buffer, e.g., a source follower, is needed to prevent the load from reducing f_R and Q of the tank.

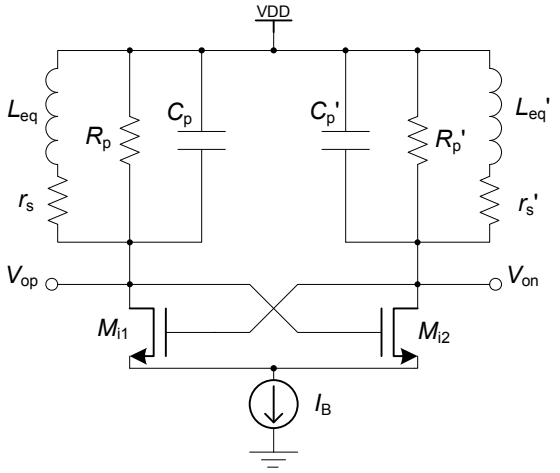


Figure 4-2 An active-inductor oscillator.

The equivalent active-inductor components in Fig. 4-2 are calculated with the extra parasitic capacitances and conductances of M_{i1} and M_{i2} as well as of the output buffers (not shown in figure) absorbed.

4.1.3 Reducing Output Voltage Harmonic Distortion

Equating M_1 and M_2 in Fig. 4-2 circuit to a negative resistor is convenient and is the common microwave-design method [85, 86]. However, different from the microwave design, where the negative resistor is almost always the amplitude limiting element, since the impedance-transformation network to which it is connected is usually passive and has much higher linearity, amplitude limiting in active-inductor oscillators can happen anywhere, since the whole circuit is active.

This active-inductor oscillator operates in voltage mode, and we need the differential output voltage, $V_{op} - V_{on}$, to be low in harmonic distortion. However,

different from a passive *L*-*C* oscillator, the active inductor is nonlinear and has a low limit on its maximum signal amplitude, since it is made of transistors. Thus, besides the negative resistor M_1 - M_2, the active inductor can also limit the oscillation amplitude. Further design analysis is needed.

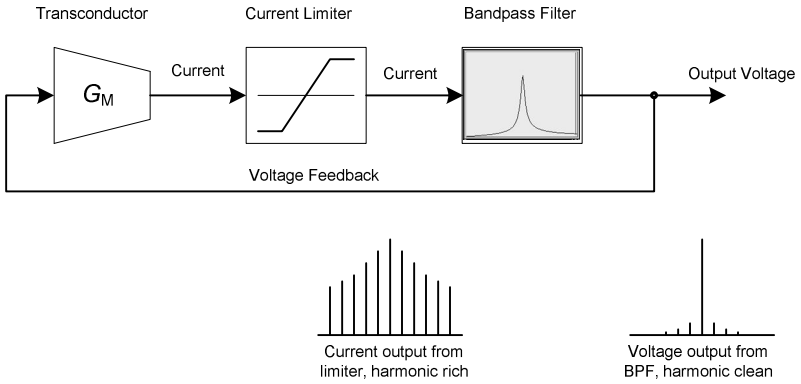


Figure 4-3 Active-inductor oscillator block diagram.

Figure 4-3 shows the block diagram of the active-inductor oscillator. The signals are drawn as single lines for simplicity, and are differential in a real circuit implementation. The G_M (the M_1 - M_2 differential pair) converts the output voltage into a current. The bandpass filter is in fact the active inductor by itself, and has current input and voltage output, that is $T(s) = Z_{in}(s)$. In between is a current limiter, whose output is clamped and rich in harmonics due to its limiting effect. The bandpass filter eliminates most of the harmonics in the input current and outputs a harmonically clean voltage. The current limiter, as we shall see in more detail, is actually part of the function of the differential pair M_1 - M_2. Qualitatively, the minimum and maximum output currents from M_1 or M_2 drains are 0 and I_B, respectively, therefore M_1 and M_2 implement the G_M and the current limiter at the same time.

To ensure the above scenario happens as planned, I_B must be kept at a low level,

such that at the output current peak at G_M, the active-inductor BPF output voltage is not clamped or distorted. If I_B is high, the active inductor will become the limiting element in the feedback loop, and its output voltage will be distorted. It should be noted that due to the high operating frequency and effects from parasitic capacitances, we will not see clipped current or voltage signals; instead, they will be compressed at their peaks when limited.

The transfer function of the bandpass filter has the impedance profile of the active inductor. For the circuit in Fig. 4-2, neglecting r_s since at $f \approx f_R$ $|R_p| >> r_s$, we have

$$T(s) = Z_{in}(s) = \frac{s/C_p}{s^2 + s/(R_p C_p) + 1/(L_1 C_p)} = \frac{s\frac{\omega_R}{Q_R}R_p}{s^2 + s\frac{\omega_R}{Q_R} + \omega_R^2} \tag{4.1}$$

with the magnitude being

$$|T(\omega)| = \frac{\omega\frac{\omega_R}{Q_R}R_p}{\sqrt{\left(\omega_R^2 - \omega^2\right)^2 + \left(\omega\frac{\omega_R}{Q_R}\right)^2}} \tag{4.2}$$

Thus we have

$$|T(\omega_R)| = R_p, \quad |T(2\omega_R)| = \frac{R_p}{\sqrt{\frac{9}{4}Q_R^2 + 1}}, \quad |T(3\omega_R)| = \frac{R_p}{\sqrt{\frac{64}{9}Q_R^2 + 1}} \tag{4.3}$$

The higher Q_R is, the higher is the attenuation of the harmonic components in the input current, with a maximum limit on Q_R as we will see in the next section. The phase of this bandpass filter is

$$\angle T(s) = \frac{\pi}{2} - \tan^{-1}\frac{\omega\omega_R/Q_R}{\omega_R^2 - \omega^2} = 0, \text{ when } \omega = \omega_R \tag{4.4}$$

4.1.4 Designing the Oscillator Loop Gain

Common perception has it that since the oscillator in Fig. 4-3 has a high-Q active-inductor BPF as "frequency-selecting element," the oscillation frequency f_0 will automatically be the BPF center frequency, f_R, because the BPF "selects" the oscillation frequency. In reality, f_0 usually does not equal f_R, due to the phase shifts from the parasitic elements inside and outside of the devices. There are two necessary conditions to build up and sustain a stable oscillation:

1. The loop gain is greater than 1, that is, $G_M > 1/R_p$, with margin, as we will see below.
2. The loop phase shift is a multiple of 2π.

The final steady-state frequency is determined by the phase condition, and not because the frequency-selecting element "selected" the frequency. Passive- and active-inductor resonators come in handy for designing oscillators, because when placed in the feedback loop, as in Fig. 4-3, they happen to have the maximum impedance (and in turn, gain) at f_R, when their phase is 0°. The rejection of frequencies away from f_R is hence a desirable coincidence. For active inductors, the maximum impedance, R_p, is approximately proportional to Q_R (Eq. 2.8). Therefore, the higher Q_R is, the better does the resonator filter out unwanted harmonics per Eq. (4.3). However, for GHz-oscillator design, besides the high circuit sensitivities associated with high Q_R, there is another issue.

Figure 4-4 shows the magnitude and phase profile of an example resonator, with a very much scaled down f_R. At f_R = 3 kHz, its phase $\phi = 0$ and R_P = 100 Ω. When

placed in the loop in Fig. 4-3, if G_M and current limiter both have 0° phase shift, we expect the oscillation frequency $f_0 = f_R$ = 3 kHz, and to make the loop gain > 1 we need G_M > 10 mS. However, if due to parasitic capacitance, G_M, current limiter and signal wires have a total phase shift of, say, –35°, to satisfy the 0°-loop-phase requirement, f_0 will shift down to approximately 2.85 kHz, and the magnitude is reduced to 83 Ω. To oscillate, G_M will have to be greater than 12 mS. If G_M is not designed with sufficient margin, and/or Q_R is overly high, the oscillator may not oscillate. When $f_0 \neq f_R$, the resonator will amplify the desired signal less and the circuit noise more, another unwanted result.

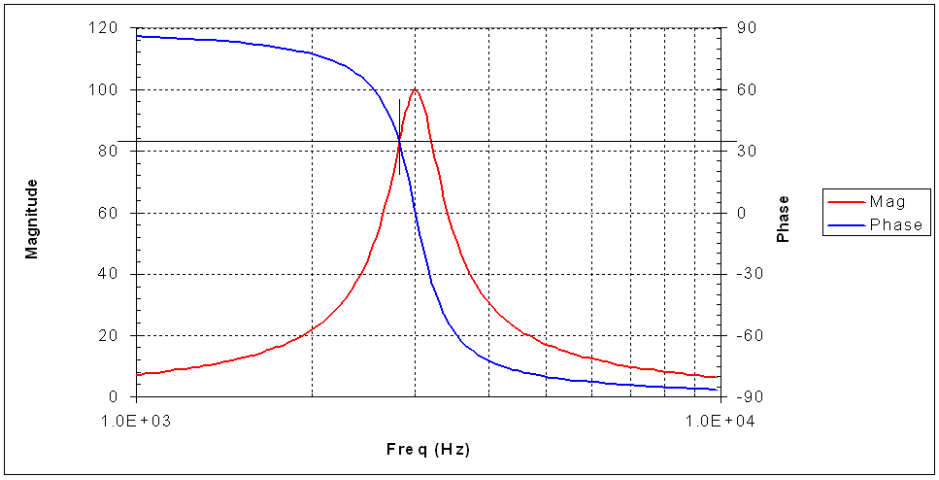


Figure 4-4 The magnitude and phase of an example shunt *R*-*L*-*C* resonator.

This phenomenon is highly visible in GHz designs because of the high frequency. To generate 35° phase lag at 3 kHz and 3 GHz, delays of 32.4 μs and 32.4 ps, respectively, are needed. Therefore, the distributed-*R*-*C* or transmission-line delays in IC interconnections will be much more sensitive in the 3 GHz design than in the 3 kHz design. In addition, if G_M has an internal pole, its phase will increase with frequency.

4.2 RF Oscillators in This Work

4.2.1 The Circuit and AC Analysis

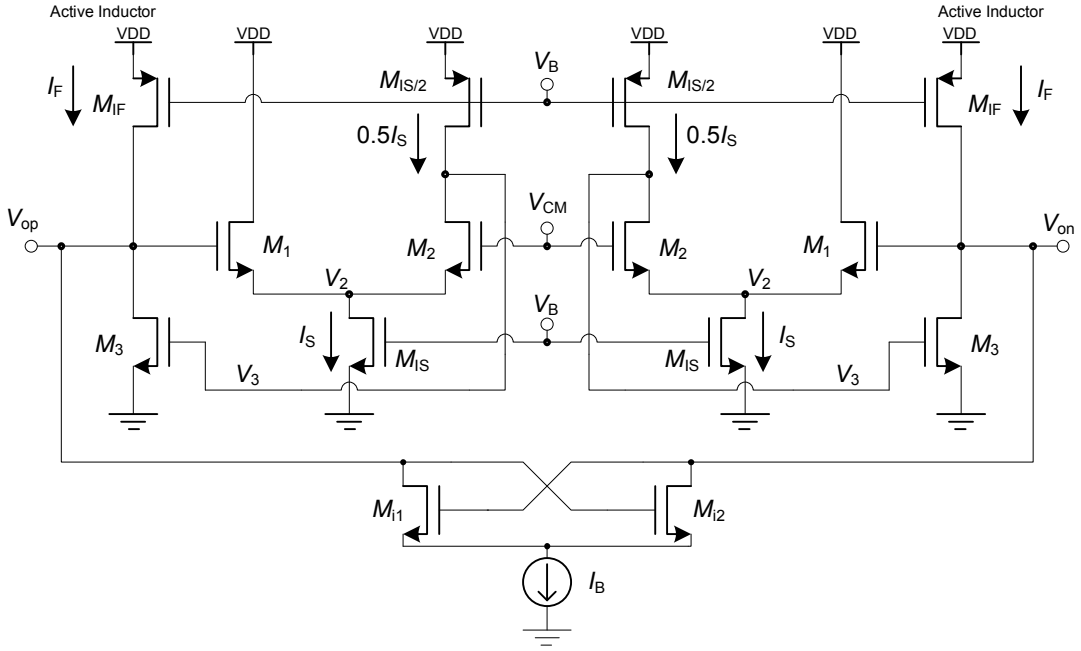


Figure 4-5 The all-NMOS active-inductor oscillator in a pseudo-differential structure.

Figure 4-5 shows the all-NMOS active-inductor oscillator in a pseudo-differential structure. The differential pair M_{i1} - M_{i2} implements both the gain element and the current limiter in the feedback loop. The required source followers at V_{op} and V_{on} are not shown for clarity. M_{i1} and M_{i2} can be assumed to have very low phase shift since their parasitic capacitance can be considered as extrinsic. When Q_R of the active inductor is sufficiently high (> ~20), the oscillation frequency of the circuit is approximately the active inductor self resonance frequency f_R (Eq. 2.55),

$$\omega_0 \approx \omega_R = \sqrt{\frac{g_{m1}g_{m2}g_{m3}}{GC_1C_3}} \approx \sqrt{\frac{0.5g_{m1}g_{m3}}{C_1C_3}} = \frac{1}{\sqrt{L_{EQ}C_1}} \tag{4.5}$$

The active-inductor impedance at f_R is (Eq. 2.62),

$$R_p = \frac{1}{g_1 + \frac{C_1}{C_3} g_3 + \frac{C_2 g_1 g_3}{C_3 G} - \omega^2 \frac{C_1 C_2}{G}} = \frac{Q_R}{\omega_R C_1} = Q_R \sqrt{\frac{L_{eq}}{C_1}} \tag{4.6}$$

When M_{i1} and M_{i2} operate as current limiter as discussed before, the single-ended and differential output-signal amplitudes are approximately

$$V_{o,a} \approx \frac{I_B \cdot R_p}{2} = \frac{I_B/2}{g_1 + \frac{C_1}{C_3} g_3 + \frac{C_2 g_1 g_3}{C_3 G} - \omega^2 \frac{C_1 C_2}{G}} = \frac{I_B Q_R}{2\omega_R C_1} = \frac{I_B Q_R}{2} \sqrt{\frac{L_{eq}}{C_1}}, \text{ single-ended}$$
$$V_{o,d} = 2 \cdot V_{o,a}, \text{ differentially.} \tag{4.7}$$

The factor of 2 in the denominator of V_{oa} is because $2V_{o,a} = I_B R_p - 0R_p$.

The circuit parameters used above need to be updated to reflect the extra parasitic capacitance and conductance from the differential pair and output drivers:

$$\begin{aligned} C_1 &= C_{1,\text{active inductor}} + 4 \cdot C_{gd,Mi} + C_{jd,Mi} + C_{gs,Mi} \\ g_1 &= g_{1,\text{active inductor}} + g_{ds,Mi} \end{aligned} \tag{4.8}$$

4.2.2 Oscillator-Noise Analysis

Since oscillators, whether built with passive or active inductors, must have active elements to replenish energy, they inevitably generate noise (a passive inductor generates noise, too, but at a lower level compared with active devices). The output noise of oscillators can be projected on two dimensions, amplitude noise and phase noise. Amplitude noise represents the random signal amplitude variation and is usually less of a concern since all oscillators have amplitude-regulating mechanism, and the noise contribution from active elements to the oscillation amplitude is largely dissipated before reaching the output. Phase noise represents the short-term periodic

fluctuation of the oscillation, and regularly gains designers' attention for a couple of reasons:

1. It is detrimental since it can introduce adjacent channel interference in communication systems [83, 87] and it cannot be easily reduced.
2. It is not thoroughly modeled and unanimously understood, even though simulators have progressed in predicting the phase noise in recent years.

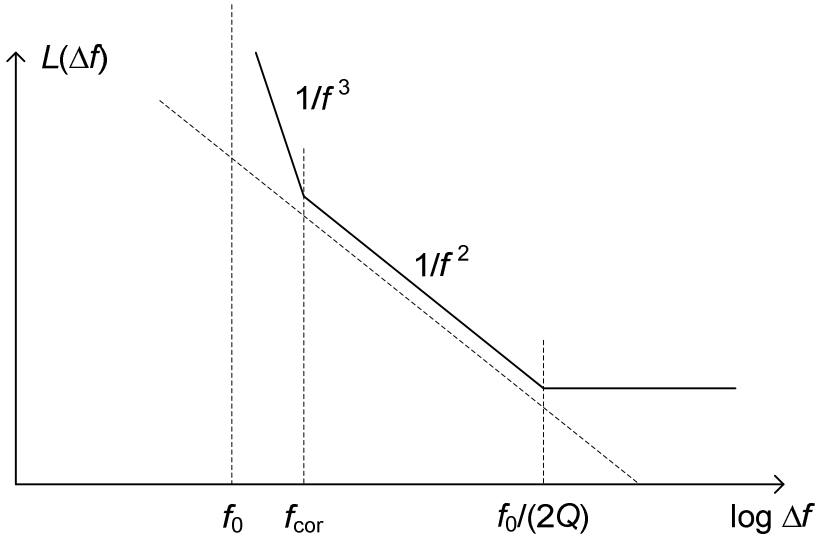


Figure 4-6 A typical oscillator phase-noise profile.

A typical phase-noise profile is shown in Fig. 4-6, where $L(\Delta f)$ represents the squared phase-noise voltage or current, or power. At frequencies close to the oscillation frequency f_0, $L(\Delta f)$ is proportional to $1/f^3$ due to flicker noise; at intermediate frequencies, $L(\Delta f)$ is proportional to $1/f^2$ due to thermal noise; and beyond a certain frequency, phase noise reaches a floor and does not reduce any further. Phase noise does not become infinite when Δf approaches 0, but shows a Lorentzian spectrum profile at or near f_0 [83].

Leeson introduced a phenomenological model of phase noise in 1966 [88]

modeling the $1/f^2$ and the flat portions of phase noise and has been generously referred in the study of phase noise in recent years. Leeson's model, however, contains a few empirical parameters that are circuit- and process-dependent and must be determined experimentally or empirically. In the past decade or so, Razavi, Lee and Abidi contributed independent theories that treat the phase noise from different approaches [1, 83, 87, 89, 90].

There are two steps in providing an analytical expression of oscillator phase noise: (1) how is the thermal noise converted into phase noise; (2) up-conversion of the flicker ($1/f$) noise.

Lee solved the thermal noise conversion by examining the impedance profile of an inductor resonator with loss compensation [83], which is infinite at the oscillator frequency f_0 in steady state, since the compensation must cancel the circuit loss perfectly, no more, no less. The thermal noise is modeled as a shunt white noise current, which is shaped by the impedance profile of the resonator. Razavi approaches this issue by studying the closed-loop transfer-function sensitivity to noise, and shows the identical result, with the added benefit of being able to apply the theory on non-resonator oscillators, such as ring oscillators.

The flicker noise of active devices near dc is up-converted into $1/f^3$ phase noise near f_0 due to circuit nonlinearities. Lee solved this problem by introducing periodic time-varying impulse sensitivity functions; Razavi's method is similar, but done in the frequency domain. The flicker noise conversion is important for low-noise oscillators, such as passive-inductor oscillators. The phase-noise level of active-inductor oscillators is dominated by thermal noise which is 30-40 dB higher than that of

passive inductors at practical power levels [90], therefore the $1/f^3$ region is hardly visible. Thus we concentrate on the $1/f^2$ phase noise, or thermal noise conversion only.

The phase noise floor is usually empirically modeled and not analyzed by the researchers. It is not modeled in circuit simulators either. Therefore, we will not try to analyze it.

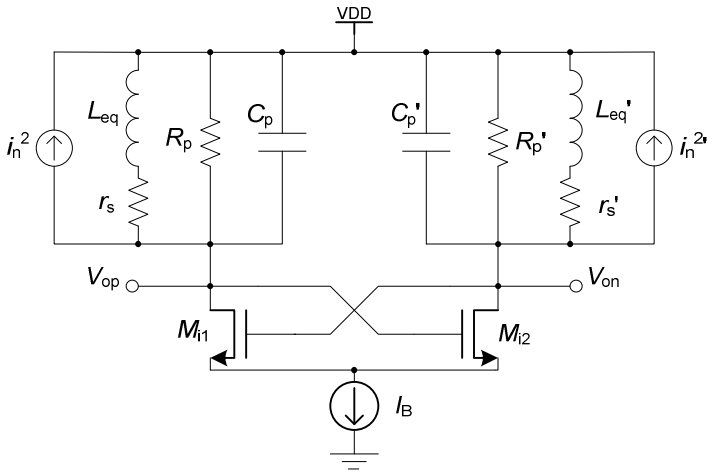


Figure 4-7 The equivalent circuit of the active-inductor oscillator showing the noise elements.

Figure 4-7 shows the equivalent circuit of the active-inductor oscillator with noise elements. Per discussions in Chapter 2, the shunt noise current i_n^2 sufficiently represents the active-inductor noise and is given by Eq. (2.50). For the oscillator, i_n^2 must also include the noise from M_{i1} and M_{i2},

$$\begin{aligned} i_n^2 &= 4kT\left(K_{NF2}G_{M2} + \frac{\omega_R^2}{\omega^2}K_{NF1}G_{M1} + \Gamma_n G_{Mi1}\right) \\ &\approx 4kT\left(K_{NF2}G_{M2} + K_{NF1}G_{M1} + \Gamma_n G_{Mi1}\right) \end{aligned} \tag{4.9}$$

when $\omega \approx \omega_R$. K_{NF1} and K_{NF2} for the all-NMOS active inductor are given by Eqs. (2.69) and (2.71), respectively. The noise from the tail current source I_B generates mostly a common-mode voltage and is neglected.

The loss of the active-inductor resonator at steady oscillation is 100%

compensated by the negative resistor, no more, no less, and as a result, the impedance looking into the oscillator output is ∞, just like in a lossless *L*-*C* resonator:

$$Z(\omega)=\frac{1}{j\omega C_1+\frac{1}{j\omega L_{eq}}}=\frac{j\omega L_{eq}}{1-\frac{\omega^2}{\omega_0^2}}=\frac{j(\omega_0+\Delta\omega)L_{eq}}{1-\frac{(\omega_0+\Delta\omega)^2}{\omega_0^2}}=\frac{j(\omega_0+\Delta\omega)L_{eq}}{1-1-2\frac{\Delta\omega}{\omega_0}-\frac{\Delta\omega^2}{\omega_0^2}}\approx-\frac{j\omega_0 L_{eq}}{2\frac{\Delta\omega}{\omega_0}} \quad (4.10)$$

Using the relationship of $\omega_0^2 = 1/(L_{eq}C_1)$, it becomes

$$Z(\omega)=-j\frac{\omega_0 L_{eq}}{2\frac{\Delta\omega}{\omega_0}}=-j\frac{1}{2\Delta\omega C_1} \quad (4.11)$$

The noise voltage at the oscillator output therefore is

$$\begin{aligned}\frac{v_n^2}{\Delta f}&=\frac{i_n^2}{\Delta f}\left|Z(\omega)\right|^2=\frac{i_n^2}{\Delta f}\frac{1}{(2\Delta\omega C_1)^2}\\&\approx 4kT\left(K_{NF2}G_{M2}+K_{NF1}G_{M1}+\Gamma_n G_{Mi1}\right)\frac{1}{(2\Delta\omega C_1)^2}\\&=\frac{kT\left(K_{NF2}G_{M2}+K_{NF1}G_{M1}+\Gamma_n G_{Mi1}\right)}{(\Delta\omega C_1)^2}\end{aligned} \quad (4.12)$$

Phase noise is the ratio of noise voltage to the signal amplitude. Using Eq. (4.7), we have,

$$\begin{aligned}L(\omega)&=10\log\left(\frac{\frac{v_n^2}{\Delta f}}{v_a^2/2}\right)\\&=10\log\frac{8\omega_0^2 kT\left(K_{NF2}G_{M2}+K_{NF1}G_{M1}+\Gamma_n G_{Mi1}\right)}{\Delta\omega^2 I_B^2 Q_R^2},\ \text{dBc/Hz}\end{aligned} \quad (4.13)$$

The division by two in the denominator, $V_a^2/2$, is because V_a is a peak value and needs to be converted into RMS, since noise is an RMS value.

In deriving the phase noise (Eq. 4.13), we use half of the pseudo-differential circuit to calculate both the noise and signal, therefore, unlike the bandpass filter (end

of Section 3.2.2), we do not need to add 3 dB to the phase noise for a pseudo-differential circuit.

Lee [83] states that the thermal noise in Eq. (4.12) contributes equally to the fluctuations of oscillation amplitude and phase, i.e., AM noise and PM noise, per the equipartition theorem of thermodynamics; further, when an amplitude-limiting scheme exists, as in every practical oscillator, only half of the noise (PM noise) shows up as phase noise, and the other half (AM noise) disappears (presumably into heat). On the other hand, Ken Kundert, the primary designer of the Cadence® SpectreRF® simulator which we use to simulate the phase noise, states that when an amplitude-limiting scheme exists, the AM noise actually mostly turns into PM noise rather than disappearing; consequently, almost 100% of the noise in Eq. (4.12) shows up as phase noise [91]. The simulator is implemented assuming that the thermal noise is 100% converted into phase noise. The difference between Lee's theory and that of Kundert is 3 dB. As shown by Eq. (4.13), we use Kundert's theory here, since this is how the simulator is implemented, and several RF engineers whom the author surveyed stated that they did not see a (3-dB) phase noise discrepancy between silicon and SpectreRF®.

Once again, Eq. (4.13) does not take into account the noise-to-frequency translation due to the oscillator nonlinearity and the phase noise floor. However, as we shall see below, it yields results with reasonable accuracy, mainly because the thermal noise of active-inductor oscillators is 30-40 dB higher than that of passive *L*-*C* oscillators and it dominates all other sources and mechanism in overall phase noise.

4.2.3 Example of Active-Inductor Oscillator

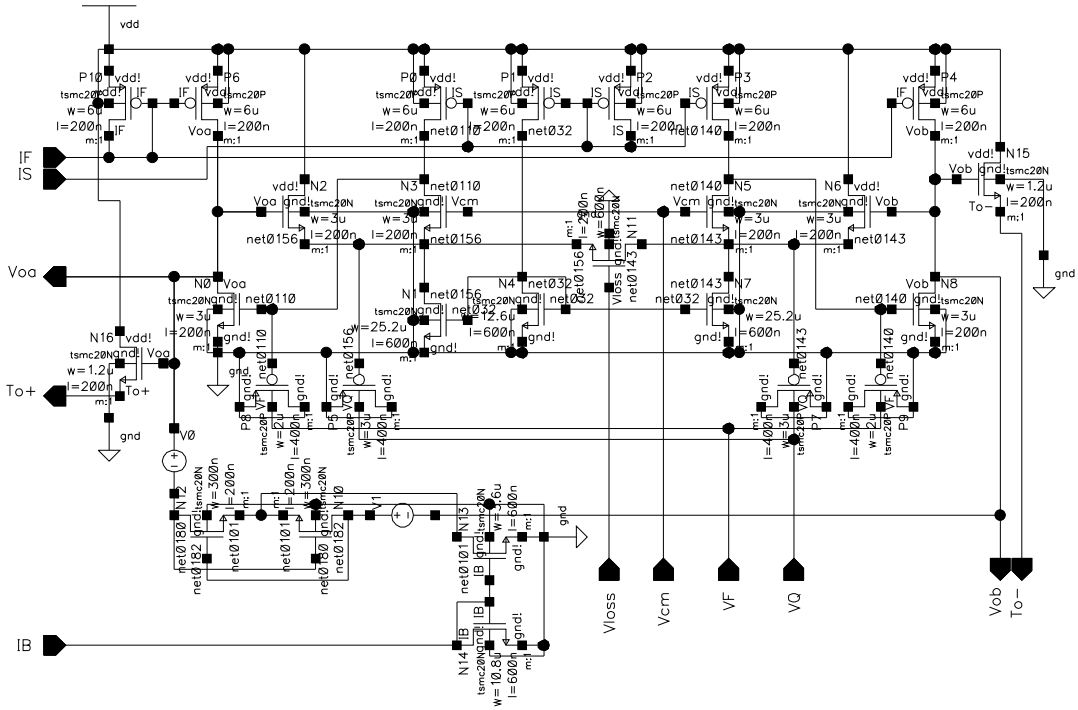


Figure 4-8 The oscillator circuit. $I_S = I_F = 250$ μA, $I_B = 50$ uA, $V_F = V_Q = 0.5$, $V_{CM} = 1.35$, $V_{loss} = 0$.

The oscillator circuit in this design is shown in Fig. 4-8. I_F and I_S are external biasing currents that provide the biasing voltages for the single-transistor current sources P4, P6, P0, P3 and P1. The current from P1 is duplicated by NFETs N4, N1 and N7 to provide the tail currents for the differential pairs N2-N3 and N5-N6. PFETs P8-P9 and P5-P7 implement the varactors for frequency and Q tuning, respectively. NFETs N0, N2 and N3 form an all-NMOS active inductor, and N5, N6, N8 form the mirrored active inductor to realize a pseudo-differential circuit.

N11, whose gate voltage is controlled by V_{loss}, operates in the linear region since its source and drain are connected to equal voltages. By increasing V_{loss}, N11 can be turned on and acts as a resistor R_{loss} across the differential circuit. R_{loss} is equivalent to a grounded resistor of value $R_{loss}/2$ for each half of the circuit. Since $R_{loss}/2$ is in

parallel with g_2 in Fig. 2-28, per Eq. (2.58), it has the effect of decreasing the circuit Q_R. N11 is designed as a risk mitigation measure in case the circuit is unstable due to inaccurate transistor modeling or parasitic extractions and is normally turned off.

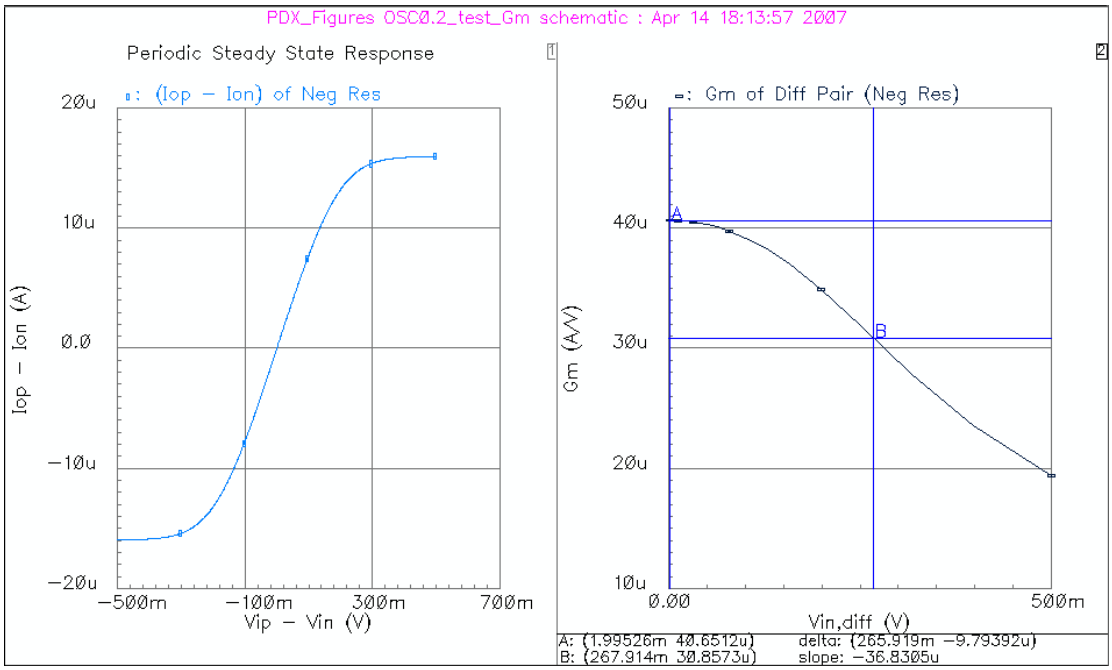


Figure 4-9 The limiting effect of the differential-pair negative resistor. (a) dc simulation results; (b) Periodical Steady State (PSS) simulation results. Markers A and B show the maximum G_M and steady-oscillator G_M, respectively.

The IB terminal connects to an external biasing current I_B, and generates the gate voltage for the tail-current source of the differential pair N10-N12. N10 and N12 implement a negative resistor due to their cross connection. As shown in Fig. 4-3, the differential pair doubles as a current limiter by proper transistor sizing and biasing. This is shown in Fig. 4-9. Under biasing conditions identical to its operation within the oscillator circuit, the *V-I* transfer function of the differential pair was simulated. The dc simulation shows that the output current is clipped at about 14 uA, and the G_M plot shows that as the input signal amplitude increases, the effective G_M decreases smoothly to allow for smooth oscillation amplitude settling. To make the loop gain > 1

and start an oscillation, the active inductor R_p must be greater than 1/73 μS = 13.7 kΩ.

By tuning I_B, the oscillation amplitude can be adjusted, since I_B determines the "starving" point of G_M in the oscillation loop. However, as seen in Fig. 4-5, I_B diverts a small portion of current out of N0 and N8, and will therefore change f_R a little bit. This effect can be reduced by adjusting I_F and I_B jointly. As discussed before, if I_B is overly large, the oscillation will be voltage limited by the active inductor and the output harmonic distortion will be high.

4.2.4 Design Considerations

Per Eq. (4.3), it is desirable to have a higher Q_R so that the oscillator-output harmonics are low. On the other hand, a higher Q_R will increase the sensitivity to the G_M phase error. Considering both, a $Q_R \approx 100$ is chosen for the active inductor. Q_R will be decreased by the g_{ds} of N10 and N12. If the terminal currents and voltages of the cross-connected differential pair N10 and N12 are monitored, significant phase shifts are found on their drain currents, due to the two C_{gd} terms. However, both can be considered as extrinsic to the two NFETs and absorbed by C_P in the active inductor (Fig. 4-2). With this treatment, when N10 and N12 are closely placed in layout, the phase shift of their intrinsic G_M is very close to 0°. Similarly, their C_{gs}s and C_{jd}s can be absorbed into C_P, reducing f_0 a little bit. To keep the parasitic capacitance balanced in the differential circuit, the cross connections of N10 and N12 are made fully symmetrical in layout through the use of dummy interconnects.

To prevent the oscillator load from reducing f_0, the source followers N15 and

N16 are placed within the oscillator layout to reduce their gate-connection lengths.

4.2.5 Simulation Results and Analysis

Figure 4-10 shows the transient simulation results from Cadence SpectreRF™, for both the single-ended and differential output voltages. Figure 4-11 shows the PSS results, with f_0 = 5.929 GHz, $V_{pp,diff}$ = 536.7 mV, THD = 0.6% (–44.4 dB). The output current of G_M, in contrast, has a THD of 6.2% (–24.2 dB), showing that G_M is acting as the amplitude limiter as designed. I_{out} of G_M lags the G_M input voltage ($V_{oa} - V_{ob}$) by 41.7°, because the effect of the C_{gd}s is included in I_{out} of G_M, which cannot be extracted from simulation. The output current of G_M is

$$I_{out} = \left(g_m - j\omega_0 2C_{gd}\right)V_{Gate} \tag{4.14}$$

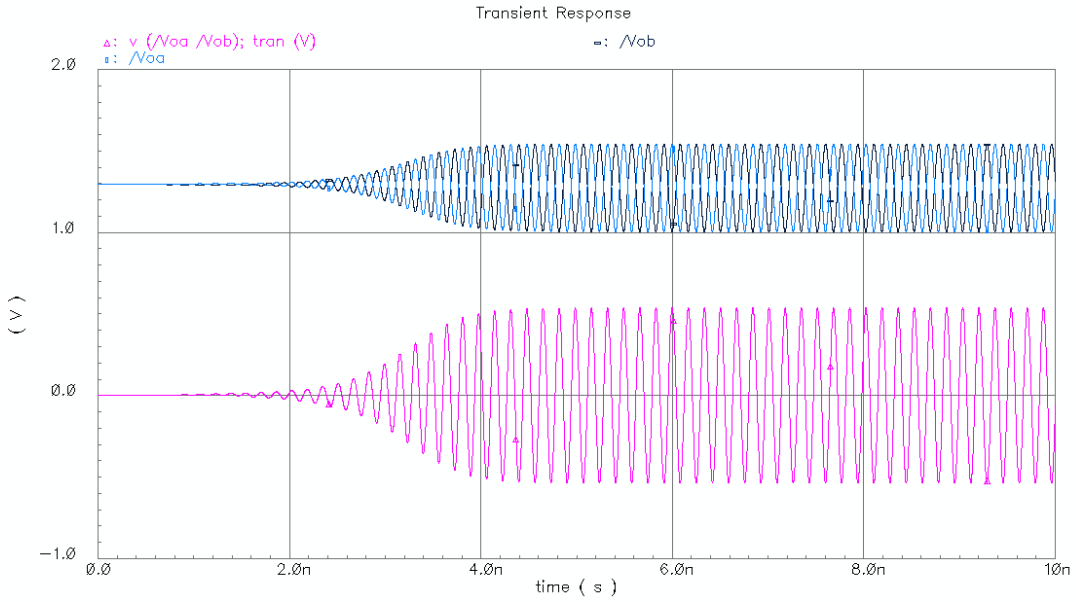


Figure 4-10 Transient simulation results of the oscillator (OSC0.2).

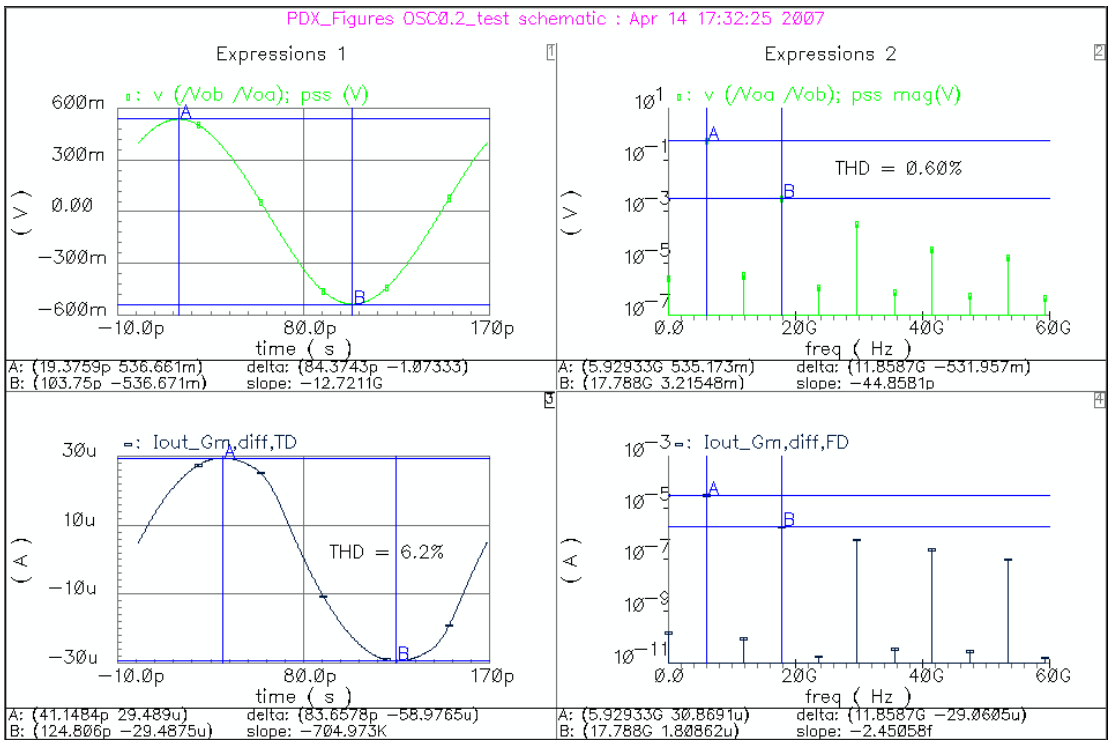


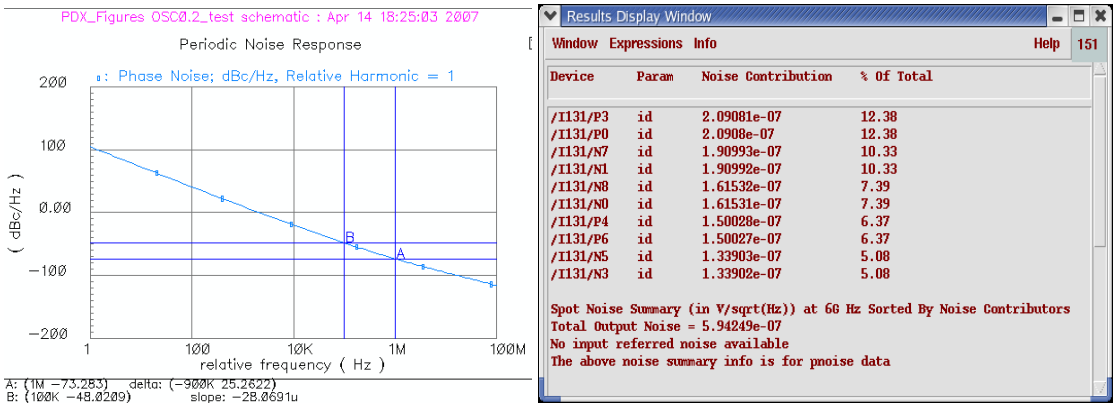
Figure 4-11 PSS simulation results of the oscillator. (1) Output voltage $V_{oa} - V_{ob}$ in time domain. (2) Spectrum of $V_{oa} - V_{ob}$. (3) Output current of differential-pair G_M in time domain. (4) Spectrum of G_M output current.

The factor of 2 arises from the fact that due to the cross connection, V_{gate} and V_{drain} of the G_M cell are complementary. Per the discussion in Section 4.2.2, the C_{gd}s can be absorbed by active inductor C_p and thus the G_M phase lag is in fact much less than the apparent value 41.7°.

In Fig. 4-11, when dividing I_{out} = 29.5 μA by the G_M input voltage $V_{oa} - V_{ob}$ = 536.7 mV we get the effective transconductance $G_{M,eff}$ = 54.97 μS, contradicting the value of 57.3 μS at the signal amplitude of 236 mV, as predicted by Fig. 4-9(b). The apparent paradox is again due to the parasitic capacitances C_{gd}s of N10 and N12, which generate an orthogonal current and inflate the observed I_{out}, per Eq. (4.14). Since we know that the angle of I_{out} is about 41.7° from simulation, we have

$$G_{\mathrm{M,eff}} = \frac{29.5\ \mu\mathrm{A} \cdot \cos 41.7^{\circ}}{536.7\ \mathrm{mV}} = 41\ \mu\mathrm{S} \tag{4.15}$$

very close to the Fig. 4-9(b) prediction of 40.65 μS.



(a) (b)

Figure 4-12 (a) Phase noise of the oscillator. (b) Noise summary.

Figure 4-12(a) shows the phase noise, which is –73.28 dBc/Hz at 1 MHz offset from f_0, not very good compared with passive *L*-*C* oscillators, whose phase noise is around –100 to –110 dBc/Hz at 1 MHz offset when f_0 = 1.6 – 2.4 GHz. But we will look at this issue further and see where the limitation to good phase noise comes from. Figure 4-12(b) shows the noise summary. The top ten noise contributors are all primary FETs within the active inductor, therefore, there is not much one can do to reduce the phase noise without sacrificing something else.

Table 4-1 shows the calculated versus simulation results. The small-signal parameters are extracted from the dc operating points, and are almost the same as those of the active inductor, as the dc biasing is the same. There are a few minor differences because of the addition of the negative-resistor differential pair, which modifies the circuit biasing current by a small amount. The addition of the cross-coupled differential pair does change the biasing slightly. It is found that the

calculated f_0, oscillation amplitude $V_{o,a}$, and phase noise are all very close to the simulation results, confirming the validity of the analysis.

Table 4-1 Calculated versus Simulated Oscillator Parameters

	Para-meter	Unit	Value	Para-meter	Unit	Sims	Calc'd	Equ-ation
Active Inductor	g_{m1}	mS	**1.22**	GammaN		0.8786		(2.73)
	g_{m2}	mS	**1.09**	GammaP		0.9685		(2.73)
	g_{m3}	mS	**1.18**	K_{NF1}		3.6942		(2.69)
	C_1	fF	19.77	K_{NF2}		1.8471		(2.71)
	C_2	fF	**22.35**					
	C_3	fF	**20.30**	I_n	pA/ sqrt(Hz)	**10.85**	**10.448**	(4.9)
	g_1	uS	126.16					
	g_3	uS	**170**	f_0	GHz	**5.929**	**5.930**	(4.5)
	G	mS	**2.39**	ω_0	Grad/s		**37.26**	(4.5)
negative resistor	C_1 extra, (M_{i1}, M_{i2})	fF	3.52	R_p	Kohm		**33.35**	(4.6)
	g_1 extra, (M_{i1}, M_{i2})	uS	1.4	Q_R			**28.94**	(2.58)
	I_B	uA	15.8	$V_{o,a}$	mV	**267.6**	**263.47**	(4.7)
	G_{mi}	uS	81.4	Phase Noise @ 1 MHz offset	dBc/Hz	**-73.28**	**-74.35**	(4.13)
Adjusted Values	C_1	fF	**23.29**					
	g_1	uS	**127.56**					

4.3 Scaling of the Active-Inductor Oscillator

The active-inductor oscillation frequency f_0 is roughly proportional to the ratio of g_m/C, where g_m is the average FET transconductance, and C is the total effect of C_{gs}, C_{jd}, interconnect, etc. If the gate-overdrive voltage $V_{OD} = V_{GS} - V_{TH}$ is to be kept the same because V_{DD} is the same, we need to have $W \propto L$. Since [92]

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}),\ C_{gs} \approx \frac{2}{3} W \cdot L \cdot C_{ox} \tag{4.16}$$

we have

$$f_0 \propto \frac{g_m}{C_{gs}} \propto \frac{1}{L^2} \tag{4.17}$$

In reality, C_{gs} is only about 25-30% of the total capacitance. C_{jd} is proportional to W, not to $W \cdot L \propto L^2$ when V_{OD} is fixed. For this design, all high-frequency signal interconnect widths are at the minimum required by the topology design rules (TDRs), and the dc currents they carry are all well under electron migration (EM) limits, hence within the ranges in this design, the parasitic capacitance from interconnects does not scale. The overall effect is that when L increases, the f_0 reduction is less than the $1/L^2$ prediction. Put this in another way, if we further reduce all gate lengths by half, f_0 will increase, but to a value less than quadruple.

To validate the L scaling and provide a remedial plan in case device modeling and parasitic extractions are incorrect, the active-inductor oscillator was also designed with $L = 0.4$ μm, with the same power dissipation. The simulation results are shown in Fig. 4-13.

Another dimension of circuit scaling is power, which translates into transistor W. If V_{DD}, transistor V_{OD} and L are not changed, for the same circuit, we can double all transistor Ws, make the circuit consume doubled power and occupy doubled silicon area, and reduce the noise level by 3 dB [1]. Alternatively, we can scale W down, reducing the power dissipation and area, at the cost of a higher noise level. However, there are a few practical considerations that limit how small the oscillator can be.

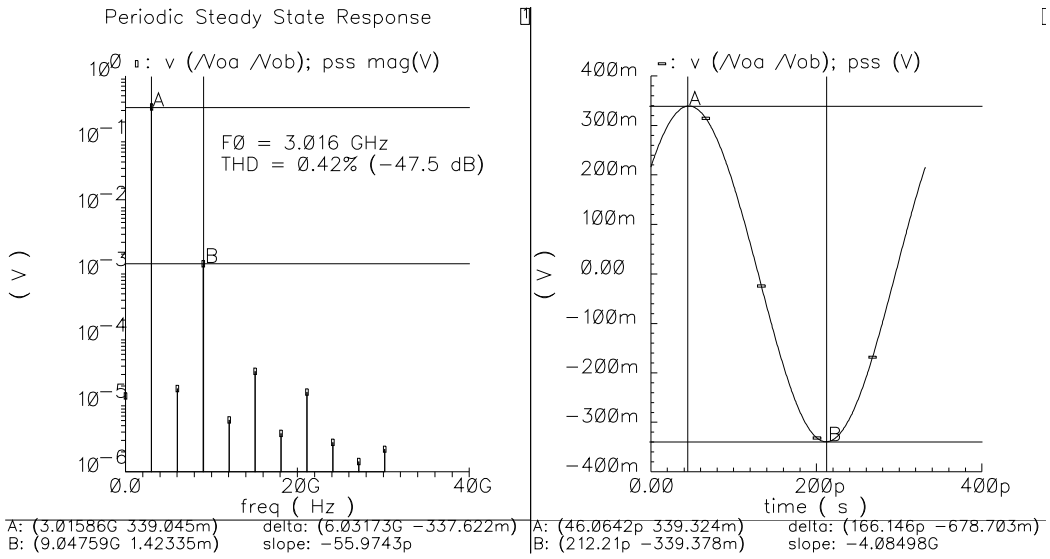


Figure 4-13 Simulation results of the L = 0.4 μm oscillator (OSC0.4).

First, for each particular IC process, TDRs set a limit on the minimum circuit feature size, be it a MOSFET or connection, and consequently transistor Ws cannot be arbitrarily small. Second, the external loading of 50-Ω from instruments does not scale and requires the same driving capability on the output buffer, thus a smaller core circuit will require a higher-performance buffer, since the driving capability of the core decreases and the input capacitance of the output buffer must reduce correspondingly. Third, the minimum-width interconnects can carry currents for MOSFETs much larger than their minimums, and the interconnect capacitance does not scale with W in the operating frequency equation:

$$f_0 \propto \frac{g_{\mathrm{m}}}{C_{\mathrm{gs}} + C_{\mathrm{jd}} + C_{\mathrm{interconnect}}} \tag{4.18}$$

Thus, within a certain range ($W \approx$ 0.2 - 16 μm and L = 0.2 μm), g_{m} scales with C_{gs} and C_{jd} linearly, with $C_{\mathrm{interconnect}}$ being a constant, and circuits using minimum Ws will be penalized with a lower f_0, because $C_{\mathrm{interconnect}}$ is a major portion in the total

capacitance and does not change. On the other hand, if *W*s are close to the upper limit (≈16 μm), f_0 will be higher and closer to the limit set by the active devices, but the circuit consumes more current. The OSC0.2 example uses W = 3 μm for primary NFETs, so we are closer to the low end of f_0 and did not fully explore the device potential. The reason of not using large *W*s is that due to the high f_0, power dissipation will become excessive (> 20 mW) when *W*s close to the high end is used.

4.4 Conclusion

Active inductors can be used to implement oscillators by means of a feedback scheme or negative resistor. The phase shift of the feedback scheme must be kept small, or the circuit may not oscillate at several GHz. To keep the harmonic distortion of the output voltage low, the negative resistor must be the amplitude limiter, not the active inductor. The oscillation frequency, amplitude, and phase noise of the active-inductor oscillator have been analyzed and the calculated results match the simulated results.

CHAPTER 5

IMPLEMENTATION AND LAB TESTING

5.1 The Need for Differential Signaling

All filters and oscillators are designed differentially to suppress noise coupling and double the dynamic range. This is especially important at several GHz, because the substrate and interconnects can act as a feed-forward "bridges" between filter input and output due to the parasitic capacitive coupling of the signals, as illustrated in Fig. 5-1(a). If all signals are differential and closely placed in layout, as shown in Fig. 5-1(b), the positive and negative signal lines will tug the local substrate in opposite directions and inject minimum capacitance-coupled currents into the substrate; thus there is very little substrate coupling. The cost is that the parasitic capacitances appearing to the differential signal nodes become larger, since they are now connected to virtual grounds instead of resistive substrate or other parts of the circuit through a metal connection.

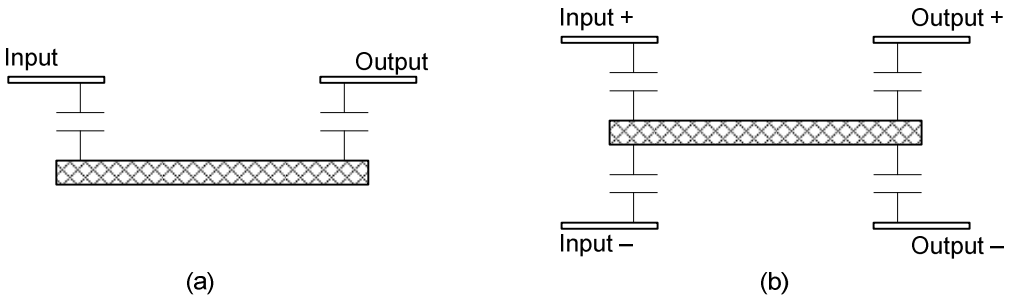


Figure 5-1 Substrate and interconnect coupling. (a) Single-ended circuit. (b) Differential circuit.

This principle in fact applies to any interconnects, such as power rails, that have to bridge two differential signals. It also applies to any signals that require isolation, not only between the inputs and outputs. The general rule is to keep differential signals

symmetrical and reasonably close (not so close as to incur unnecessarily large parasitic capacitance); if there is any coupling to other interconnects, the coupling should be kept symmetrical, even at the cost of placing dummy metals and incurring extra capacitances.

5.2 The Input and Output Buffers Design

5.2.1 The Need for Input and Output Buffers

Since all the core circuits are designed differentially and the testing instruments are single-ended (differential Vector Network Analyzers, VNAs, are commercially available, but expensive at this time), we need to convert the input signals to the filters from single-ended to differential. This is commonly done by "baluns" at RF. Since we do not have access to differential (GSGSG, G-ground, S-signal) microprobes, to use a balun, the differential input signals will have to be connected to bondpads that will have to be accurately characterized. Further, a bondwire will have a bandpass effect due to its inductance. To mitigate the risks, we decided to use a single-ended (GSG) microprobe to inject the input signal, and design an on-chip input buffer to implement the single-ended-to-differential conversion. The input buffer must provide the proper termination resistance to the input to prevent signal reflections and the correct signal common-mode voltage to the filter-core inputs, as shown in Fig. 5-2. Ideally, the input buffer should provide a pair of differential output signals that are equal in amplitude, and out of phase by 180°, for all frequencies processed by the RF filter.

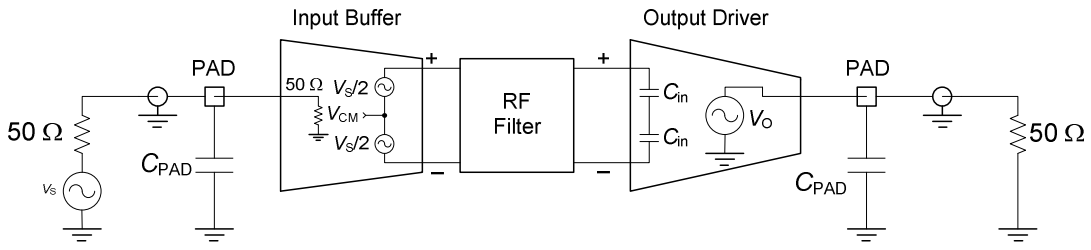


Figure 5-2 The need for input and output buffers/drivers.

An on-chip output driver is needed to convert the differential signals back into a single-ended signal, and more importantly, to drive the 50-Ω load plus the large probe-pad parasitic capacitance (≈ 170 fF). Its input capacitance presented to the RF filter core must be very low so as to minimize reducing f_0. Ideally, its transfer function from the inverting and noninverting inputs to the output should be equal in amplitude and phase (excluding the 180°), at all frequencies of interest to the filter.

The filters will need both the input buffer and output driver, and the oscillators will need the output driver only.

5.2.2 The Input Buffer Design

The most difficult part of the input-buffer design is to obtain fully symmetrical differential output signals at 1-7 GHz using only active devices, i.e., the function of a balun. Between roughly 20 and 500 MHz, transformers with double secondary winding can be used to implement baluns. For higher frequencies, microwave devices, such as the 180° Hybrid [85], can be used to implement balun functions. Both can produce theoretically fully symmetrical differential outputs. However, for this design, the differential outputs cannot be fully symmetrical since only transistors can be used.

As shown in Fig. 5-3, a signal-inverting mechanism is required for the inverting

output path. It could be part of the signal driver function or separate, but in either case, the two signal paths are not fully symmetrical, because the basic MOSFET circuitry cannot implement inverting and non-inverting functions using the same topology. The inverting output will experience more delay, and a different (usually higher) attenuation, thus for a certain sinusoidal input test signal, V_{O+} and V_{O-} will be different in amplitude and phase. The amplitude and phase differences will vary with frequency as well, as the signal-inverting block, its loading to the input and loading by the signal driver are all functions of frequency. When the differential inputs are not fully symmetrical, the filter operation is degraded due to the equivalent common-mode RF signal input. Our goal is to make the amplitude and phase differences as small as possible from 1 to 7 GHz.

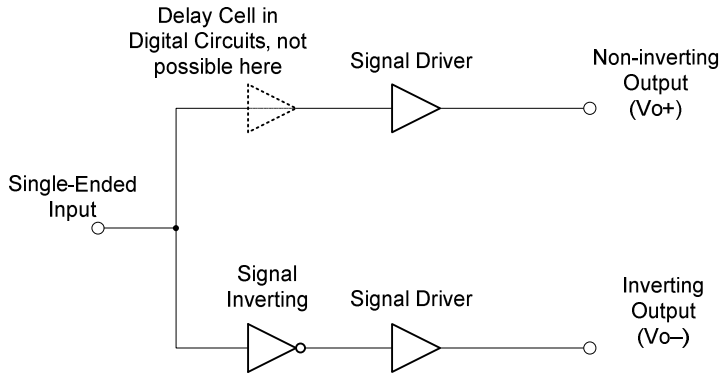


Figure 5-3 The signal path of single-ended to differential conversion.

Note that a common technique used in the digital circuitry is to insert a delay cell in the non-inverting path, as shown in Fig. 5-3, to balance the delay from the inverting block, which is a CMOS inverter. The delay cell is a CMOS pass-gate switch in the ON state, with identical MOSFETs as those of the CMOS inverter. This technique can improve the differential pulse signal matching significantly, but cannot be used here

since the signals are sinusoidal and inverter outputs will become pulses.

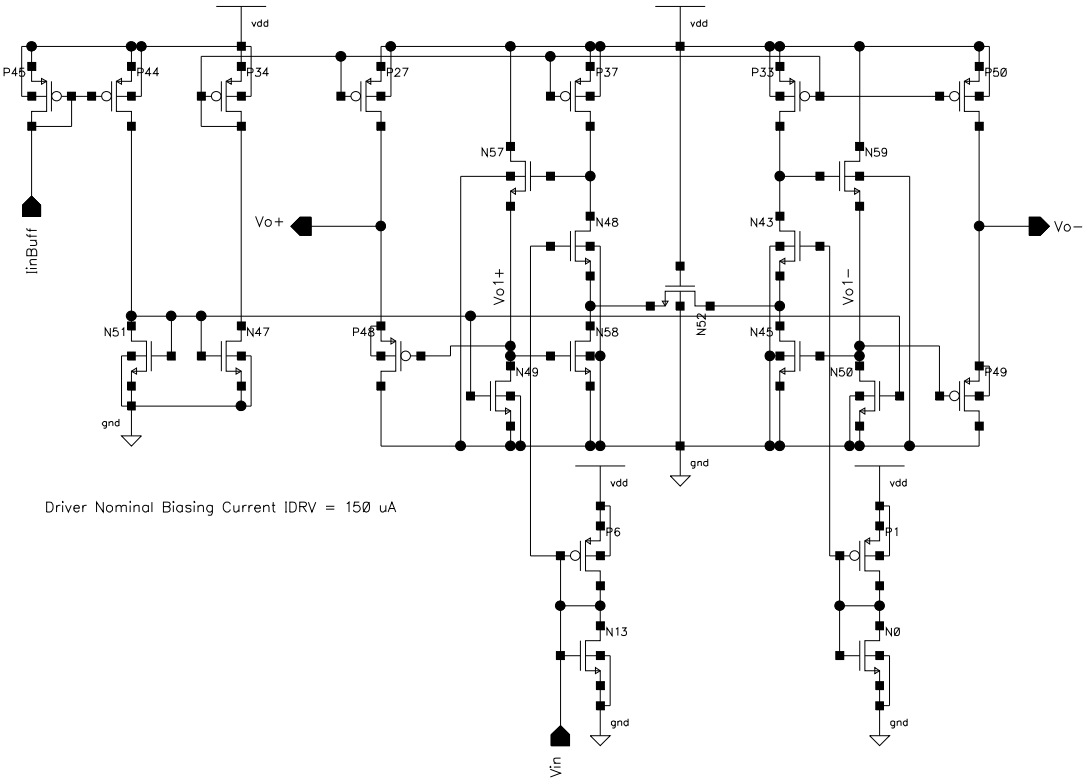


Figure 5-4 The input buffer circuit schematic.

The complete schematic of the input buffer is shown in Fig. 5-4. The input signal is connected to the drains of N13 and P6, which are both diode-connected. By proper biasing and choice of aspect ratio, N13 and P6 provide a resistance around 50 Ω for input matching and a common-mode voltage of 1.1 V to N48 and N43. The core of the circuit is a differential transconductor [46], with one input connected to ac ground at P1 and N0. The signal-inverting function is implemented through the differential structure. N52 operates in the linear region and is a resistor. Different from the transconductor, which has NFETs mirroring the I_{ds} of N58 and N45, the gate voltages of N58 and N45 are buffered using source followers (P48 and P49) as output voltages. P48 and P49 also provide the desired common-mode voltage of 1.35 V to the filter.

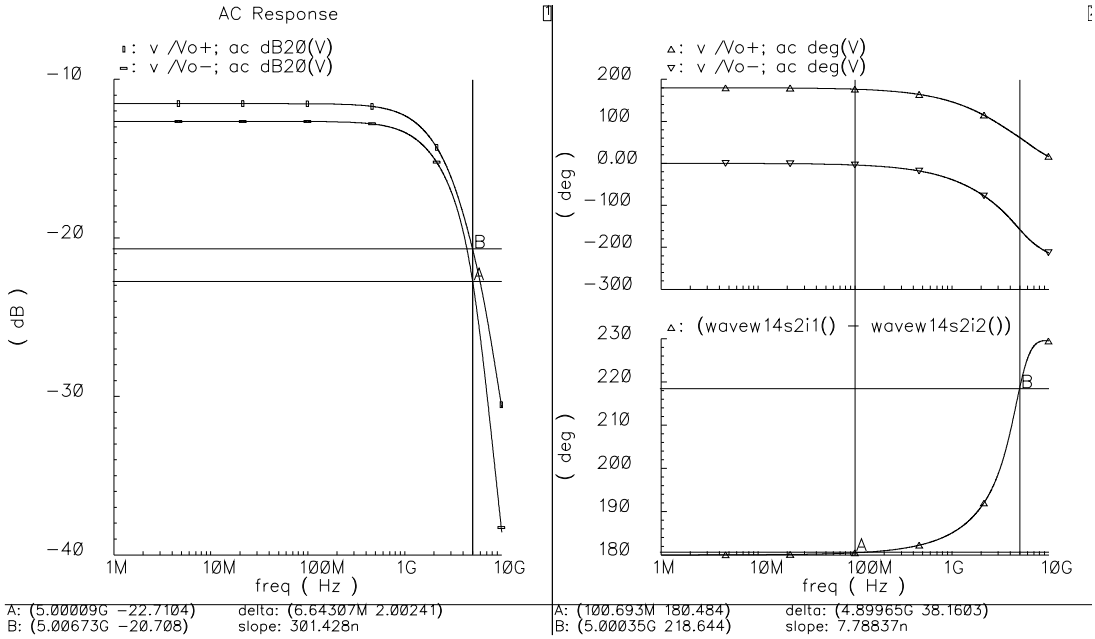


Figure 5-5 ac simulation results of the input buffer: magnitude (left) and phase (right).

This circuit is chosen mainly for its symmetry of the differential outputs. The simulation results are shown in Fig. 5-5. The two output magnitude and phase differences at 5 GHz are 2 dB and 38°, respectively, not ideal, but close enough and are the best among the possible choices. The balun function design is non-trivial due to the high operating frequency.

5.2.3 The Output Buffer Design

The fundamental issue in designing the output buffer is to obtain some voltage gain, or rather, an acceptable level of attenuation, at 1-7 GHz, when driving a load of 50 Ω plus a capacitance of a few hundred fF with a low C_{in} of less than 10 fF. To a lesser extent, the individual transfer functions from the two differential inputs to the single output should have equal amplitude and be 180° out of phase, and the gain profile should be as flat as possible from 1 to 7 GHz. MOSFETs need gate voltage (V_{gs}) to

generate output current, and in turn, gain. However, at these frequencies, the load, $|1/(j\omega C_{gs})|$ becomes very low, and hardly any voltage can be generated; hence it is difficult to obtain gain from cascade stages.

A 10 M – 18 GHz dc blocker will be inserted in the output path, so the 50-Ω load will not draw dc currents due to a non-zero signal common-mode voltage. Passive inductors cannot be used to neutralize the load capacitance and expand the bandwidth through "shunt peaking" [16, 83] because the resulting buffer will be narrow-band and inductors are not available in the TSMC LOG018 process. A wide-band buffer is required since a large simulation-silicon discrepancy is expected and we do not know beforehand what f_0 shift to expect.

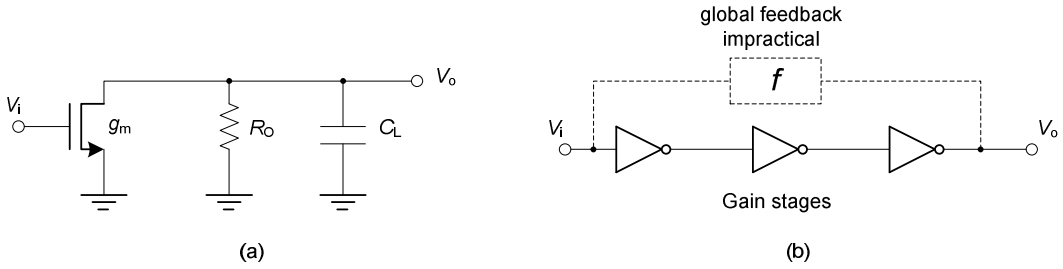


Figure 5-6 (a) A single gain stage. (b) Cascaded gain stages.

Figure 5-6(a) shows the simplified equivalent circuit of a single-amplifier stage. The FET has to be in CS configuration, since CG or CD configurations have less gain. The output is loaded with R_O, which includes g_{ds} terms, but more likely, also an intentional small resistance from other transistors. The transfer function is

$$T(s) = \frac{g_m / C_L}{s + \frac{1}{R_O C_L}} \tag{5.1}$$

and two examples are shown in Fig. 5-7. A lower $R_O \approx 1/g_m$ will yield a wider bandwidth ($f_{-3\ dB}$) but also incur some extra parasitic capacitance because the C_{jd} from

a current-source load will become C_{gs} or some other larger capacitance, but it will never increase the absolute gain at frequencies from 1-7 GHz. However, relatively low R_O has to be chosen because otherwise the dc gain will be too high, and possibly saturate the dc operating point of the driver when multiple stages are cascaded, as illustrated in Fig. 5-6(b).

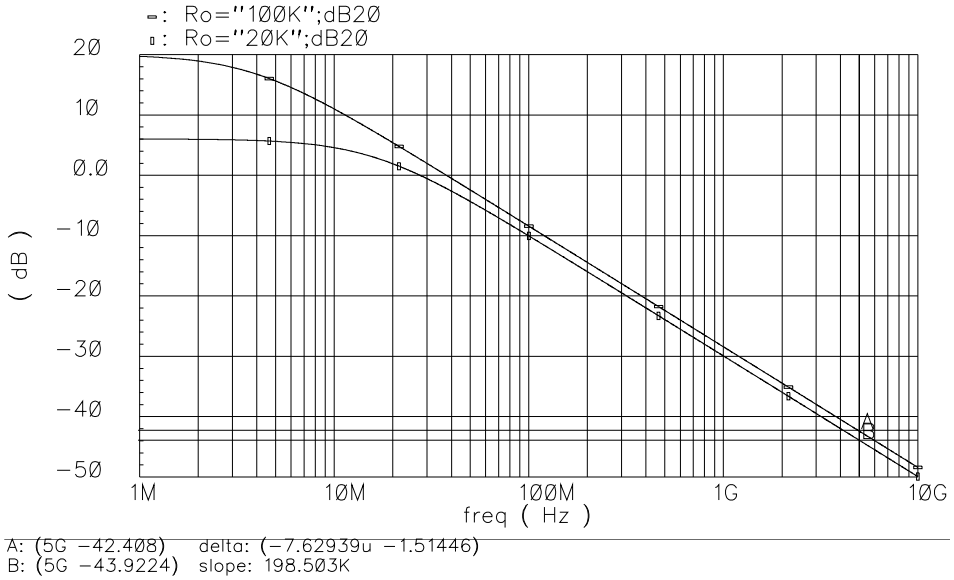


Figure 5-7 The frequency response of the circuit in Fig. 5-6(a). C_L = 500 fF and R_O = 20 kΩ; C_L = 420 fF and R_O = 100 kΩ.

To increase the absolute gain at 5 GHz, we can increase g_m, but that means a larger transistor has to be used, and presenting a larger load to the filter core. Or we can cascade a few stages, to boost the driving capability, but the attenuation at 5 GHz will increase, because the voltage gain of each stage at 5 GHz is less than 1. Therefore, a delicate balance between keeping C_{in} low and using more stages has to be stricken.

One may suggest that high-dc-gain stages be used, and then using feedback to make the gain profile flat and expand the $f_{-3\,dB}$, as shown in Fig. 5-6(b). This proves to be impossible to implement at 1-7 GHz, as stability cannot be maintained due to the

phase shift of the circuits at these frequencies. Local feedback was judiciously used in the final circuit.

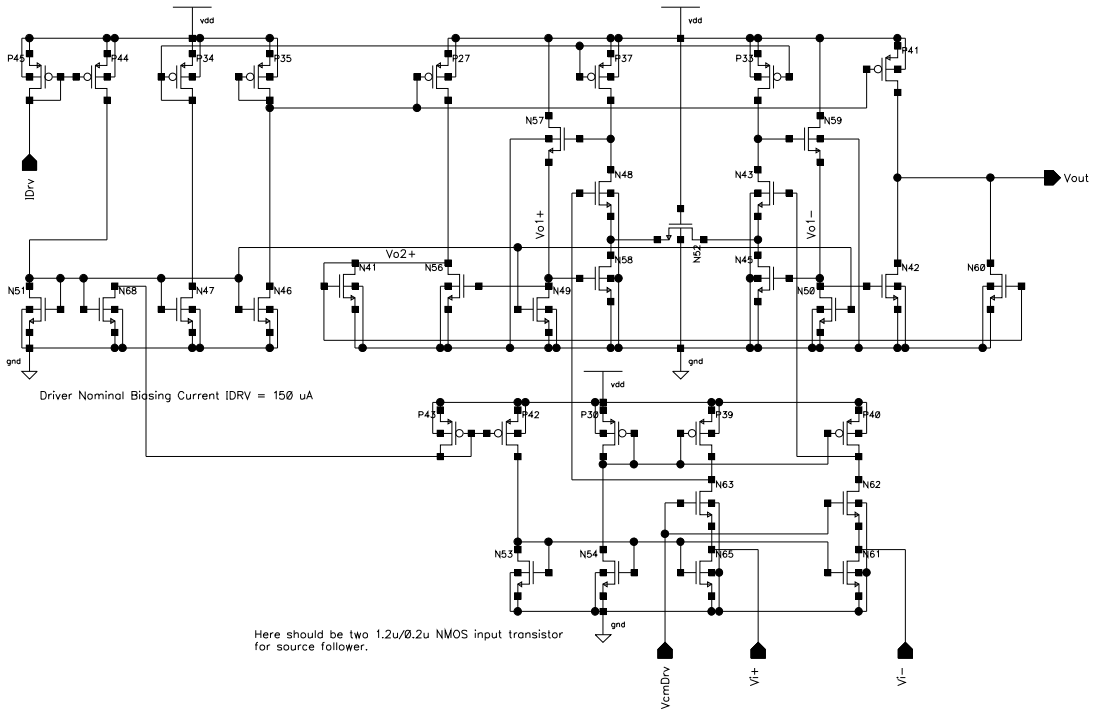


Figure 5-8 The output-driver circuit schematic.

The output-driver circuit is shown in Fig. 5-8. Current sources N65 and N61 are the load of the source followers, and cascode devices N63 and N62 convert the source follower voltages into currents into the C_{in} of the driver core. The driver core is again a transconductor [46], with one of the outputs mirrored back to the same node as the other output via N41 and N60. The only internal node of the signal-inverting circuit, V_{o2+}, is low-impedance, to ensure that its pole frequency is far higher than the dominant pole at V_{out}.

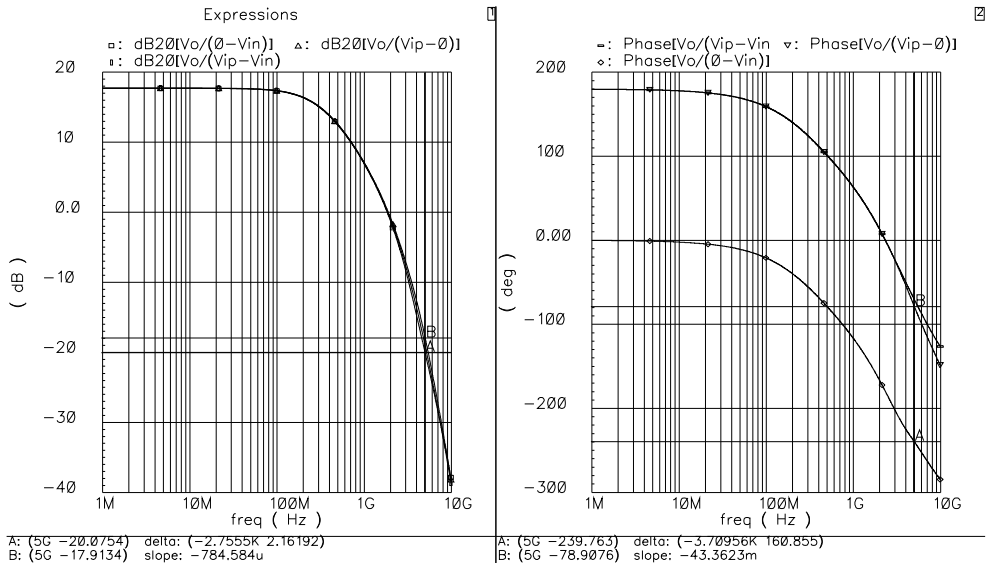


Figure 5-9 The simulation results of the output driver. Panel 1: cursors A and B are gains from single-ended input on the V_{ip} and V_{in} terminals, respectively. The differential-input gain, $V_o/(V_{ip} - V_{in})$, is –19.05 dB.

The ac simulation results of the output driver are shown in Fig. 5-9. It is seen that the gain difference and phase errors at 5 GHz for the two differential input terminals are 2 dB and 20°, respectively, and the gain at 5 GHz is about –19 dB.

Similar to the input buffer, the output driver is not ideal. It was selected based on the stringent requirements and various tradeoffs.

5.3 Circuit Modules Design

Due to the lack of confidence in the available device models and parasitics-extraction data, the active-inductor filter and oscillator are both designed in several different versions: gate length L = 0.2 μm and 0.4 μm, regular Q and higher Q. As an example, Fig. 5-10 shows the regular-Q 0.2-μm bandpass filter module (BP0.2), which consists of three cascade blocks: the input buffer, the filter, and the output driver.

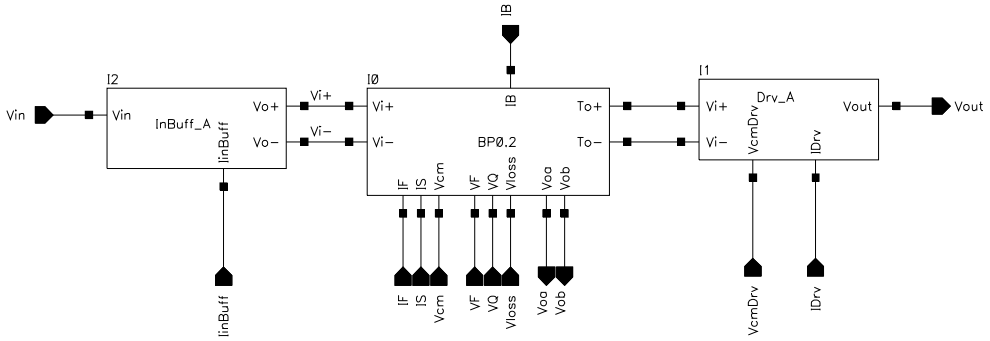
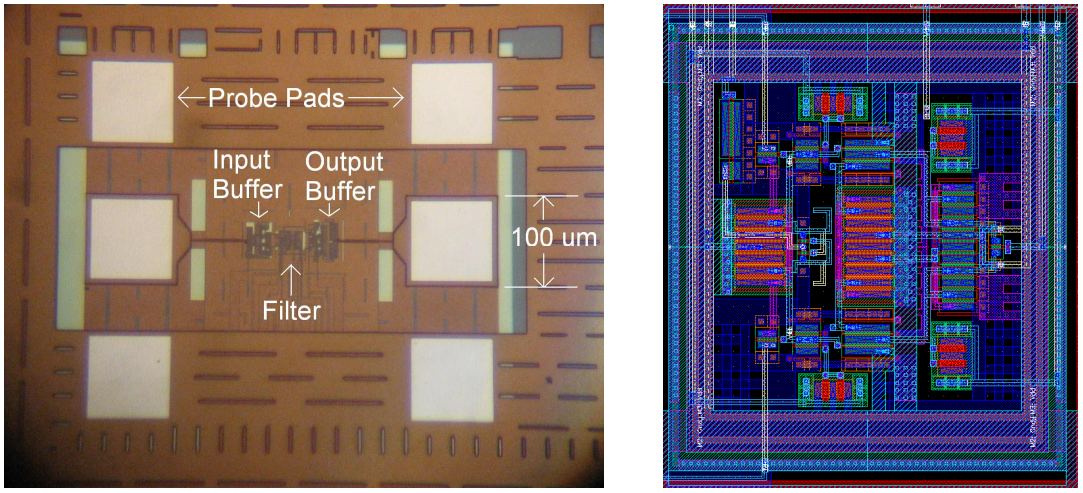


Figure 5-10 Regular-*Q* 0.2-μm-gate-length bandpass-filter module (BP0.2).



(a) (b)

Figure 5-11 (a) The 0.2-μm-bandpass-filter (BP0.2) module layout (microphotograph). (b) The BP0.2 filter-core layout (screen capture).

The module's layout is shown in Fig. 5-11. The active-inductor filter core occupies 26.6 μm × 30 μm, including biasing and tuning transistors. In contrast, a spiral inductor alone typically occupies 300 μm × 300 μm. In doing the circuit layout, the following considerations should be attended to simultaneously:

1. Parasitic capacitance should be minimized to maximize the operating frequency. The layout should be generally compact; however, there is a tradeoff between reducing length of interconnects and reducing the lateral capacitance between metal traces. Since the capacitance is inverse proportional to the spacing, high-

frequency trace spacing is maintained at twice or more the TDR minimum when possible.

2. To reduce drain-diffusion capacitance, MOSFET drains should be shared whenever possible.
3. Device and interconnect layouts are symmetrical for the differential circuit. Due to the low device count, generally a common-centroid method cannot be used, but symmetry should be maintained. Dummy poly strips should guard peripheral transistors to ensure that their gates are similar to those of the internal ones [93].
4. Metal widths should be carefully evaluated for each connection: the width should be low to reduce parasitic capacitance, but should be wide enough to comply with electron migration rules, and more frequently, not to introduce any excess dc voltage drop.
5. Long signal wires should be routed using top metal layers to reduce their capacitance to the substrate. Metal isolations may be used to decouple signals.

It is noted that all of the above considerations are tradeoffs and should be evaluated on a case-by-case basis. There are no fixed rules as to what is best.

5.4 Chip Level Design

Since each active-inductor oscillator or filter module has about 9 biasing terminals, 10 modules would need a 90-pin package. PGA (pin grid array) packaging can provide more than 90 pins, but it requires expensive mounting and PCB (printed circuit board) technologies. To keep the logistics work simple, a 40-pin dual-in-line package (DIP40) is used, and the biasing pins are multiplexed among the modules, as shown by

the chip-level schematic in Fig. 5-12. The chip-level schematic is also important for layout verification. As shown in Fig. 5-13 (a), to satisfy the layer-density requirement by the foundry and create decoupling capacitance, the power and biasing nets need to be expanded and blanket the entire chip, for poly and all 6 metal layers. Due to the vast variation in layout scale between filter/oscillators cores and the entire chip, short- or open-circuit mistakes often happen, and LVS (layout versus schematic) checker will report these as discrepancies, even though locating a short-circuit place is still not easy and requires experience.

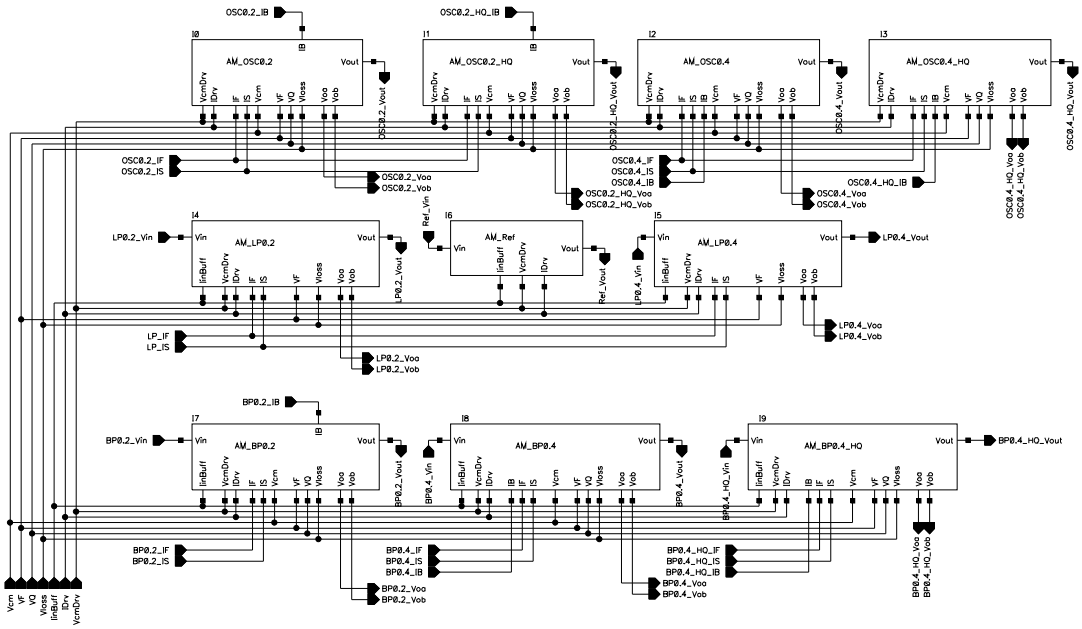
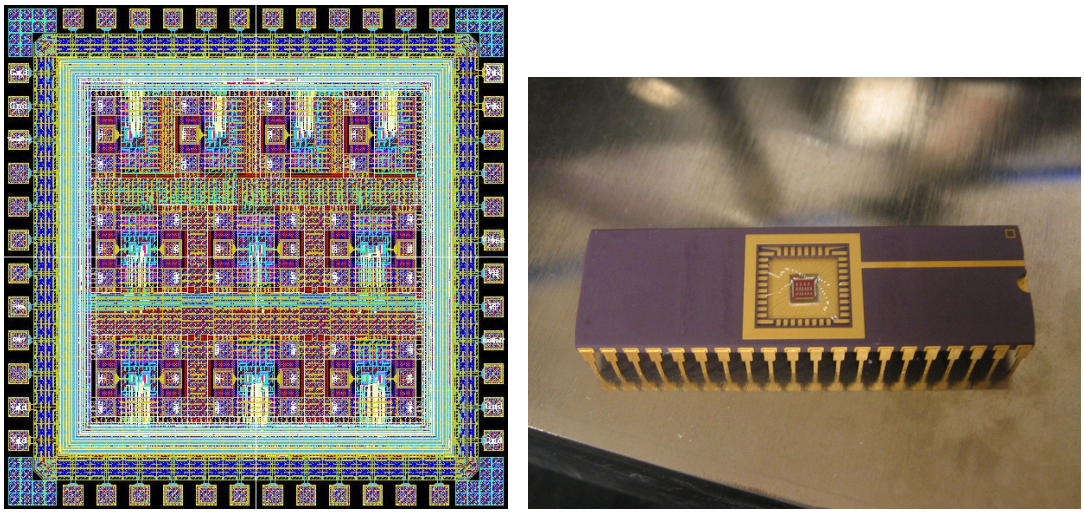


Figure 5-12 The chip-level schematic.



(a) (b)

Figure 5-13 (a) The test-chip layout including probe pads and bond pads. (b) The packaged test chip (1 out of a lot of 40).

The chip-level design involves the following aspects:

1. Floorplanning: the test chip area is 7 mm^2 and needs to be shared among bond pads, power rails, test modules including their probe pads, and separation between the test modules. These layout elements need to be properly organized to allow for an orderly implementation of various requirements.
2. Bondpads and probe pads: there were no library pads by the time of tapeout, so all pads are created manually. The pads are stacks of every available metal layers stitched together by vias at a density and pattern dictated by the foundry. The signal pads of RF microprobe pads contain only the top-layer metal (metal-6) to reduce their parasitic capacitance to the substrate, but need to have a metal-1 ground shield to decouple them from the substrate. All bond pads have ESD (electro-static discharge) protection diodes which are located beneath the power rails.

3. Power and signal busses: they need to be sufficiently wide to reduce the dc voltage drop. The busses are arranged in concentric rings to even the voltage drop and reduce connection resistance.
4. Layer density compliance: all physical layers (poly, metals 1-6) need to occupy a pre-defined percentage of the overall reticle as required by the chemical planarization step during fabrication. This is done by expanding the power and ground nets, with an added benefit of noise filtering.
5. Wide metal stress and separation rules: to prevent mechanical stress and damages during thermal cycles, metals spanning more than 25 μm in either the x or the y direction need to have slots in between. The minimum spacing is doubled when either adjacent metal strip is wider than twice the minimum, to reduce the chances of short circuits. These two design rules are not implemented in the tool package and have to be manually added to the rule files.

5.5 Biasing and Lab Testing

As shown in Fig. 5-14, a small daughter-PCB board is designed to hold the test chip under the microscope. A 3-foot-long 40-wire-wide flat cable is used to connect the daughter board to a mother board, which contains a number of switches and potentiometers to allow quick permutations of the test setup for the different modules. 25-turn precision potentiometers are used for generating biasing voltages and currents, which are monitored by a multimeter, so that currents and voltages can be adjusted with resolutions up to 0.1 μA and 0.1 mV, respectively.

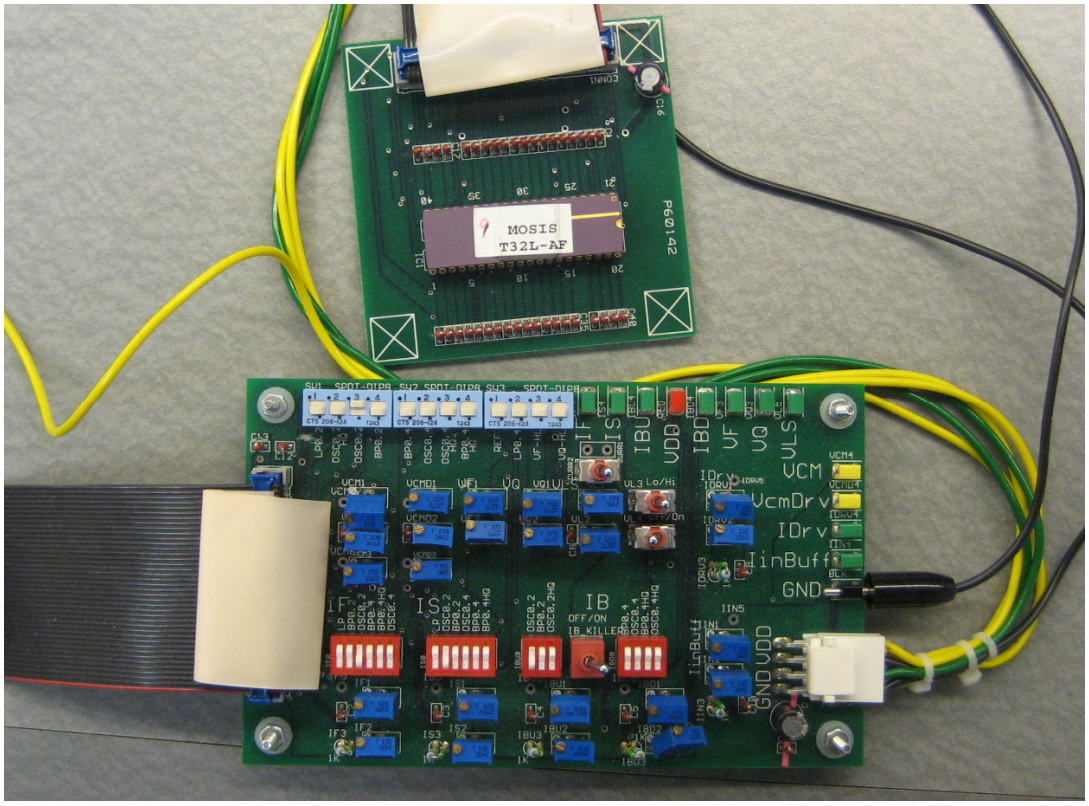


Figure 5-14 Biasing circuit for the test chip. The small circuit board carries the test chip and goes under the microscope. The larger circuit board generates tunable biasing voltage and current.

Microprobes are used to gain access to the test circuit modules for RF signals and connect them to the appropriate instruments, such as a VNA (vector network analyzer) and spectrum analyzers.

5.6 Test Results

5.6.1 5-GHz Active Inductor Oscillator (OSC0.2, L = 0.2 μm)

Figure 5-15 shows the output spectrum of a 5-GHz oscillator, at the same nominal biasing as the active inductor in Fig. 2-29, with I_B = 80 μA. The oscillation frequency of 5.645 GHz is about 91% of the simulation results as we shall see below. The phase noise is –66.6 dBc/Hz at 1-MHz offset, measured with an Agilent™ 8562EC

Spectrum Analyzer. The oscillator module is simulated at the same biasing conditions with output buffer and load, as shown in Fig. 5-17. The simulation results are shown in Fig. 5-18 for comparison.

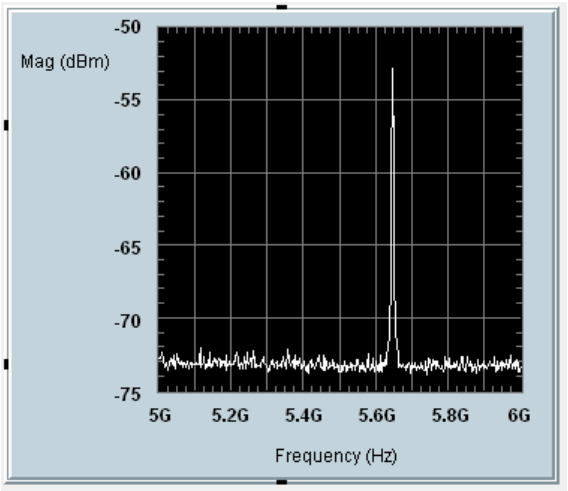


Figure 5-15 Output spectrum of a 5.6-GHz oscillator (including a 50-Ω output driver). The center frequency is f_0 = 5.645 GHz, the magnitude is –52.78 dBm, corresponding to a peak voltage of 134 mV at the circuit core. The attenuation of the output buffer at 5.645 GHz is 39.3 dB. The 2nd and higher harmonics are below the noise floor (≈ –73 dBm). (Data Ref# OSC0.2-C22-SPA-00040)

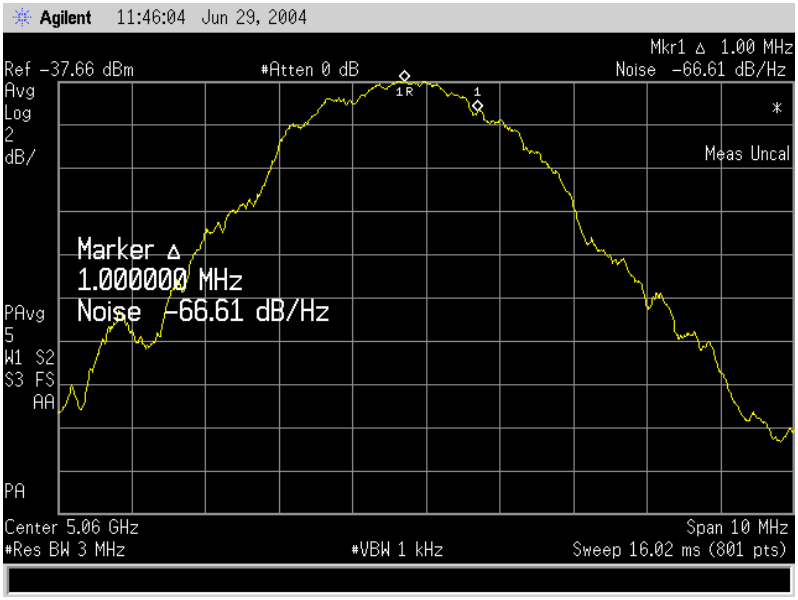


Figure 5-16 Measured phase noise of the 5-GHz oscillator, including the output buffer.

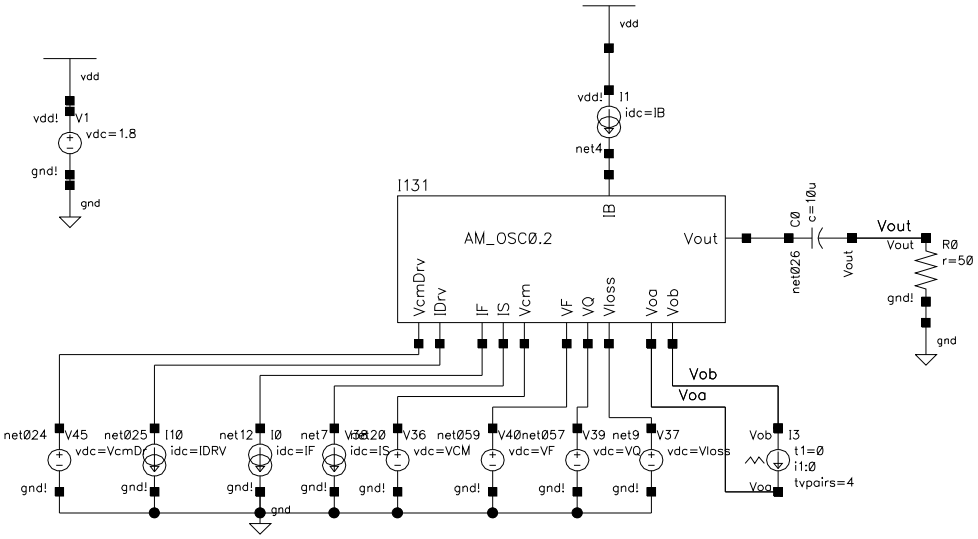


Figure 5-17 Test-bench configuration for the 5-GHz oscillator (L = 0.2-µm).

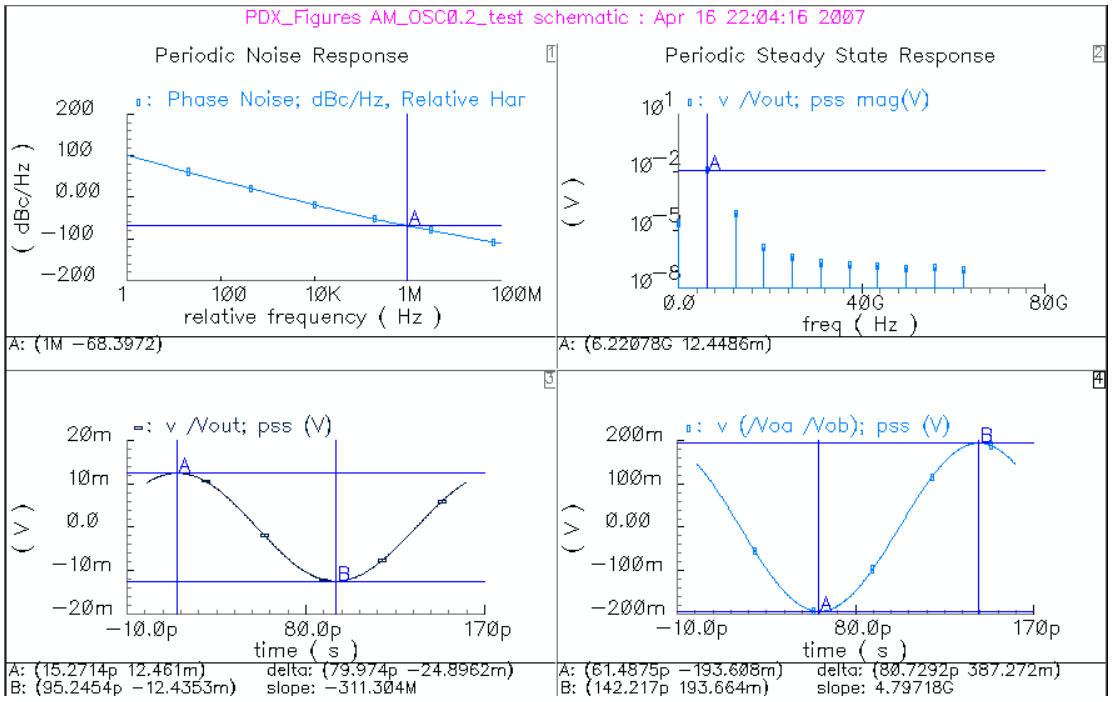


Figure 5-18 Simulation results of the fabricated 5-GHz oscillator with output buffer and load.

The signal amplitude on the 50-Ω load is 12.45 mV, corresponding to –25.1 dBm. The output-buffer gain is calculated to be –23.8 dB, close to the simulation result of –24.8 dB at 6.22 GHz. The phase noise is –68.4 dBc/Hz at 1 MHz offset,

about 1.8 dB better than the measured result. We note that a minor design flaw in the fabricated oscillator degraded the phase noise by about 4 dB, as shown in Figs. 5-19 and 5-20.

N13, N1, N4 and N7 in Fig. 5-19 are all biasing transistors, and they do not affect the active-inductor oscillator's frequency directly. Hence they do not have to be minimum-length devices. They are minimum length (0.2 μm) in the fabricated oscillator, but have tripled length (0.6 μm) and widths in the improved circuit in Fig. 4-8. The phase noise of the latter is lower by 4.1 dB, because these transistors contribute less flicker noise due to the increased gate area. The frequency is reduced by about 6% due to the use of 0.6-μm devices.

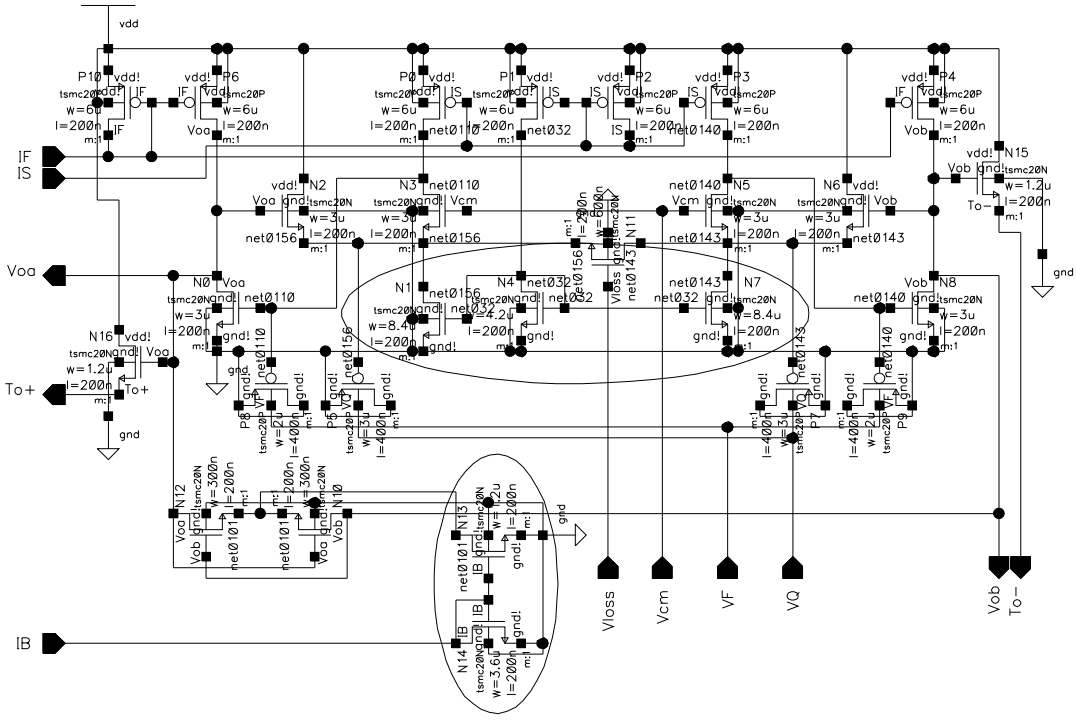


Figure 5-19 A minor design flaw in the fabricated oscillator, shown by the circle.

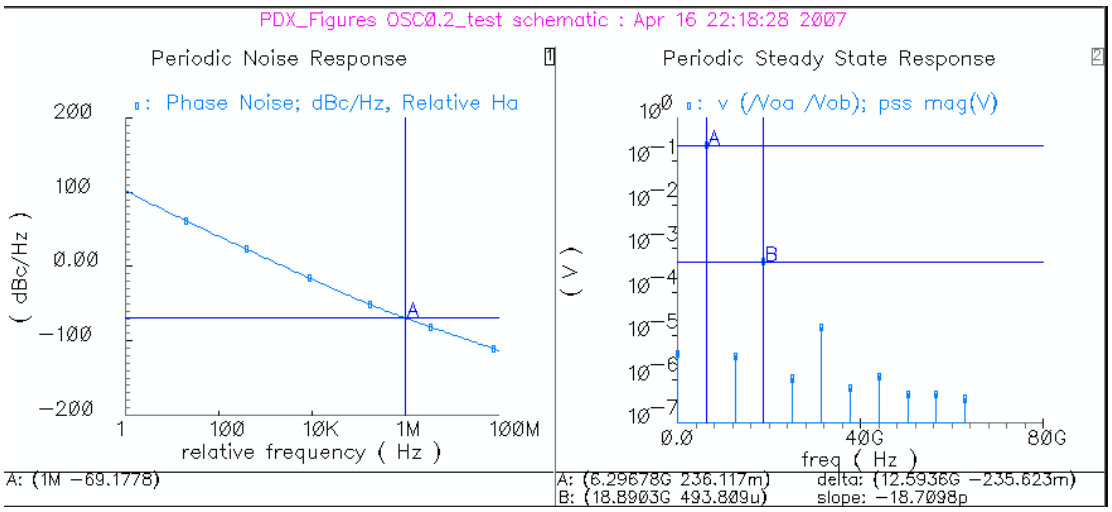
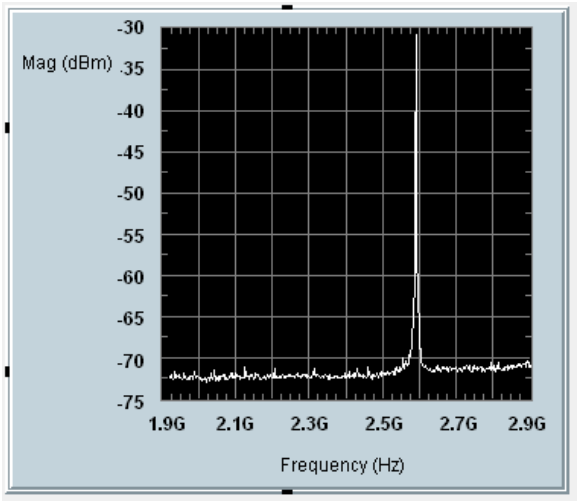


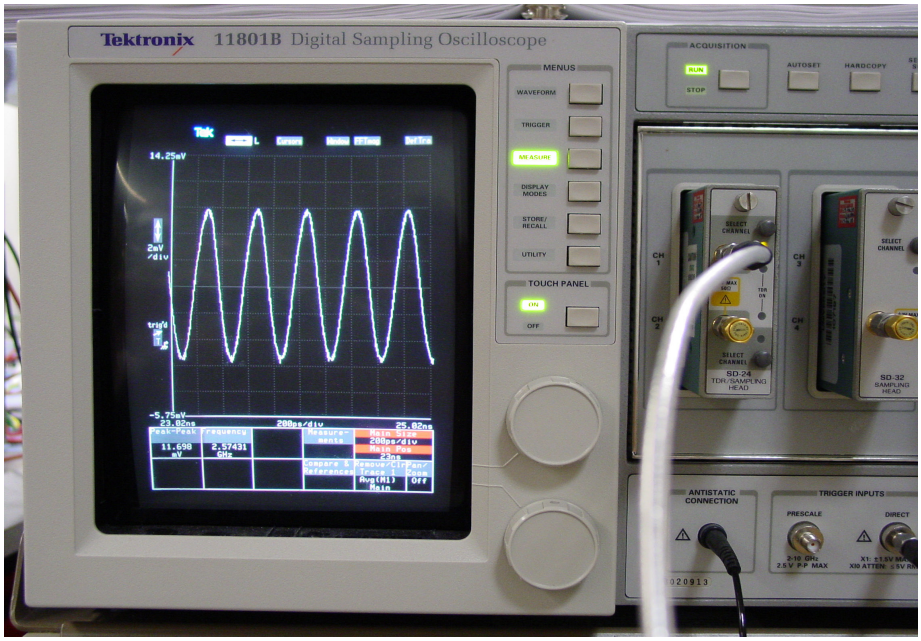
Figure 5-20 The simulated phase noise of the fabricated OSC0.2 core without output buffer is 4.1 dB worse than the example shown in Fig. 4-8 due to the smaller L in the tail biasing FET.

5.6.2 The 2.6-GHz Active Inductor Oscillator (OSC0.4, L = 0.4 μm)

Figure 5-21 shows the output spectrum of the 2.6-GHz oscillator. The measured frequency is 2.59 GHz, and the measured phase noise is –73.2 dBc/Hz at 1 MHz offset, as shown in Fig. 5-22. The simulated results are shown in Fig. 5-23. The 3.1-dB phase noise difference between simulation and measurement can be explained by the difference in their f_0s. Per Eq. (4.13), the phase noise is proportional to f_0. Thus if f_0 increases from 2.363 GHz to 3.036 GHz we should see an increase of phase noise by 20*log(3.036/2.363) = 2.2 dB.



(a)



(b)

Figure 5-21 2.6-GHz-oscillator lab results. (a) The output spectrum of the 2.6-GHz oscillator (with 50-Ω output driver), the center frequency is f_0 = 2.589 GHz, the magnitude is –30.79 dBm, corresponding to a peak voltage of 130 mV at the circuit core. (b) Output signal of the 2.6-GHz oscillator displayed on a Tektronix 11801B high-speed digital sampling oscilloscope. The measured signal has a peak-to-peak amplitude of 11.698 mV at a frequency of 2.574 GHz, corresponding approximately to a peak voltage of 186 mV at the circuit core when the power splitter and cable attenuation of 7 dB is deducted.

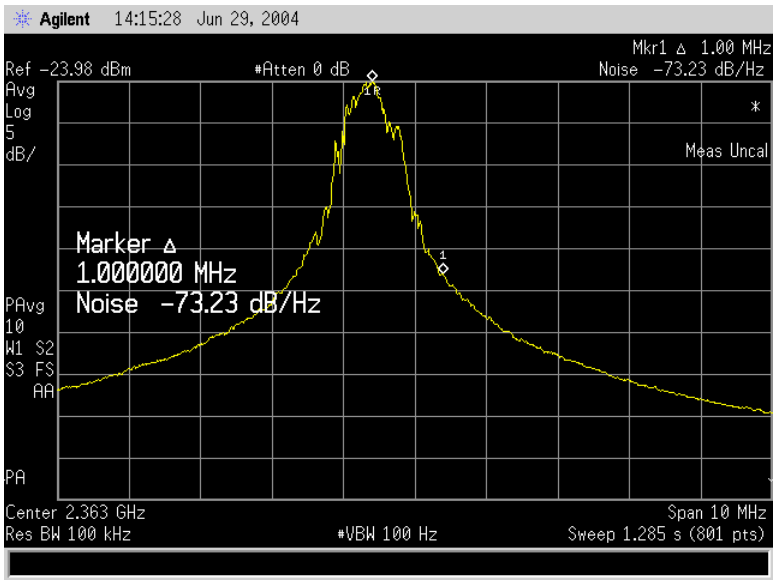


Figure 5-22 Measured phase noise of the 2.6-GHz oscillator (OSC0.4, L = 0.4 µm).

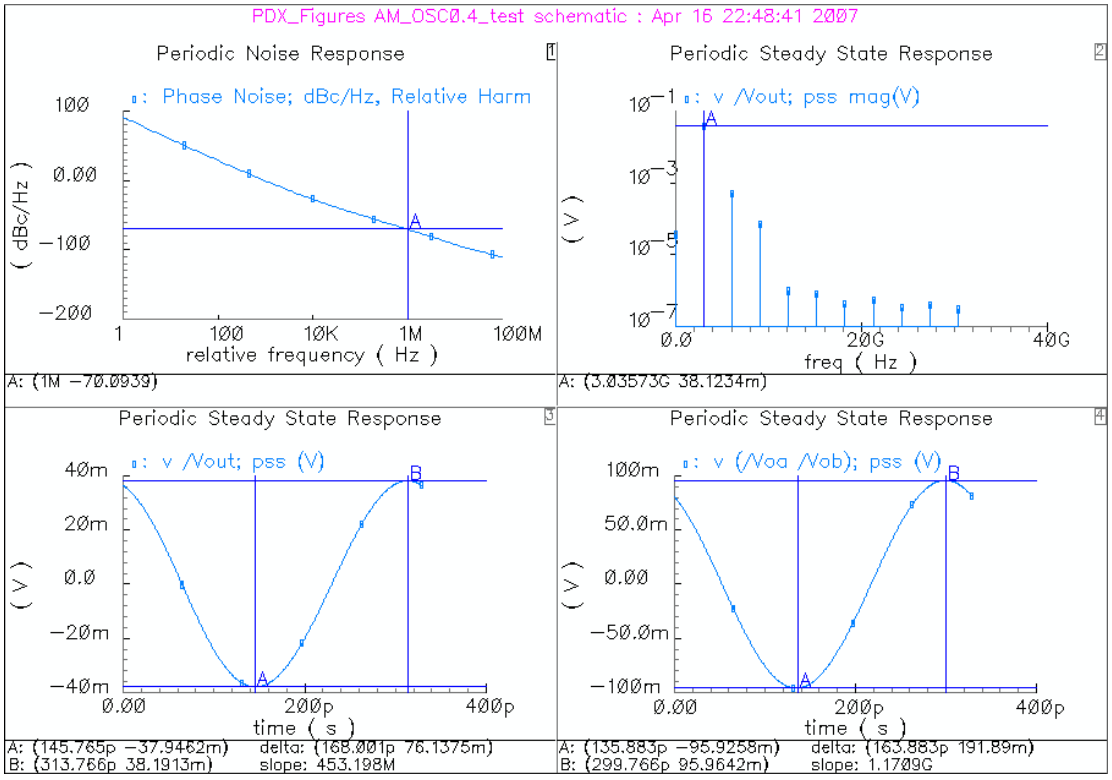
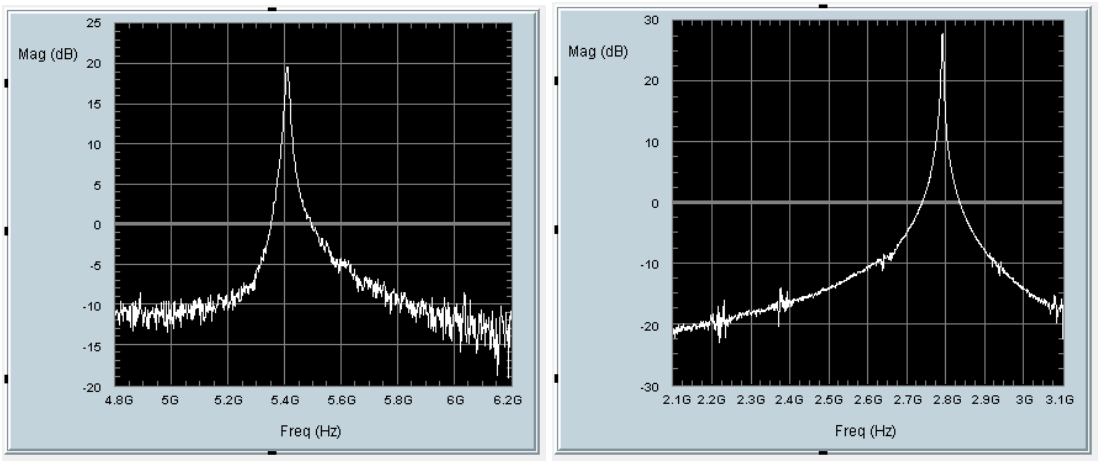


Figure 5-23 Simulation results of the fabricated 2.6-GHz oscillator with output buffer and load.

5.6.3 The High-*Q* Active-Inductor Bandpass Filters

Figure 5-24 shows the frequency profiles of the high-*Q* bandpass filters, for L = 0.2 μm and L = 0.4 μm, respectively. Figure 5-25 shows the f_0-variation when Q is tuned via the varactor voltage V_Q. V_Q changes C_2 in Fig. 2-28, and due to 2nd-order effects, changes f_0 by a small amount. Since the bandpass filter's Q is the active inductor Q_R modified by the extra parasitic elements from the input G_M and output buffer, the Q_R tuning characteristic of an active inductor will be the same (of course, we cannot measure Q_R directly).



(a) (b)

Figure 5-24 Measured frequency responses of the bandpass filters (S21). (a) L_{gate} = 0.2 μm, f_0 = 5.4 GHz, Q = 365; (b) L_{gate} = 0.4 μm, f_0 = 2.79 GHz, Q = 661. The midband gain is set at 20 to 30 dB for high SNR and can be adjusted via I_B.

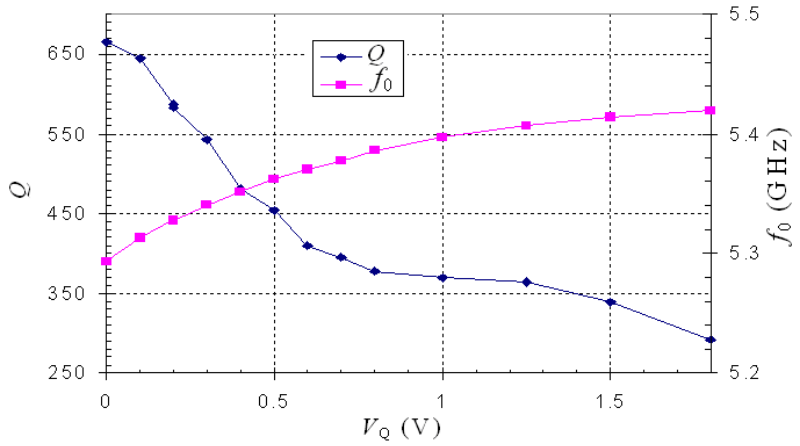


Figure 5-25 Measured Q-tuning characteristic of the 0.2-μm gate-length bandpass filter vs. the varactor voltage V_Q for $292 \leq Q \leq 665$. Over this range, f_0 decreases from 5.42 GHz to 5.3 GHz (a 2% change). Note that Q can be tuned over different ranges depending on the baseline Q as set by the choice of biases. Here, the baseline Q was set to 410 at $V_Q = 0.6$ V by choosing $V_{CM} = 1.29$ V with all other biasing conditions given in Fig. 2-29.

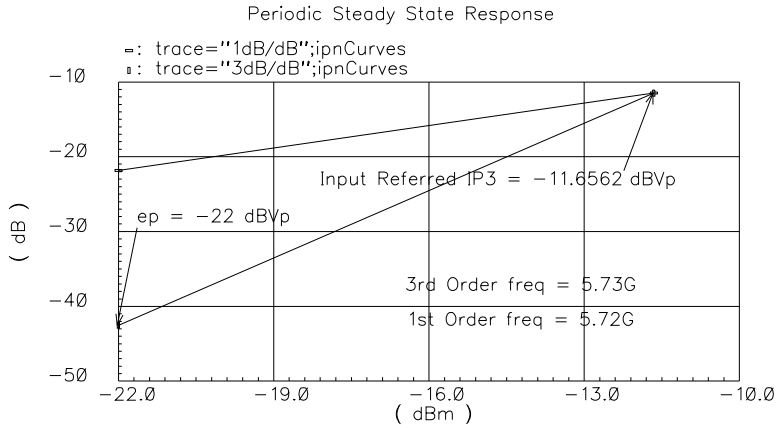


Figure 5-26 Simulation results of *IIP3*, which is 0.523 V_{pp}, differentially.

The simulated input-referred 3rd-order intercept point (IIP3) is 0.523 V_{pp}, as shown in Fig. 5-26. The simulated 1-dB compression point is shown in Fig. 5-27. The simulated noise figure is shown in Fig. 5-28.

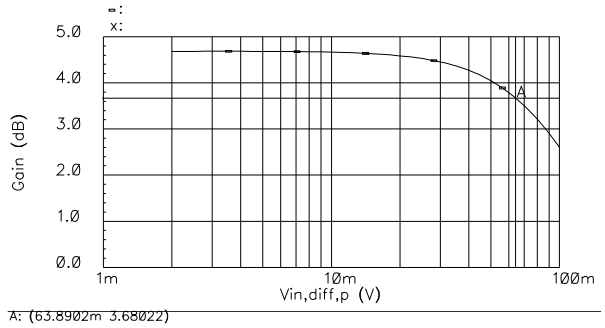


Figure 5-27 Simulation results for deriving the input 1-dB compression point, which is 0.128 Vpp, differentially.

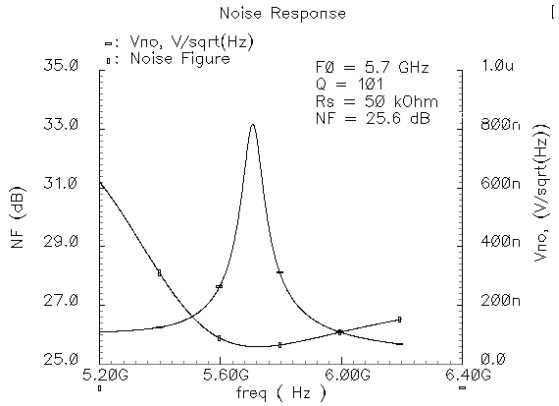


Figure 5-28 Simulated Noise Figure (R_S = 50 kΩ) and equivalent output noise.

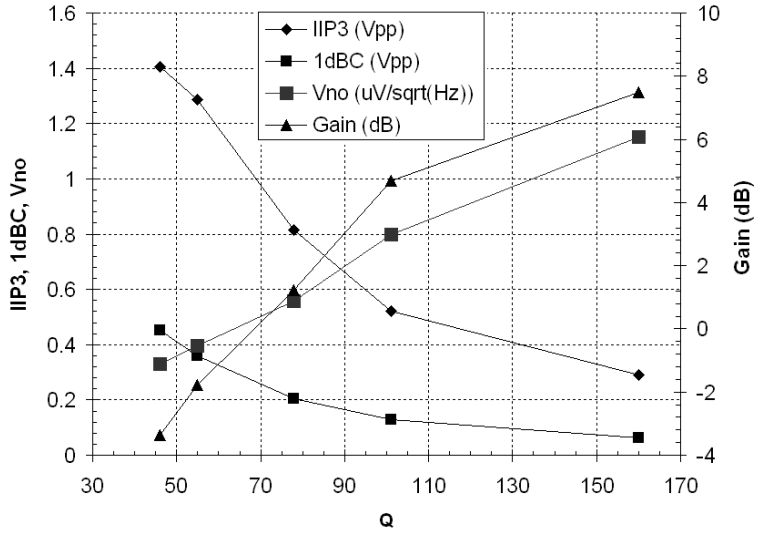


Figure 5-29 Plot of *IIP3*, input 1-dB compression point, and equivalent output noise.

A higher Q_R is associated with an approximately proportional higher shunt resistor R_p in the active inductor per Eq. (2.62), and consequently, the midband gain is

higher. However, this means that the input signal and active-inductor internal noise current will both be amplified more; consequently, *IIP3* and 1-dB compression point will reduce and the output noise voltage will be higher. This tradeoff is shown in Fig. 5-29.

The performance of the 5.4-GHz active-inductor filter is compared with two other recent designs in Table 5-1.

Table 5-1 Performance Summary of the Active-Inductor Filter and Comparison

Specifications	This Work	Ref. [45]	Ref. [8]
Technology	0.20-μm CMOS	0.35-μm CMOS	BJT, 0.35-μm SiGe BiCMOS
Filter order	2	2	2
Layout area	26.6 μm × 30 μm	200 μm × 140 μm	< 200 μm × 200 μm
V_{DD}	1.8	2.7	3.3
I_{DD}	2.44 mA	17 mA, Q dependent	-
Power	4.4 mW	45.9 mW	< 25.2 mW
f_0	5.4 GHz	0.9 GHz	6.5, 8.3, and 10 GHz
f_0 tuning range	3.34 GHz to 5.72 GHz	0.4 to 1.1 GHz	6.5 to 10 GHz
Q tuning range	2 to 665 (∞ possible)	2 to 80	2 to 38[1]
IIP3	0.523 V_{PP} or –1.65 dBm from 50 Ω[1], 5.7 GHz, 4.7 dB midband gain, Q = 101	–15 dBm (0.112 V_{PP}), 0.9 GHz, Q = 40, gain unknown	–26 dBm[1] (0.032 V_{PP}), 8.5 GHz, 15.1 dB gain, Q unknown
1-dB input compression	0.128 V_{PP} or –13.9 dBm from 50 Ω[1], 5.7 GHz, 4.7 dB midband gain, Q = 101	-	–34 dBm[1] (12.6 mV_{PP}), 8.5 GHz, 15.1 dB gain, Q unknown
Output Noise	0.8 μV/Hz$^{1/2}$ [1], 5.7 GHz, 4.7 dB midband gain, Q = 101	–147 dBm/Hz	-
Noise Figure	25.6 dB at 5.7 GHz[1], R_S = 50 kΩ, others same as above	-	8.8 – 10.4 dB[1], R_S unknown
f_0 statistics, σ, L_{gate} = 0.2 / 0.4 μm, lot of 40	1.78% / 0.72% f_0	-	-
f_0 statistics, range, L_{gate} = 0.2 / 0.4 μm, lot of 40	±4.2% / ±1.65% f_0	-	-

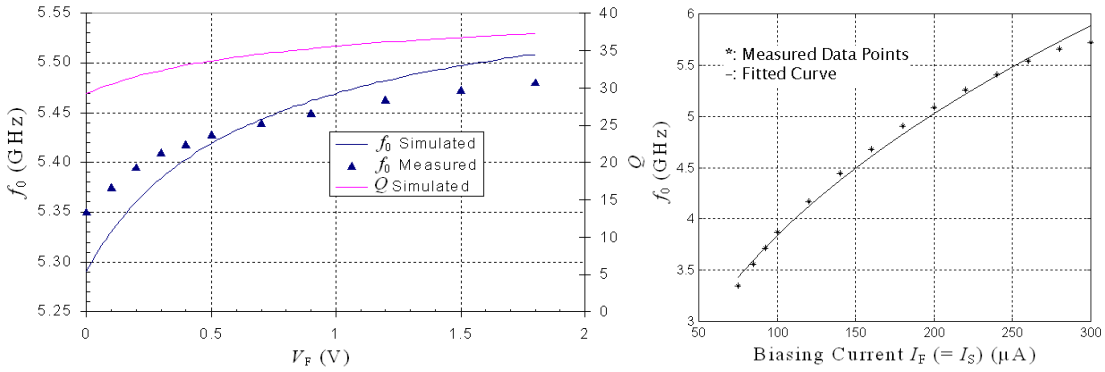
[1] Simulation results.

5.6.4 Frequency Tuning of the Active Inductor

When used as a resonator in oscillators and bandpass filters, the active inductor's f_R and Q_R need to be tuned to desired values. We have seen the filter Q tuning in Fig. 5-25. Since the bandpass filter's Q is the active inductor Q_R modified by the extra parasitic elements from the input G_M and output buffer, the Q_R tuning characteristic of an active inductor will be the same.

Active inductor's f_R can be tuned via the biasing currents I_F and I_S as well as the varactor control voltage V_F. Current tuning can be used as coarse tuning or as a design

measure, and V_F tuning can be used as fine tuning. A tuning example is shown in Fig. 5-30. The results are measured from an active-inductor oscillator. Similarly, since the oscillator's f_0 is the active inductor's f_R modified by the extra parasitic elements from the cross-connected differential pair and output buffer, the f_0 tuning characteristic in Fig. 5-30 represents the active inductor f_R tuning characteristic as well.



(a) (b)

Figure 5-30 Tuning the filter center frequency (L_{gate} = 0.2 μm): (a) frequency-tuning via the varactor voltage V_F; (b) frequency-tuning via biasing currents I_F and I_S.

In the example, for 0 V ≤ V_F ≤ 1.8 V, f_0 is measured in the range 5.35 GHz ≤ f_0 ≤ 5.48 GHz; the simulated f_0 changes from 5.29 GHz to 5.51 GHz. For this range of V_F the simulated Q changes from 29 to 37, with the baseline Q set at 34 by V_{CM} = 1.31 V. Note that Q will be more sensitive to V_F if the baseline Q is high. The difference between simulation and measurement of f_0 is mainly due to the inaccuracies in extracting the parasitic capacitors. When the biasing currents I_F and I_S are varied from 75 μA to 300 μA, f_0 changes from 3.34 GHz to 5.72 GHz. Q_R varies over a large range when varying I_F and must be reset by iterative circuit biasing. For this reason f_0-control via I_F is intended to be a design measure rather than an on-chip tuning method.

Of course, another design measure for f_0 is the gate length L of the primary FETs in the active inductor, per Eq. (4.17).

5.6.5 Measured Frequency Statistics

A total of 40 chips are available for testing. This permits us to derive some statistical information, which reflects to some extent the process variation and the active inductor's sensitivities to it. Figure 5-31 shows the frequency histogram of the oscillators. The distribution is approximately Gaussian.

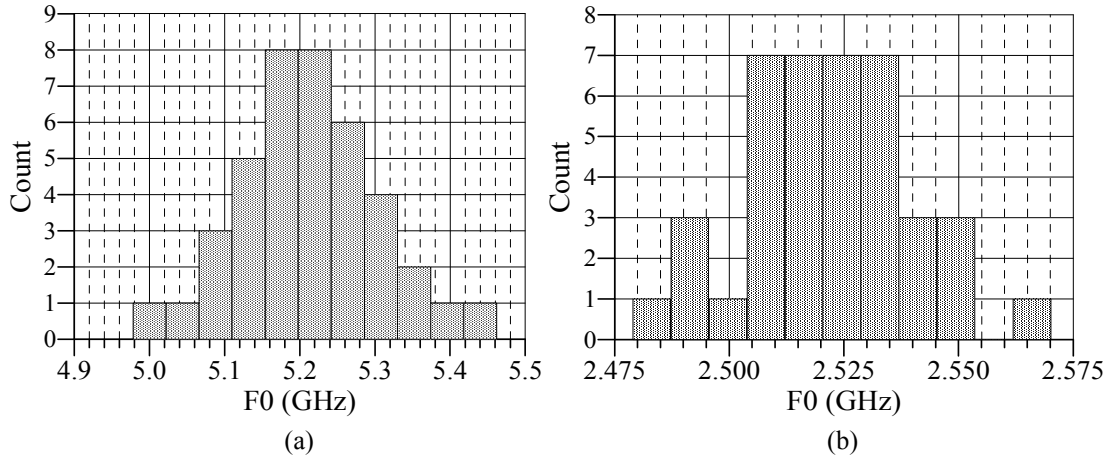


Figure 5-31 Histograms of oscillator f_0 at nominal biasing. (a) 5-GHz oscillator, L_{gate} = 0.2 μm, OSC0.2; (b) 2.5-GHz oscillator, L_{gate} = 0.4 μm, OSC0.4.

Table 5-2 shows the statistics results. Each oscillator module is tested on all 40 chips at two biasing levels, nominal ($I_F = I_S$ = 250 μA) and higher ($I_F = I_S$ = 280 μA). We may therefore calculate the statistics of the Δf_0 between the two biasing settings. The average f_0 of the higher-Q modules is always lower than that of regular-Q modules because of their larger Q-tuning varactor used to increase C_2 in Fig. 2-28, which increases the total module capacitance. The standard deviation of f_0 for the 2.5-GHz modules is only about 20% that of the 5-GHz modules, because their larger transistor W and L translate into a smaller process-variation percentage.

We expect the same f_0 statistics for high-Q bandpass filters since the filters and oscillators are designed using the same active-inductor core. Table 5-3 summarizes the

measured results on the oscillators and filters.

Table 5-2 Frequency (F_0) statistics of the oscillators.

		OSC0.2	OSC0.2HQ	OSC0.4	OSC0.4HQ
Nominal Biasing ($I_F = I_S$ = 250 μA)	Average (GHz)	5.216	4.938	2.521	2.463
	Std Dev (MHz)	92.67	101.5	18.05	21.33
	Min (GHz)	5.0	4.73	2.483	2.409
	Max (GHz)	5.44	5.128	2.566	2.5
	Range (MHz)	440	398	82.9	90.6
	Range/Std Dev	4.748	3.921	4.592	4.247
Higher Biasing ($I_F = I_S$ = 280 μA)	Average (GHz)	5.289	5.015	2.567	2.507
	Std Dev (MHz)	88.83	97.47	17.96	21.59
	Min (GHz)	5.075	4.818	2.53	2.454
	Max (GHz)	5.503	5.2	2.611	2.544
	Range (MHz)	428	382	81.5	90.4
	Range/Std Dev	4.818	3.919	4.537	4.188
Delta f_0 between the two biasings	Average (MHz)	73.81	77.41	45.5	44.15
	Std Dev (MHz)	5.085	5.882	1.234	1.488
	Min (MHz)	63.0	65.0	43.0	42.0
	Max (MHz)	85.0	93.0	48.4	46.4
	Range (MHz)	22.0	28.0	5.4	4.2
	Range/Std Dev	4.327	4.76	4.377	2.822

5.6.6 Summary of Measured Results

Table 5-3 Summary of measured results.

	OSC0.2		OSC0.4		BP0.2		BP0.4	
	Measure	Simul'd	Measure	Simul'd	Measure	Simul'd	Measure	Simul'd
L_{gate} (μm)	0.2	0.2	0.4	0.4	0.2	0.2	0.4	0.4
f_0 (GHz)	5.645	6.221	2.6	3.036	5.4	6.4[2]	2.8	-
Peak Amp (mV)	134	194	130	96	-	-	-	-
Phase Noise @ 1 MHz (dBc/Hz)	–66.6[1]	–68.4[1]	–73.2[1]	–70.1[1]	-	-	-	-
Q	-	-	-	-	365	Varies	661	-
f_0 mean (GHz)	5.216	-	2.521	-	-	-	-	-
f_0 stdev (MHz)	92.67	-	18.05	-	-	-	-	-

[1] due to a design flaw (see Section 5.6.1), the phase noise is 4 dB higher than it could be.

[2] Figure 3-7.

5.7 Results of Active-Inductor Lowpass Filters

Active-inductor lowpass filters with L_{gate} = 0.2 μm (LP0.2) and 0.4 μm (LP0.4) were

fabricated and measured, with results shown in Figs. 5-32 and 5-33, respectively.

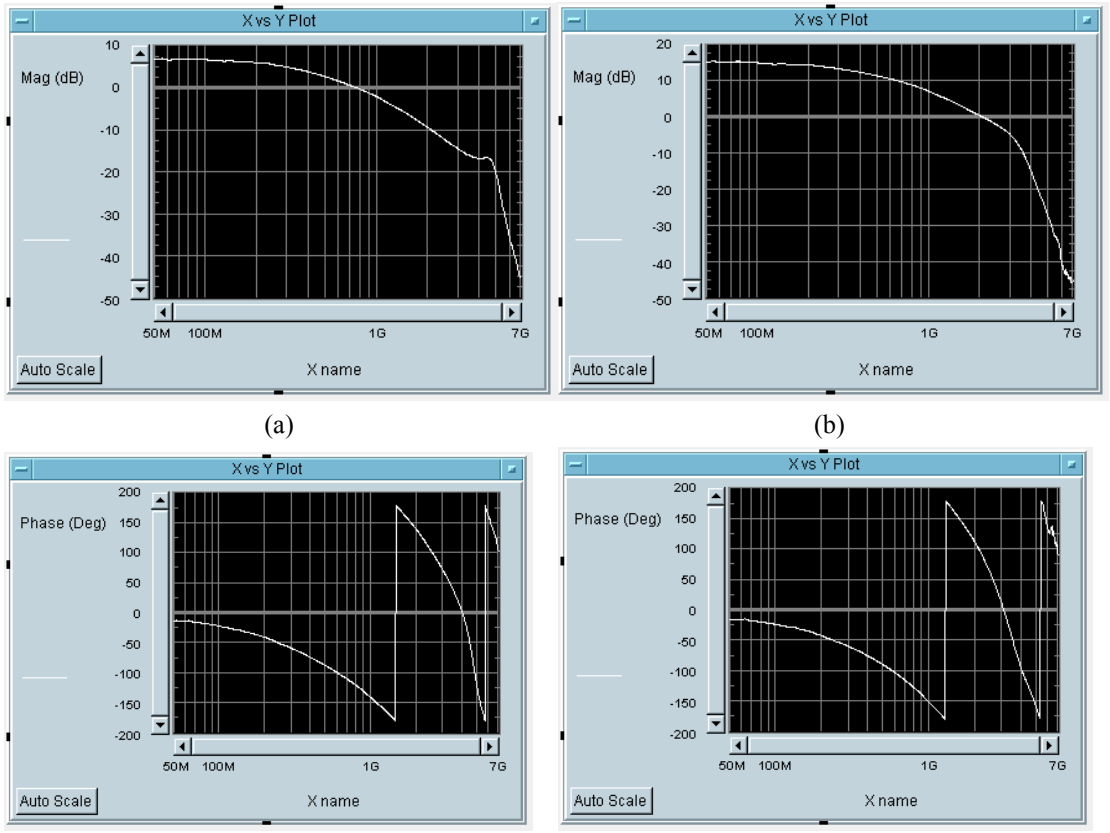


Figure 5-32 Examples of magnitude and phase responses of the module LP0.2, including the input buffer and the output driver. (a, c) *Q* is a little too high as shown by the peaking at the passband corner. The pole frequency is about 4.5 GHz; (b, d) *Q* is reduced via the loss resistor, resulting in less peaking. (Data Ref# LP0.2-C17-VNA-00010 and LP0.2-C17-VNA-00020)

The filters operate as intended, as shown by the frequency profiles. However, since the frequency-sweep range is very wide, from 50 MHz to 7 GHz, the frequency response of the microprobe contact and cable assembly is not constant across the frequencies, and distorts both the measured lowpass filter and reference channel gain profiles. Therefore, after subtracting the reference channel to exclude the effects of the input and output buffers, the lowpass filter frequency profile is distorted, as shown in Fig. 5-35, even though the distortion is barely visible in the raw data of the lowpass filter; the reason is, in part, because the distortion is the result of subtracting two large

numbers. Nevertheless, the measured results confirm that via appropriate connections the active inductor can operate as lowpass filters.

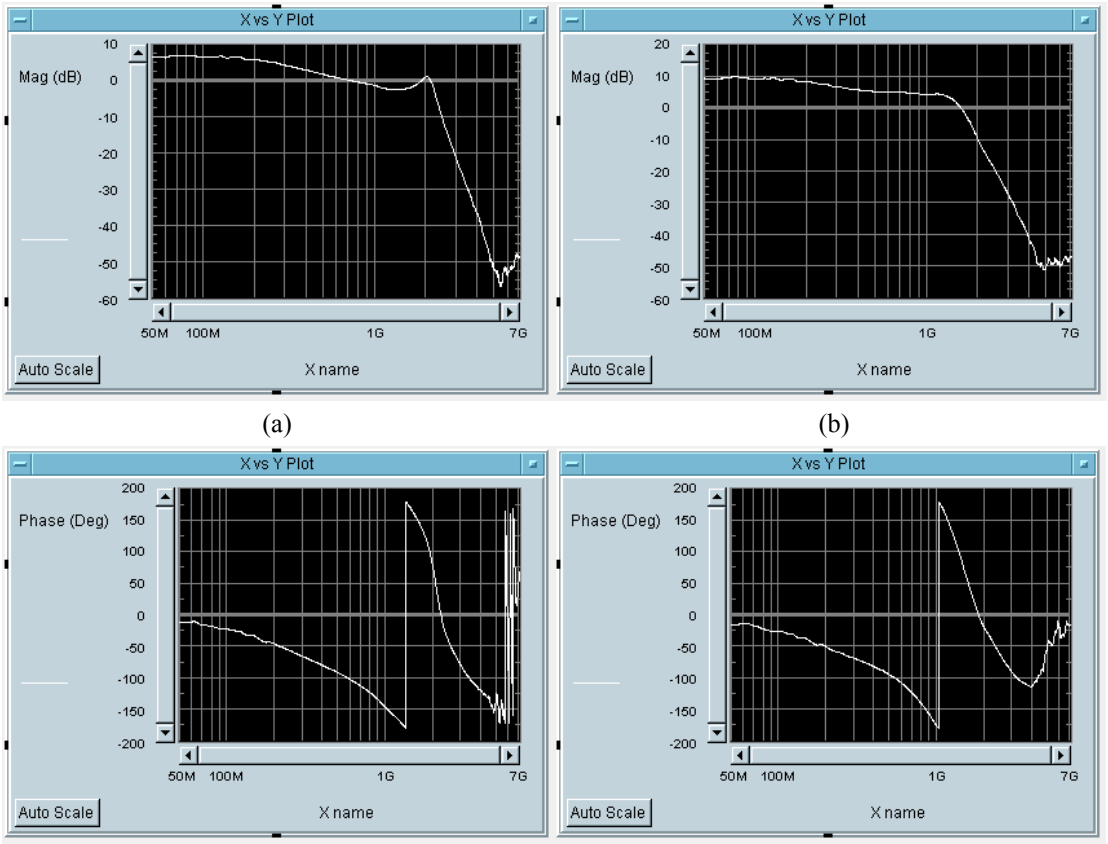
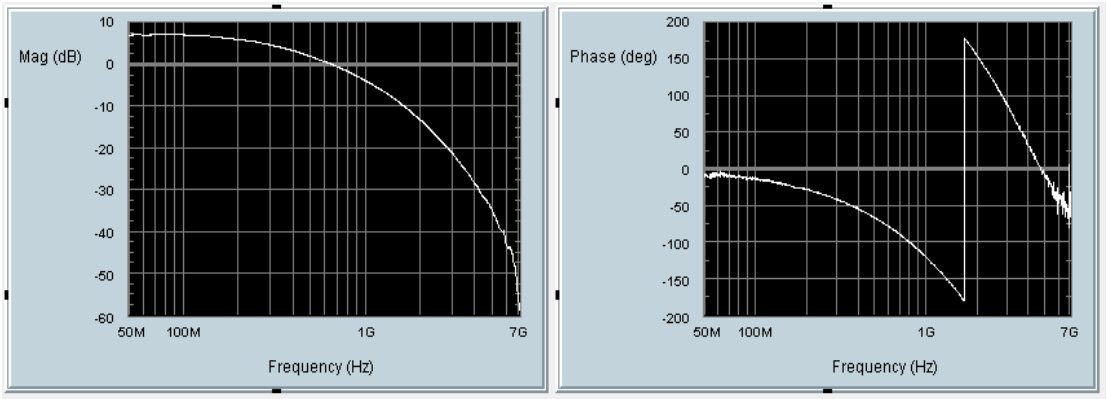


Figure 5-33 Examples of magnitude and phase responses of the module LP0.4, including the input buffer and the output driver. (a, c) *Q* is a little high, leading to peaking at the passband corner. The pole frequency is about 2 GHz; (b, d) *Q* is reduced via the loss resistor, leading to less peaking. (Data Ref# LP0.4-C17-VNA-00010 and LP0.4-C17-VNA-00020)



(a) (b)

Figure 5-34 Magnitude and phase responses of the reference channel. (Data Ref# Ref-C17-VNA-00020, -00011)

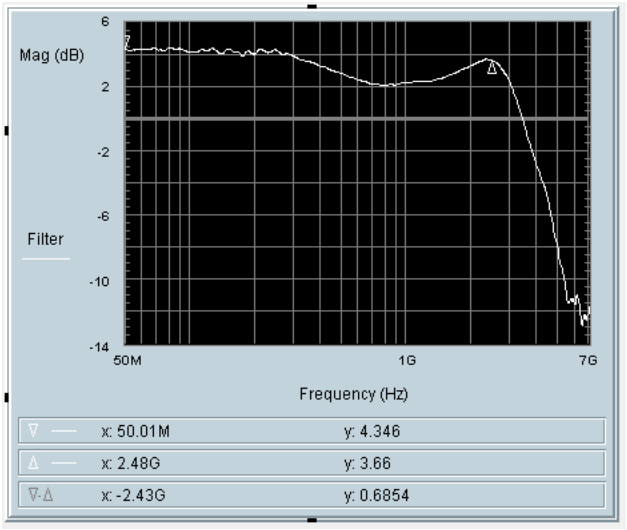


Figure 5-35 0.2-μm lowpass filter frequency response, after subtracting the reference channel. (Data Ref# LP0.2-C28-VNA-00090 and Ref-C26-VNA-00080)

Different from the bandpass filters, the passband gain of the lowpass filters is approximately 1, while the bandpass filter can have 20-30 dB gain by choice of the input G_M value. The high-frequency feed-through effect due to parasitic capacitance and substrate, however, is about the same for both the lowpass and bandpass filters, and sets a limit on stopband attenuation. Therefore, the gain difference between passband and stopband is expected to be much smaller for lowpass filters and to limit their use.

5.8 Conclusion

The all-NMOS active inductor circuit obtained in this work was used to design oscillators, bandpass and lowpass filters, for a total of 10 circuit module, including an input-output buffer reference module. The oscillators and filters are fabricated in TSMC's 0.18-μm logic CMOS process (LOG018) and the 40 ICs are all tested. All circuits are functional, with frequencies being about 80-90% those of the simulation results, due to model and parasitic-capacitance extraction errors.

CHAPTER 6

CONCLUSION

The rapid growth of wireless applications in consumer products and industrial systems has generated considerable interest in radio-frequency integrated circuits (RFICs), and a demand for a great variety of different products with emphasis on low cost. The passive on-chip inductor is the staple of wireless communication ICs in order for implementing RF filters and oscillators as well as impedance matching. Passive inductors typically occupy 20-50% of the total silicon area and require special technologies, such as thicker metal layers or a high-resistivity substrate, resulting in higher cost. Their lack of tunability makes designing a robust product across process corners challenging and requires stringent modeling accuracy. Active inductors, on the other hand, occupy merely 1-10% the area of passive inductors, and they can be continuously tuned to cover process/temperature variations and to operate over a wide frequency range. When properly designed, they use only transistors and can be fully compatible with standard digital CMOS circuitry on the same die.

The main disadvantages of active inductors are their higher noise, nonlinearity, and power consumption, because translating capacitors into simulated inductors requires multiple-transistor circuitry that has to be biased at high current densities with low-value capacitors to achieve high operating frequencies; linearization schemes usually cannot be used as they generate unavoidable parasitic poles and reduce the frequency range of operation. To date, to the author's knowledge, no active inductors, including this work, can meet the noise and dynamic-range requirements of RF band-

selection filters or local oscillators in short/long-range wireless communication ICs and consume an acceptable amount of power. However, active inductor circuits have the advantage of saving significant silicon area and may be used in less stringent applications, such as limiting amplifiers and digital clock generators.

The goal of this research was to design and test narrow-band (very-high-Q) bandpass filters and oscillators operating in several GHz using active inductors. To achieve this goal, a high-frequency high-Q active-inductor circuit is required. Various active inductors have been proposed in the literature, and some structures have been adopted by industry. However, as discussed in Chapter 2, the majority of these circuits have low Qs due to the presence of a transistor source/emitter terminal at the inductor's primary (input or gyration) node, and/or have biasing difficulties. Therefore, an all-NMOS-signal-path inductor circuit is proposed and experimentally validated in silicon. The circuit has a moderate intrinsic Q; but by tuning the parasitic capacitance at an internal node, the output loss of short-channel devices can be partially or totally compensated, and Q can be arbitrarily high. A practical difficulty, though, is that an excessively high Q leads to excessively high circuit sensitivities.

The signal path of the inductor circuit consists of only NFETs, which have higher device mobility than PFETs, hence the circuit can operate at a higher frequency, when compared with one that consists of both PFETs and NFETs in its signal path.

The all-NMOS active inductor was used to design high-Q bandpass filters and oscillators, using TSMC's 0.18-μm logic process, and both were fabricated in 0.2-μm

and 0.4-μm gate lengths. The highest center frequency was measured to be 5.7 GHz in 0.2-μm gate length, and the maximum repeatably measured *Q* was 665. The oscillator phase noise was measured to be –66.6 dBc/Hz at 1 MHz offset from 5.1-GHz center frequency with 4.4-mW power dissipation. The simulated noise figure for the active-inductor filter is 25.6 dB at a 50-kΩ source impedance. The area of the filter is 26.6 μm x 30 μm.

Based on the same gyrator and feedback principle, a circuit labeled all-NMOS-II, was developed. It has superior signal fidelity when used as a voltage follower or signal driver, because its gain is unity and constant across process and temperature variations; the input and output dc voltages are the same, limited only by device mismatches.

The all-NMOS active-inductor circuit was granted a US patent, and all-NMOS-II circuit has a US patent pending.

This research proved the possibility of designing very-high-*Q* active-inductor filters and oscillators at 1-5 GHz using MOSFETs only in standard digital CMOS processes. However, the high level of noise, as determined by the fundamental limits in devices and the requirement of high frequency, will limit their direct use.

LIST OF REFERENCES:

1. Behzad Razavi, RF Microelectronics, Prentice Hall, 1998.

2. Steven C. Chan, Kenneth L. Shepard and Phillip J. Restle, "Distributed Differential Oscillators for Global Clock Networks," JSSC, Vol. 41, No. 9, pp. 2083-2093, Sept. 2006.

3. The American Heritage Dictionary of the English Language, 4th Edition, Houghton Mifflin Company, 2000.

4. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, 3rd-Ed., McGraw-Hill, New York, 2002.

5. Dandan Li, Y. P. Tsividis, "A Loss-Control Feedback Loop for VCO Indirect Tuning of RF Integrated Filters," IEEE Transactions on Circuits and Systems II, Vol. 47, No. 3, pp. 169-175, March 2000.

6. W. A. Gee, P. E. Allen, "CMOS Integrated Transformer-Feedback Q-Enhancement LC Bandpass Filter for Wireless Receivers," IEEE Intl. Symp. on Circuits and Systems (ISCAS 2004), Vol. 4, pp. 253-256, May 23-26, 2004.

7. Da-Chiang Chang and Ching-Wen Hsue, "Wide-band Equal-Ripple Filters in Nonuniform Transmission lines," IEEE Trans. On Microwave Theory and Techniques, Vol. 50, No. 4, pp. 1114-19, April 2002.

8. S. Andersson and C. Svensson, "An Active Recursive RF Filter in 0.35 μm BiCMOS," Analog Integrated Circuits and Signal Processing, Vol. 44, pp. 213-218, 2005.

9. Bernard D. H. Tellegen, "The gyrator, a new electric network element", Philips Res. Rep. 3 (1948) pgs 81-101.

10. Rolf Schaumann, Mac E. Van Valkenburg, "Design of Analog Filters," Oxford University Press, New York, 2001.

11. Peter Ashburn, SiGe Heterojunction Bipolar Transistors, John Wiley & Sons, West Sussex, England, 2003.

12. Jafar Savoj, Behzad Razavi, High-Speed CMOS Circuits for Optical Receivers, Kluwer Academic Publishers, 2001.

13. Tian Jun, et al., "1.25 Gb/s Low Power CMOS Limiting Amplifier for Optical Receiver," 2004 Intl. Conf. on Solid-State and Integrated Circuits Tech., vol. 2, pp. 1469-1471, Oct. 18-21, 2004.

14. Jong Hwa Lee, et al., "Design of a 2.5 GBPS CMOS Trans-Impedance Amplifier (TIA) for Optical Communication," the 8th Russian-Korean Intl. Symp. on Science and Technology (KORUS 2004), vol. 1, pp. 229-233, June 26 – July 3, 2004.

15. Eduard Sachinger and Wilhelm C. Fischer, "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receivers," IEEE Jour. Of Solid-State Circuits, vol. 35, No. 12, Dec. 2000.

16. George E. Valley and Henry Wallman, Vacuum Tube Amplifiers (Radiation Lab Series, 18), McGraw Hill, 1948.

17. Hung Tien Bui, Yvon Savaria, "Shunt-Peaking of MCML Gates Using Active Inductors," the 2nd Annual IEEE Northeast Workshop on Circuits and Systems (NEWCAS 2004), pp. 361 – 364, June 20-23, 2004.

18. J. H. C. Zhan, J. S. Duster, K. T. Kornegay, "A 7.3-GHz, 55% Tuning Range Emitter Degenerated Active Inductor VCO," 2004 Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), pp. 60 – 63, Sept. 13-14, 2004.

19. Jo-Yi Foo, Robert J. Weber, "Low Power 5 GHz Quadrature Phase CMOS LC Oscillator with Active Inductor," 2004 IEEE Intl. Symp. on Comm. and Info. Tech. Vol. 2, pp. 1084-1089, Oct. 26-29, 2004.

20. Johan van der Tang, et al., "A 9.8-11.5 GHz Quadrature Ring Oscillator for Optical Receivers," 2001 IEEE Conf. on Custom Integrated Circuits, pp. 323-326, May 6-9, 2001.

21. Yanjie Wang, M. Zamin Khan, S. Masood Ali, et al., "A Fully Differential CMOS Limiting Amplifier with Active Inductor for Optical Receiver," 2005 Canadian Conf. on Electrical and Computer Engr., pp. 1751-1754, May 1-4, 2005.

22. Chia-Hsin Wu, Jieh-Wei Liao, Shen-Iuan Liu, "A 1 V 4.2 mW Fully Integrated 2.5 Gb/s CMOS Limiting Amplifier using Folded Active Inductors," 2004 Intl. Symp. on Circuits and Systems (ISCAS 2004), vol. 1, pp. 1044-1047, May 23-26, 2004.

23. Flora Carreto-Castro, Jose Silva-Martinez, Roberto Murphy-Arteaga, "RF Low-Noise Amplifiers in BiCMOS Technologies," IEEE Trans. On Circuits and Systems – II, vol. 46, pp. 974-977, July 1999.

24. Shinji Hara, Tsuneo Tokumitsu, Toshiaki Tanaka, Masayoshi Aikawa, "Broadband Monolithic Microwave Active Inductor and Application to a Miniaturized Wide Band Amplifier," 1988 IEEE Microwave and Millimeter-Wave Monolithic circuits Symp., pp. 117-120, May 24-25, 1988.

25. Shinji Hara, Tsuneo Tokumitsu, Toshiaki Tanaka, Masayoshi Aikawa, "Broad-band Monolithic Microwave Active Inductor and Its Application to Miniaturized Wide-Band Amplifiers," IEEE Trans. On Microwave Theory and Techniques, vol. 36, No. 12, pp. 1920-1924, Dec. 1988.

26. Hitoshi Hayashi, et al., "A Novel Loss Compensation Technique for High-Q Broad-band Active Inductors," IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symp., pp. 103-106, June 16-18, 1996.

27. Hitoshi Hayashi, et al., "A High-*Q* Broad-band Active Inductor and Its Application to a Low-Loss Analog Phase Shifter," IEEE Trans. On Microwave Theory and Techniques, vol. 44, No. 12, pp. 2369-2374, Dec. 1996.

28. Yong-Ho Cho, et al, "A Novel Active Inductor and Its Application to Inductance-Controlled Oscillator," IEEE Trans. On Microwave Theory and Techniques, vol. 45, No. 8, pp. 1208-1213, Aug. 1997.

29. Yongho Cho, et al., "Monolithic VCO using a Novel Active Inductor," IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symp., pp. 155-158, June 16-18, 1996.

30. Yongho Cho, et al., "Monolithic VCO using a Novel Active Inductor," 1996 IEEE MTT-S Intl. Microwave Symp., vol. 1, pp. 137-140, June 17-21, 1996.

31. W. D. Jemison, P. R. Herczfeld, "A Pulsed Microwave Oscillator Using Optically Controlled Active Feedback," IEEE Microwave and Guided Wave Letters, vol. 2, No. 5, pp. 177-179, May 1992.

32. Stepan Lucyszyn, Ian D. Robertson, "High Performance MMIC Narrow Band Filter using Tunable Active Inductors," IEEE 1994 Microwave and Millimeter-Wave Monolithic Circuits Symp., pp. 91-93, May 22-25, 1994.

33. Stepan Lucyszyn, Ian D. Robertson, "Monolithic Narrow-Band Filter using Ultrahigh-*Q* Tunable Active Inductors," IEEE Trans. On Microwave Theory and Techniques, vol. 42, No. 12, pp. 2617-2622, Dec. 1994.

34. E. C. Krantz and G. R. Branner, "Synthesis of Active Microwave Filters Incorporating Noise Effects," 36th Midwest Symp. on Circuits and Systems, vol. 2, pp. 805-808, Aug. 16-18, 1993.

35. R. Kaunisto, et al., "A Low-Power HBT MMIC Filter Based on Tunable Active Inductors," IEEE Microwave and Guided Wave Letters, vol. 7, No. 8, pp. 209-211, Aug. 1997.

36. Shinji Hara, Tsuneo Tokumitsu, Masayoshi Aikawa, “Lossless, Broadband Monolithic Microwave Active Inductors,” 1989 IEEE MTT-S Intl. Microwave Symp. Digest, vol. 3, pp. 955-958, June 13-15, 1989.

37. Shinji Hara, Tsuneo Tokumitsu, Masayoshi Aikawa, “Lossless Broad-band Monolithic Microwave Active Inductors,” IEEE Trans. On Microwave Theory and Techniques, vol. 37, No. 12, pp. 1979-1984, Dec. 1989.

38. Shinji Hara, Tsuneo Tokunitsu, “Monolithic Microwave Active Inductors and Their Applications,” 1991 IEEE Symp. on Circuits and Systems, vol. 3, pp. 1857-1860, June 11-14, 1991.

39. Wei Li, et al., “High Q Active Inductor with Loss Compensation by Feedback Network,” Electronic Letters, vol. 35, pp. 1328-1329, Aug. 1999.

40. Sung-Gi Yang, et al., “Fully Symmetrical, Differential-Pair Type Floating Active Inductors,” 1997 IEEE Intl. Symp. on Circuits and Systems (ISCAS 1997), vol. 1, pp. 93-96, June 9-12, 1997.

41. Yue Wu, Mohammed Ismail, and Hakan Olsson, “A Novel CMOS Fully Differential Inductorless RF Bandpass Filter,” 2000 IEEE Intl. Symp. on Circuits and Systems, vol. 4, pp. 149-152, May 28-31, 2000.

42. Yue Wu, Mohammed Ismail, and Hakan Olsson, “Inductorless CMOS RF Bandpass Filter,” Electronic Letters, vol. 37, No. 16, pp. 1027-1029, August 2001.

43. Yue Wu, Mohammed Ismail, and Hakan Olsson, “CMOS VHF/RF CCO Based on Active Inductors,” Electronic Letters, vol. 37, No. 8, pp. 472-473, Apr. 2001.

44. Yue Wu, Mohammed Ismail, and Hakan Olsson, “CMOS Active Inductor and Its Application in RF Bandpass Filter,” 2004 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 655-658, June 6-8, 2004.

45. Yue Wu, Mohammed Ismail, and Hakan Olsson, “RF Bandpass Filter Design Based on CMOS Active Inductors,” IEEE Trans. On Circuits and Systems-II, vol. 50, No. 12, pp. 942-949, Dec. 2003.

46. David Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons, Inc., New York 1997.

47. Bosco H. Leung, VLSI for Wireless Communication, Pearson Education, 2002.

48. Jhy-Neng Yang, et al., “A Design of CMOS Broadband Amplifier with High-Q Active Inductor,” 3rd IEEE Intl. Workshop on System on Chip for Real Time Appl., pp. 86-89, June 30-July 2, 2003.

49. Jhy-Neng Yang, et al., "A 1.75 GHz Inductorless CMOS Low Noise Amplifier with High-Q Active Inductor Load," 44th IEEE Midwest Symp. on Circuits and Systems (MWSCAS 2001), vol. 2, pp. 816-819, Aug. 14-17, 2001.

50. W. Zhuo, et al., "Programmable Low Noise Amplifier with Active-Inductor Load," 1998 IEEE Intl. Symp. on Circuits and Systems (ISCAS 1998), vol. 4, pp. 365-368, May 31-June 3, 1998.

51. Ming-Juei Wu, Jyh-Neng Yang, and Chen-Yi Lee, "A Constant Power Consumption CMOS LC Oscillator Using Improved High-Q Active Inductor with Wide Tuning Range," 47th IEEE International Midwest Symp. on Circuits and Systems (MWSCAS 2004), vol. 3, pp. 347-500, July 25-28, 2004.

52. Chao-Chih Hsiao, et al., "Improved Quality-Factor of 0.18-um CMOS Active Inductor by a Feedback Resistance Design," IEEE Microwave and Wireless Components Letters, vol. 12, No. 12, pp. 467-469, Dec. 2002.

53. K. Manetakis, et al., "Wideband CMOS Analog Cells for Video and Wireless Communications," 3rd IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS 1996), vol. 1, pp. 227-230, Oct. 13-16, 1996.

54. U. Yodprasit and J. Ngarmnil, "Q-Enhancing Technique for RF CMOS Active Inductor," 2000 IEEE Intl. Symp. on Circuits and Systems (ISCAS 2000), vol. 5, pp. 589-592, May 28-31, 2000.

55. W. Zhuo, J. Pineda de Gyvez, E. Sanchez-Sinencio, "Programmable Low Noise Amplifier with Active-Inductor Load," 1998 IEEE Intl. Symp. on Circuits and Systems, vol. 4, pp. 365-368, May 31-June 3, 1998.

56. Chao-Chih Hsiao, et al., "Improved Quality-Factor of 0.18-um CMOS Active Inductor by a Feedback Resistance Design," IEEE Microwave and Wireless Components Letters, vol. 12, No. 12, pp. 467-469, Dec. 2002.

57. Jyh-Neng Yang, et al., "A 1.75 GHz Inductor-less CMOS Low Noise Amplifier with High-Q Active Inductor Load," 44th IEEE Midwest Symp. on Circuits and Systems (MWSCAS 2001), vol. 2, pp. 816-819, Aug. 14-17, 2001.

58. Jyh-Neng Yang, et al., "A Design of CMOS Broadband Amplifier with High-Q Active Inductor," 3rd IEEE Intl. Workshop on System-on-Chip for Real-Time Applications, pp. 86-89, June 30-July 2, 2003.

59. Risto Kaunisto, Kari Stadius and Veikko Porra, "A 3 GHz Silicon-BJT Active Resonator and Filter," 1998 IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS 1998), vol. 3, pp. 197-200, Sept. 7-10, 1998.

60. Apinunt Thanachayanont and Alison Payne, "VHF CMOS Integrated Active Inductor," Electronic Letters, vol. 32, No. 11, pp. 999-1000, May 1996.

61. Rahim Akbari-Dilmaghani and Alilson Payne, "An RF CMOS Differential Bandpass Amplifier using an Active Inductor," IEE Colloquium on Systems on a Chip, pp. 16/1-16/6, Sept. 5, 1998.

62. R. Akbari-Dilmaghani, A. Payne and C. Toumazou, "A High Q RF CMOS Differential Active Inductor," 1998 IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS 1998), vol. 3, pp. 157-160, Sept. 7-10, 1998.

63. Rahim Akbari-Dilmaghani and Alison Payne, "An RF BiCMOS Bandpass Amplifier using an Active Inductor," 6th IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS 1999), vol. 2, pp. 611-614, Sept. 5-8, 1999.

64. Markus Grözing, et al., "A 2.5V CMOS Differential Active Inductor with Tunable L and Q for Frequencies up to 5 GHz," 2001 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 271-274, May 20-22, 2001.

65. Aydin Ilker Karsilayan and Rolf Schaumann, "A High-Frequency High-Q CMOS Active Inductor with dc Bias Control," 43rd IEEE Midwest Symp. on Circuits and Systems (MWSCAS 2000), vol. 1, pp.486-489, Aug. 8-11, 2000.

66. Haiqiao Xiao and Rolf Schaumann, "Very-High-Frequency Lowpass Filter Based on a CMOS Active Inductor," 2002 IEEE Intl. Symp. on Circuits and Systems (ISCAS 2002), Vol. 2, pp. 1-4, May 26-29, 2002.

67. H. Xiao and R. Schaumann, "A Low-Voltage Low-Power CMOS 5-GHz Oscillator Based on Active Inductors," 9th IEEE Intl. Conf. on Electronics, Circuits and Systems (ICECS 2002), Vol. 1, pp. 231-234, Sept. 15-18, 2002.

68. S. Sae-Ngow and A. Thanachayanont, "A ±1 Volt Very High Frequency Class AB CMOS Active Inductor," The 46th IEEE Intl. Midwest Symp. on Circuits and Systems (MWSCAS'03), Vol. 1, pp. 157-160, Dec. 27-30, 2003.

69. S. Sae-Ngow and A. Thanachayanont, "A Low-Voltage, Wide Dynamic Range CMOS Floating Active Inductor," Conf. on Convergent Technologies for Asia-Pacific Region (TENCON'03), Vol. 4, pp. 1460-1463, Oct. 15-17, 2003.

70. Apinunt Thanachayanont, "Low Voltage Low Power CMOS Inductorless RF Bandpass Filter with High Image Rejection Capability," The 45th Midwest Symp. on Circuits and Systems (MWSCAS'02), Vol. 3, pp. 548-551, Aug. 4-7, 2002.

71. Apinunt Thanachayanont, "2-V 3.36-mW 2.5-GHz Fourth-Order Inductorless CMOS RF Bandpass Filter," 2002 Asia-Pacific Conf. on Circuits and Systems (APCCAS'02), Vol. 1, pp. 127-130, Oct. 28-31, 2002.

72. Apinunt Thanachayanont and S. Sae-Ngow, "Low Voltage High-Q VHF CMOS Transistor-Only Active Inductor," The 45th Midwest Symp. on Circuits and Systems (MWSCAS'02), Vol. 3, pp. 552-555, Aug. 4-7, 2002.

73. Apinunt Thanachayanont, "CMOS Transistor-Only Active Inductor for IF/RF Applications," 2002 IEEE Conf. on Industrial Technology (ICIT'02), Vol. 2, pp. 1209-1212, Dec. 11-14, 2002.

74. Apinunt Thanachayanont and S. Sae-Ngow, "Class AB VHF CMOS Active Inductor," The 45th Midwest Symp. on Circuits and Systems (MWSCAS'02), Vol. 1, pp. 64-7, Aug. 4-7, 2002.

75. Apinunt Thanachayanont, "A 1.5-V CMOS Fully Differential Inductorless RF Bandpass Amplifier," 2001 IEEE Intl. Symp. on Circuits and Systems (ISCAS'01), Vol. 1, pp. 49-52, May 6-9, 2001.

76. Apinunt Thanachayanont, "Low Voltage CMOS Fully Differential Active Inductor and Its Application to RF Bandpass Amplifier Design," 2001 Intl. Symp. on VLSI Technology, Systems and Applications, pp. 125-28, Apr. 18-20, 2001.

77. Apinunt Thanachayanont and A. Payne, "CMOS Floating Active Inductor and Its Applications to Bandpass Filter and Oscillator Designs," IEE Proc. On Circuits, Devices and Systems, Vol. 147, pp. 42-48, Feb. 2000.

78. Apinunt Thanachayanont, "A 1.5-V High-Q CMOS Active Inductor for IF/RF Wireless Applications," 2000 Asia-Pacific Conf. on Circuits and Systems (APCCAS'00), pp. 654-57, Dec. 4-6, 2000.

79. Apinunt Thanachayanont and Alison Payne, "A 3-V RF CMOS Bandpass Amplifier Using an Active Inductor," 1998 IEEE Intl. Symp. on Circuits and Systems (ISCAS'98), Vol. 1, pp. 440-443, May 31 - June 3, 1998.

80. Haiqiao Xiao, Rolf Schaumann and W. Robert Daasch, High-Frequency Active Inductor, US Patent 7,042,317, Sept. 8th, 2004.

81. H. Xiao, Schaumann, et al., "A Radio-Frequency CMOS Active Inductor and Its Application in Designing High-Q Filters," IEEE Intl. Symp. on Circuits and Systems (ISCAS2004), Vol. 4, pp. 197-200, May 23-26, 2004, Vancouver, Canada.

82. Haiqiao Xiao and Rolf Schaumann, "A 5.4-GHz High-Q Tunable Active-Inductor Bandpass Filter in Standard Digital CMOS Technology," Analog Integrated Circuits and Signal Processing, Vol. 51, pp. 1-9, April 2007.

83. Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd Ed., Cambridge Univ. Press., 2003.

84. B. Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2000.

85. D. M. Pozar, Microwave Engineering, Wiley, John and Sons, Inc., 2004.

86. Guillermo Gonzalez, Microwave Transistor Amplifiers, 2nd edition, Prentice Hall, Upper Saddle River, New Jersey, 1997.

87. Behzad Razavi, "A Study of Phase Noise in CMOS Oscillators," IEEE J. of Solid-State Circuits, Vol. 31, No. 3, pp. 331-343, March 1996.

88. D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," Proc. Of IEEE, Vol. 54, No. 2, pp. 329-330, 1966.

89. Asad A. Abidi, Analog Circuit Design – RF Analog-to-Digital Converters; Sensor and Actuator Interfaces; Low-Noise Oscillators, PLLs and Synthesizers, Kluwer Academic Publishers, Boston, Nov. 1997.

90. Asad A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," IEEE J. of Solid-State Circuits, Vol. 41, No. 8, pp. 1803-1815, Aug. 2006.

91. Cadence SpectreRF® User's Manual, Cadence Design Systems, San Jose, CA.

92. P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th Ed., John Wiley and Sons, Inc., New York, 2001.

93. Alan Hastings, Art of Analog Layout, 2nd Ed., Prentice Hall, 2005.

94. Slawomir Koziel, Rolf Schaumann and Haiqiao Xiao, "Analysis and Optimization of Noise in Continuous-Time OTA-*C* Filters," IEEE Transactions on Circuits and Systems, Vol. 52, pp. 1086-94, June 2005.