Portland State University

PDXScholar

Dissertations and Theses

Dissertations and Theses

10-16-1996

Design of a Second-order Filter Using the g_m -C Technique

Girish Chandrasekaran
Portland State University

Follow this and additional works at: https://pdxscholar.library.pdx.edu/open_access_etds

Part of the [Electrical and Computer Engineering Commons](#)

Let us know how access to this document benefits you.

Recommended Citation

Chandrasekaran, Girish, "Design of a Second-order Filter Using the g_m -C Technique" (1996). *Dissertations and Theses*. Paper 5241.

<https://doi.org/10.15760/etd.7114>

This Thesis is brought to you for free and open access. It has been accepted for inclusion in Dissertations and Theses by an authorized administrator of PDXScholar. Please contact us if we can make this document more accessible: pdxscholar@pdx.edu.

THESIS APPROVAL

The abstract and thesis of Girish Chandrasekaran for the Master of Science in Electrical and Computer Engineering were presented October 16, 1996, and accepted by the thesis committee and the department.

COMMITTEE APPROVALS:

Rolf Schaumann, Chair

W. Robert Daasch

Tom Schubert

Representative of the Office of Graduate Studies

DEPARTMENT APPROVAL:

Rolf Schaumann, Chair

Department of Electrical Engineering

ACCEPTED FOR PORTLAND STATE UNIVERSITY BY THE LIBRARY

by _____

on 1 Nov 1996

ABSTRACT

An abstract of the thesis of Girish Chandrasekaran for the Master of Science in Electrical and Computer Engineering presented October 16, 1996.

Title: Design of a second-order filter using the g_m - C technique

This thesis deals with the design, layout, fabrication, testing and characterization of a second-order filter (biquad) using the transconductance- C (g_m - C) technique. The biquad was designed to realize the four filter functions – lowpass, highpass, bandpass and notch – by appropriate choice of input and output terminals and element values. The tunable range of frequencies for the biquad was designed to be 18–59MHz. The quality factor of the biquad was designed to be tunable from approximately 1/3 to 3. The filter was designed in LEVEL2 SPICE, laid out using MAGIC, and the circuit was fabricated using MOSIS's 2 μ m CMOS analog (n-well) process. The circuit board for testing the chip was designed using the PCB design system – PADS-PCB. The chip was tested using the Network Analyzer HP 4195A. The performance of the filter was then compared with the design objectives and simulation results.

Both the pole frequency and the quality factor were found to be tunable by the same factor as the design. Noise analysis showed the output noise to be less than –65dB. The notch function could not be experimentally verified due to high sensitivity of this function to component tolerances and process variations. Power dissipation of the filter was found to be 6mW.

DESIGN OF A SECOND-ORDER FILTER USING THE g_m -C TECHNIQUE

by

Girish Chandrasekaran

A thesis submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE
in
ELECTRICAL AND COMPUTER ENGINEERING

Portland State University
1996

ACKNOWLEDGEMENTS

I should express my most sincere appreciation to my academic advisor, Dr. Rolf Schaumann, for his careful review of my work and generous advice throughout the course of my work on this project. I also thank Dr. Robert Daasch who helped me with the tools, with the fabrication of the circuit by MOSIS, and also with his feedback on my writing. A special thank you to Jonathan Walker and Tom Kautzmann for helping me build the circuit board to test the chip. I would also like to acknowledge Marijan Persun's help with the formatting of the documentation as well as his suggestions on certain aspects of testing. I also record my gratitude to David Chiang who helped me with his valuable hints while working on a similar design project.

I would also like to thank Shirley Clark and Laura Riddell at the EE office for their continued support. Marcin Stegawski deserves special mention for his review and feedback on the chapter on test results. Finally, I would like to thank all my friends for being a constant source of inspiration and support.

TABLE OF CONTENTS

LIST OF TABLES	vi
LIST OF FIGURES	vii
CHAPTER 1	
1 INTRODUCTION	1
1.1 Active realization of LC networks using the $g_m - C$ technique	1
1.2 Inductor realization using the principle of the gyrator	2
1.3 Resistor realization using transconductors	4
1.4 The OTA- C integrator – principle behind construction	6
1.5 The biquad	8
CHAPTER 2	
2 THE OTA-C INTEGRATOR	10
2.1 The OTA- C integrator as a building block	10
2.2 Design of the transconductance element	10
2.3 Second-order effects causing deviations from predicted linearity	12
2.3.1 Body effect	12
2.3.2 Mobility variation	13
2.4 The negative resistance load	14
2.4.1 Effect of channel-length modulation	14
2.4.2 Cancellation of output resistance using the negative resistance load	14
2.5 Frequency response from the small-signal equivalent circuit	15

2.6 Low-output resistance floating voltage source V_B	19
2.7 Voltage source $V_{DD} - V_A$	21

CHAPTER 3

3 FINAL DESIGN AND SIMULATION OF THE INTEGRATOR	22
3.1 Final design of the integrator	22
3.2 MOS model parameters	23
3.3 Simulation results	23

CHAPTER 4

4 THE BIQUAD – DESIGN AND SIMULATION	32
4.1 The biquad	32
4.1.1 Lowpass function	33
4.1.2 Highpass function	33
4.1.2 Bandpass function	34
4.1.3 Notch function	34
4.2 Fully-differential biquad realized using transconductors	35
4.2.1 Realization of the bandpass filter	36
4.2.2 Realization of the lowpass filter	36
4.2.3 Realization of the highpass filter	37
4.2.4 Realization of the notch filter	37
4.3 Simulation results	38
4.3.1 Lowpass filter	38
4.3.2 Bandpass filter	40

4.3.3 Highpass filter	42
4.3.4 Notch filter	42
4.4 Conclusions	44
CHAPTER 5	
5 LAYOUT, FABRICATION AND TEST RESULTS	45
5.1 Layout	45
5.2 Circuit board design	49
5.3 Test results	53
5.3.1 Lowpass filter	54
5.3.2 Bandpass filter	57
5.3.3 Highpass filter	58
5.3.4 Notch Filter	59
5.3.5 Power Dissipation Measurement	60
5.4 Comparisons	61
CHAPTER 6	
6 CONCLUSION	64
6.1 Conclusion	64
6.2 Further work	64
REFERENCES	66
APPENDIX A	67
A.1 Spice model parameters used for design	67
A.2 Spice model parameters from the process used for fabrication	67

LIST OF TABLES

TABLE	PAGE
3.1 OTA characteristic parameters	23
3.2 Results of Fourier analysis with a $1V_{p-p}$ sine wave input	27
5.1 Lowpass filter test results	54
5.2 Bandpass filter test results	57
5.3 Highpass filter test results	58
5.4 Comparison between results from SPICE simulations and tests	61

LIST OF FIGURES

FIGURE		PAGE
1.1	Gyrator symbol, generic small-signal equivalent, gyrator simulation of a grounded inductor, gyrator simulation of a floating inductor	3
1.2	Simulation of resistors using transconductors	5
1.3	Conceptual block diagram of the OTA-C integrator and its small-signal equivalent circuit	7
1.4	<i>LC</i> ladder-based general single-ended biquad	8
2.1	Circuit schematic of the CMOS OTA-C integrator	11
2.2	Small-signal equivalent half-circuit of the OTA-C integrator	15
2.3	Simplified small-signal model of the half-circuit of the OTA-C integrator	16
2.4	Simplified half-circuit of the transconductor	18
2.5	Complete circuit diagram of the OTA-C integrator	19
2.6	Circuitry used to implement the floating voltage source V_B	19
2.7	ac schematic of the output transistor Ma3 and its small-signal equivalent	20
3.1	Complete circuit diagram of the modified OTA-C integrator	22
3.2	Frequency response of the OTA over its tuning range (in dB)	24
3.3	Frequency response of the OTA over its tuning range (in μS)	24
3.4	Tuning capability of the OTA element	25
3.5	Tuning capability of the OTA element	26
3.6	Transient analysis with a $1V_{p-p}$ sine wave input	27

3.7	Frequency response of the OTA–C integrator	28
3.8	Tuning of output resistance – variation of dc gain	29
3.9	Tuning of output resistance – variation of phase	29
3.10	Common–mode rejection ratio	30
3.11	Power–supply rejection ratio	30
4.1	Differential version of the biquad realized using transconductors	35
4.2	Pole frequency tuning of the lowpass filter	39
4.3	Q –tuning of the lowpass filter	40
4.4	Pole frequency tuning of the bandpass filter	41
4.5	Q –tuning of the bandpass filter	41
4.6	Pole frequency tuning of the highpass filter	42
4.7	Q –tuning of the highpass filter	43
4.8	Zero frequency tuning of notch filter	43
5.1	Layout of the transconductor (OTA) in MAGIC	46
5.2	Layout of the filter in MAGIC	47
5.3	Layout of the filter within the MOSIS pad frame in MAGIC	48
5.4	Circuit schematic of the buffer	49
5.5	Pinout of the chip	50
5.6	Different components used in the design of the board and the symbols used to represent them in the board schematic	51
5.7	Schematic of the circuit board	51
5.8	Layout of the board in PADS–PCB	52
5.9	Magnitude and phase responses of the lowpass filter	55

5.10	Magnitude response of the lowpass filter and output noise	55
5.11	Pole frequency tuning of the lowpass filter	56
5.12	Q -tuning of the lowpass filter	56
5.13	Distortion analysis of a 1MHz output signal for the lowpass filter	57
5.14	Frequency response of the bandpass filter	58
5.15	Frequency response of the highpass filter	59
5.16	Comparison between lowpass filter transfer functions	61
5.17	Comparison between the bandpass filter transfer functions	62
5.18	Comparison between highpass filter transfer functions	62

CHAPTER 1

INTRODUCTION

1.1 Active realization of *LC* networks using the g_m -*C* technique

LC filter networks play a very important role in the area of communications and measurement equipment. Lowpass filters may be used to eliminate high frequency noise in a system. Notch filters are typically used to eliminate any troublesome frequencies, for instance, a 60-Hz power supply interference. Bandpass filters are needed to eliminate low-frequency and high-frequency components when making measurements over a relatively narrow signal bandwidth. There are many important features associated with *LC* filters. *LC* resonance circuits allow impedances to have extremely rapid changes in magnitude and phase. By appropriate interconnection of these impedances, one can realize filters with very steep slopes between passbands and stopbands. Series or parallel resonance can be used to block or transmit completely some frequencies. Also, *LC* ladder filters exhibit very low passband sensitivities to element tolerances. Inductors, however, present a problem in such realizations, especially if the filter is to be realized on an integrated circuit chip, as they tend to be large and bulky. This implies the need for active simulations of passive *LC* filters.

A large majority of simulated *LC* filters are built with operational amplifiers (op amps) and operational transconductance amplifiers (OTAs) [1]. OTAs have much higher bandwidths than op amps, can be easily tuned and provide much simpler circuitry for integration with other analog or digital circuits on the same silicon chip. Also analog filters

realized with OTAs often have fewer components than their op amp counterparts. For these reasons, OTAs are being increasingly used to build integrated filter networks.

Since any filter can be realized using the three passive elements – namely the resistor, inductor and capacitor, active realization of inductors and resistors using OTAs reduces the *RLC* filter network to just a set of transconductors and capacitors. The most popular method for active realization of inductors is based on the principle of the gyrator. The gyrator is constructed using OTAs. Resistors are realized from transconductors by simply connecting the output back to the inverting input. Hence, the basic building block in such filters is the capacitively loaded transconductor or the OTA–*C* integrator and this technique of filter implementation is called the OTA–*C* or g_m –*C* technique [1,2].

1.2 Inductor realization using the principle of the gyrator

Inductors can be simulated using the gyrator [1]. A gyrator, shown in Fig. 1.1, is a two–port network in which the current through each port is proportional to the voltage across the other port. The gyrator construction is thus inherently based on using transconductances. The input impedance Z_{in} in such networks is inversely proportional to the output impedance Z_{out} , *i.e.* $Z_{in} \propto 1/Z_{out}$. As will be shown in this section, this network simulates an inductive impedance at the input when loaded capacitively at the output.

Figure 1.1 (a) Gyrator symbol; (b) Generic small-signal equivalent circuit; (c) Gyrator simulation of a grounded inductor; (d) Gyrator simulation of a floating inductor

From Figs. 1.1(b) and (c),

$$\frac{V_1}{I_1} = \frac{V_1}{g_{m2}V_2} \quad (1.1)$$

But

$$V_2 = \frac{-I_2}{sC} = \frac{g_{m1}V_1}{sC} \quad (1.2)$$

Hence

$$\frac{V_1}{I_1} = \frac{V_1}{g_{m2}(\frac{g_{m1}V_1}{sC})} = \frac{sC}{g_{m2}g_{m1}} = sL \quad (1.3)$$

where

$$L = \frac{C}{g_{m1}g_{m2}} \quad (1.4)$$

Hence by choosing an appropriate value for the load capacitor C and tuning the transconductors g_{m1} and g_{m2} , the inductance value L looking into the input port (for the grounded inductor) can be varied over the desired range. A floating inductor can be realized by cascading two grounded gyrators and a capacitor as shown in Fig. 1.1(d). In this case

$$V_x = -\frac{I_{1x} + I_{2x}}{sC} = -\frac{(-g_m V_1 + g_m V_2)}{sC} = \frac{g_m(V_1 - V_2)}{sC} \quad (1.5)$$

Also

$$I_1 = -I_2 = g_{mx} V_x = \frac{g_{mx} g_m (V_1 - V_2)}{sC} \quad (1.6)$$

Hence

$$\frac{V_1 - V_2}{I_1} = \frac{sC}{g_{mx} g_m} = sL \quad (1.7)$$

where

$$L = \frac{C}{g_{mx} g_m} \quad (1.8)$$

1.3 Resistor realization using transconductors

Resistors can be easily constructed from transconductors by connecting their outputs back to their inverting inputs. Fig. 1.2 shows a transconductor and the realization of both grounded and floating resistors using transconductors.

Figure 1.2 Simulation of resistors using transconductors (a) transconductor; (b) grounded resistor; (c) floating resistor

The single-ended transconductor in Fig. 1.2(a) is described via

$$I_o = g_m(V_2 - V_1) \quad (1.9)$$

so that the single-ended simulated resistor in Fig. 1.2(b) leads to the equation

$$I_1 = g_m V_1 \quad (1.10)$$

$$\frac{V_1}{I_1} = \frac{1}{g_m} \quad (1.11)$$

Similarly, for implementing the floating resistor in Fig. 1.2(c), we find

$$I_1 = I_2 = g_m(V_1 - V_2) \quad (1.12)$$

$$\frac{V_1 - V_2}{I_1} = \frac{1}{g_m} \quad (1.13)$$

By tuning g_m , the resistance looking into the input node (in the case of the grounded resistor) or the resistance between V_1 and V_2 (in the case of the floating resistor) can be tuned to any desired value.

1.4 The OTA- C integrator – principle behind construction

The OTA- C integrator is the basic building block in the construction of g_m - C filters [1,2]. A key performance parameter for the integrator is the phase shift at its unity-gain frequency. Deviations from the ideal -90° phase are due to finite dc gain (finite output resistance) and parasitic poles of the transconductor. Also, any non-linearities of the transconductor result in signal-level-dependent frequency response deviations of gain and phase in both the integrator and the filter. Therefore, to avoid deviations in the filter characteristics, a high-dc-gain integrator, with parasitic poles located much higher than the filter cutoff frequency is required to keep the integrator phase at -90° . Also, a highly linear transconductance element is required to keep the filter characteristics independent of the signal level.

Figure 1.3 (a) Conceptual block diagram of the OTA-C integrator with high dc gain; (b) small-signal macromodel including parasitic output resistance R_{out} in parallel with a negative resistance R_N

The conceptual block diagram of the OTA-C integrator used in this design is shown in Fig.1.3(a) [5]. This comprises two fully-differential OTAs of transconductances g_{m1} and g_{m2} and a load capacitor C . The OTAs are assumed to be non-ideal with finite output resistances $r_{o1} = 1/g_{o1}$ and $r_{o2} = 1/g_{o2}$. OTA2 forms a negative resistance load (since its non-inverting input is connected to its non-inverting output terminal and the inverting input is connected to its inverting output) with an equivalent resistance $R_N = -1/g_{m2}$ that compensates the parasitic output resistance $R_{out} = 1/(g_{o1} + g_{o2})$. The voltage transfer function for this integrator from the small-signal equivalent circuit of Fig. 1.3(b) is

$$\frac{V_{out}}{V_{in}} = - \frac{g_{m1}}{sC - g_{m2} + \frac{1}{R_{out}}} \quad (1.14)$$

Choosing g_{m2} equal to $1/R_{out}$ results in a g_m - C integrator with infinite dc gain but $g_{m2} > 1/R_{out}$ leads to instability due to a right-half plane (RHP) pole. This dc gain en-

hancement method does not introduce any bandwidth limitation since no additional internal nodes are generated [5]. (Internal node in a circuit refers to any node besides the power supply, ground, dc bias points, input and output nodes).

1.5 The biquad

Active filters which realize transfer functions of the form

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + s \frac{\omega_0}{Q_p} + \omega_0^2} \quad (1.15)$$

are called *biquads* [1]. Biquads form a fundamental building block for the construction of higher-order filters in the form of cascade or multiple-loop feedback topologies. A cascade of biquads and first-order sections can realize arbitrary transfer functions because each biquad can be configured to implement zeroes anywhere in the s -plane.

Unlike biquads, LC ladders can implement zeroes only along the $j\omega$ -axis. LC ladders are extensively used in filter design because of their low passband sensitivity to component tolerances. To implement arbitrary transmission zeroes without destroying the poles, the input signal voltage V_i is fed forward into any nodes lifted off ground or a current proportional to V_i is fed into any of the floating nodes. Ladder-based biquads retain the advantage of the ladder topology, *i.e.* low sensitivity to component variations, and are capable of implementing transmission zeroes at any location.

Figure 1.4 (a) LC ladder-based general single-ended biquad; (b) non-inverting transconductor; (c) inverting transconductor

Fig. 1.4(a) shows an LC ladder-based biquad [1] made of single-ended transconductors. Fig. 1.4(b) and 1.4(c) show the symbols used for the non-inverting and inverting transconductors, respectively. The circuit in Fig. 1.4(a) realizes the transfer functions

$$V_{o1} = \frac{s^2 C^2 V_3 + sC(g_{m1}V_3 - g_{m2}V_2) + g_{m0}g_{m2}V_1}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} \quad (1.16)$$

$$V_{o2} = \frac{s^2 C^2 V_2 - sCg_{m0}V_1 + sCg_{m3}V_3}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} \quad (1.17)$$

which can implement any arbitrary type of second-order function by appropriate choice of input and output terminals, and element values. (g_{m0} , g_{m1} , g_{m2} and g_{m3} are the transconductances of transconductors 0, 1, 2 and 3 respectively. C is the load capacitance at output nodes V_{o1} and V_{o2}). When the grounded nodes V_2 and V_3 are lifted off ground and used as inputs, the numerators in equations (1.16) and (1.17) are generated.

This thesis deals with the design of a biquad of the type shown in Fig. 1.4(a) using differential transconductors. The design and fabrication is performed using MOSIS's $2\mu\text{m}$ CMOS analog n-well process.

CHAPTER 2

THE OTA–C INTEGRATOR

2.1 The OTA–C integrator as a building block

The OTA–C integrator is the basic building block in the construction of high–performance filters using the g_m –C technique. Four important factors to be considered in the design of OTAs are linearity, bandwidth, output resistance and phase. High linearity over a wide dynamic range is required to keep the OTA output current and hence the filter characteristics independent of the input signal level. The OTA being a voltage–controlled current source should ideally have infinite output resistance. A finite output resistance reduces the dc gain and hence affects the phase response of the integrator and consequently the quality factor (Q) of the filter in which it is used. Also, the OTA should have a high bandwidth with its parasitic poles located much higher than the cut–off frequency of the filter for the output phase to remain unaffected.

2.2 Design of the transconductance element

The design of a linear, fully–balanced, voltage–tunable CMOS operational transconductance amplifier [5] is addressed in this section. It uses two cross–coupled differential NMOS pairs M1, M2 and M3, M4 as in Fig. 2.1. The devices are identical and operate in saturation. A dc current sink $2I_0$ is used to bias the OTA. A floating voltage source V_B with low output resistance is used to tune the transconductance g_m . The negative resistance load composed of transistors M5, M6, M7 and M8 cancels out the parasitic output resistance of the transconductor and hence enhances the dc gain. The voltage difference

$V_{DD}-V_A$ is used to tune the negative resistance load. Since this topology does not introduce any additional internal nodes, dc-gain enhancement is obtained without any bandwidth limitation. (c and d are examples of internal nodes in Fig. 2.1).

Figure 2.1 Circuit schematic of the CMOS OTA-C integrator

Using the current equation for the MOS transistor in saturation, the currents I_1 and I_2 shown in Fig. 2.1 are:

$$I_1 = k_n(V_P - V_{Tn})^2 + k_n(V_Q - V_B - V_{Tn})^2 \quad (2.1)$$

$$I_2 = k_n(V_Q - V_{Tn})^2 + k_n(V_P - V_B - V_{Tn})^2 \quad (2.2)$$

where $k_n = 0.5\mu_n C_{ox} W/L$ is the transconductance parameter, μ_n is the effective surface mobility of electrons in the channel, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor and V_{Tn} is the threshold voltage. V_P and V_Q

are the gate–source voltages of M1 and M2, respectively. The small–signal differential output current $I_{out} = I_1 - I_2$ can be expressed in terms of V_B as

$$I_{out} = I_1 - I_2 = 2k_n V_B (V_P - V_Q) = 2k_n V_B V_{id} = g_m V_{id} \quad (2.3)$$

where $V_{id} = V_P - V_Q$ is the differential input voltage. Thus, the transconductor exhibits a perfectly linear characteristic, $g_m = 2k_n V_B$ which is tunable by varying V_B . The input signal is assumed to be fully balanced around a common–mode value.

2.3 Second–order effects causing deviations from predicted linearity

(2.3) predicts a perfectly linear transconductor with $g_m = 2k_n V_B$. In actuality, second–order effects, such as body–effect and mobility reduction, introduce non–linearities.

2.3.1 Body effect

Assuming implementation in a $2\mu\text{m}$ CMOS n–well process, the identical NMOS transistors M1, M2, M3 and M4 are placed in a common p–substrate tied to ground. Since the source–body voltage V_{SB} for these transistors is non–zero and not constant with the applied differential input voltage, the threshold voltage V_{Tn} for each transistor is

$$V_{Tn} = V_{Tn0} + \gamma[(2\Phi_b + V_{SB})^{\frac{1}{2}} - (2\Phi_b)^{\frac{1}{2}}] \quad (2.4)$$

where V_{Tn0} is the threshold voltage with no body–effect, γ is the bulk–threshold parameter, and Φ_b is the strong–inversion surface potential [4]. This implies that the threshold voltages of the transistors M3, M4 are different from the threshold voltages of the transistors M1, M2.

2.3.2 Mobility variation

The mobility μ_n of carriers in the channel is not constant with increase in the gate–source voltage. In order to simulate this effect, a variation of the parameter μ_n with the gate–source voltage is introduced. This is modeled in LEVEL2 SPICE [3] by the equation

$$\mu'_n = \mu_n \left(\frac{\epsilon_s}{\epsilon_{ox}} \frac{U_c t_{ox}}{V_{GS} - V_{TH} - U_t V_{DS}} \right)^{U_e} \quad (2.5)$$

where the parameter U_c is the gate–to–channel critical field, the term $(V_{GS} - V_{TH} - U_t V_{DS})/t_{ox}$ represents the average electric field perpendicular to the channel, U_t represents the contribution of the drain voltage to the gate–to–channel electric field and U_e is the exponential coefficient for the mobility. μ'_n and μ_n are the mobilities with and without mobility variation.

In practice, it is found [5] that proper scaling of MOS devices M1, M2, M3 and M4 is required to eliminate non–linearities. Assuming parameters $k_{n1,2}$, $V_{Tn1,2}$ for transistors M1 and M2 and $k_{n3,4}$, $V_{Tn3,4}$ for transistors M3 and M4, equations (2.1) and (2.2) can be modified as

$$I_1 = k_{n1,2}(V_P - V_{Tn1,2})^2 + k_{n3,4}(V_Q - V_B - V_{Tn3,4})^2 \quad (2.6)$$

$$I_2 = k_{n1,2}(V_Q - V_{Tn1,2})^2 + k_{n3,4}(V_P - V_B - V_{Tn3,4})^2 \quad (2.7)$$

$$\begin{aligned} I_1 - I_2 = & V_{id}[k_{n1,2}(V_P + V_Q - 2V_{Tn1,2}) \\ & - k_{n3,4}(V_P + V_Q - 2V_B - 2V_{Tn3,4})] \end{aligned} \quad (2.8)$$

Eq. (2.8) can be written as

$$\begin{aligned} I_1 - I_2 = & V_{id}[(k_{n1,2} - k_{n3,4})(V_P + V_Q) \\ & + 2(V_{Tn3,4}k_{n3,4} - V_{Tn1,2}k_{n1,2}) + 2k_{n3,4}V_B] \end{aligned} \quad (2.9)$$

For achieving perfect linearity,

$$(k_{n1,2} - k_{n3,4})(V_P + V_Q) + 2(V_{Tn3,4}k_{n3,4} - V_{Tn1,2}k_{n1,2}) = 0 \quad (2.10)$$

This implies,

$$\frac{k_{n1,2}}{k_{n3,4}} = \frac{V_P + V_Q - 2V_{Tn3,4}}{V_P + V_Q - 2V_{Tn1,2}} \quad (2.11)$$

Eq. (2.8) now reduces to

$$I_{out} = I_1 - I_2 = 2k_{n3,4}V_B \quad (2.12)$$

where $k_{n1,2} = 0.5\mu_{n1,2}C_{ox}(W/L)_{1,2}$ and $k_{n3,4} = 0.5\mu_{n3,4}C_{ox}(W/L)_{3,4}$. Hence, to achieve non-linearity cancellation, appropriate scaling of the W/L ratios of the transistors becomes necessary.

2.4 The negative resistance load

2.4.1 Effect of channel-length modulation

Since the transistors M1, M2, M3 and M4 that form the transconductance element operate in saturation, channel-length modulation causes a slight increase in the drain-source current with an increase in the drain-source voltage. This is represented by the equation

$$I_{ds} = k \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \quad (2.13)$$

where λ is the channel-length modulation factor and k is μC_{ox} [4]. This implies that the transconductance element has a finite output resistance. A negative resistance load is hence used to cancel out this output resistance.

2.4.2 Cancellation of output resistance using the negative-resistance load

The negative resistance load in Fig. 2.1 composed of PMOS transistors M5, M6, M7 and M8 has exactly the same topology as the basic transconductance element. The nega-

tive resistance is realized due to the fact that the output of the transconductor forming the negative resistance load is fed back to its non-inverting input. Assuming that all the transistors are operating in saturation and applying the square law characteristic for the devices M5–M8, the current difference $I_a - I_b$ can be expressed as

$$I_a - I_b = 2k_p(V_{DD} - V_A)V_{out} \quad (2.14)$$

where $V_{out} = V_a - V_b$ is the differential output voltage.

Assuming V_A is positive and $V_A < V_{DD}$, the equivalent negative resistance R_N is

$$R_N = -\frac{V_{out}}{I_a - I_b} = -\frac{1}{2k_p(V_{DD} - V_A)} \quad (2.15)$$

and is linear if second-order effects are neglected. The resistance R_N is varied by tuning the voltage difference $V_{DD} - V_A$.

2.5 Frequency response from the small-signal equivalent circuit

Fig. 2.2 shows the small-signal half-circuit equivalent of the integrator that is used to study the frequency response of the OTA-C integrator [5]. Fig. 2.3 shows the simplified final version.

Figure 2.2 Small-signal equivalent half-circuit of the OTA-C integrator

Figure 2.3 Simplified small-signal model of the half-circuit of the OTA-C integrator

It is assumed that the widths W_i , $i = 1, 2, 3, 4$, of all the transistors in the transconductance element, are equal. C_{gd} represents the gate-drain capacitance, C_{ds} represents the drain-source capacitance, and $g_{oi} = 1/R_{oi}$ represents the output conductance of the MOS transistor.

Applying this model, the transfer function is given by

$$A(s) = - \frac{g_m}{s(C_L + C_P) + \frac{1}{R_P} + \frac{1}{R_N}} \quad (2.16)$$

where the parameters of the model are defined as

$$g_m = g_{m1} - g_{m4} \quad (2.17)$$

$$C_{in} = C_{gs1} + C_{gs3} + 2C_{gd} \quad (2.18)$$

$$C_P = C_{ds1} + C_{ds4} + C_{ds5} + C_{ds8} + C_{gs5} + C_{gs7} + 2C_{gd} + 2C_{gd7} + 2C_{gd8} \quad (2.19)$$

$$R_P = \frac{1}{g_{o1} + g_{o4} + g_{o5} + g_{o8}} \quad (2.20)$$

$R_N = -R_P$ implies infinite dc gain. The maximal dc gain of the integrator is limited only by mismatch. To avoid stability problems due to the creation of right-half plane poles, g_o in the transfer function

$$\frac{v_o}{v_i} = \frac{g_m}{sC + g_o} \quad (2.21)$$

should be positive. *i.e.*,

$$g_o = |g_P| - |g_N| > 0 \quad (2.22)$$

This implies

$$|g_P| \geq |g_N| \quad (2.23)$$

or from Eq. (2.15)

$$V_A \geq V_{DD} - \frac{1}{2k_p R_P} \quad (2.24)$$

Tuning of the negative resistance load (NRL) is necessary to obtain better accuracy in filter response (Q -tuning).

Scaling the transistors in the transconductance element introduces a zero due to non-equal gate-drain overlap capacitances of the transistors M1, M4 and M2, M3. Simplifying the small-signal equivalent circuit in Fig. 2.2 to include only the transconductance element without the NRL and considering only the gate-drain overlap capacitances and ignoring all other capacitances, the small-signal equivalent circuit can be redrawn as shown in Fig. 2.4.

Figure 2.4 Simplified half-circuit of the transconductor

Assuming the output voltage swing to be zero or very small compared to the input swing v_{id} , the output current i_{out} can be expressed as

$$\frac{i_{out}}{2} = (g_{m1} - g_{m4}) \frac{v_{id}}{2} + s(C_{gd4} - C_{gd1}) \frac{v_{id}}{2} \quad (2.25)$$

$$\frac{i_{out}}{v_{id}} = (g_{m1} - g_{m4}) + s(C_{gd4} - C_{gd1}) \quad (2.26)$$

Equation (2.26) has a zero at,

$$s = - \frac{g_{m1} - g_{m4}}{C_{gd4} - C_{gd1}} \quad (2.27)$$

Eq. (2.27) shows the location of the zero due to unequal gate-drain overlap capacitances.

The complete circuit diagram of the OTA-C integrator with the circuitry used to implement the floating voltage source V_B , the voltage source $V_{DD} - V_A$ and the current sink $2I_0$ is shown in Fig. 2.5.

Figure 2.5 Complete circuit diagram of the OTA-C integrator with circuitry used to implement the floating voltage source V_B and the current sink $2I_0$.

2.6 Low-output resistance floating voltage source V_B

Figure 2.6 Circuitry used to implement the floating voltage source V_B .

Fig. 2.6 shows the circuitry used to implement the floating voltage source V_B with low output resistance. The voltage V_B can be approximated from the loop equation as

$$V_B = V_{gsma3} + (V_{gsma1} - V_{Tma1}) - (V_{gsma2} - V_{Tma2}) \quad (2.28)$$

$$V_B = V_{gsma3} + \left(\frac{I_{CF}}{k_{nma2}}\right)^{\frac{1}{2}} - \left(\frac{I_S - I_{CF}}{k_{nma1}}\right)^{\frac{1}{2}} \quad (2.29)$$

Since the transistors Ma1 and Ma2 are in saturation with constant drain currents, the small-signal drain current $g_m v_{gs}$ through each of these transistors is zero. This implies that the small-signal voltage $v_{gs} = 0$, *i.e.* the gate and source voltages track each other. This implies further that the voltages at the nodes *a*, *b* and *c* in Fig. 2.6 track each other. Hence, for the transistor Ma3, the gate and drain terminals are ac short, so that the small-signal equivalent circuit for Ma3 is as shown in Fig. 2.7.

Figure 2.7 (a) ac schematic of output transistor Ma3; (b) Small-signal equivalent of Ma3

From Fig. 2.7(b),

$$i_x = g_{ma3}v_{gsa3} + \frac{v_{gsa3}}{r_o} \quad (2.30)$$

Since $v_{gsa3} = v_x$,

$$i_x = g_{ma3}v_x + \frac{v_x}{r_o} \quad (2.31)$$

so that for $r_o \gg \frac{1}{g_{ma3}}$,

$$r_{out} = \frac{v_x}{i_x} = \frac{1}{g_{ma3} + \frac{1}{r_o}} \approx \frac{1}{g_{ma3}} \quad (2.32)$$

Hence, this topology realizes a low-impedance floating voltage source with output resistance $1/g_m$ which is very small compared to the output resistance r_o of the transistor in saturation.

2.7 Voltage source $V_{DD}-V_A$

A single transistor M9 is used to implement the voltage $V_{DD} - V_A$ that is used to tune the NRL. For M9 operating in the linear region, the small-signal current through it is expressed as

$$i_{ds} = g_m v_{gs} + g_{ds} v_{ds} \quad (2.33)$$

Since the gate and source are at fixed potentials, the small-signal gate voltage v_{gs} is zero.

Hence

$$i_{ds} = g_{ds} v_{ds} \quad (2.34)$$

The output resistance is given by

$$\frac{v_{ds}}{i_{ds}} = \frac{1}{g_{ds}} \quad (2.35)$$

Since M9 is operating in the linear region, its conductance g_{ds} is large, or alternately its output resistance is small.

3.1 Final design of the integrator

3.2 MOS model parameters

The design was simulated in LEVEL 2 SPICE with MOS model parameters from run N52W of MOSIS's 2 μ m CMOS analog process provided by ORBIT. The model parameters are listed in Appendix A.1.

3.3 Simulation results

The OTA was characterized to have the parameters in Table 3.1 from simulation of the spice netlist.

Table 3.1 OTA characteristic parameters ($V_{DD} = 5V$, $V_{bias} = 1.2V$, $V_{CF} = 0.8V-1.3V$)

Characteristic	Value
Transconductance range	170–563 μ S
Bandwidth	>1GHz
DC voltage gain	>71dB
Power Consumption	2.94mW
Total Harmonic Distortion	0.11%
CMRR	45dB @ 50MHz
PSRR	46.5dB @ 50MHz
Output Resistance	13–117M Ω
Differential input capacitance	0.0235pF
Differential output capacitance	0.07pF

The power consumption, as is typical in CMOS circuits, is very low : 2.94mW. Simulations show that the OTA has a very high bandwidth – above 1GHz. This can be seen in Fig. 3.2 which shows the frequency response of the OTA in dB ($20\log_{10}(g_m)$) . The high bandwidth is attributed to a pole–zero cancellation at the occurrence of the dominant pole. Fig. 3.3 shows the frequency response of the transconductor in μ S. Fig. 3.2 and Fig. 3.3 show the frequency response of the OTA for different values of the transconductance g_m . The OTA is tuned by changing the voltage V_{CF} .

Figure 3.2 Frequency response of the OTA over its tuning range.

Figure 3.3 Frequency response of the OTA over its tuning range.

Fig. 3.4 shows the DC transfer curve of the OTA. It shows the plot of the output current against the differential input voltage. The voltage V_{CF} , taken as the parameter, (for the family of curves shown in the figure) changes the slope of the DC transfer curve and hence g_m .

Figure 3.4 Tuning capability of the OTA element with V_{CF} taken as parameter.

Fig. 3.5 shows the transconductance g_m against the differential input voltage. It is obtained from the derivative of the output current in Fig. 3.4. The transconductance could be varied from $170\mu S$ to $563\mu S$ by changing the voltage V_{CF} from $0.8V$ to $1.3V$. Fig. 3.5 shows the OTA to be most linear for a g_m of $280\mu S$ (for $V_B = 1V$) over an input differential voltage range of $\pm 0.5V$. The OTA is found to be less linear for lower or higher values of g_m . This is possibly due to the fact that the simulated voltage source V_B has the smallest output resistance for a specific voltage V_B that corresponds to $g_m = 280\mu S$. Harmonic distortion analysis with g_m set to this value and a load resistance of $1/g_m = 3.58k\Omega$ (differen-

tial load of $2 \times 3.58 \text{ k}\Omega = 7.16 \text{ k}\Omega$) shows a harmonic distortion of 0.11% for a differential signal of $1 V_{p-p}$ of frequency 1 kHz. The results of the Fourier Analysis are shown in Table 3.2. The input and output waveforms from the transient analysis are shown in Fig. 3.6.

Figure 3.5 Tuning capability of the CMOS OTA element with V_{CF} taken as parameter. The transconductance g_m could be tuned from $170 \mu\text{S}$ – $563 \mu\text{S}$

Harmonic Distortion [7] is defined as

$$\text{THD} = 100 \frac{(V_2^2 + V_3^2 + V_4^2 + \dots V_9)^{\frac{1}{2}}}{V_1} \% \quad (3.1)$$

where V_1 is the amplitude of the output signal and V_n , $n = 2, 3, 4, \dots, 9$ are the amplitudes of the second, third, fourth and higher harmonics.

Table 3.2 Results of Fourier analysis with a $1V_{p-p}$ sine wave input and a load resistance of $1/g_m$.

Number of harmonics: 10, THD: 0.11%

Harmonic	Frequency (Hz)	Magnitude	Phase (in degrees)	Norm. Mag	Norm. Phase
0	0	-4.62e-06	0	0	0
1	1000	0.49	-144	1	0
2	2000	1.17e-05	-91.52	2.36e-05	52.47
3	3000	0.0004	108.43	0.000976	252.43
4	4000	5.95e-06	-109.41	1.20e-05	34.59
5	5000	0.0001	-177.44	0.00037	-33.44
6	6000	8.32e-06	-34.72	1.67e-05	109.27
7	7000	0.0001	70.35	0.00029	214.35
8	8000	1.9e-05	-74.99	3.84e-05	68.99
9	9000	0.0001	-38.65	0.00021	105.34

Figure 3.6 Transient analysis with a $1V_{p-p}$ sine wave input, $g_m = 280\mu S$ and $R_L = 1/g_m$.
Gain = $g_m R_L = 1$

The frequency response of the OTA-C integrator (capacitive load of 0.5pF) is shown in Fig. 3.7. The integrator shows finite dc gain due to finite output resistance. The dc gain (g_m/g_o) and the unity-gain frequency (g_m/C) are tuned by varying the transconductance g_m . This is seen in Fig. 3.7 where the voltage V_{CF} is taken as the parameter. Fig. 3.8 shows the variation of the dc gain (g_m/g_o) with variation in the output resistance ($1/g_o$) obtained by tuning the NRL control voltage V_{CQ} for a fixed g_m . The dc gain could be kept above 71dB by varying the voltage V_{CQ} from 2.64V to 2.86V. Calculations show the output resistance to be as high as 117M Ω if the NRL element is appropriately tuned. The maximal dc gain of the integrator is limited only by mismatch. Fig. 3.9 shows the phase response of the integrator. The phase is -90° at high frequencies. As V_{CQ} is increased, the integrator gets overcompensated resulting in output phase reversal. This indicates instability due to the creation of right-half-plane poles.

Figure 3.7 Frequency response of OTA-C integrator with V_{CF} taken as parameter, $V_{CQ} = 2.63V$

Figure 3.8 Tuning of output resistance – V_{CQ} taken as parameter. $V_{CF} = 1.04V$.

Figure 3.9 Tuning of output resistance – output phase approaching ideal -90° phase at high frequencies. V_{CQ} taken as parameter. Phase reversal occurs at high V_{CQ} .

Figure 3.10 Common-mode rejection ratio of the OTA element

Figure 3.11 Power-supply rejection ratio of the OTA element.

Fig. 3.10 and Fig. 3.11 show the Common Mode Rejection Ratio (CMRR) and the Power Supply Rejection Ratio (PSRR) as a function of frequency. The simulations were performed with 0.5% mismatch in device parameters k_n , k_p , V_{Tn} and V_{Tp} . The CMRR was found to be 45dB at 50MHz. The PSRR is 46.5dB at 50MHz.

CMRR is defined as

$$CMRR = \frac{A_d}{A_c} \quad (3.2)$$

where A_d is the differential gain and A_c is the common-mode gain. The common-mode gain A_c is computed from the average of the ac signals at the two outputs with an ac common-mode input signal of amplitude 1V.

PSRR is defined as

$$PSRR = \frac{A_d}{A_s} \quad (3.3)$$

where A_d is the differential gain and A_s is the gain of the path from an ac signal at the power supply to the output. It is computed from the differential output ac signal with an ac signal of 1V amplitude superimposed on the dc power supply and zero input differential ac signal.

CHAPTER 4

THE BIQUAD – DESIGN AND SIMULATION

4.1 The biquad

The fully-differential biquad in Fig. 1.4 realizes the second-order transfer function of the form

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} = \frac{a_2(s + z_1)(s + z_2)}{(s + p_1)(s + p_2)} \quad (4.1)$$

where $-z_1, -z_2$ are the zeroes and $-p_1, -p_2$ are the poles of the transfer function. For complex poles and zeroes, where $z_1 = z_2^*$ and $p_1 = p_2^*$, equation (4.1) can be expressed using the standard filter performance parameters as

$$H(s) = K \frac{s^2 + (\frac{\omega_z}{Q_z})s + \omega_z^2}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \quad (4.2)$$

where $\omega_p = 2\pi f_p$ and $\omega_z = 2\pi f_z$, f_p and f_z being the pole and zero frequencies of the filter and Q_p, Q_z are the pole and zero quality factors, respectively. The biquad serves as the building block for a variety of active filters. The dc gain and the asymptotic gain of such a filter are given by

$$20 \log_{10} |H(j0)| = 20 \log_{10} (K \frac{\omega_z^2}{\omega_p^2}) \quad (4.3)$$

$$20 \log_{10} |H(j\infty)| = 20 \log_{10} (K) \quad (4.4)$$

Any filter function can be realized from the transfer function in (4.1) by setting the coefficients a_2 , a_1 , a_0 and b_1 , b_0 to appropriate values.

4.1.1 Lowpass function

If in equation (4.1) $a_2 = a_1 = 0$, $H(s)$ is a second-order lowpass function described by

$$H_{LP}(s) = \frac{a_0}{s^2 + b_1s + b_0} = \frac{K\omega_p^2}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \quad (4.5)$$

The dc gain $|H_{LP}(j0)|$ in this case is K and for $\omega \gg \omega_p$, $H_{LP}(j\omega)$ decreases at the rate of 40dB/decade. The quality factor Q_p is defined as shown in (4.6).

$$\frac{H_{LP}(j\omega_p)}{H_{LP}(0)} = \frac{KQ_p}{K} = Q_p \quad (4.6)$$

4.1.2 Highpass function

If $a_1 = a_0 = 0$, $H(s)$ is a highpass function described by

$$H_{HP}(s) = \frac{a_2s^2}{s^2 + b_1s + b_0} = \frac{Ks^2}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \quad (4.7)$$

The high-frequency gain $|H_{HP}(j\infty)|$ is K and for low frequencies $H_{HP}(j\omega)$ increases with a slope of 40dB/decade. The Q in this case is defined as in (4.8).

$$\frac{H_{HP}(j\omega_p)}{H_{HP}(j\infty)} = \frac{KQ_p}{K} = Q_p \quad (4.8)$$

4.1.3 Bandpass function

If $a_0 = a_2 = 0$, $H(s)$ is a bandpass function described by

$$H_{BP}(s) = \frac{a_1 s}{s^2 + b_1 s + b_0} = \frac{K(\frac{\omega_p}{Q_p})s}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \quad (4.9)$$

For $\omega \ll \omega_p$, the gain $H(j\omega)$ increases at the rate of 40dB/decade and for $\omega \gg \omega_p$, the gain falls by 40dB/decade. The midband gain

$$H_{BP}(j\omega_p) = K \quad (4.10)$$

and

$$Q_p = \frac{\omega_p}{\Delta \omega} \quad (4.11)$$

where $\Delta \omega$ is the -3dB bandwidth of the filter.

Also

$$H_{BP}(j0) = 0 \quad (4.12)$$

$$H_{BP}(j\infty) = 0 \quad (4.13)$$

4.1.4 Notch function

If $a_1 = 0$, $H(s)$ is a bandreject or notch filter described by

$$H(s) = \frac{a_2 s^2 + a_0}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} = \frac{K(s^2 + \omega_z^2)}{s^2 + (\frac{\omega_p}{Q_p})s + \omega_p^2} \quad (4.14)$$

where $K = H(j\infty)$ is the high-frequency gain. This function provides infinite attenuation for $\omega = \omega_z$.

$$H_{NF}(j\omega_z) = 0 \quad (4.15)$$

Also, we have from (4.14),

$$H_{NF}(j0) = K \left(\frac{\omega_z^2}{\omega_p^2} \right) \quad (4.16)$$

$$H_{NF}(j\infty) = K \quad (4.17)$$

4.2 Fully-differential biquad realized using transconductors

Figure 4.1 Differential version of the biquad realized using transconductors

In Fig. 4.1 is shown a second-order section realized using transconductors. This is the differential version of the biquad in Fig. 1.4.

This biquad implements the transfer functions in equations (1.16) and (1.17) which are repeated in (4.18) and (4.19) for convenience.

$$V_{o1} = \frac{s^2 C^2 V_3 + sC(g_{m1}V_3 - g_{m2}V_2) + g_{m0}g_{m2}V_1}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} \quad (4.18)$$

$$V_{o2} = \frac{s^2 C^2 V_2 - sCg_{m0}V_1 + sCg_{m3}V_3}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} \quad (4.19)$$

4.2.1 Realization of the bandpass filter

The biquad in Fig. 4.1 realizes the bandpass function in (4.9) at V_{o2} by setting $V_2 = V_3 = 0$.

$$V_{o2} = - \frac{sCg_{m0}}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} V_1 \quad (4.20)$$

This is of the form shown in equation (4.9) where

$$\omega_p = \left(\frac{g_{m2}g_{m3}}{C^2} \right)^{\frac{1}{2}} \quad (4.21)$$

$$Q_p = \frac{(g_{m2}g_{m3})^{\frac{1}{2}}}{g_{m1}} \quad (4.22)$$

$$K = \frac{g_{m0}}{g_{m1}} \quad (4.23)$$

4.2.2 Realization of the lowpass filter

The biquad realizes the lowpass function in (4.5) at node V_{o1} by setting $V_2 = V_3 = 0$.

$$V_{o1} = \frac{g_{m0}g_{m2}}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} V_1 \quad (4.24)$$

This is of the form of equation (4.5) where

$$\omega_p = \left(\frac{g_{m2}g_{m3}}{C^2}\right)^{\frac{1}{2}} \quad (4.25)$$

$$Q_p = \frac{(g_{m2}g_{m3})^{\frac{1}{2}}}{g_{m1}} \quad (4.26)$$

$$K = \frac{g_{m0}}{g_{m3}} \quad (4.27)$$

4.2.3 Realization of the highpass filter

The biquad realizes the highpass function in (4.7) at node V_{o2} by setting $V_1 = V_3 = 0$.

$$V_{o2} = \frac{s^2 C^2}{s^2 C^2 + sCg_{m1} + g_{m2}g_{m3}} V_2 \quad (4.28)$$

This is of the form shown in equation (4.7) where

$$\omega_p = \left(\frac{g_{m2}g_{m3}}{C^2}\right)^{\frac{1}{2}} \quad (4.29)$$

$$Q_p = \frac{(g_{m2}g_{m3})^{\frac{1}{2}}}{g_{m1}} \quad (4.30)$$

$$K = 1 \quad (4.31)$$

4.2.4 Realization of the notch filter

The biquad realizes the notch function in equation (4.14) at node V_{o1} by setting $V_1 = V_2 = V_3$ and $g_{m1} = g_{m2} = g_m$.

$$H(s) = \frac{s^2 C^2 + g_{m0}g_m}{s^2 C^2 + sCg_m + g_m g_{m3}} V_1 \quad (4.32)$$

This is of the form of equation (4.14) where

$$\omega_z = \left(\frac{g_{m0}g_{m3}}{C^2}\right)^{\frac{1}{2}} \quad (4.33)$$

$$H_{NF}(j0) = \frac{g_{m0}}{g_{m3}} \quad (4.34)$$

4.3 Simulation results

Simulations were carried out on the biquad in Fig. 4.1 using the transconductor shown in Fig. 3.1. The effective load capacitance at nodes V_{o1} and V_{o2} (after parasitic absorption) was 1pF.

It is observed in Fig. 3.5, that the wider the range over which g_m can be tuned, the smaller is the linearity at the extremes, *i.e.*, at either too high or too low values. Since the range of frequencies over which the filter can be tuned depends on the range of values over which g_m can be varied, the filter is less linear for very high or very low pole (or zero) frequencies.

4.3.1 Lowpass filter

The pole frequency can be tuned at a constant Q by setting $g_{m0} = g_{m1} = g_{m2} = g_{m3} = g_m$ and varying g_m . From equations (4.25), (4.26) and (4.27), this yields

$$K = 1 \quad (4.35)$$

$$Q_p = 1 \quad (4.36)$$

and enables tuning of the pole frequency f_p (where $\omega_p = 2\pi f_p$) from 27MHz to 89MHz by varying g_m from 169 μ S to 563 μ S. The simulation results in Fig. 4.2 are close to predicted responses.

Figure 4.2 Pole frequency tuning of the lowpass filter for $K = 1$ and $Q_p = 1$

Q -tuning is achieved by holding $g_{m2} = g_{m3} = g_{m0} = \text{constant}$ and varying g_{m1} . This allows Q -tuning at a single pole frequency and for a constant dc gain, $K = 1$. Varying g_{m1} in $170\mu\text{S} < g_{m1} < 563\mu\text{S}$ enables tuning of Q by a factor of 3 (approximately) as shown in Fig. 4.3.

Figure 4.3 Q -tuning of the lowpass filter for dc gain, $K = 1$ and pole frequency of 44MHz

4.3.2 Bandpass filter

As in the case of the lowpass filter, the pole frequency is tuned by setting $g_{m0} = g_{m1} = g_{m2} = g_{m3} = g_m$ and varying g_m . From equations (4.21), (4.22) and (4.23), this yields

$$K = 1 \quad (4.37)$$

$$Q_p = 1 \quad (4.38)$$

and enables tuning of the pole frequency in the range 27MHz to 89MHz. This is seen in Fig. 4.4. Q -tuning (by a factor of 3) is achieved by holding $g_{m2} = g_{m3} = g_{m0} = \text{constant}$ and varying g_{m1} . This allows Q -tuning at a single pole frequency as shown in Fig. 4.5.

Figure 4.4 Pole frequency tuning of the bandpass filter

Figure 4.5 Q -tuning of the bandpass filter

4.3.3 Highpass filter

The pole frequency is tuned by setting $g_{m1} = g_{m2} = g_{m3} = g_m$ and varying g_m . From equations (4.32) and (4.33), this allows tuning of pole frequency ($27\text{MHz} \leq f_p \leq 89\text{MHz}$) at a constant Q_p as shown in Fig. 4.6. Fig. 4.7 shows Q -tuning by a factor of 3 at a constant pole frequency. This is done by setting $g_{m2} = g_{m3} = g_m$ and varying g_{m1} .

Figure 4.6 Pole frequency tuning of the highpass filter

4.3.4 Notch filter

The notch filter by definition has infinite Q_z . The zero frequency is tuned in $27\text{MHz} < f_z < 89\text{MHz}$ (where $\omega_z = 2\pi f_z$) by varying g_m , g_{m0} and g_{m3} simultaneously. From equations (4.33) and (4.34), this allows zero frequency tuning at a constant dc gain. This is shown in Fig. 4.8.

Figure 4.7 *Q*-tuning of the highpass filter

Figure 4.8 Zero frequency tuning of the notch filter

4.4 Conclusions

The simulation results show tuning of the pole frequency for the different filter functions over the expected range by tuning g_{m2} and g_{m3} . The quality factor Q was also tuned for the different filter setups. The notch function shows the attenuation at the zero frequency to be only -15dB , which is a consequence of the finite output resistance of the OTA. Equation (4.39) shows the modified output V_{o1} with the OTA output resistance taken into account.

$$V_{o1} = \frac{s^2 C^2 V_3 + sC((g_{m1} + g_1)V_3 - g_{m2}V_2) + g_{m0}g_{m2}V_1}{s^2 C^2 + sC(g_2 + g_{m1} + g_1) + g_{m2}g_{m3} + g_2(g_{m1} + g_1)} \quad (4.39)$$

where $g_1 = g_{o1} + g_{o0} + g_{o3} + g_{i1} + g_{i2}$ and $g_2 = g_{o2} + g_{i3}$, are the equivalent conductances at nodes V_{o1} and V_{o2} , respectively in Fig. 4.1 and g_{oi} , g_{ii} represent the output and input conductances of the i -th OTA.

For the notch function, setting $g_{m1} = g_{m2} = g_m$ and $V_1 = V_2 = V_3$, equation (4.39) becomes

$$V_{o1} = \frac{s^2 C^2 + sCg_1 + g_{m0}g_m}{s^2 C^2 + sC(g_2 + g_m + g_1) + g_mg_{m3} + g_2(g_m + g_1)} \quad (4.40)$$

From equations (4.2) and (4.14), this implies a finite zero quality factor Q_z (dependent on g_1) making the notch function sensitive to the output and input resistances of the OTAs. This can be alleviated by tuning the control voltage V_{CQ} of the OTA to increase its output resistance.

CHAPTER 5

LAYOUT, FABRICATION AND TEST RESULTS

5.1 Layout

The transconductor and filter were laid out using the layout editor MAGIC. SPICE-based parameter extraction from the layout of the OTA revealed a total parasitic input capacitance of approximately 0.1pF and an output capacitance of 0.2pF. Hence, the effective parasitic capacitance at node $V_{o1} = 0.1\text{pF} + 0.2\text{pF} = 0.3\text{pF}$ and the effective parasitic capacitance at node $V_{o2} = 2(0.1)\text{pF} + 3(0.2)\text{pF} = 0.8\text{pF}$.

The load capacitors were implemented with poly1–poly2 capacitors. The biquad was designed for an effective load capacitance of 1.5pF. This large value allows for process variations so that the actual variation in load capacitance will be a smaller fraction of the absolute design value. This choice implies pole frequency tuning from 18 to 59MHz as opposed to the original design of 27 to 89MHz. Simulation of the layout shows closeness of tuning range to expected values.

The layout of the transconductor is shown in Fig. 5.1. The layout of the filter with the load capacitors is shown in Fig. 5.2. Fig. 5.3 shows the filter within the standard 40-pin MOSIS pad frame. The diode-based protection circuitry at the ac signal outputs is replaced by buffers (source followers as shown in Fig. 5.4) to avoid loading the high-impedance output nodes. The protection circuitry was also removed for the ac inputs to reduce parasitic capacitance. To compensate for substrate-feedthrough and the effect of output buffers, a pair of reference lines (coming out through buffers) are run through the

chip and the response of the filter is measured with respect to the response of these lines. The chip was fabricated using MOSIS's 2 μ m CMOS analog process (n-well) provided by ORBIT.

Figure 5.1 Layout of the transconductor (OTA) in MAGIC

Figure 5.2 Layout of the filter in MAGIC

Figure 5.3 Layout of the filter with the MOSIS pad frame in MAGIC

Figure 5.4 Circuit schematic of the buffer

5.2 Circuit board design

The circuit board for testing the chip was designed on a double-sided PC board using the PCB design system – PADS-PCB. This is a software package that runs on a PC. It activates a milling machine for the actual routing of the copper board. The pinout of the chip is shown in Fig. 5.5. Fig. 5.6 shows the components used in the design of the board and the symbols used to represent them in the board schematic. The schematic of the circuit board is shown in Fig. 5.7. The copper plane serves as the ground plane. A 40-pin socket, located at the center of Fig. 5.7, holds the chip. BNC connectors are used for the power supply voltage (5V), ac inputs and ac outputs. Transformers are used for converting the single-ended ac input signals from the function generator to differential ones before being applied to the filter and also for converting the differential output signals from the filter to single-ended ones before measurement. For maximum power transfer, the transformers are loaded with matching impedances (100Ω) at their differential ends. Each of the ac inputs to the chip is biased at 2.5V through a resistive divider. Capacitors

(10nF in parallel with 10 μ F) are used with the transformers for dc isolation. Potentiometers (100k Ω) provide the bias voltages to tune the filter, set the bias currents for the OTAs and for the output buffers. Bypass capacitors (0.1 μ F), located close to the chip, eliminate high-frequency noise at each of the dc bias inputs. Jumpers are used to configure the filter to implement any of the four functions – lowpass, bandpass, highpass and notch. The layout of the circuit board in PADS-PCB is shown in Fig. 5.8.

NC		IN3A
GND		VCF3
REFO1		VCF2
REFO2		VCQ
VDD		IN3B
REFBIAS		GND
NC		REFBIAS
REFI1		OUTB2
REFI2		OUTA2
NC	40-PIN	IN2B
GND	SOCKET	OUTB0
NC		NC
NC		OUTA0
NC		NC
VDD		INB0
NC		GND
NC		INA0
VDD		VDD
IN2A		VCF0
VBIAS		VCF1

Figure 5.5 Pinout of the chip

Figure 5.6 (a) Different components used in the design of the board; (b) the symbols used to represent them in the board schematic

Figure 5.7 Schematic of the circuit board

Figure 5.8 Layout of the board in PADS-PCB

5.3 Test results

The filter was configured to perform each of the four filter functions, namely low-pass, bandpass, highpass, and notch. The following performance parameters were then characterized for each of the four functions.

1. Pole Frequency Tuning (Zero Frequency Tuning for notch filter).
2. Quality Factor Tuning.
3. DC gain (Low Frequency Gain)

In addition, the distortion of the output signal of the lowpass filter was observed with a 1MHz sine wave input signal. The power dissipation of the chip was also measured.

For all the filter types, the following voltages were fixed. Referring to Fig. 3.1 and Fig. 5.4, $V_{BIAS} = 1.2V$, $V_{CQ} = 0V$, buffer bias $V_{REF} = 1.5V$. For best results, the ac input signal levels were set at $0.2V_{p-p}$ for all measurements. The filters performed predictably for input signal levels up to $0.8V_{p-p}$. The non-linearity of the transconductor for higher input signal levels results in output signal distortion.

The transfer characteristics and output noise were observed on the Network Analyzer, HP 4195A. The power supply for the filter was obtained from the precision power supply, PS 5004. The bias voltages were set using the multimeter, 1450 (Data Precision). The distortion analysis was done with a 1MHz input signal (obtained from the function generator, FG504 – 40MHz Function Generator).

Noise was measured to be below $-70dB$ at 1MHz.

5.3.1 Lowpass filter

For the filter in Fig. 4.1, the pole frequency and the quality factor for the lowpass filter were tuned by varying the bias voltages ($V_{CF1} - g_{m1}$, $V_{CF2} - g_{m2}$, $V_{CF3} - g_{m3}$ and $V_{CF4} - g_{m4}$). The results obtained are shown in Table 5.1.

Table 5.1 Lowpass filter test results

LOWPASS FILTER	CASE I	CASE II (Pole frequency tuning)	CASE III (Q – tuning)
V_{CF0}	1.3V	0.65V	1.3V
V_{CF1}	1.3V	0.65V	0.65V
V_{CF2}	1.3V	0.65V	1.3V
V_{CF3}	1.3V	0.65V	1.3V
dc gain	-0.4dB	-2.3dB	-0.1dB
-3dB frequency	32.76MHz	8.75MHz	39.2MHz
gain at pole frequency	0.9dB	-2dB	3.6dB

CASE I shows the performance parameters of the filter when $V_{CF1} = V_{CF2} = V_{CF3} = V_{CF4} = 1.3V$, implying all the g_{ms} are equal and at their highest values. CASE II shows the results of tuning of the pole frequency while ideally retaining K and Q as unity. CASE III shows the results of Q -tuning at the highest pole frequency.

Fig. 5.9 shows the magnitude and phase responses of the lowpass filter. As expected, the output is seen to be 180° out of phase with the input. Fig. 5.10 shows the magnitude response and output noise for the lowpass filter. Noise is found to be below $-70dB$ at 1MHz. Fig. 5.11 shows pole frequency tuning of the lowpass filter. The lowpass filter pole frequency could be tuned from 8.75MHz to 32.76MHz. Fig. 5.12 shows Q -tuning at a

single pole frequency for the lowpass filter. Q -tuning could be observed by varying g_{m1} to observe the change in the gain at the pole frequency. Fig. 5.13 shows the distortion analysis of the output signal for a 1MHz sine wave input for the lowpass filter. The second and higher harmonics are found to be at least 40dB below the 1MHz signal.

Figure 5.9 Magnitude and phase responses of the lowpass filter (The upper marker lies on the phase curve and the lower marker lies on the magnitude curve).

Figure 5.10 Magnitude response of the lowpass filter and output noise. (The upper curve corresponds to the magnitude response and the lower curve corresponds to the noise).

Figure 5.11 Pole frequency tuning of the lowpass filter. V_{CF2} and V_{CF3} were varied in the range 0.65–1.3V for tuning the pole frequency in the range 8.7–32.7MHz.

Figure 5.12 Q -tuning of lowpass filter. V_{CF1} was varied in the range 0.65–1.3V.

Figure 5.13 Distortion analysis of a 1MHz output signal for the lowpass filter

5.3.2 Bandpass filter

Table 5.2 shows the test results for the bandpass filter.

Table 5.2 Bandpass filter test results

BANDPASS FILTER	CASE I	CASE II (Pole frequency tuning)	CASE III (Q – tuning)
V_{CF0}	1.3V	0.65V	1.3V
V_{CF1}	1.3V	0.65V	0.65V
V_{CF2}	1.3V	0.65V	1.3V
V_{CF3}	1.3V	0.65V	1.3V
dc gain	-28.2dB	-17.6dB	-28dB
-3dB frequency	25.25MHz	7.3MHz	25.77MHz
gain at pole frequency	-5dB	-8.3dB	-1dB

Fig. 5.14 shows the transfer characteristic of the bandpass filter for CASE I . The bandpass filter shows finite dc gain (low–frequency gain) due to the fact that the output

resistance of the transconductor is low.

Figure 5.14 Frequency response of the bandpass filter for CASE I

5.3.3 Highpass filter

Table 5.3 shows the highpass filter test results.

Table 5.3 Highpass filter test results

HIGHPASS FILTER	CASE I	CASE II (Pole frequency tuning)	CASE III (Q – tuning)
V _{CF0}	1.3V	0.65V	1.3V
V _{CF1}	1.3V	0.65V	0.65V
V _{CF2}	1.3V	0.65V	1.3V
V _{CF3}	1.3V	0.65V	1.3V
dc gain	-26.5dB	-8dB	-26.5dB
-3dB frequency	19MHz	5MHz	19MHz
Gain at pole frequency	-2.3dB	-2.14dB	-0.3dB

Fig. 5.15 shows the transfer characteristic of the highpass filter for CASE III. The highpass filter also shows finite dc gain implying that the poly1–poly2 capacitor is lossy.

Figure 5.15 Frequency response of the highpass filter for CASE I.

5.3.4 Notch filter

The notch function could not be measured, possibly due to low output resistance of the transconductor. Also, any process variation could lead to unequal capacitances at the nodes V_{o1} and V_{o2} . This becomes obvious from simulations using model parameters from the process used for fabrication of the filter. The transfer function for the notch with finite output resistance and unequal capacitances at the two output nodes can be derived as follows.

$$V_{o1} = \frac{s^2 C_1 C_2 V_3 + s(C_2(g_{m1} + g_1)V_3 - C_1 g_{m2} V_2) + g_{m0} g_{m2} V_1}{s^2 C_1 C_2 + s(C_1 g_2 + C_2(g_{m1} + g_1)) + g_{m2} g_{m3} + g_2(g_{m1} + g_1)} \quad (5.1)$$

where g_1 and g_2 are the conductances at nodes V_{o1} and V_{o2} , C_1 and C_2 are the capacitances at nodes V_{o1} and V_{o2} . Since the notch is sensitive to absolute cancellation of the middle terms in the numerator of (5.1), any finite output resistance or unequal capacitances could result in a notch with low Q .

Process variation resulting in possible asymmetries in the chip is probably another reason for not being able to measure the notch. Also, the notch function is highly sensitive to the phase of the OTA- C integrator.

5.3.5 Power dissipation measurement

The calculations that follow are used to estimate the power dissipation of each OTA. It is obtained by measuring the total current delivered by the power supply (5V) with the board powered up and with the chip inserted. The current consumed by the board alone is measured after removing the chip. The current consumed by the each output buffer is estimated from simulation results. With these data, the current consumed by the 4 OTAs alone can be calculated. The measured currents are:

Current drawn from the supply for the board alone without the chip: 0.5mA

Current drawn from the supply with chip on the board: 4.7mA

Current drawn by 6 output buffers is $6 \times (0.5\text{mA})$: 3mA

Current drawn by the filter (4 OTAs): $(4.7 - 0.5 - 3)\text{mA} = 1.2\text{mA}$

Power dissipation of filter: $5\text{V} \times (1.2\text{mA}) = 6\text{mW}$

Current drawn by each OTA: $1.2\text{mA}/4 = 0.3\text{mA}$

Power dissipation of each OTA: $5\text{V} \times (0.3\text{mA}) = 1.5\text{mW}$

5.4 Comparisons

Table 5.4 shows a comparison of the results from SPICE simulation of the layout (with the model N63J from the process used for fabrication) and tests on the chip. The range of pole frequencies over which the different filter functions could be tuned are shown in both the cases.

Table 5.4 Comparison between results from SPICE simulations and tests

Filter function	SPICE simulation	Test results
Lowpass filter	14.6–46MHz	8.7–32.7MHz
Bandpass filter	11.2–37MHz	7.3–25.5MHz
Highpass filter	8.8–30MHz	5–19MHz

Figures 5.16, 5.17 and 5.18 show the comparisons between the lowpass, bandpass and highpass filter transfer functions from simulations and tests for $V_{CF0,1,2,3} = 1.3V$.

Figure 5.16 Comparison between lowpass filter transfer functions.

Figure 5.17 Comparison between the bandpass filter transfer functions.

Figure 5.18 Comparison between highpass filter transfer functions.

Table 5.4 shows the range of pole frequencies obtained from tests to be lower than those obtained from simulation results with the same model. The high DC gain of the bandpass filter implies that the OTA has a low output resistance. This calls for a closer examination of the filter design. Since the pole frequency is determined by the g_m of the OTAs, a possible approach involves fabricating the OTA in isolation and characterizing its behavior. This should provide information regarding the robustness of the design and its sensitivity to process variations. Another reason for the difference between the simulation and test results could be the accuracy of the models (LEVEL 2) used.

Also, the DC gain in the highpass filter transfer characteristic implies a lossy poly1–poly2 capacitor. This could be either due to faults in fabrication or any damage that occurred in the course of handling the chip.

CHAPTER 6

CONCLUSION

6.1 Conclusion

The objective of the work reported in this thesis was to build and evaluate the performance of a general second-order filter tunable from 18 to 59MHz. Measurements show the realization of the lowpass, bandpass, and highpass functions. Both the pole frequency and Q could be tuned for all three functions. The pole frequencies could be tuned approximately in the range 8–32MHz. Simulations show tuning over a higher range of frequencies. The difference is possibly due to process variations resulting in an OTA with different performance characteristics. The accuracy of the models (LEVEL 2) used in the simulations could be another reason for the differences in results. The notch function could not be measured since it is extremely sensitive to any process variations which could result in varying poly1–poly2 capacitances or an OTA with low output resistance.

6.2 Further work

This project is a classic example of filter design using the g_m – C technique. The results have proved that the design of the biquad which can realize all filter functions by setting element values and selecting the appropriate input and output terminals is indeed feasible in a system or application that requires a programmable filter function. Since the test results are different from the simulation results, the design of the OTA should be studied more closely. It is likely, that this particular topology is highly sensitive to process variations resulting in a shift in the tuning range. Further efforts are needed to investigate

ways to make the design robust against process variations. Also, higher-level models should be used in simulations to make the simulation results more accurate. Design of higher-order filters using the biquad as the building block should also be investigated.

REFERENCES

- [1] R. Schaumann, M. S. Ghausi and K. R. Laker, *Design of Analog Filters: Passive, Active RC and Switched Capacitor*, Prentice–Hall, 1990
- [2] Y. P. Tsividis and J. O. Voorman, *Integrated Continuous–Time Filters: Principles, Design and Applications*, pp. 1–10, New York: IEEE Press, 1993
- [3] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE*, McGraw–Hill, Inc., 1993
- [4] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective*, Addison–Wesley Publishing Company, 1994
- [5] S. Szczepanski, J. Jakusz and R. Schaumann, "A linear fully–balanced CMOS OTA for VHF filtering applications", ISCAS, Seattle, Washington, May 1995
- [6] S. Szczepanski, A. Wyszynski and R. Schaumann, "Highly Linear Voltage–Controlled CMOS Transconductors", IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications, vol.40, no.4, pp. 258–262, April 1993
- [7] Paul W. Tuinenga, *SPICE A Guide to Circuit Simulation and Analysis Using PSpice*, Prentice Hall, 1988

APPENDIX A

A.1 Spice model parameters used for design

* N52W SPICE LEVEL 2 PARAMETERS

```
.MODEL CMOSN NMOS LEVEL=2 PHI=0.700000 TOX=4.2400E-08
XJ=0.200000U TPG=1
+ VTO=0.8184 DELTA=4.0370E+00 LD=3.4300E-07 KP=4.5103E-05
+ UO=553.8 UEXP=1.2310E-01 UCRIT=9.6810E+04 RSH=1.4910E-01
+ GAMMA=0.5799 NSUB=6.7190E+15 NFS=1.0890E+11 VMAX=5.9760E+04
+ LAMBDA=3.3160E-02 LAMBDA=3.3160E-02 CGDO=4.1902E-10
+ CGSO=4.1902E-10 CGBO=3.4911E-10 CJ=1.2010E-04 MJ=0.6285
+ CJSW=4.7113E-10 MJSW=0.3275 PB=0.800000
```

* $W_{eff} = W_{drawn} - \Delta W$

* + GAMMA=0.5799 NSUB=6.7190E+15 NFS=1.0890E+11 VMAX=5.9760E+04

* The suggested ΔW is 1.5426E-08

```
.MODEL CMOSN PMOS LEVEL=2 PHI=0.700000 TOX=4.2400E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.9477 DELTA=4.6250E+00 LD=3.6240E-07 KP=1.6761E-05
+ UO=205.8 UEXP=2.8980E-01 UCRIT=8.3070E+04 RSH=1.1050E-01
+ GAMMA=0.6899 NSUB=9.5090E+15 NFS=1.1000E+11 VMAX=9.9990E+05
+ LAMBDA=4.6050E-02 LAMBDA=4.6050E-02 CGDO=4.4272E-10
+ CGSO=4.4272E-10 CGBO=3.9342E-10 CJ=3.0933E-04 MJ=0.6176
+ CJSW=2.8778E-10 MJSW=0.4045 PB=0.800000
```

* $W_{eff} = W_{drawn} - \Delta W$

* The suggested ΔW is -3.0100E-07

A.2 Spice model parameters from the process used for fabrication

```
* N63J SPICE LEVEL2 PARAMETERS.MODEL CMOSN NMOS LEVEL=2
PHI=0.700000 TOX=3.9500E-08 XJ=0.200000U TPG=1
+ VTO=0.8577 DELTA=2.7790E+00 LD=1.3330E-07 KP=5.9272E-05
+ UO=678.0 UEXP=8.7500E-02 UCRIT=6.7780E+03 RSH=1.2930E+01
+ GAMMA=0.5361 NSUB=6.6170E+15 NFS=9.3830E+10 VMAX=4.8300E+04
+ LAMBDA=3.0840E-02 CGDO=1.7480E-10 CGSO=1.7480E-10
+ CGBO=3.4582E-10 CJ=1.34E-04 MJ=0.535 CJSW=6.11E-10
+ MJSW=0.200 PB=0.40
```

* $W_{eff} = W_{drawn} - \Delta W$

* The suggested ΔW is 2.0000E-09

.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=3.9500E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.8721 DELTA=3.0970E+00 LD=1.0210E-07 KP=1.6129E-05
+ UO=184.5 UEXP=4.3620E-01 UCRIT=2.0720E+05 RSH=1.0190E-01
+ GAMMA=0.5972 NSUB=8.2120E+15 NFS=6.0720E+11 VMAX=9.9990E+05
+ LAMBDA=3.9420E-02 CGDO=1.3389E-10 CGSO=1.3389E-10
+ CGBO=4.0174E-10 CJ=3.34E-04 MJ=0.585 CJSW=3.97E-10
+ MJSW=0.127 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.4180E-07.MODEL CPOLY1-2 C CJ=453e-6