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High-performance Input/Output Circuit for CMOS Integrated Circuit Interface

Chee How Lim
Portland State University

THESIS APPROVAL

The abstract and thesis of Chee How Lim for the Master of Science in Electrical and Computer Engineering were presented July 1, 1997, and accepted by the thesis committee and the department.

COMMITTEE APPROVALS: [redacted]

W. Robert Daasch, Chair

[redacted]

Douglas V. Hall

[redacted]

Richard G. Hamlet

Representative of the Office of Graduate Studies

DEPARTMENT APPROVAL: [redacted]

Rolf Schaumann, Chair

Department of Electrical and Computer Engineering

****

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ABSTRACT

An abstract of the thesis of Chee How Lim for the Master of Science in Electrical and Computer Engineering presented July 1, 1997.

Title: High-Performance Input/Output Circuit for CMOS Integrated Circuit Interface.

In recent years, strong demand for high-performance electronic products has fueled the need for high-speed and high-integration VLSI circuits. This demand is expected to continue growing in the future, which will lead to development of IC's that are much more compact and operate at higher frequencies. As a result, preserving signal integrity for proper IC communications becomes an increasingly difficult challenge.

In this thesis, an understanding of IC noise in relation to IC packaging is sought. An IC package is modeled with sophisticated 3-D simulators to extract its corresponding parasitics. These parasitics, expressed in terms of resistance, inductance, and capacitance (RLC), are lumped into their RLC circuit equivalent,

and are incorporated into I/O circuits to form a simulatable IC noise model. In addition to SPICE analyses, the behavior of noise is modeled mathematically, and the results are compared to measurement.

With sufficient understanding of IC noise behavior, two circuits are proposed to effectively control IC noise. The first circuit is a modified I/O circuit that monitors the local output switching condition, and intelligently adjusts its slew rate such that the I/O can switch as fast as possible without jeopardizing noise performance. The second circuit is a PVT-compensation control circuit, which senses process (P), voltage (V), and temperature (T) variations, and compensates the I/O circuit's current drive accordingly. This feature makes the I/O circuits more robust under a range of environmental stress.

From analyses and simulations, the proposed I/O and PVT-compensation control circuits show great potential for IC noise control. They control IC noise to less than 10% variation between single and multiple simultaneous output switchings as compared to a conventional I/O circuit with 56% variation. The proposed circuits also show potential for reduced power dissipation in the I/O circuits by a factor of 3. Finally, applications of these circuits are discussed with respect to test and program time reduction as well as commonly used asynchronous circuit interface.

HIGH-PERFORMANCE INPUT/OUTPUT CIRCUIT FOR CMOS INTEGRATED CIRCUIT INTERFACE

by

CHEE HOW LIM

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On a personal note, I would like to express my utmost gratitude to my family for their unconditional support, and for providing me the opportunity to pursue my education in the United States. Most of all, I would like to dedicate this thesis to Baongoc D. Ho for her love and encouragement throughout this important part of my life.

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CHAPTER 1

INTRODUCTION

In the last decade, the soaring performance of VLSI (Very Large Scale Integration) circuits has significantly improved the capability of computation and communication products. This growth is fueled by strong market demand for high-performance electronic products and supported by advancements in process technology and circuit techniques. Essentially, the trend of VLSI circuits (refer to [1] and [2]) is towards higher level of integration and higher operating frequencies, as suggested by Moore's Law since 1965.

However, the challenges that lie ahead are increasingly difficult to resolve. One of the major concerns in high-performance VLSI circuits is inter-chip signal integrity (refer to [3] - [7]). This issue limits the capability of VLSI circuits to communicate with each other. In particular, the interface of high-density IC's (integrated circuit) are susceptible to IC package parasitics. These parasitics translate into noise that degrades signal quality on and off the chip. Once the signals are corrupted, catastrophic system failures may occur. Furthermore, with predicted IC trends of higher density and speed, the challenge of signal integrity will only be

greater in the years to come. Therefore, the primary objectives of this thesis are to study the issue of signal integrity, and to provide a viable circuit solution to control IC noise.

1.1 Motivation

In contemporary digital circuits, CMOS (Complementary Metal Oxide Semiconductor) technology is preferred because of its low power operation and its ability to provide full voltage swing. However, going along with the idea of a "system-on-a-chip," the CMOS IC's are moving towards higher and higher densities. In addition to the higher level of integration, systems are pushed to operate at faster speeds. Consequently, higher density and speed lead to greater number of I/O (input/output) pins per IC and faster switching frequency. These two conditions contribute to IC noise.

From an IC interface's perspective, a large portion of IC noise is the result of package parasitics that change signal quality at high frequency. To illustrate the issue of IC noise, a measurement is taken for a circuit with 16 simultaneous output switchings. This result is shown in Figure 1.1, and it can be observed that the ground reference has been elevated with respect to the output signal. The ground reference is, therefore, corrupted with noise and may propagate false logic to successive logic gates. With a 64-bit data bus as in PCI (Peripheral Component

Interconnect) systems, 16- or 32-bit switching is not uncommon (refer to [8]). This type of switching behavior can be observed during large data transfers or during initialization routines. As a result, a great challenge is imposed on the IC designers.

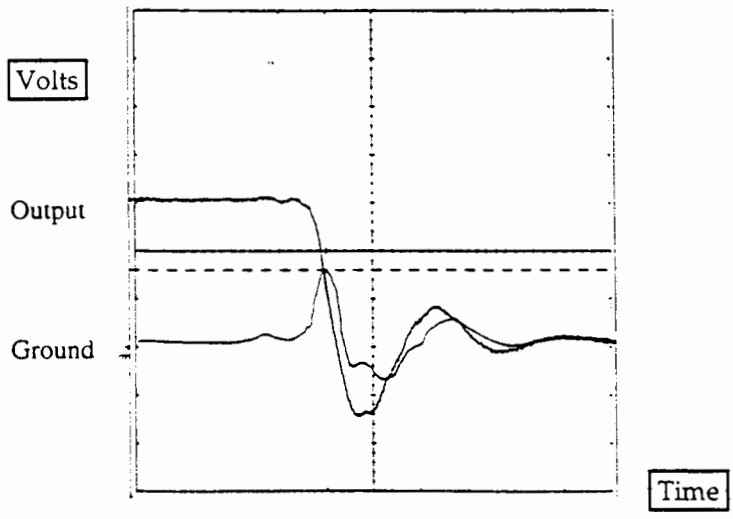

Figure 1.1: IC Noise from Simultaneous Output Switchings

To achieve the objectives of understanding inter-chip signal integrity problems and providing a circuit solution, the physical IC package is modeled using 3-D simulators, and the results are used to model the IC noise in a lumped circuit form. Once the models are simulated and analyzed, their outcomes are compared to measured values for verification. After the models are proven to work appropriately, two circuits are developed to dynamically control IC noise. Lastly, these circuits are simulated with the IC noise models to illustrate their effectiveness in controlling IC noise.

1.2 Thesis Outline

Chapter 2 provides some background information regarding two major classes of IC noise: crosstalk and ground bounce. Simplified expressions and diagrams are included to describe the characteristics of these noises. In addition, it discusses some contemporary I/O circuits that feature noise control. These circuits will be used as a comparison in Chapter 5.

Chapter 3 describes the work involved in modeling the IC package. It discusses the methodologies and simulators used to generate resistance, inductance, and capacitance (RLC) values that correspond to the physical IC package. The information gained from this effort is used in Chapter 4 to perform IC noise modeling. In addition, some discussions with respect to high frequency effects are included.

Chapter 4 discusses the work involved in modeling the IC noise. It describes how the information in Chapter 3 is used to model IC noise in SPICE, and analyzes the lumped IC noise model mathematically. The results of the IC noise models are compared to measured values. Finally, a few experiments are designed to investigate the behavior of IC noise across process, voltage, and temperature variations as well as slew rate. The outcome of these experiments guide the development of the proposed I/O circuits.

Chapter 5 introduces two circuits that feature noise control and power reduction. The first circuit provides slew rate control as a function of local switching conditions, and the second circuit senses and compensates process, voltage, and temperature variations. These circuits are the results of the study from Chapters 3 and 4. This chapter also analyzes the simulation results of these circuits, and finally, some useful applications for these circuits are discussed.

Chapter 6 concludes the thesis, and it provides a summary of key points achieved in this thesis. Finally, it provides some guidelines of possible future work in this area of study.

CHAPTER 2

BACKGROUND

As introduced in Chapter 1, the increasing demand for high-speed and high-integration IC's has escalated the concern for signal integrity. To increase speed, output buffers are forced to sink or source a large amount of current. This current reacts with the IC package parasitics to induce IC noise. Coupled with multiple simultaneous switching pins, such as in address and data buses, the noise performance can, therefore, be severely jeopardized. Sections 2.1 and 2.2 introduce the concepts of crosstalk and ground bounce, and Section 2.3 discusses some contemporary I/O circuits that feature noise control.

2.1 Crosstalk

From a simplified diagram in Figure 2.1, there are two types of couplings that cause crosstalk: inductive and capacitive. *Crosstalk* is a phenomena in which a signal traveling through a conductor induces an undesired signal in its neighboring conductor.

Inductive coupling is a result of the mutual inductance between the conductors. When there is a change in current in Conductor 1, it induces magnetic field in the direction based on the right-hand rule. This field may extend to Conductor 2 in the same direction, and therefore, induce a current in Conductor 2, parallel to Conductor 1. Since the conductor has finite inductance, the field opposes a change in current and a voltage potential in Conductor 2 is generated (refer to (2.1) and (2.2)). This voltage is the induced crosstalk.

$$V_1 = L_{11} \cdot \frac{dI_1}{dt} + L_M \cdot \frac{dI_2}{dt} \tag{2.1}$$

$$V_2 = L_{22} \cdot \frac{dI_2}{dt} + L_M \cdot \frac{dI_1}{dt} \tag{2.2}$$

where,

L_{11} is the self-inductance of Conductor 1, and

L_{22} is the self-inductance of Conductor 2.

Refer to Figure 2.1 for the remaining terms used in (2.1) and (2.2).

Furthermore, the conductors are separated by some dielectric material, namely air, plastic, etc., and this situation conveniently fits the definition of a capacitor. As such, when a voltage change occurs, a current is induced to reduce the voltage difference (refer to (2.3) and (2.4)). This result is known as *capacitive coupling*.

$$I_1 = C_{11} \cdot \frac{dV_1}{dt} + C_M \cdot \frac{d(V_1 - V_2)}{dt} \tag{2.3}$$

$$I_2 = C_{22} \cdot \frac{dV_2}{dt} + C_M \cdot \frac{d(V_2 - V_1)}{dt} \qquad (2.4)$$

where,

C_{11} is the capacitive coupling of Conductor 1 to ground, and

C_{22} is the capacitive coupling of Conductor 2 to ground.

Figure 2.1 shows the remaining terms used in (2.3) and (2.4).

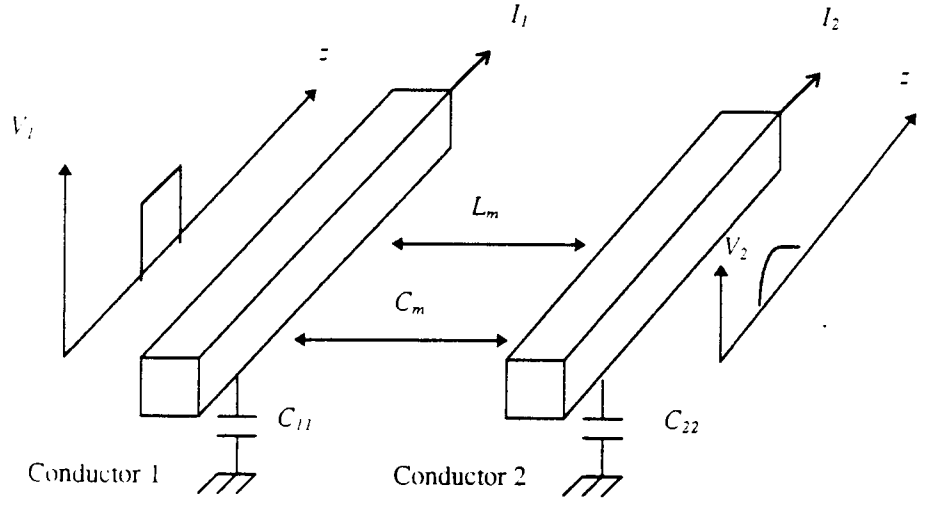

Figure 2.1: Crosstalk or Interconnect Coupling

2.2 Ground Bounce

In addition to crosstalk, another effect of the conductor's parasitic RLC characteristics is *ground bounce*. When an output is driven from high (5V) to low (0V), the output load is switched by a discharging current through the internal ground reference, which is the node between the NMOS transistor and the ground pin (represented by R_g, L_g, and C_g) in Figure 2.2. This sudden change in current

causes the inductance of the ground pin to react, and therefore, a voltage potential is induced. Consequently, this induced voltage elevates the internal ground reference. Equations (2.4) and (2.5) show the relationships of the voltage induced on the internal ground reference.

$$V_b = L_g \cdot \frac{dI}{dt} \tag{2.4}$$

where,

$$I = -C_{load} \cdot \frac{dV}{dt} \tag{2.5}$$

Because I is a small current, ground bounce is usually not an issue with single output switching. However, multiple simultaneous switching outputs can increase the amount of current substantially. Consequently, the internal ground reference can be elevated high enough to cause functional failures within the IC. Hence, it is vital to preserve ground signal quality by managing the output switching behavior.

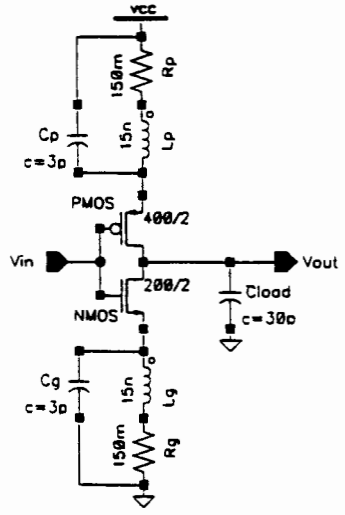

Figure 2.2: Simplified Ground Bounce Circuit

2.3 High-Speed I/O Circuits

In order to preserve signal quality, I/O circuits have been designed to reduce the effects of IC package parasitics that induce IC noise (refer to [3] - [7]). For example, differential techniques provide a noise cancellation advantage, but their implementations are expensive in terms of pin counts. Hence, only single-ended signaling techniques will be presented in this section.

In the first I/O circuit (presented in [3]), a current controlling buffer is proposed (see Figure 2.3). It uses pre-drive circuits to control the slew rate of the output buffer by changing the turn-on time. In effect, when all the pre-drive transistors are turned on (by connecting the gates of all the N- and P-devices in the pre-drive circuit to INPUT), the slew rate would be highest, but when the pre-drive transistors are turned-off, the slew rate would be decreased accordingly. From (2.4), when the slew rate is decreased, the induced noise will also be decreased. Nonetheless, this approach has a major disadvantage. The slew rate of this I/O circuit is fixed during design cycle with *Metal1* mask. This metal layer permanently connects the transistors for a certain target slew rate. However, as the local environmental conditions of the IC change, the I/O circuit's slew rate will also change. This change in slew rate may cause unreliable noise performance.

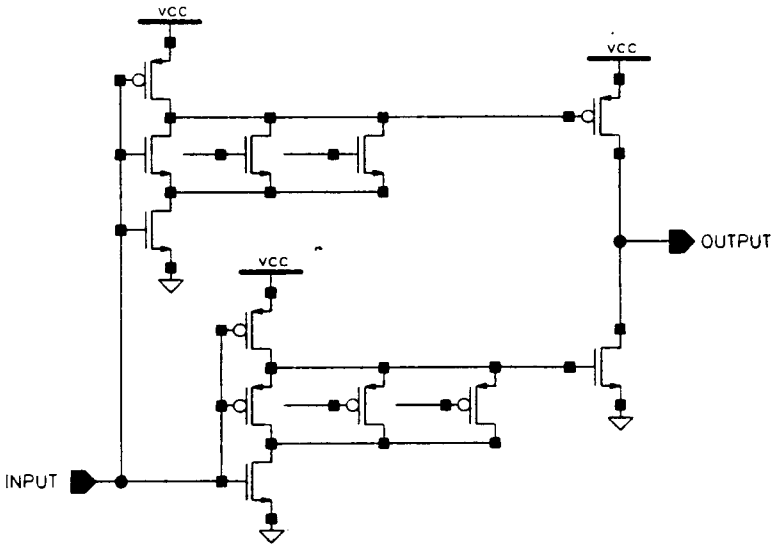

Figure 2.3: Current Controlling Output Buffer

The second I/O circuit (presented in [4]) implements a sophisticated circuit that reduces noise by combining output presetting techniques together with adequate driving of the output pull-up and pull-down transistors. This I/O circuit technique is used mainly for memory IC's. The main idea of this circuit is to preset the output to a certain value (between power and ground) when a read operation is detected, and once the data is available, the output is switched from the preset value to the final value (power or ground). In theory, this technique reduces the peak switching current by presetting the output voltage. Reducing the peak current decreases dI in (2.4), which leads to lower induced noise. However, this I/O circuit

requires substantial increase in control circuitry, and its performance relies heavily on the layout and fabrication.

In the third circuit (presented in [5]), an output buffer with oscillation damping capability is introduced. This technique suggests that ground bounce can be suppressed by controlling the I/O buffer's on-resistance. Adjusting the on-resistance can effectively force the parasitic RLC circuit in an IC package into a critically-damped or over-damped condition. This adjustment reduces ground reference oscillations, and therefore, decreases noise. To adjust the on-resistance, a process, voltage, and temperature (PVT) compensation reference circuit is utilized. This reference circuit detects PVT variations and controls a set of parallel-connected transistors that are located between power and P-device of output buffer, and between ground and N-device of output buffer. When more parallel transistors are turned on, the effective resistance of the output circuit is decreased. Nevertheless, this technique requires separate power/ground buses for the I/O circuits and internal circuits. In addition, the PVT-compensation circuit utilized in this technique senses variation for N-devices only (variations in N-devices and P-devices are not the same) and requires external resistors.

The fourth circuit (presented in [6]) implements an output buffer with an on-chip compensation circuit similar to the third circuit example. In this technique, the slew rate of the output drivers is controlled such that it is constant across process,

voltage, and temperature variations. To achieve constant slew rate, the effective channel width of the output buffer is digitally controlled by an internal PVT-compensation circuit. In effect, the output current is adjusted based on the PVT codes (labeled as *p_codes* and *n_codes* in Figure 2.4) that represent certain IC conditions. The main disadvantage of this technique is that the slew rate is independent of the number of output switchings, which is one of the major contributions to IC noise.

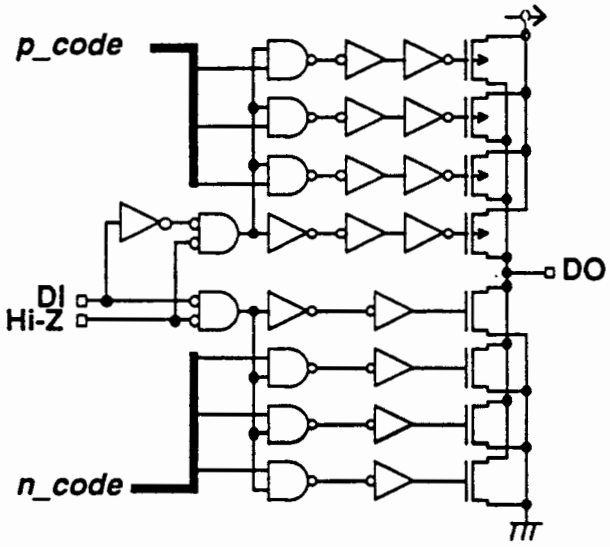

Figure 2.4: Output Buffer with Constant Current

In a fifth circuit (presented in [7]), an output buffer with ringing-cancellation is proposed. This circuit transmits a superimposed two-step pulse that almost completely cancels the ringing in the receiver end. When a step pulse is transmitted from an I/O circuit, multiple reflections occur on the transmission line. These reflections cause an oscillatory waveform at the receiving end with period *T*.

However, when another step pulse is transmitted with a delay of $T/2$ from the first pulse, its corresponding overshoot will cancel the undershoot of the first step pulse in the receiving end, and vice versa. Therefore, the output signals can be detected by the receiver with better quality. This technique, however, requires precise control of the pulse timing, and consumes twice as much power because of dual transmission. In addition, it does not account for multiple switching conditions, which may corrupt the transmitted signals. Hence, it does not fully address the problem of signal integrity.

From the information discussed in this chapter, it is clear that the noise issue is real, and has attracted a lot of industry attention. The concern about signal noise will only grow in the future because of increasing pin counts and operating frequencies, and new circuit solutions are sought. Hence, this thesis will present a new circuit technique that provides high-speed signaling while preserving signal quality.

CHAPTER 3

MODELING OF IC PACKAGE

In an IC package, the bond-wires and lead-frames serve as the interconnect between the VLSI die and the external world (i.e. printed circuit board traces or other components). Since these interconnects are made of metals, they have electrical properties that contribute to signal noise, such as resistance, capacitance, and inductance. Furthermore, as system integration or complexity increases, the number of I/O pins also increases. Along with higher operating frequencies, the effects of IC package parasitics become more pronounced. Hence, it is necessary to model these electrical properties carefully in order for a circuit designer to incorporate these parasitics when designing high-speed interface circuits. Section 3.1 describes the simulation of the IC package parasitics, and Section 3.2 discusses high-frequency effects on those simulated values.

3.1 IC Package Simulation

For most cases, the primary goal of IC package modeling is to simulate the parasitics, and generate their RLC circuit equivalent. By incorporating non-ideal

circuit behaviors into the design flow, robust circuits can be designed. In essence, the task is to convert physical properties into computable form. Figure 3.1 (not drawn to scale) shows a sketch of a typical cross-section for an IC.

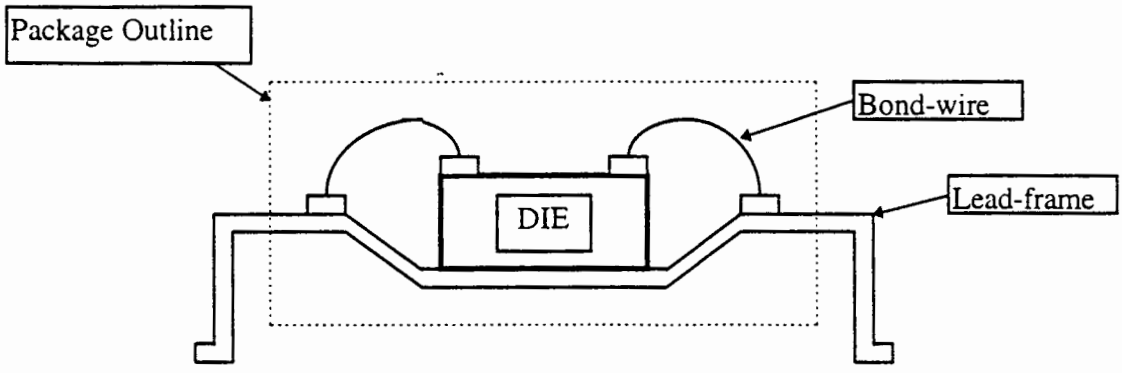

Figure 3.1: Cross-section of an IC Package

To model the IC package, Henry™ (refer to [9]), a 3-D simulator from OEA International, Inc., is used to calculate self-inductance and mutual inductance of bond-wires and lead-frames. In addition, it calculates the resistance for a given structure. The main inputs to Henry™ are the conductor's volume and resistivity.

For lead-frame modeling, these input requirements are achieved by specifying the X, Y, and Z (XYZ) coordinates representing an end of one or more centerlines of the structure, width, thickness, and its corresponding resistivity in Ω-cm. As output, Henry™ generates a SPICE circuit equivalent (resistors and inductors) of the 3-D structure.

For bond-wire modeling, information such as bonding technique (ball-wedge or wedge-wedge) coordinates for pad on die and tip of lead-frame, bond-wire diameter, package plane to bond-wire angle, and height of the bond-wire, would have to be provided. Similarly, the output is a SPICE circuit equivalent of the 3-D structure.

Figure 3.2 shows various inductors for a PQFP (Plastic Quad Flat Pack) 160-pin IC package. On the X-axis, pin at location 0 indicates the center pin of one of the sides of the IC package. Since the bond-wires and lead-frames of the center pins are the shortest, they exhibit less self-inductance as compared to the pins closer to the package corners; this is illustrated in Figure 3.2 as **Self_L**. In addition, the contribution of mutual inductance of neighboring pins to the center pin is shown as **Mutual_L** in Figure 3.2. It can be observed that the mutual inductance between the pins decays approximately by the reciprocal of distance between the pins. This result is expected because the magnetic flux generated by current through the pin decays in the same way.

Figure 3.3 shows the resistances of the pins for a PQFP 160-pin IC package. Similarly, on the X-axis, pin at location 0 indicates the center pin of one of the sides of the IC package. Resistance of the center pin (pin at location 0) is highest because it has the smallest cross-section area.

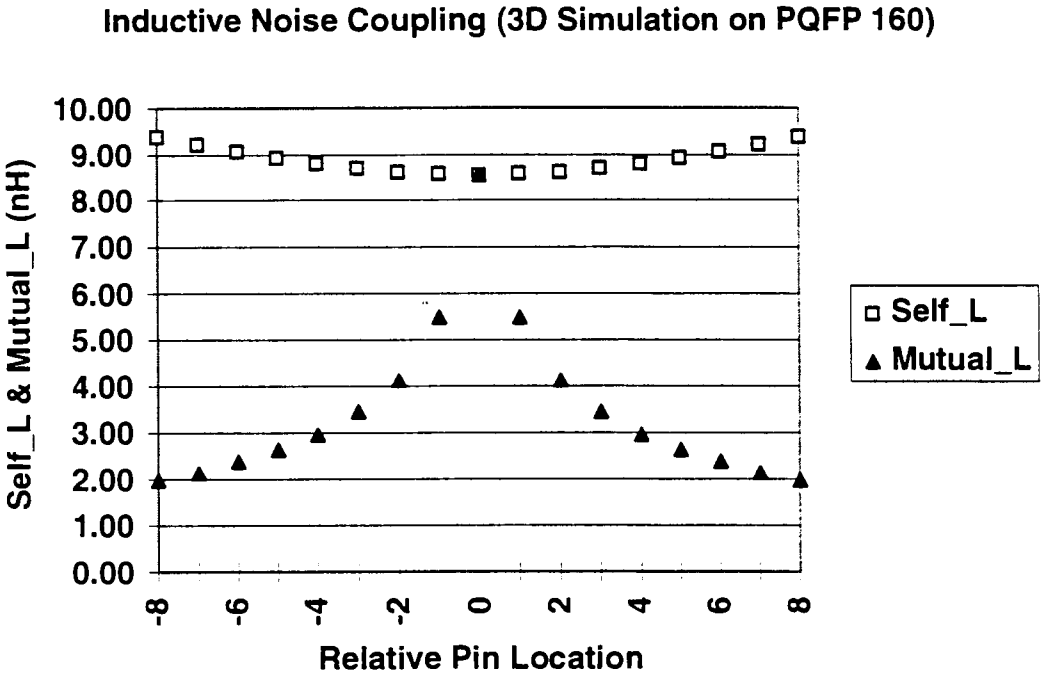

Figure 3.2: Pin Self and Mutual Inductance versus Pin Location (PQFP 160)

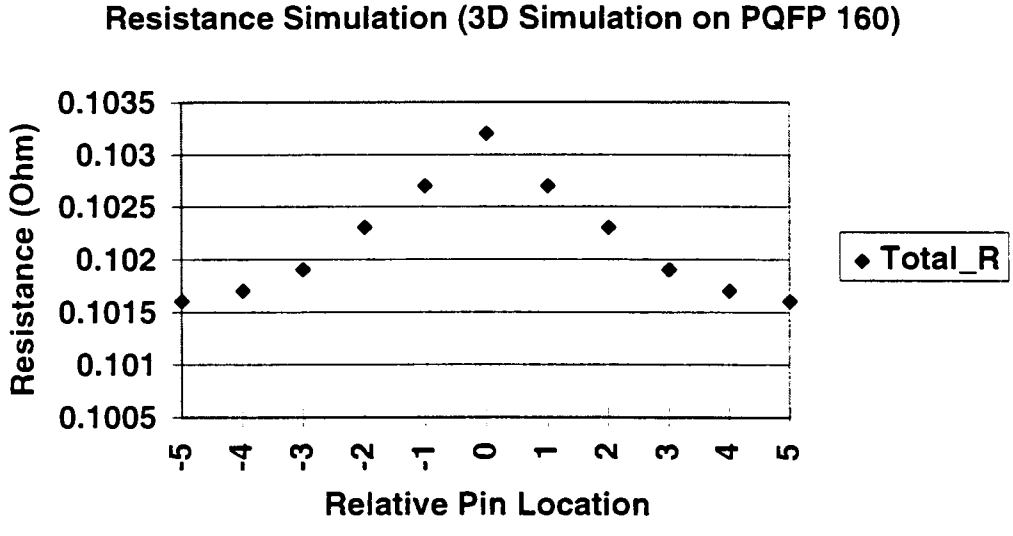

Figure 3.3: Pin Resistance versus Pin Location (PQFP 160)

To complete the package model, the capacitive properties of the IC package have to be accounted for. This can be achieved by using a 3-D capacitance simulator called Metal™ (refer to [10]). Metal™ is used to calculate capacitances of bond-wires and lead-frames with respect to ground plane and neighboring conductors. The input file to Metal™ contains information, such as material properties (of printed circuit board, IC package, and conductors), spatial information (i.e. XYZ coordinates), and relative position of ground plane(s). In return, the simulator generates SPICE circuit equivalent capacitors of the 3-D structure.

Figure 3.4 shows the pin capacitances for a PQFP 160-pin IC package. It can be observed that the self-capacitance (indicated by **Self_C**) of the center pin is slightly lower than the pins closer to the package corner. This result is due to the fact that the center pin has lower conductive surface than the corner pins. In this simulation, it is important to observe that the overall capacitance of the center pin is contributed mostly by two of its nearest pin neighbors (refer to **Mutual_C**). This result is used to establish the I/O circuit in Chapter 5.

From the above results, the equivalent circuits composed from resistances (R), inductances (L), and capacitances (C) of the IC package are obtained. These circuits, as shown in Figure 4.1, can be combined by circuit designers with their I/O circuits to simulate package noise performance.

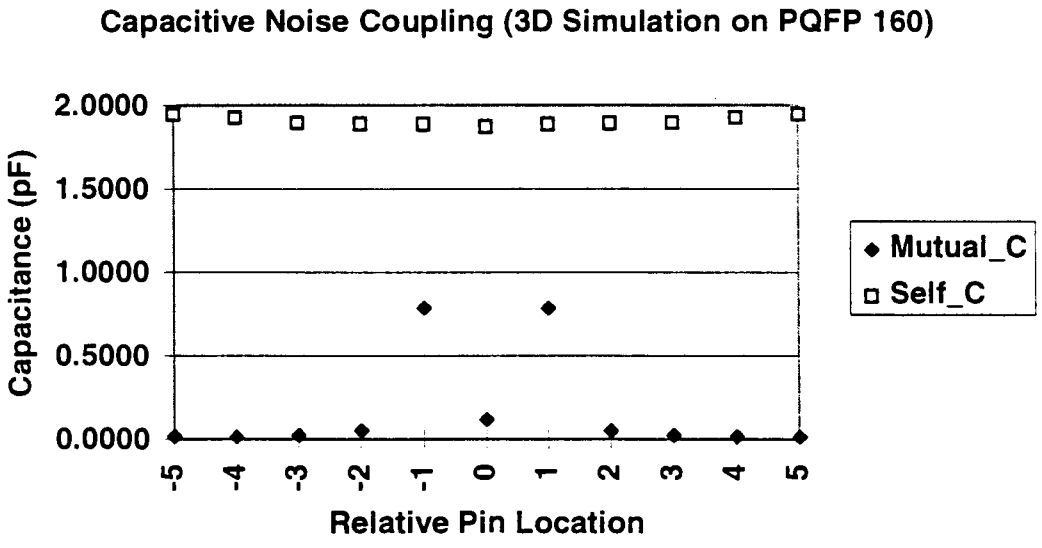

Figure 3.4: Pin Capacitance versus Pin Location (PQFP 160)

3.2 High Frequency Effects on IC Package Simulation

In Section 3.1, the package simulators (Henry™ and Metal™) calculate the RLC (resistance, inductance, and capacitance) values under low frequency condition. While this calculation is valid (refer to [9] and [10]) for a large frequency range (from DC to GHz), it's results will vary at very high frequencies.

When frequency is increased, the effective cross-section area of a conductor for current passage is reduced [11] (refer to Figure 3.5). As a result, current crowding at the conductor's surface increases the resistance. This phenomena is known as the *skin-effect*. Figure 3.6 illustrates the increase in resistance as a function of frequency (ω).

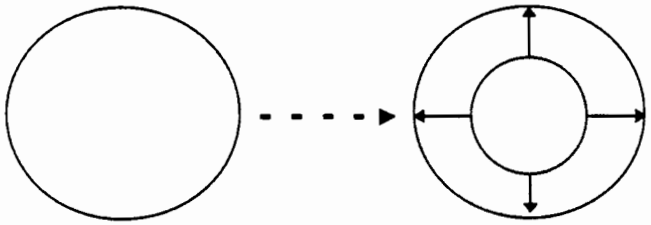

Figure 3.5: Current Density within Cross-section of a Conductor

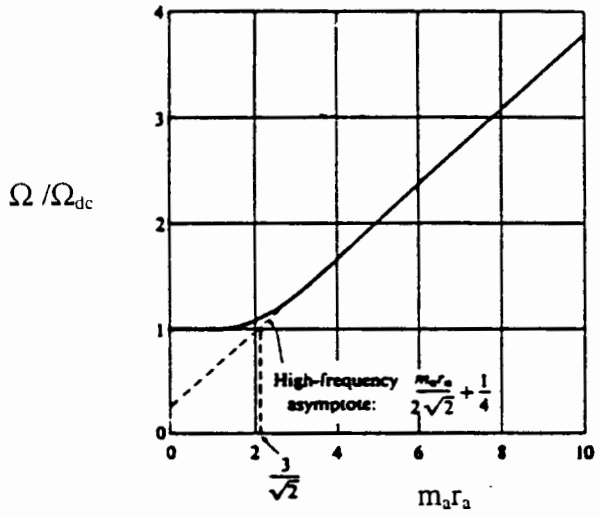

Figure 3.6: Effective Resistance versus Frequency

The symbols used in Figure 3.6 are described as follows:

Ω is the effective resistance at high frequency,

Ω_{dc} is the resistance at DC,

r_a is the conductor's radius, and

$$m_a = \sqrt{\mu \cdot \sigma \cdot \omega} \qquad (3.1)$$

where,

μ is the conductor's permeability,

σ is the conductor's conductivity, and

ω is the signal's frequency.

From [12], a single time-constant circuit with 1 ns rise time (t_{rise}) has a fundamental frequency f_0 of approximately 350 MHz, as shown below:

$$f_0 \approx \frac{0.35}{t_{rise}} \tag{3.2}$$

Assuming the conductor or pin is made of copper, and is in free space, the estimated resistance of the center pin of the PQFP 160-pin IC package increases from 0.1046 to 1.0334 Ω (about 10 times higher than in DC). Nevertheless, since the effective resistance remains small relative to the characteristic impedance Z_0 (50 to 110 Ω) of the transmission line at the printed circuit board trace, this effect can be neglected.

On the other hand, as frequency increases, the effective inductance decreases. This observation is due to the fact that the magnetic flux contributed by the current within the conductor is reduced (refer to [13]). However, the amount of reduction in inductance is calculated to be less than 9.5% (up to the GHz range) of the DC value. Similarly, the capacitances between conductors show negligible dependence on frequency (refer to [10]).

Hence, to obtain a worst-case IC package model, the low-frequency resistances, inductances, and capacitances calculated by Henry™ and Metal™ can

be utilized with reasonable accuracy. At this point, the translation of physical properties that correspond to the IC package into a computable form has been completed. These results will be used in the next chapter to model the IC noise behavior.

CHAPTER 4

MODELING OF IC NOISE

In Chapter 3, the RLC values of the interconnects (bond-wires and lead-frames) are calculated using sophisticated 3-D simulators. These values are used to form a lumped RLC circuit to model the IC package pin parasitics. From a circuit designer's point of view, the two main IC noises of concern are crosstalk and ground bounce. Once these IC noises can be characterized, the circuit designer can use the information to effectively design noise-tolerant interface circuits. Section 4.1 describes the analyses of IC noise through SPICE simulations, and Section 4.2 approaches the IC noise analyses from a mathematical standpoint. Finally, Section 4.3 provides measurement data that verify the IC noise models.

4.1 Circuit Analyses of IC Noise Model

Using the results from Chapter 3, the lumped RLC circuit in Figure 4.1 can be created (refer to [14]). The output buffer (shown as a simple inverter) is connected in series with a lumped circuit equivalent of the IC package pin. From

this circuit model, HSPICE simulations can be performed to understand the behavior of crosstalk and ground bounce.

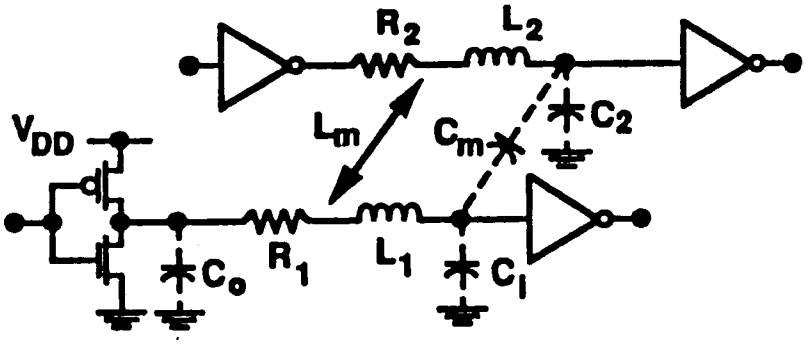

Figure 4.1: Lumped RLC Circuit Model

In the first experiment, the primary objective is to characterize the behavior of ground bounce versus the number of simultaneous switching I/O's. A set of circuits with configurations similar to Figure 4.1 is simulated with a 2-micron technology from MOSIS. In addition, the internal power and ground references are connected to an external power supply via RLC circuits that model the corresponding IC pins. The results are shown in Figure 4.2.

Referring to Figure 4.2, the ground bounce (V_b) increases with number of switching I/O's. However, it is shown the relationship is non-linear with decreasing slope, and the cause of this non-linearity is examined in the next section.

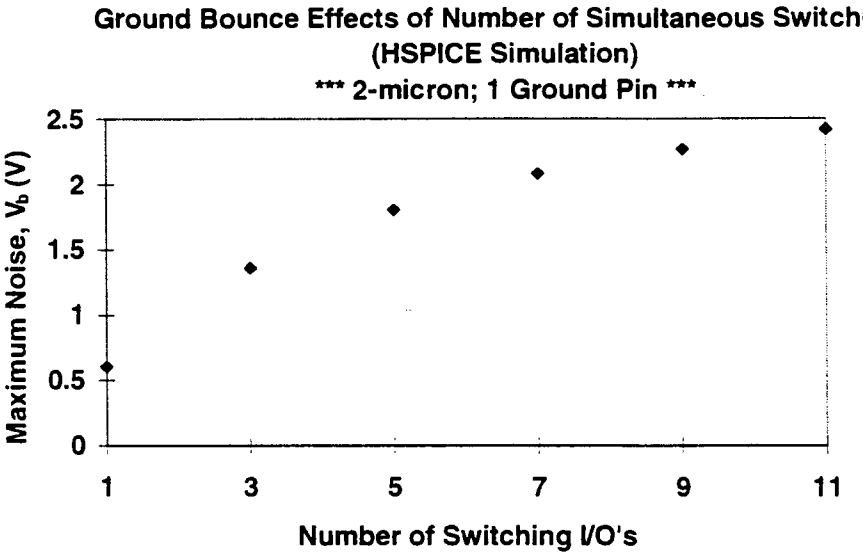

Figure 4.2: Ground Bounce versus Number of Switching I/O's (HSPICE)

In the second experiment, the goal is to characterize the behavior of ground bounce as a function of the number of ground pins for a particular IC. Similar to the first experiment, a set of I/O circuits is simulated. However, instead of varying the number of switching outputs, the number of ground pins is varied. The results are shown in Figure 4.3. Note that **SSO** means simultaneous switching output. The ground bounce reduces as the number of ground pins available to the IC is increased. The non-linear relationship is also examined in the next section.

In the third experiment, the objective is to characterize the behavior of crosstalk in relation with the number of neighboring pins switching. For this experiment, the I/O pin of interest is held at quiescent low while its nearest neighbors (on both sides) are switched. The results are shown in Figure 4.4.

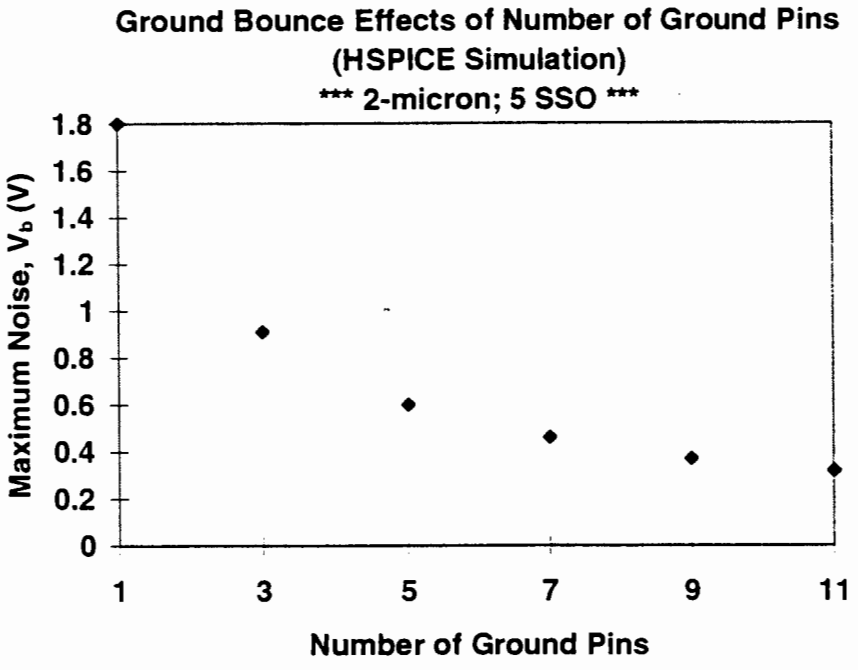

Figure 4.3: Ground Bounce versus Number of Ground Pins (HSPICE)

Figure 4.4 shows that crosstalk exhibits non-linear dependence on the number of switching pins. **Vc_ground** is obtained by simulating ground bounce without the mutual coupling effects; in contrast, **Vc_total** is obtained by simulating ground bounce with the mutual coupling effects between pins. The noise contribution as a result of mutual coupling, as indicated by the difference between **Vc_total** and **Vc_ground**, becomes more significant as the number of switching pins increases.

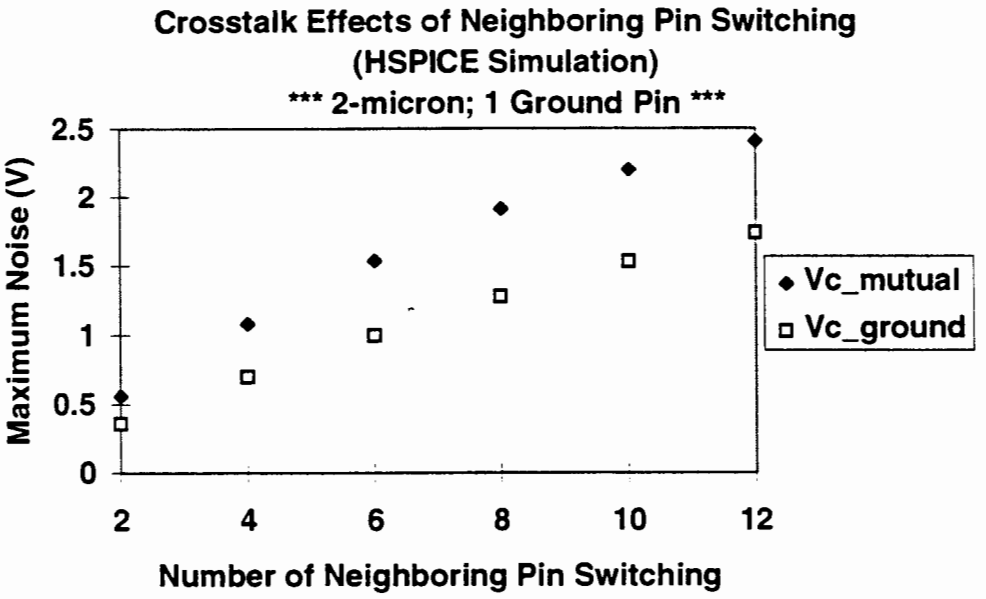

Figure 4.4: Crosstalk versus Number of Switching Neighbor Pins (HSPICE)

From the SPICE simulations, it is observed that ground bounce varies significantly with the switching behavior of the I/O's. These results are very important because memory IC's, such as DRAM's and SRAM's, are susceptible to multiple switching outputs (refer to [4]). As a result, the probability of generating a glitch or false logic from elevated ground bounce cannot be neglected. In the next section, the noise characteristics are examined closely to understand the non-linear relationship.

4.2 Mathematical Analyses of IC Noise Model

In the previous section, it is demonstrated that IC noises, namely ground bounce and crosstalk, exhibit non-linear dependence on the number of simultaneous switchings and ground pins. To understand the cause of the non-linear characteristics, the I/O and lumped RLC circuits are examined mathematically (refer to [15]).

Figure 4.5 illustrates the circuit model that will be involved in the mathematical analysis. In this model, the IC package parasitics are represented by the RLC circuits, and the N-device is used to discharge the output load (from 5V to 0V).

To analyze the effects of n switching outputs, the MOSFETs in Figure 4.5 can be modeled by:

$$I_{ds} = \frac{\beta}{2} \cdot (V_{gs} - V_t)^2 \tag{4.1}$$

V_{gs} in (4.1) can be rewritten to highlight the ground bounce effect:

$$I_{ds} = \frac{\beta}{2} \cdot [(V_{in} - V_b) - V_t]^2 \tag{4.2}$$

where,

I_{ds} is the transistor's saturation current,

V_{gs} is the transistor's gate-to-source voltage,

β is the current gain,

V_{in} is the input gate voltage,

V_b is the ground bounce voltage, and

V_t is the constant threshold voltage.

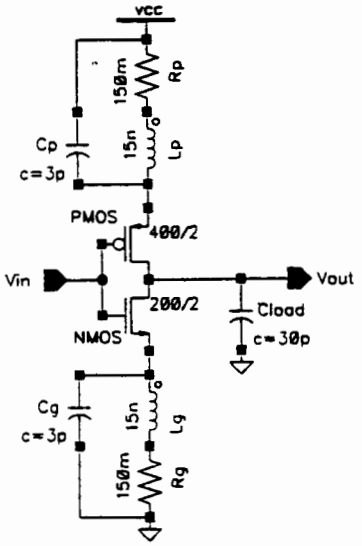

Figure 4.5: Simple Model for Ground Bounce versus Number of Switching I/O's

Therefore, from Kirchoff's Current Law and for n switching outputs,

$$I_{total} = n \cdot \frac{\beta}{2} \cdot [(V_{in} - V_b) - V_t]^2. \qquad (4.3)$$

I_{total} is the total current being discharged from the outputs to the ground reference. Note that the internal ground reference is denoted by V_b, and this reference is connected to the external power supply via the IC's ground pin (R_g,, L_g , and C_g). Since the ground pin is susceptible to the IC package parasitics, the following expression describes the internal ground reference:

$$V_b = \frac{L_g \cdot (I_{total} - I_{cg})}{T/2} + R_g \cdot (I_{total} - I_{cg}), \qquad (4.4)$$

where,

T is the switching period when the current is conducting,

I_{cg} is the current through capacitor C_g,

L_g is the IC's ground pin inductance, and

R_g is the IC's ground pin resistance.

To estimate I_{cg}, the following expression is used:

$$I_{cg} = C_g \cdot \frac{V_{OL}}{T_{fall}}. \qquad (4.5)$$

Because the value of I_{cg} is typically very small (less than 5 mA for target maximum output voltage to be considered as logical low, V_{OL}=0.8V, and fall time, T_{fall} =1ns) as compared to I_{total} (more than 200mA), it can be neglected to yield a more manageable expression:

$$V_b = \frac{L_g \cdot I_{total}}{T/2} + R_g \cdot I_{total}. \qquad (4.6)$$

Substituting (4.6) into (4.3) creates a quadratic expression as shown in (4.7). This expression can be solved to obtain the appropriate I_{total}.

$$I_{total} = n \cdot \frac{\beta}{2} \cdot [V_{in} - (\frac{L_g \cdot I_{total}}{T/2} + R_g \cdot I_{total}) - V_t]^2. \qquad (4.7)$$

Once the appropriate value of I_{total} is calculated, it can be back-substituted to (4.6)

determine the ground bounce voltage, V_b. Figure 4.6 shows the results of this analysis, calculated using the IC package values from Chapter 3 and a typical 1-micron process technology. Note that the 1-micron technology is used for mathematical analyses only, and is different from 2-micron technology used in the prior SPICE simulation. This difference is insignificant to the estimation of IC noise behavior because the package parasitics will not be affected.

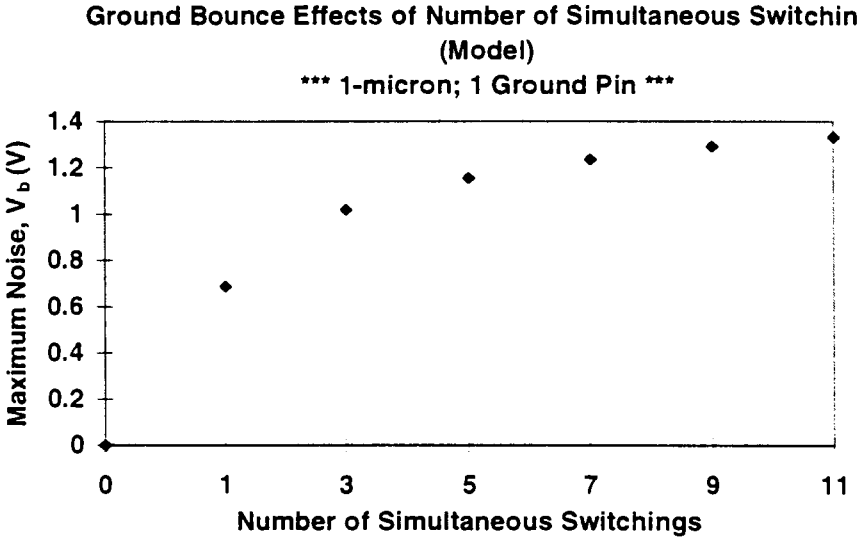

Figure 4.6: Ground Bounce versus Number of Switching I/O's (MODEL)

Note that the RLC circuit representing the ground pin has a resonant frequency of about 750 MHz, from (4.8), limiting the performance of the I/O circuit at high frequency.

$$\omega_0 = \sqrt{\frac{1}{L_g C_g} - \left(\frac{R_g}{L_g}\right)^2} \qquad (4.8)$$

On the other hand, Figure 4.7 illustrates the circuit model that will be involved in the mathematical analysis of ground bounce versus number of ground pins. Similar to the analysis above, the IC package parasitics are represented by the RLC circuits, and the N-device is used to discharge the output load (from 5V to 0V).

Analysis of the circuit in Figure 4.7 yields the following expression, which is similar to (4.3):

$$I_{total} = n \cdot \frac{\beta}{2} \cdot [(V_{in} - V_b) - V_t]^2. \qquad (4.9)$$

where,

$$V_b = L_g \cdot \frac{(I_{total}/m)}{T/2}, \qquad (4.10)$$

and

m is the number of ground pins.

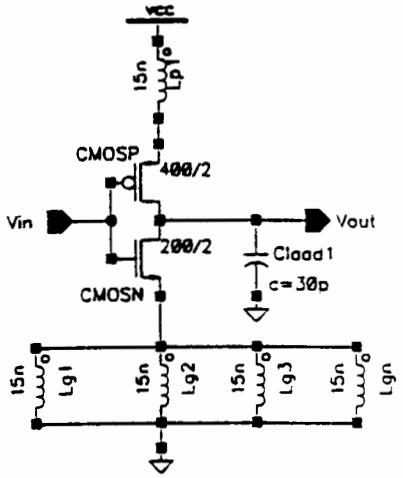

Figure 4.7: Simple Model for Ground Bounce versus Number of Ground Pins

Substituting (4.10) into (4.9) creates similar quadratic expression as shown below:

$$I_{total} = n \cdot \frac{\beta}{2} \cdot [V_{in} - (L_g \cdot \frac{(I_{total}/m)}{T/2}) - V_t]^2. \qquad (4.11)$$

From (4.11), I_{total} can be solved and back-substituted to (4.10). This solution lead to Figure 4.8, where the IC package parasitics from Chapter 3 and a typical 1-micron technology are used.

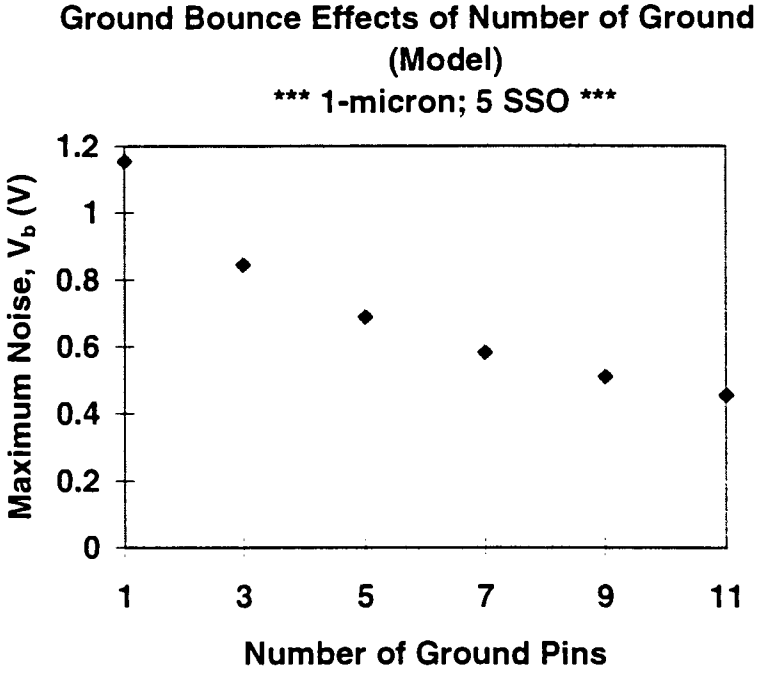

Figure 4.8: Ground Bounce versus Number of Ground Pins (MODEL)

In the case of crosstalk, the increase in number of switching neighbor pins was determined to cause a non-linear increase in noise. This can be modeled with

the aid of Figure 3.2. From (4.12), it is shown that the induced voltage, V_c, is directly proportional to the mutual inductance contributions of the neighboring pins.

$$V_c = L_{11} \cdot \frac{dI_1}{dt_1} + L_{M12} \cdot \frac{dI_2}{dt_2} + L_{M13} \cdot \frac{dI_3}{dt_3} + \ldots \qquad (4.12)$$

where,

L_{11} is the self-inductance,

L_{m12} is the mutual coupling with the second pin,

L_{m13} is the mutual coupling with the third pin, etc.

Assuming that all pins have the same slew rate, (4.12) can be reduced to the following expression:

$$V_c = (L_{11} + L_{M12} + L_{M13} + \ldots) \cdot \frac{dI}{dt}. \qquad (4.13)$$

By examining Figure 3.2, it can be observed that the value of L_{m1n} diminishes as n is increased or as the pins are further apart (refer to the **Mutual_L** curve). Therefore, the cumulative contribution to V_c (e.g. the center pin in Figure 3.2) increases non-linearly.

From the mathematical analyses above, the non-linear characteristics of ground bounce are shown to be consistent with the earlier SPICE simulations. Note that the mathematical analyses and SPICE simulations are based on different process technologies. Hence, it is important to compare the behavior and not the absolute noise magnitude.

Most importantly, it is demonstrated that the induced ground bounce (V_b) causes a negative feedback to the circuit, which effectively reduces V_{gs}. Consequently, the saturation current diminishes as V_b increases. It is this phenomena that causes the non-linear relationships. Although the models and simulations exhibit consistent behavior, these results have to be correlated with physical measurements. The next section discusses the measurements taken to verify the models' predictions.

4.3 IC Noise Measurement

In previous discussions, a number of concepts and models were introduced to understand the properties of IC noise. First, the RLC parasitics of the IC package were simulated; second, these RLC values were used to create a lumped circuit; and finally, the lumped circuit was simulated and analyzed in noise models with N- and P-devices. While the results seem reasonable, it is still necessary to verify the models' predictions through physical measurements. In addition to verification, physical measurements can provide insights on circuit behaviors that tend to be overlooked.

To verify the models, an existing IC (complex programmable logic device) developed under a 0.7-micron technology is measured with lumped capacitance (35 pF) connected to each output pin. The relationship between ground bounce and

number of simultaneous switching pins is shown in Figure 4.9. The maximum ground bounce voltages (V_b) were measured over three operating supply voltages: 4.5 V, 5.0 V, and 5.5 V with 1 ns rise time. Note that only one power and ground pair is connected to the external power supply. Since the technologies used for the models and measurement are different, the important information presented in Figure 4.9 is the trend and not the absolute voltage magnitude.

Nonetheless, to accurately calculate the noise magnitude, the square-law equations above should be modified to incorporate velocity saturation effects, body effects, short-channel effects, etc., especially for sub-micron devices (refer to[16]). These modifications will not be done in this thesis.

From Figure 4.9, it can be observed that the ground noise exhibits a non-linear relationship with the number of switching I/O circuits. This result is consistent with the models simulated and analyzed in Section 4.1 and 4.2. Hence, the models can concluded to be a reliable characterization of the IC noise behavior.

In addition to verification, two sets of measurements were taken to observe the behavior of IC noise across temperature and process corners. The first set of measurements shows that the IC noise for this I/O circuit is inversely proportional to temperature. This result (refer to Figure 4.10) is largely due to the fact that the mobility of electrons in the N-device is reduced when the temperature is increased.

Hence, the total current through the ground pin is decreased, which translates to a direct reduction in ground noise.

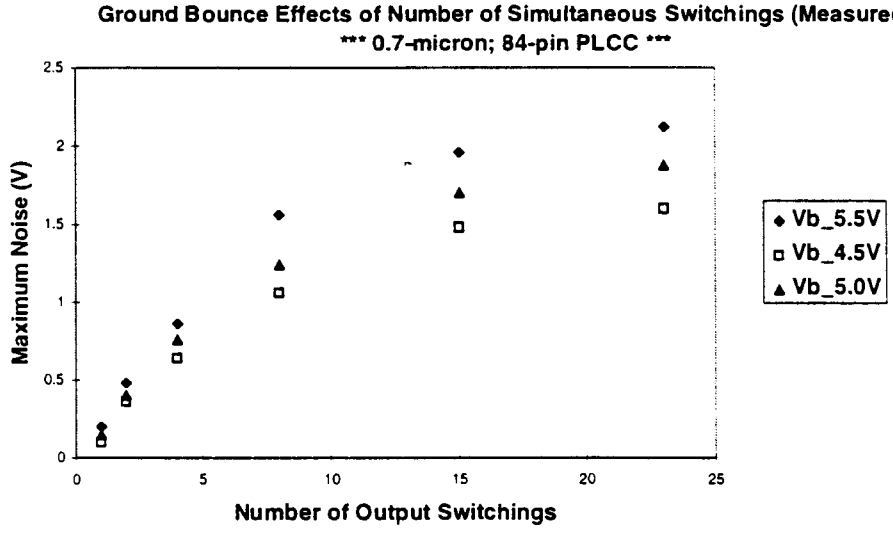

Figure 4.9: Ground Bounce versus Number of Switching I/O's (MEASURED)

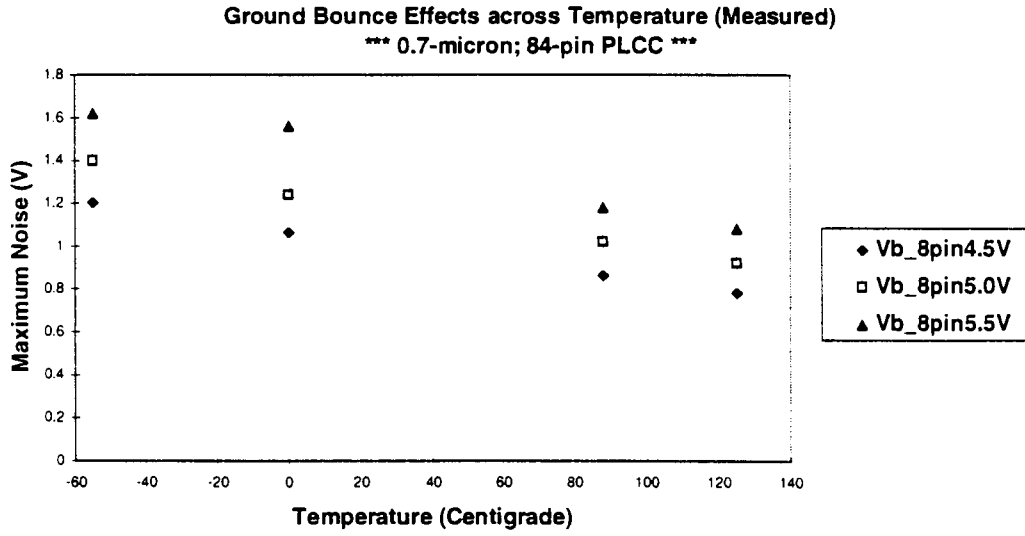

Figure 4.10: Ground Bounce versus Temperature (MEASURED)

From the second set of measurements, it is shown in Figure 4.11 that the IC noise varies significantly across the fast and slow process corners. The fast corner consists of devices with shorter channel length, 5.50 V supply voltage, and 0°C temperature. On the contrary, the slow corner consists of devices with longer channel length, 4.50 V supply voltage, and 88°C temperature. These variations cause differences in the device (N-device for discharging and P-device for charging the load) saturation current, which in turn affects the induced ground bounce. Since these two corners show about 45% variation in IC noise, it imposes a great challenge for circuit designers to develop high-speed I/O circuits without violating noise specifications.

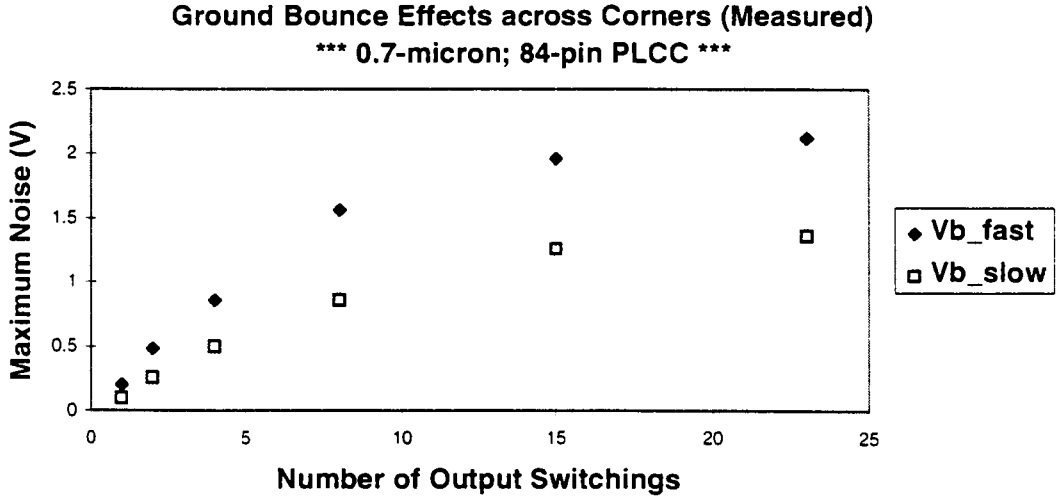

Figure 4.11: Ground Bounce versus Process Corners

In practice, there is not much a circuit designer can do to the package inductance to lower the induced ground bounce; however, he or she has control

over the slew rate. This option carries a trade-off between noise performance and switching rate. Referring to (2.4), when the slew rate (dI/dt) is decreased, there is a direct reduction in ground bounce, V_b. Nevertheless, decreasing the slew rate also results in slower speed. Figure 4.12 shows the measurement of two identical I/O circuits with different slew rates.

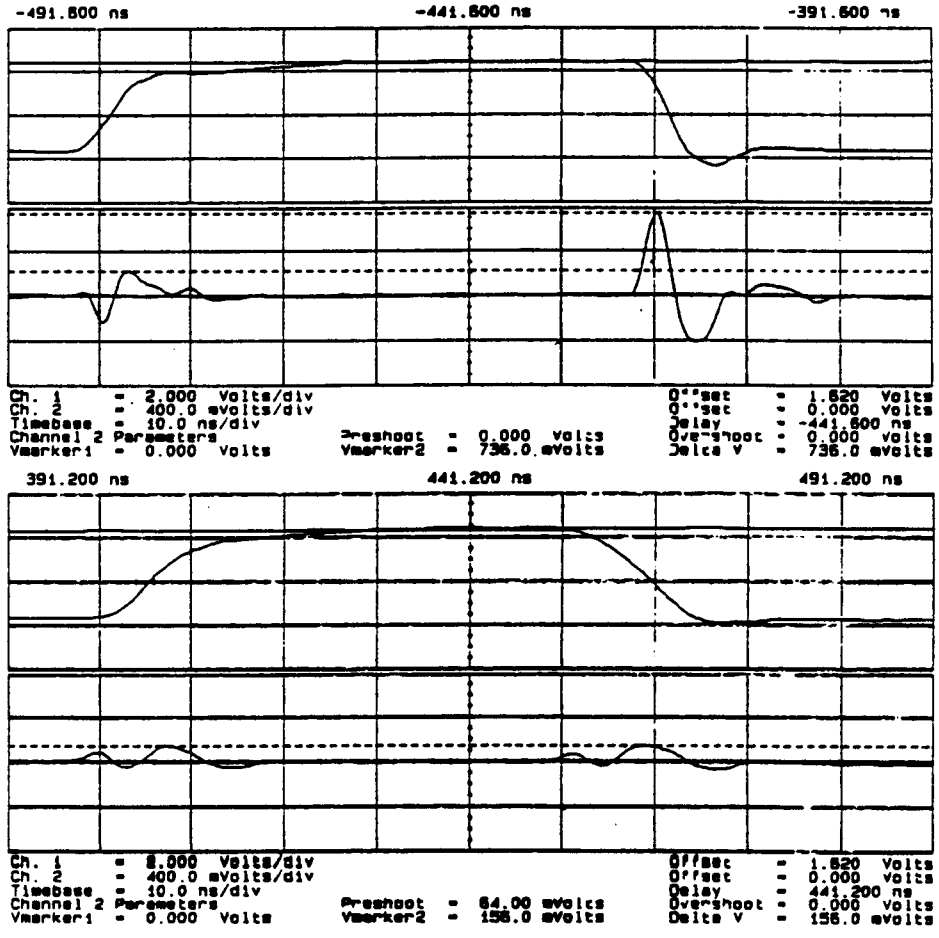

Figure 4.12: Ground Bounce with Different Slew Rates (MEASURED)

On the bright side, it is shown in Figure 4.12 that the trade-off favors noise reduction. A 56% reduction in speed would cause 78% reduction in noise.

Therefore, changing the slew rate becomes an attractive option for I/O circuit designers.

In this chapter, a set of IC package models has been created, analyzed, and verified. In addition to these results, two carefully constructed experiments revealed that the IC noise varies significantly across process corners, supply voltage, and temperature. While it imposes a great challenge for circuit designers, the third experiment shows that properly managed slew rates can aid in noise reduction.

CHAPTER 5

HIGH-SPEED I/O CIRCUIT WITH ON-CHIP PVT-COMPENSATION

From a system standpoint, it is necessary for each of its component to maintain functionality over a range of environmental stress conditions. The collapse of an IC component could result in catastrophic system failure. One of the major IC failures is signal quality degradation, and it manifests itself through false logic transitions or logic glitches. Therefore, to achieve consistent signal quality, a self-adjusting I/O circuit is designed to vary its slew rate based on local switching conditions. This circuit enables better noise control, and it is described in Section 5.1. In addition, a PVT-compensated control circuit is developed to maintain I/O drive capability over a range of PVT variations. This control circuit is introduced in Section 5.2. Section 5.3 analyzes the performance of the I/O circuits with PVT-compensation, and finally, Section 5.4 discusses some applications that will benefit from these circuits.

5.1 I/O Circuit with Self-Adjusting Slew Rate

In Chapter 4, the analyses of the IC models revealed a non-linear relationship between IC noise and the number of switching outputs. Based on those results, an output buffer is developed to detect multiple output switching conditions within neighboring pins, to adjust its slew rate accordingly, and to thus minimize IC noise.

In contrast to the I/O circuits discussed in Section 2.3, the proposed I/O circuit adjusts its slew rate based on neighboring output switching conditions. This technique allows the I/O circuit to reduce its slew rate only when necessary. As a result, the I/O circuit can benefit greatly in speed while maintaining signal quality.

Figure 5.1 illustrates the proposed I/O circuit. The NAND, NOR, PDRIVE, and NDRIVE topology forms a tristateable output buffer. The additional N- or P-devices connected in series are the elements that provide control over the turn on speed of the PDRIVE or NDRIVE transistor, respectively. Note that the IOSELN and IOSELP signals are broadcast from the PVT-compensated control circuit that will be described in Section 5.2. These signals turn on the drivers when asserted (IOSELN is high and IOSELP is low), or tristate the drivers when deasserted. In addition to the PVT-compensation signals, CL and CR are the signals from EXOR gates that compare the switching conditions of the left and right pins with respect to the I/O pin of interest. For example, for I/O pin 3, the CL signal is the output of the EXOR gate that compares I/O pins 2 and 3. On the other hand, the CR signal is the

output of the EXOR gate that compares I/O pins 3 and 4. This topology is shown in Figure 5.2. The CLB and CRB signals are the complements of CL and CR, respectively.

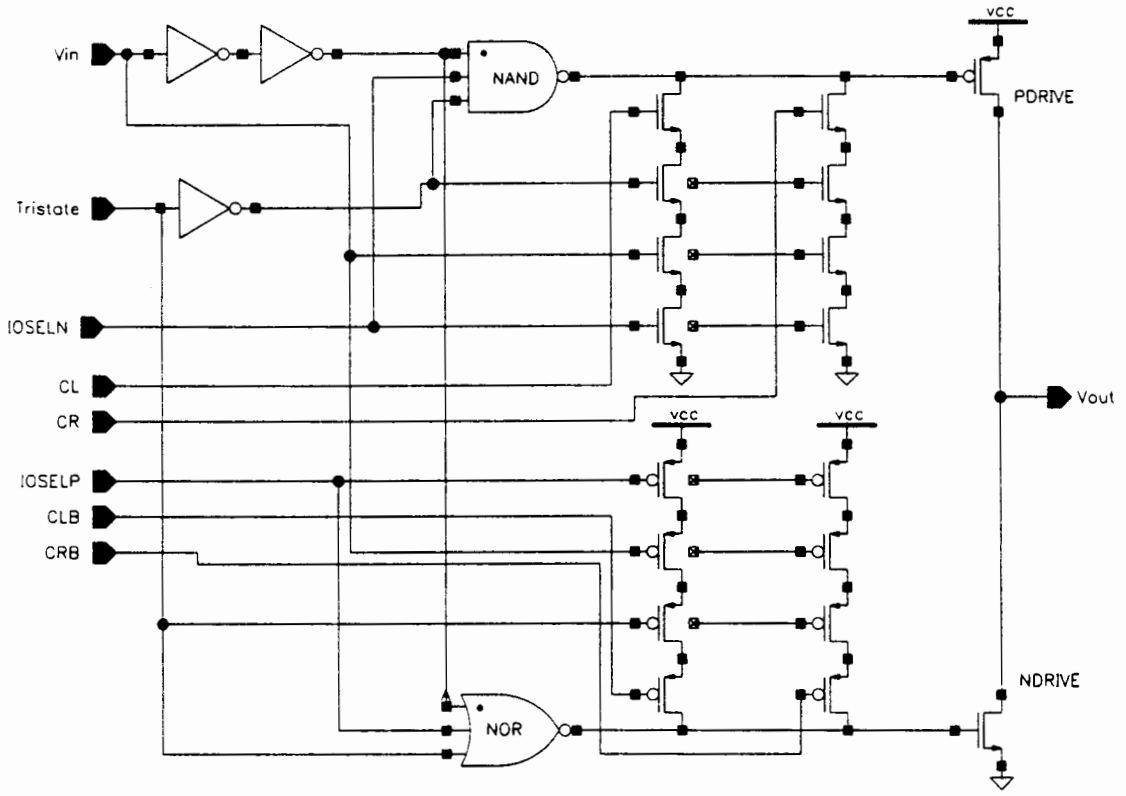

Figure 5.1: I/O Circuit with Self-Adjusting Slew Rate

In this I/O circuit, when both the neighboring pins are detected to be switching in the same direction as the I/O pin of interest, the additional series N- and P-devices that provide boost to the slew rate will be turned off. As a result, the slew

rate of the output drivers will be slowest. If either the left or right I/O pin is switching in the same direction as the I/O pin of interest, only one set (CL or CR) of series N- and P-devices will be turned off; therefore, the slew rate is moderate. However, if the I/O pin of interest is the only pin switching, both sets (CL and CR) of series N- and P-devices will be turned on to provide fastest slew rate.

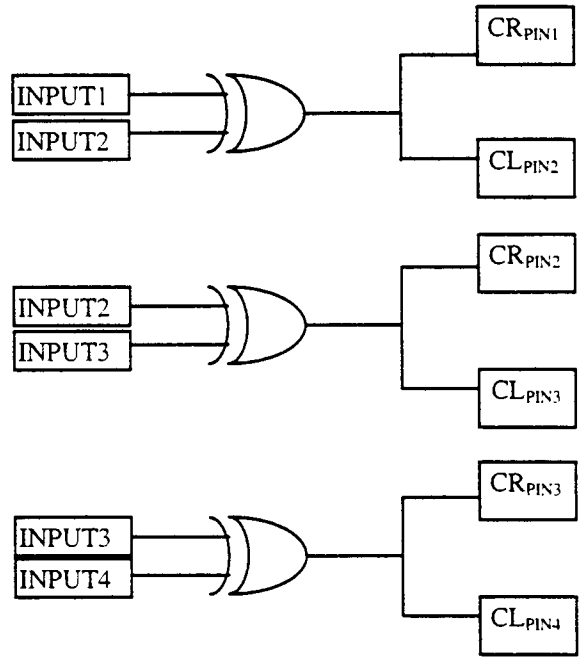

Figure 5.2: Output Switching Detection Circuit

Figure 5.3 shows how the PVT-compensation control circuit and the self-adjusting mechanism control the output drive capability. The PVT-compensation control circuit detects the state of the IC, and this translates to the selection of one of the vertical boxes. Each of the vertical boxes represents a certain current drive.

The highest box indicates the slow corner where the current drive prior to compensation is weakest, and therefore, the PVT-compensation control circuit turns on all output drivers (maximum drive capability) to ensure the deteriorated current drive is compensated. As a result, the effective current drive is maintained. On the contrary, the lowest box represents the fast corner, and therefore, the current drive is decreased to the minimum. This compensation mechanism allows the I/O circuit to operate in a constant current drive mode. Consequently, the IC noise can be stabilized to a predictable range of values.

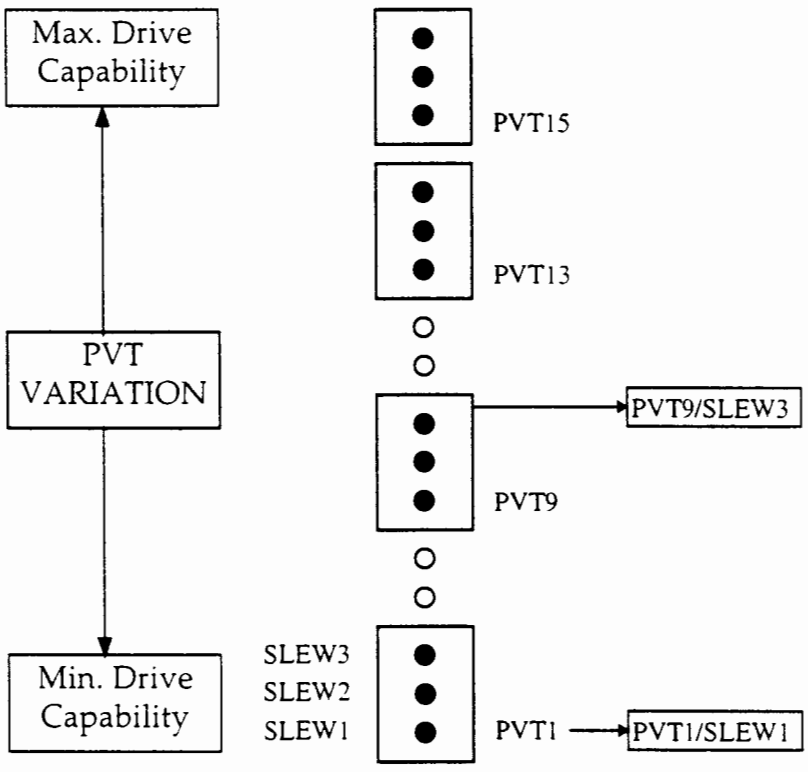

Figure 5.3: Current Control in the Proposed I/O Circuit

While the PVT-compensation control circuit provides a method to stabilize switching noise, the self-adjusting I/O circuit can dynamically optimize the slew rate such that maximum switching speed can be obtained without violating noise specifications. This method is equivalent to selecting a particular point within the PVT box (refer to Figure 5.3). Each point corresponds to a different slew rate, with the highest being fastest and the lowest being slowest. For example, if an IC is operating in its fast corner, and both neighboring I/O pins are switching along with the I/O pin of interest, the optimum PVT-compensation and slew rate combination is at PVT1/SLEW1. In contrast, if an IC is operating in its nominal corner, and only the I/O pin of interest is switching, the optimum PVT-compensation and slew rate combination is at PVT9/SLEW3.

Schematically, the complete set of I/O circuits for a particular output is shown in Figure 5.4. Note that the circuit consists of 4 blocks (IO8, IO4, IO2, and IO1), where the circuit for each block is shown in Figure 5.1. The size or drive capability of each block is binary-weighted, which is activated by the codes (IOSELN1..IOSELN8 and IOSELP1..IOSELP8) from the PVT-compensated control circuit. For example, in the fast corner, the IOSELN1..IOSELN8 and IOSELP1..IOSELP8 signals will all be asserted to select the PVT1 box. In the nominal corner, IOSELN1, IOSELN8, IOSELP1, and IOSELP8 will be asserted

while the other signals are deasserted. As such, this combination will select the PVT9 box.

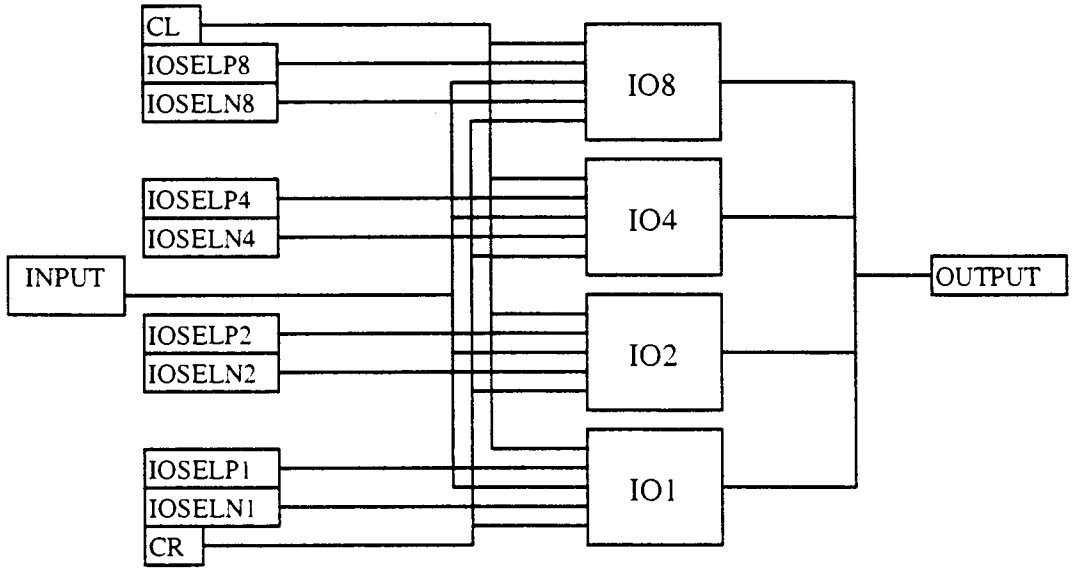

Figure 5.4: Proposed I/O Circuit

In addition to noise control, the proposed I/O circuit has a property that makes it even more attractive: power reduction. The feature of this I/O circuit is that it slows the slew rate whenever there is multiple switching. As a result, the power consumption is also reduced.

$$P = \frac{1}{T} \cdot C \cdot V^2 \qquad (5.1)$$

where,

P is the dynamic power dissipation,

T is the time taken to charge/discharge an output load,

C is the switched capacitance, and

V is the supply voltage.

From (5.1), it can be observed that slowing the slew rate (increasing T) will lead to a lower dynamic power dissipation. For comparison, under 3-output switching environment, conventional I/O circuits would yield $3(1/T)CV^2$ in power dissipation. However, the proposed I/O circuits would only yield $3(1/3T)CV^2$. This calculation shows a factor of 3 in power savings.

Since the I/O circuits typically drive larger output loads (about 35 pF per pin) as compared to the internal circuits, the amount of power being saved can be significant. Furthermore, as the proposed I/O circuit could effectively control IC noise, the need for large noise margin is diminished. Consequently, the supply voltage, V, in (5.1) could be scaled down to further reduce power dissipation without jeopardizing noise performance.

5.2 PVT-Compensated Control Circuit

As described in Chapter 4, the variations in IC conditions in terms of process, supply voltage, and temperature (PVT) can significantly affect its noise performance. Therefore, a circuit is developed to sense these variations, and communicate the results to the I/O circuits such that signal integrity can be sustained.

The basic concept underlying the PVT-compensated control circuit is that process, voltage, and temperature variations cause a device to change its capability to charge or discharge an output load. Since the output load is assumed to be capacitive, the current through the device (N-device for discharging and P-device for charging) is the focus. By examining (2.4), the greater the current change (indicated by dI/dt), the greater the induced IC noise. Therefore, the control circuitry should sense the current variation as a function of the environment. The state of the IC can be communicated through some coding mechanism such that the I/O circuits can react accordingly to maintain constant current drive.

Figure 5.5 shows the circuit topology for the proposed PVT-compensated control circuit (based on [5]). In this circuit, a binary-weighted scheme is used to turn the N- and P-devices on or off. Basically, turning on the P-devices in parallel is equivalent to increasing the effective width of a single P-device. Hence, the number of P-devices being turned on reflects the state of a P-device under certain PVT combinations. Referring to (4.1), the increase in effective width allows greater saturation current, and the magnitude of this current is converted into a voltage, V_p, through the use of resistor R_p.

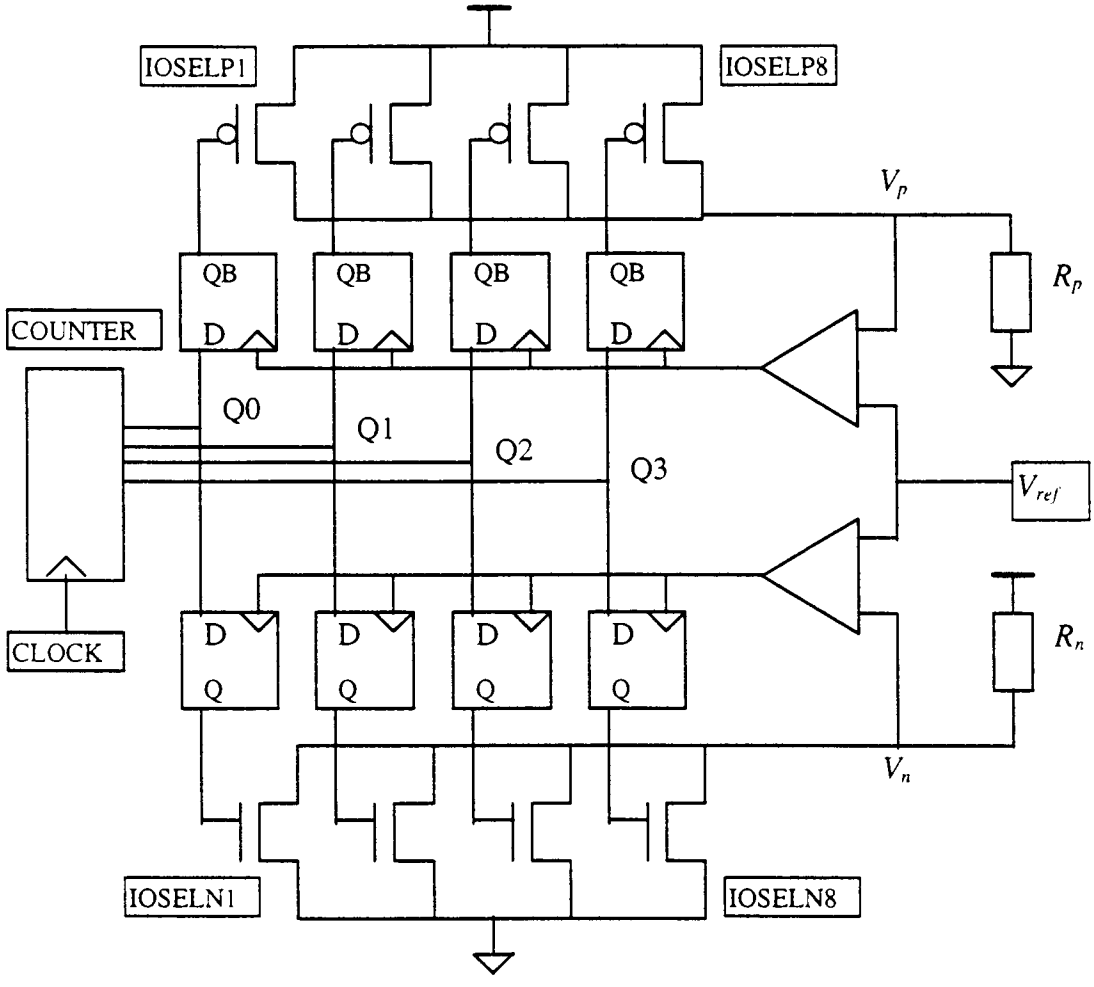

Figure 5.5: PVT-Compensated Control Circuit

With that idea in mind, the outputs of the free-running 4-bit binary counter are latched by the D-registers when the voltage at V_p falls below V_{ref}. This situation occurs when the total current provided by the P-devices is too small. As such, the resulting voltage (total current from P-devices multiplied by R_p) at V_p is less than V_{ref}. V_{ref} is the reference voltage specified for a particular technology, and can be

provided externally or through an internal bandgap reference circuit. The D-registers will continue to sample the outputs from the incrementing counter and cause more P-devices to turn on. As a result, the amount of current through R_p increases. This increase in current will correspond to an increase in V_p. Once the voltage at V_p is greater than V_{ref}, the output of the comparator flips from high to low. Consequently, the D-registers will cease to sample the outputs from the counter. The last sampled value will be the codes (IOSELP1, IOSELP2, IOSELP4, and IOSELP8) that represent the state of the IC. By symmetry, the codes (IOSELN1, IOSELN2, IOSELN4, and IOSELN8) for the N-devices can be obtained in similar manner. These codes are communicated to the I/O circuits, which are described in Section 5.1.

The 4-bit binary counter counts from 0000 to 1111, and rolls over to 0000 to begin the next cycle. Since the PVT variations occur slowly through time, the rate of the counter can be made slow (in the kHz range). If the counting rate is increased, a PVT change can be sensed faster, and the corresponding output code can be reflected in the I/O circuit earlier (this is also known as *sense recovery*). For example, a 3-stage ring oscillator can be used for slow counting. Otherwise, the IC's internal clock signal can be utilized, especially when the sense recovery rate is critical.

After sensing the PVT variations, the results of the PVT-compensated circuit are broadcast to the I/O circuits. The I/O circuits will increase, decrease, or maintain their relative drive capability depending on the PVT codes. Hence, this technique ensures that the output load can always realize a constant charge and discharge slew rate under a certain PVT condition.

With the combination of PVT-compensation and dynamic slew rate adjustment, the IC noise level can be controlled accurately. This result is critical for applications that require minimal noise while maintaining switching speed.

5.3 Simulation Analyses

As detailed in Section 5.1 and 5.2, two noise control techniques are combined to provide maximum control over switching noise. These techniques, dynamic slew rate adjustment and PVT-compensation, control the output current drive based on IC environment and switching conditions. This section discusses the simulation results obtained for the circuits mentioned above, and Section 5.4 describes some useful applications for these circuits.

A set of I/O circuits is simulated in HSPICE, and the impact of the self-adjusting slew rate mechanism on IC noise is analyzed. Referring to Figure 5.6, the top graph demonstrates the three available slew rates as a function of the number of simultaneous output switchings, and the bottom graph shows the slew rate variation

effect on ground bounce. The slew rate is the slowest when all of the three output pins are switched. On the other hand, when only one pin is switched, the slew rate is maximized. An important result to realize is that for all three switching conditions, the maximum ground bounce is almost constant. In short, when a single output is switching, the slew rate is 3 times faster than when all the 3 outputs are switching, but in all cases, the maximum noise remain the same. In essence, the IC noise is shown to be less sensitive to the number of simultaneous switchings by small adjustment to the I/O's slew rate.

Referring to Figure 5.6, the maximum ground noise is approximately 662.5 mV, and the difference between 1 and 3 output switchings is 62.5 mV (at the maximum ground noise). This figure corresponds to about 10% difference in ground noise. For comparison, the simulated ground noise (refer to Figure 4.3) using a conventional I/O circuit yields approximately a 56% difference.

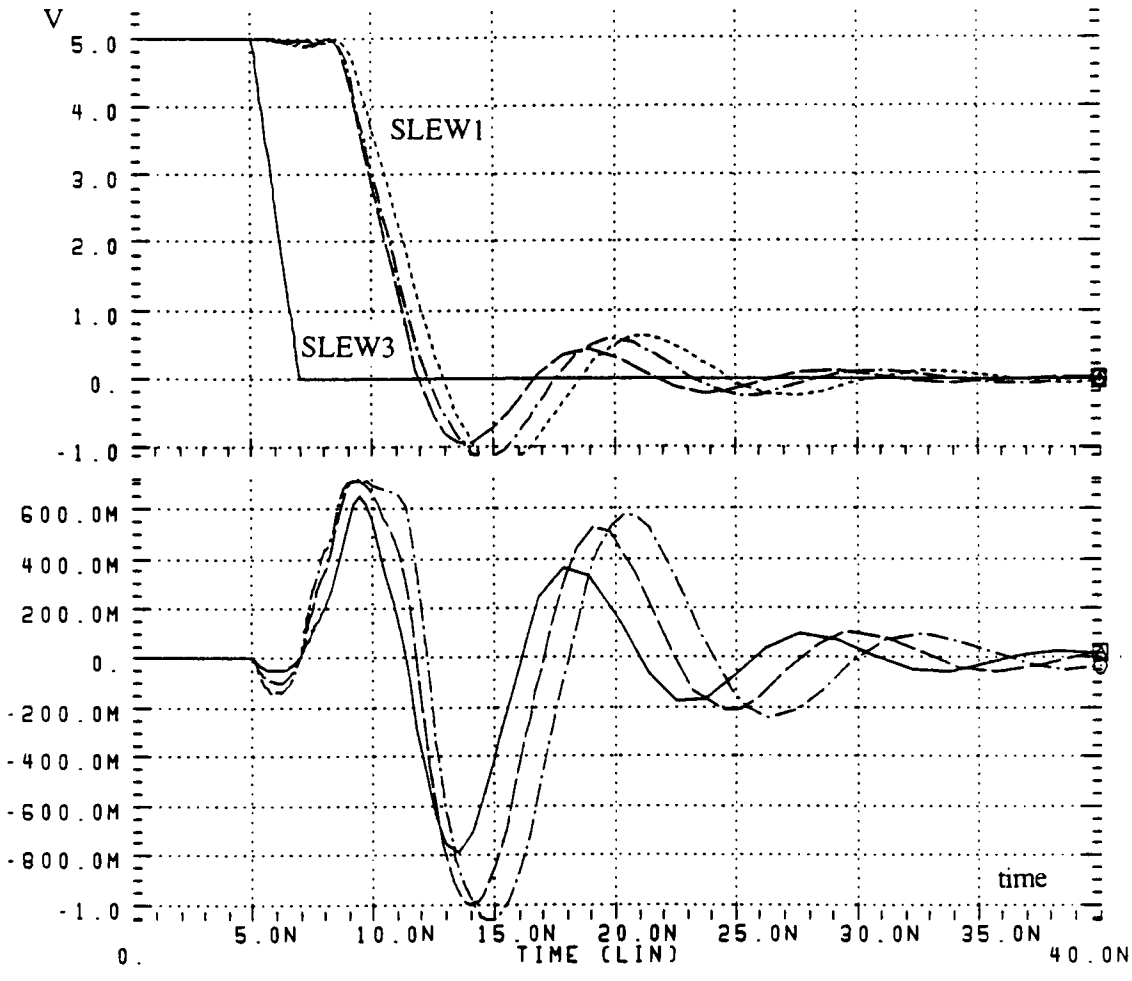

Figure 5.6: Simulation Results for I/O Circuit with Self-Adjusting Slew rate

In order to illustrate the impact of the PVT-compensation control circuit, an I/O circuit is simulated according to the criteria discussed in the previous sections. Referring to Figure 5.7, the top graph shows the slew rate as a function of PVT control codes. Each code represent a certain operating state of the IC in terms of process, voltage and temperature. As the codes are incremented in their binary weights, the slope of the output transition becomes steeper. This result is due to the

increase in current drive capability. The bottom graph shows the effects of slew rates on ground bounce. By deduction, when the operating state of the circuit causes the current drive to decrease, the PVT codes can be increased to compensate for the loss. Hence, the current drive can be maintained. The PVT-compensation control circuit monitors the IC states dynamically, and changes the PVT codes whenever deemed necessary. For comparison, Table 5.1 charts the effective width of the output driver as a function of PVT codes. The drive capability of an I/O driver without compensation is equivalent to 100%. Therefore, varying the PVT codes changes the effective current drive with respect to the I/O driver without compensation.

Code: IO8 IO4 IO2 IO1	Effective Driver Width *	Relative Drive
0 0 0 1	1·W	11%
0 0 1 1	3·W	33%
0 1 0 1	5·W	56%
0 1 1 1	7·W	78%
1 0 0 1	9·W	100%
1 0 1 1	11·W	122%
1 1 0 1	13·W	144%
1 1 1 1	15·W	167%

* W is a standard device width (e.g. 100 μm).

Table 5.1: Output Drive Capability

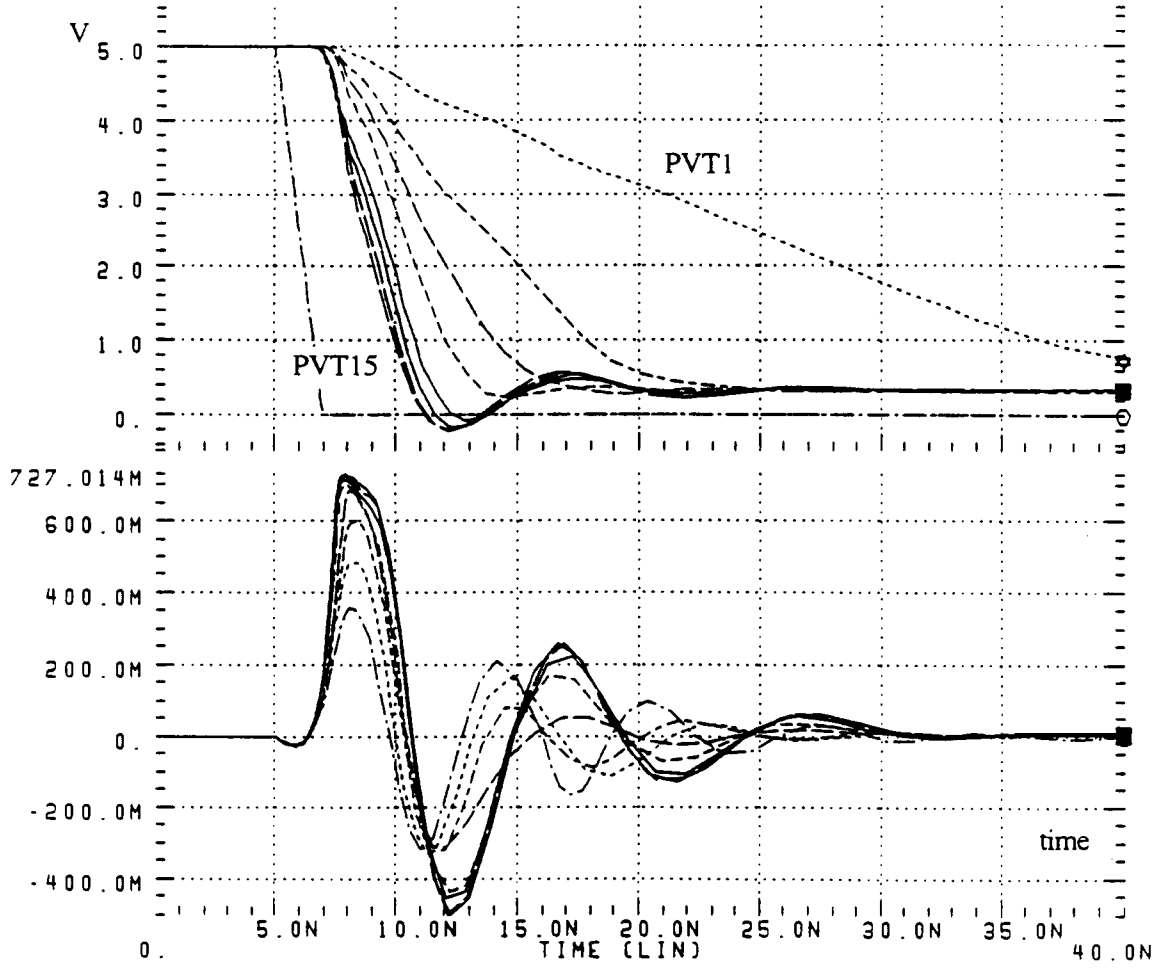

Figure 5.7: Simulation Results for PVT-Compensated I/O Circuit

On the other hand, the dynamic slew rate and PVT-compensation mechanisms cause a 0.25 ns delay in response time, which is about 8% of the overall I/O buffer propagation delay. This delay is the time taken by the EXOR gates to sense switching conditions, and can be reduced by increasing the gates' drive capability. Moreover, based on preliminary layout, the I/O pad area is increased by about 40%.

5.4 Applications

Because of their ability to control noise and reduce power dissipation, the proposed I/O circuits provide great advantages for high-performance VLSI circuits. Besides being used as conventional interface circuits, these I/O circuits can be utilized to reduce test time and enhance asynchronous circuit communications. The following discussions briefly introduce two of the applications mentioned above.

5.4.1 Test and Program Time Reduction

In recent years, the practice of in-system testing has gained huge popularity. The main standard endorsed by the industry for in-system testing is known as the IEEE 1149.1 Boundary Scan. This technique introduces 5 additional pins (TMS, TCK, TDI, TDO, and TRST) to an IC in order to perform the in-system tests. As such, many IC manufacturers design these pins with dual function. For example, the TMS pin can be used as a normal output pin, say $Data_1$, when the in-system test is disabled. This method will reduce pin count while maintaining Boundary Scan compatibility.

Since this technique uses serial data communications, the slew rate of each high-to-low or low-to-high transition becomes an important issue. The I/O circuits discussed in Section 2.3 have an inherent limitation in handling this situation. In order to reduce noise, the slew rate for all the I/O circuits are slowed down for all

conditions, and this will result in much longer test time. However, since the only output pin that is switching is the TDO pin, the proposed I/O circuit can detect this condition and allow the signal to be switched as fast as possible without violating noise specifications. As the serial data chain gets longer due to larger system tests, the total accumulated savings in test time become more appealing. From (5.2), it is shown that the total savings in test time can be significant when the serial chain length, n, is large enough. The proposed I/O circuit can reduce the t_{LH} and t_{HL} by 67% each because the neighboring pins are not switching, and therefore, the accumulative test time can be decreased.

$$Time_{TEST} = n \cdot (t_{LH} + t_{HOLDH} + t_{HL} + t_{HOLDL}) + m \cdot (t_{LOGIC}) \qquad (5.2)$$

where,

n is the length of the serial chain,

t_{LH} is the low-to-high transition time,

t_{HOLDH} is the hold time at logic high,

t_{HL} is the high-to-low transition time,

t_{HOLDL} is the hold time at logic low,

m is the number of logic blocks under test, and

t_{LOGIC} is the time to propagate through the logic block under test.

Figure 5.8 shows a typical test time plot over a range of serial chain lengths, n. **TimeCONV** is the overall test time using a conventional I/O circuit, and

TimeTEST is the test time using the proposed I/O circuit. From Figure 5.8, the overall test time is significantly reduced using the proposed I/O circuit, and this advantage can be easily translated into cost savings. Finally, as the complexity of the IC increases (as reflected by longer serial chains), the amount of test time savings also increases.

To reduce time-to-market, it is often cost-efficient to use programmable logic IC's, such as FPGA's (Field Programmable Gate Array) or CPLD's (Complex Programmable Logic Device), in board designs. Although these IC's shrink design time, they require logic programming before they can be used. Therefore, they require programming times that add up quickly in a high-volume manufacturing situation.

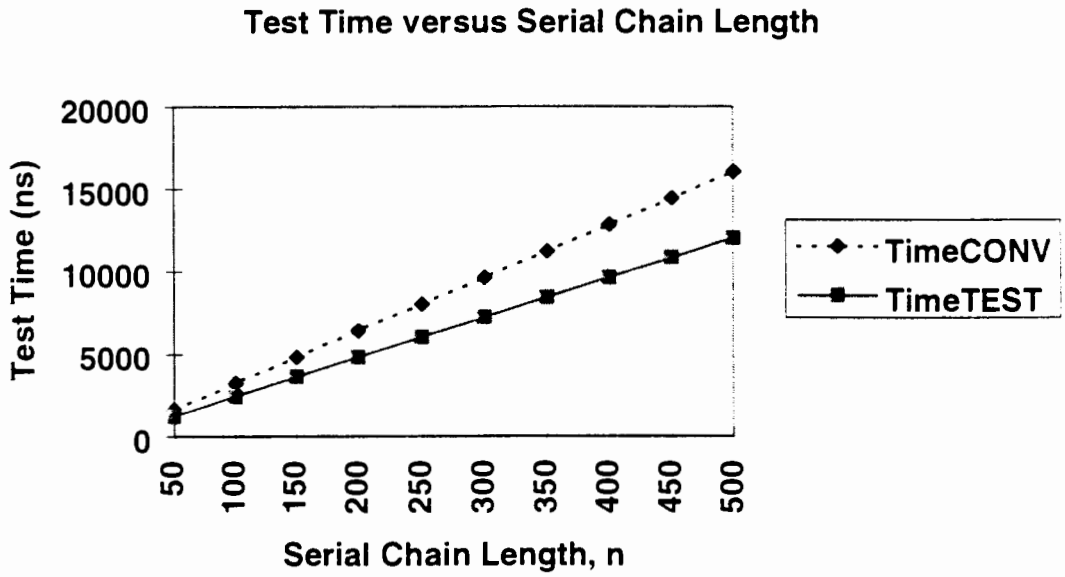

Figure 5.8: Test Time versus Serial Chain Length

In order to program the IC's, dual function I/O pins are used along with serial data communication. Some CPLD's utilize the Boundary Scan pins for programming as well as testing in order to reduce pin count. Since this situation is similar to the test time discussion above, the same benefits are gained by using the proposed I/O circuits. Therefore, (5.2) can be modified to reflect the estimated programming time, as shown in (5.3).

$$Time_{PROG} = m \cdot [n \cdot (t_{LH} + t_{HOLDH} + t_{HL} + t_{HOLDL}) + (t_{PROG})] \quad (5.3)$$

where,

n is the length of the serial chain,

t_{LH} is the low-to-high transition time,

t_{HOLDH} is the hold time at logic high,

t_{HL} is the high-to-low transition time,

t_{HOLDL} is the hold time at logic low,

m is the number of logic rows to be programmed, and

t_{PROG} is the time to program each logic row.

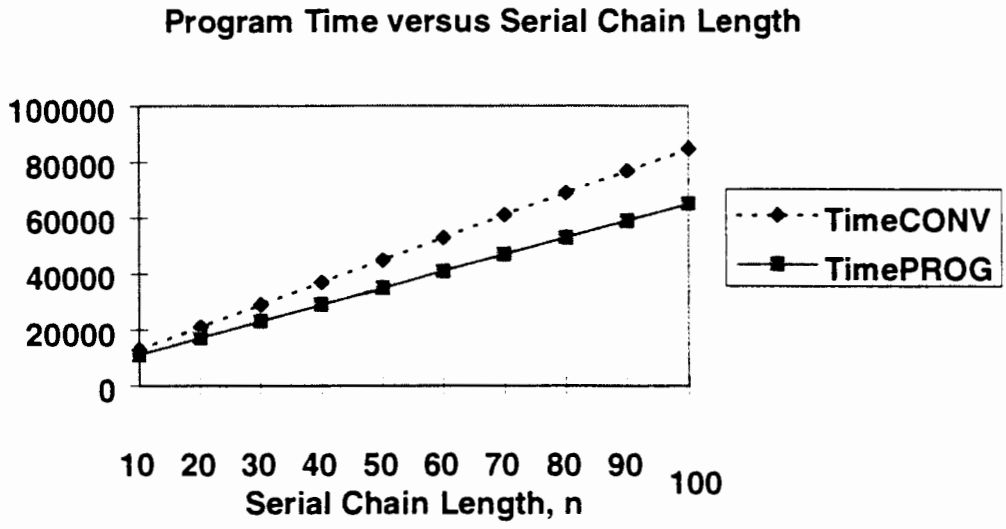

Figure 5.9: Program Time versus Serial Chain Length

Similar to the test time reduction discussion, the effect of serial chain length on the overall program time can be observed in Figure 5.9. The length of the serial chain is a measure of the IC's density, where longer chains indicate higher chip densities. In Figure 5.9, **TimeCONV** is the program time using conventional I/O circuits while **TimePROG** is the program time using the proposed I/O circuit. It is shown that the program time can be reduced using the proposed I/O circuit, and the benefit increases as the IC complexity increases (as reflected by longer serial chain lengths).

5.4.2 Asynchronous Circuit Communication

In some high-speed applications, the challenge of signal integrity has motivated circuit designers to use alternative signaling schemes. One of the popular

ideas is to implement a gray code or one-hot asynchronous scheme in the I/O interface. This scheme allows only one signal within a group of pins to be switched per clock. An example of a group of signals would be BE0#, BE1#, BE2#, and BE3# (Byte Enable) signals for a microprocessor to implement memory interleaving.

The proposed I/O circuit fits perfectly into this scheme because it rewards, yet does not demand, single output switching. Hence, the I/O pin can always be switched with the fastest slew rate. Moreover, when the IC is redesigned, or reprogrammed as in FPGA's or CPLD's, the I/O circuits need not be redesigned because they can adapt dynamically to preserve signal integrity. In addition to flexibility, since the I/O circuit can effectively control IC noise, the output can be connected to noise-sensitive circuits, such as monostable multivibrators and one-shot circuits, without risking false logic transitions.

CHAPTER 6

CONCLUSIONS

6.1 Conclusions

In the simulations performed in Chapter 3, the physical properties of an IC package are modeled using passive RLC circuitry. This lump circuit model is significant to circuit designers because it allows the IC noise characteristics to be studied in relation to IC package parasitics. The 3-D simulations yield lumped RLC circuits that represent IC package pins. These lumped circuits can be incorporated into an I/O circuit in the design process for noise performance simulations.

From the IC noise models developed in Chapter 4, the analyses and measurement show that the non-linear behavior of IC noise can be estimated. The SPICE experiments and models are based on the RLC circuits obtained from Chapter 3. In the course of the research, it is also found that the package inductance contributes the largest portion of the IC noise. This finding provides a key to the IC noise solution, which is slew rate control. Hence, understanding the IC behavior provided the basis for the development of two circuits that feature IC noise control and power reduction.

Based on the observations in Chapter 4, an I/O circuit is designed to control IC noise by monitoring local output switching conditions. In addition, a PVT-compensated control circuit is developed to control IC noise in an unstable environment. This circuit is shown in Chapter 5 to be effective in compensating the output current drive under process, supply voltage, and temperature variations. Both circuits are simulated to work efficiently together for noise control.

In conclusion, the study of signal integrity and development of two circuit techniques yield a robust I/O circuit that can effectively control IC noise. In addition to IC noise control, these I/O circuits have the capability to improve speed performance and power consumption by a factor of 3 in a single or triple output switching environment. Therefore, the objectives this thesis are achieved.

6.2 Future Work

In this field of study, there are a number of areas that need substantial research work. Since the impact of IC packaging is critical to noise performance, it is necessary to investigate better materials and package types for future packaging solutions. From another perspective, a more general approach to solving future noise issues is to develop architectures that are less susceptible to signal noise. It will also be advantageous to re-evaluate current switching techniques, and propose an entire new family of signaling schemes. Finally, in recent years, there has been

interest in the industry to develop simultaneous bidirectional I/O circuits (refer to [17] and [18]). These circuits allow simultaneous transmission and reception of signals in a single wire, and as a result, they show great promise for significant performance improvement. However, the signal noise properties as a function of PVT and slew rate remain to be investigated.

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