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THESIS APPROVAL

The abstract and thesis of Syed Sohel Hussain for the Master of Science in Electrical and Computer Engineering were presented November 20, 1996, and accepted by the thesis committee and the department.

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ABSTRACT

An abstract of the thesis of Syed Sohel Hussain for the Master of Science in Electrical and Computer Engineering presented November 20, 1996.

Title : Analysis and Optimization of a Banyan Based ATM Switch by Simulations

Asynchronous Transfer Mode (ATM) is proposed technology to create a broadband (high speed) packet switching network capable of transporting wide variety of services including voice, video and data in an integrated manner. The main concern in designing the switching fabrics used in this technology are speed, throughput, delay and variance of delay. We analyze the performance by simulations of ATM switch based on Banyan network in the uniform traffic condition.

We compare the analytical results obtained from three-state model Yan and Jenq [11] to the simulation results. Based on observation of simulation results, we propose non-blocking first stage (NBFS) to increase the throughput. In NBFS scheme, internal blocking in the switching element (SE) of the first stage is avoided. We extend the priority scheme proposed by Yan and Jenq by proposing enhanced priority (EP) scheme. In EP scheme, we give priority to the packet blocked greater number of times. The simulation results of the switch with combined NBFS and EP scheme, shows that the throughput increases, and the variance of delay decreases significantly.

We simulated the single buffer Banyan network with mixed voice and data traffic. We propose double buffer switching element to increase the throughput, and decrease delay and variance of delay, of delay sensitive voice packet in mixed traffic condition. The simulation results of fully loaded 6-stage double buffer switching network, with 30% voice traffic, shows that the throughput increases by 23.7%, and delay and variance of delay of voice packets decrease by 12%.

ANALYSIS AND OPTIMIZATION OF A BANYAN BASED ATM SWITCH BY SIMULATIONS

by

SYED SOHEL HUSSAIN

A thesis submitted in partial fulfillment of the

requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL AND COMPUTER ENGINEERING

Portland State University

1997

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Chapter 1

Introduction

1.1 Brief introduction of ATM

During the 1960s, the packet switching was developed mainly for data communications. The idea behind the packet switching network was to create a network of dedicated leased lines whose sole function was to transport digital data traffic. At the source, data is divided into group of bits called packets. The packet consist of two parts. The first part is the header field, which is a group of bits containing information such as a packet's destination, origination, priority and error codes. The second part is the actual information field. In the packet switching systems algorithms running in the switching nodes reads the packet destination address, and route the packet over the next successive link on its way to its destination. A great advantage of packet switching is its inherent statistical multiplexing [14] that is, a line is shared by data traffic between many users. The statistical multiplexing is an improvement over time division multiplexing. Statistical multiplexing allows inherently bursty data traffic to be combined into aggregate flow that can be accommodated economically by the leased line connections.

Asynchronous Transfer Mode (ATM) is proposed technology to create a broadband (high-speed) packet switching network capable of transporting a wide variety of services in an integrated manner. This services would include voice, data,

and video communications. An advantage of having all services treated in an integrated manner (single traffic class) is that the network resources can be dynamically assigned by statistical multiplexing. The traffic rate depends on packet arrival rates (which can be agreed upon), and the unused bandwidth can be used by other services. Thus the network resources are used more efficiently. This makes the switches independent of service, and the main concern in their design is to increase throughput and decrease delay for a given bandwidth. The great advantage of ATM technology is its economic advantage. It is hard and sometimes impossible to predict accurately the future demand for new services. It is hard to justify economically a technology that involves separate investments for specific service classes. ATM , on the other hand can be justified on the basis of total traffic load [13]. New services can simply use the same switching and transmission equipment that carries the current traffic. This considerably reduces planning uncertainty, an important problem considering the large investment involved.

The International Telecommunications Union-Telecommunications standardization sector (ITU-T) formally called International Telegraph and Telephone Consultative Committee (CCITT) is involved in standardizing the various specification for ATM. The primary unit in the ATM is a cell. ATM standard defined a fixed size cell with the length of 53 bytes comprised of 5-byte header and 48 byte payload as shown in the figure 1.1. The Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI) identify the destination of the cell. The Generic Flow Control

(GFC) field allows a multiplexer to control the rate of a ATM terminal. The Payload Type (PT) indicates whether the cell contains user data, signaling data, or maintenance information. The Cell Loss Priority (CLP) bit indicates the relative priority of the cells. The Header Error Check (HEC) is used for detection and correction of errors in the header.

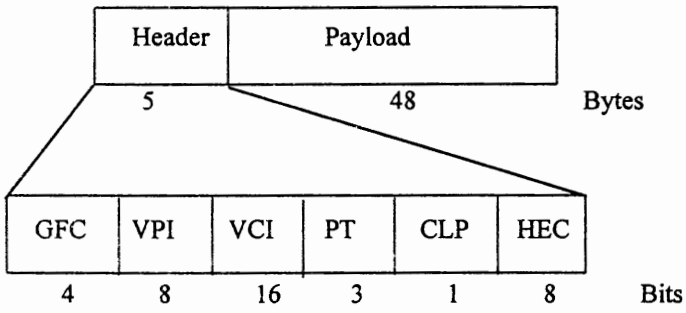

Figure 1.1 ATM cell format

1.2 Brief description of four layer ATM model

ATM is a four-layered model technology [15]. The model defines how different types of traffic can be transmitted on a single switching network. The four layer model is shown in figure 1.2. At the top of the ATM model, the user layer establishes the link between whatever device is generating the traffic (router, hub, PBX, or even an ATM workstation). The adaptation layer takes care of formatting traffic into cells. The adaptation layer actually comprises two sublayers convergence,

and segmentation and reassembly. The first combines different type of data into single stream and makes sure that each type receives the level of service it requires. Voice for instance is very sensitive to delay on the network, the variation of delay of voice traffic should be kept under acceptable limits. The segmentation and reassembly layers (as its name suggest) divides the incoming stream into 48-bytes cells for transmission over the network or reassembles the cells after receiving for presentation to the receiver.

The ATM layer is responsible to adding the 5-byte header to each cell. It also determines the path the cell will take between switches and adds that information to the header. Further, the ATM layer takes care of error correction. In order to hold down the processing overhead at the switching nodes, error correction is only performed on the header, whereas most packet switching networks use error correction on the entire message. ATM switches can then be more faster, but data error will not be discovered until the destination is reached.

The bottom layer, physical transport, includes the interface to the physical medium, which is generally fiber optic cable. ATM's wide area roots can be seen in the fact that it was originally designed to work with Sonet (Synchronous Optical network) which allows data to be transferred from 51Mbits/sec to 2.4Gbits/sec. Since Sonet is not yet widely implemented, ATM has been extended to work with T1(1.544Mbits/s) and T3(45 Mbits/s).

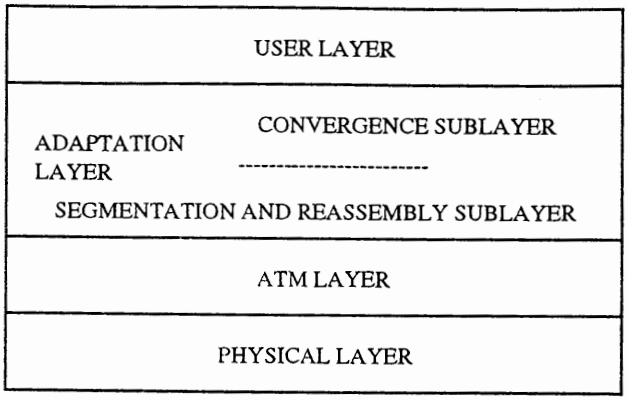

Figure 1.2 Four layer ATM technology model

1.3 ATM Switches

In the ATM layer of the ATM network is the switching fabric. Switching fabrics are patterned collections of simple switching building blocks that serve to move cells on their way to ultimate destination. The switching functions in the packet switching networks to carry data communications traffic are typically performed by means of software processing on a set of special purpose processors. The capabilities of these packet switches are very attractive for applications requiring low throughput and low delay such as inquiry/response data traffic, and those requiring high throughput, but which can tolerate higher delays such as data file transfer. However these capabilities are not sufficient for real-time ATM traffic such as voice, video or

the computer-to-computer data transfer. All the current approaches of high performance switching fabrics employ a high degree of parallelism, distributed control and routing function is performed at the hardware level. The switching fabrics are broadly classified into two categories.

1.3.1 Nonblocking switch

This switch is also known as Time Division Switch. All cells flow across a single communication highway shared by all input and output ports. This communication highway may be either a shared medium or a shared memory [4] [16]. Knock out switch [12] is an example of this type of switch. The basic structure of knock out switch is shown in figure 1.3. Each output port has a bus interface which can receive packets from each input bus line or the input port. The output port bus interface is used to resolve the output port contention. In figure 1.3, one of the output buses is shown in more detail. It has three major component. The first component is the set of N packet filters, each interfacing a bus line. The packet filters, which implement the bus routing function, detect the address of each packet on the broadcast bus and pass those destined to that on to the next component which is the concentrator. The concentrator uses an algorithm to select a fixed number of packets, say L, from the N incoming lines to the concentrator. The L selected packet are stored in their order of arrival into a shared buffer which constitutes the third component. The main philosophy behind the N to L concentration mechanism is to keep the probability of

loss minimum due to output congestion. For $N = 64$ and $L = 8$, a packet loss rate of less than 10^{-6} can be achieved. This results hold under the assumption of uniform traffic patterns. If the traffic pattern is nonuniform, L has to be higher for the same packet loss rate, depending on the nonuniformity of traffic.

Multicasting is easier in this type of network, as each input is broadcasting to every output. The blocking level and latency is low, complexity is medium, and scalability is limited in this type of architecture [13]. The speed of the network is lower as each input link is connected to all the output ports [13] [16]. Among the commercial ATM LAN vendors, switches based on TDM shared medium are Adaptive Corp.'s ATMX switch, FORE Systems's ASX-200 switch, Newbridge Networks' VIVID switch and others.

1.3.2 Blocking switch

The switch is also known as space division switch. "Blocking" occurs in the switching fabric because the switch is designed such that not every output may always be immediately accessible by every input. In spite of blocking phenomena and high complexity, these switches are more efficient in terms of scalability and speed [13] [16]. Banyan switching network falls in this category. These switches does not support multicast well and require a separate copy network. The latency of the switch is higher than non-blocking switch. Commercial ATM LAN switches based on space division are the HSS switch from ALCATEL Data Networks, LattisCell switch from Bay

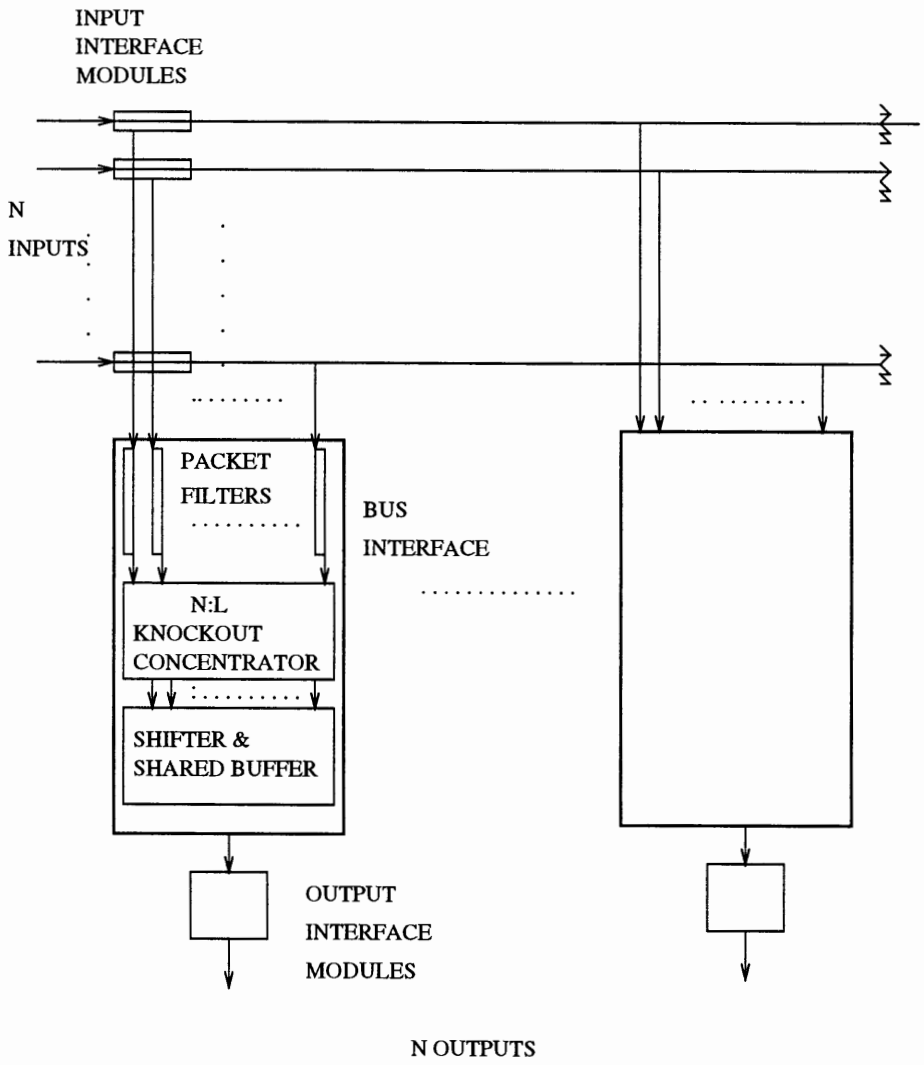

Figure 1.3 Basic structure of Knockout switch

Networks and others. The architecture, operation and performance of the switch is discussed in this thesis.

As an engineer we would like to predict the performance of given switching fabric without actually first having to build it. This prediction is referred to as performance analysis. In order to accomplish it, the performance analyst has two approaches. One approach is discrete event simulation. The other approach is to make use of statistical models of switch behavior to determine such essential performance measures as throughput, time delay. In this thesis we choose to obtain the performance analysis from simulations.

1.4 Overview of the thesis

We study the performance analysis of single buffer Banyan fabric by simulation method. Although simulation method can be used to obtain performance of switching fabric in realistic ATM network traffic condition, we concentrate on analysis of switch under uniform traffic pattern.

In chapter II we describe the functioning of single buffer Banyan switch. In chapter III we discuss simulation method. In chapter IV we compare simulation results to analytical results obtained by Yan and Jenq [11]. In chapter V we increase throughput, decrease delay and variance of delay by implementing non-blocking first stage and enhanced priority schemes. In chapter VI we present the performance of switch with mixed voice and data traffic, where priority is given to voice traffic. In

chapter VII we present the performance of double buffer switching network with two buffers on each link of switching elements. Conclusions are given in chapter VIII.

Chapter 2

Single buffer Banyan network

2.1 Structure and operation of single buffer Banyan network

The Banyan network were originally defined by Goke and Lipovski[1]. Banyan switching fabric has advantages of simplicity in hardware, speed, easy VLSI implementation and easiness of routing [3] [7]. The principal characteristics of this network are:

1.They consist of $\log_b N$ stages and N/b nodes per stage.

2.They have the self routing property for packet movement from any input to any output by using a unique k digit, base b destination address.

3.They can be constructed in a modular way from smaller subswitches.

4.They can be operated in synchronous or asynchronous mode.

5.There regularity and interconnection pattern are very attractive for VLSI implementation.

The 4-stage single buffer Banyan network is shown in Fig. 2.2. We study the performance of the network for base b = 2. Each switching element (box) is a 2x2 cross bar switch with one buffer on each input link. The buffer serves as storage element for packets during routing. The 2x2 switching element (SE) is shown in figure 2.1. A header is attached to each ATM cell for routing packets through switching network to designated output link of switching fabric. The header contains the value of

particular output link of switching fabric to which the cell is destined. The header with ATM cell constitutes a packet in switching fabric. '0' and '1' bit in the value of header is used to route the packet to the upper and the lower output link of SE respectively. The succeeding switching elements will route the packet until it reaches the destination output port.

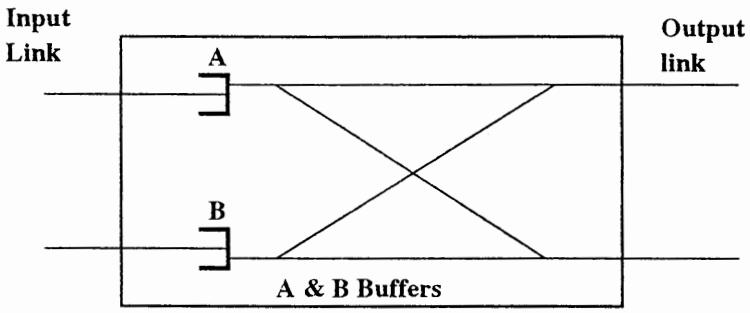

Figure 2.1 Single buffer switching element

In order for the packet to be able to move forward, either the buffer at the next stage is empty or there is a packet in the buffer and that packet is able to move forward. If the buffer at following stage is occupied by packet, the packet in succeeding stage is blocked, this blocking is known as *external blocking*. *Internal blocking* occurs when both packets in buffers are going to the same output link of SE. In this case one packet will move to next stage and the other is blocked. The switching fabric operates synchronously. In first part of the clock cycle control signals are passed from the following stage to the succeeding stage, so that every port of the succeeding

stage can determine whether to send or hold its packet. In the next part of clock cycle packets advance to following stage.

2.2 Definition of different parameters

The parameters studied in performance analysis of single buffer Banyan switching fabric are normalized throughput, normalized delay, normalized standard deviation of delay and probability of packet loss. The parameters are studied under the *uniform traffic model* i.e. the following is assumed.

- Packets are generated at each input port with equal probability.
- Packets are directed uniformly over all of the network outputs.

Normalized throughput is defined as the number of packets arriving at an output link per clock cycle. *Normalized delay* is defined as the average delay experienced by a packet at a switching element of the switching network. The variance of delay is the average of square deviations from the mean delay. The *Normalized standard deviation of delay* is the square root of the variance of delay experienced by a packet at a switching element of the switching fabric. When the buffer at the input stage is occupied by packet, the new incoming packet will be lost. *The probability of packet loss* for the switching fabric is defined as the ratio of total packets lost to the total number of packets arriving at switching fabric. However, in ATM network nodes large buffers precede the switching fabric to avoid the loss of packet.

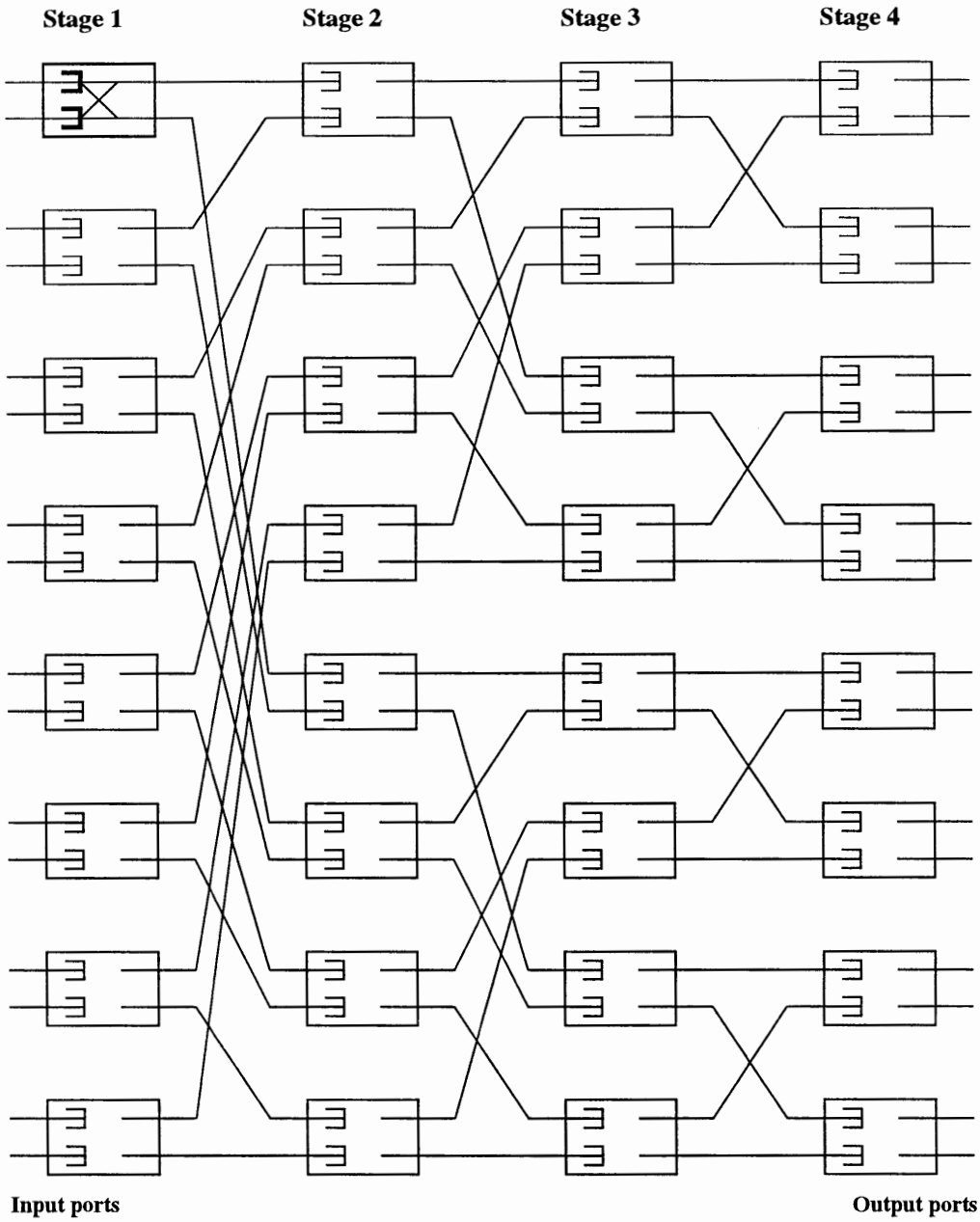

Figure 2.2 16 x 16 Banyan switch fabric

2.3 Review of related work :

The performance of Banyan network is extensively studied in last decade. Patel [2] analyzed the performance of unbuffered Banyan network under uniform traffic pattern, and provided a recursive algorithm for throughput of switching network. Jenq [3] extended Patel's work by analyzing the performance of the single buffered Banyan network under uniform traffic. In Jenq's research a simple analytical model is presented in recursive form, to analyze throughput and delay of a single buffered Banyan network that consists of 2x2 crossbar switching elements (SE). Yoon, et. al. [5] extended Jenq's model by analyzing the multibuffered Banyan network consisting of SEs with arbitrary size. Wu [6] and Kim [8] studied the performance of buffered Banyan network under non-uniform traffic conditions. Hui and Edwards [7] studied the performance of switch with the Batcher sorting network followed by a Banyan network. The Batcher sorting network sorts packets such that internal blocking in Banyan network does not occur. Ta and Meditch [9] improved the performance of the Banyan network by employing 4x4 switching blocks over 2x2 switching elements. Tridandapani and Meditch [10] analyzed the single buffer Banyan network with dilations and replications to enhance throughput. They also analyzed the delay of various types of traffic passing through the switch by assigning priorities to packets.

Jenq [3] obtained the performance of single buffer Banyan switch by analytical method assuming that load on all switching elements (SE) in switching fabric is uniformly distributed. He used "two state" Markov chain model to obtain the

throughput and delay of the switching network. He assumed that the blocked packet will generate a new random output destination port in the next clock cycle. In recent study by analytical method, "three-state" model and priority scheme is proposed by Yan and Jenq [11]. In this model they recognized that the blocked packet will not generate a new random destination in next clock cycle, instead the designated output port of blocked packet will remain the same after the packet is blocked. The three-state model results are closer to simulation results. In *the priority scheme* the packet blocked in previous clock cycle in a SE has priority to advance in next clock cycle. The priority scheme can be used to significantly reduce the variance of delay for delay sensitive traffic such as voice and video.

Chapter 3

Description of the simulation method

In this chapter we describe the simulation method used to study the parameters defined in last section. The simulation program code is written in ANSI C programming Language. The user defines number of input ports to the switching fabric *n*, and the number of stages *b* at the beginning of program.

To realize switching fabric in simulation program the packet is conceptualize as the structure. The structure is named as *atm-packet*. The structure atm-packet is defined as a global variable. The structure of atm-packet in C program is shown below.

```
struct atm-packet
{
int pac_num;
int dest_add;
int inp_arr;
char pac_type;
int blo[b];
}
```

The value in integer variable *pac_num* shows the packet number to identify the packet. The integer variable *dest_add* has the value of the particular output link of switching fabric to which the packet is destined. The integer variable *inp_arr* indicates the value

of particular input port the packet is generated. The character variable *pac_type* shows the type of traffic in the packet, 'v' denotes voice traffic and 'd' denotes data traffic. The array of integers named *blo[b]* counts number of times the packet is blocked at each stage. The size of array is equal to number of stages *b*. The structure *nopac* is similar to structure *atm-packet*, except that all its members are initialized to zero. The pointer to the structure *nopac* is named as *pxx*. *Pxx* is used to indicate empty buffer of SE.

We conceptualize the stage of switching fabric as the array of pointers to structure packet. The number of such arrays are equal to number of stages in switching fabric, hence each buffer of a stage corresponds to an element of array. In the buffer of switching fabric a packet may be present or buffer is empty, i.e., there is no packet in the buffer. In case there is no packet in the buffer, the corresponding element of array has the value of *pxx*. In case the buffer is occupied by a packet, the corresponding element of an array holds the pointer to structure *atm-packet*. When packet advances to next stage, the value in the element of array is changed to *pxx*. The value in the element of array will be *pxx* until a new pointer to *atm-packet* moves into the element in next clock cycles. The array of pointers to structure *atm-packet* called *out[n]* is used to save packets that arrive at output ports. In each clock cycle desired data from structures *atm-packet* is collected before discarding them from this array.

We declare an array of structures called *pac* of size *[nx(b+1)]*. Each element of the array is a structure *atm-packet*. The content of *atm-packet* reside in the array as

long as pointer to *atm-packet* is in switching fabric. When the pointer to *atm-packet* arrives at array *out*, the contents of structure *atm-packet* are nullified. The array of pointer to structure *atm-packet* named *pac_add* of size *[nx(b+1)]* holds pointers that are not present in switching fabric. Any element that does not hold the pointer to packet has the value of *pxx*. When a pointer to *atm-packet* arrive at array *out*, it is recorded in this array. When a new packet is generated at input port, the top most pointer to in this array will be the address of new packet.

The array *c_inp[n]* shows total number of packets destined to each output link of switching fabric from input side. The size of array is *n*. The value in the i^{th} element of array shows total number of packets destined to the i^{th} output link of the switching fabric. The array *c_out[n]* shows total number of packets arrived at each output link of switching fabric. The array has *n* elements. The value in the i^{th} element of array shows total number of packets arrived at the i^{th} output link of switching fabric. The arrays *c_inp* and *c_out* are used to verify that all packets routed in switch have reached the designated output port. The values in elements of array *c_out* are used to calculate throughput of switching fabric. The array named *t_bloc[10xb]* counts packets that are blocked. The size of array is *[10xb].* The value in i^{th} element of array is total number of packets blocked 'i' number of times. If the packet is blocked equal or more than [10xb] times, the last element ([10xb]-1) of the array is incremented by one. Before the pointer is discarded from an array *out[n],* the total number of times the packet was blocked is calculated, and the value in the respective element of array *t_bloc* is

incremented by one. The values in this array are used to calculate delay and variance of delay of switching fabric.

At the beginning of each clock cycle random numbers are generated and saved in array *ran_num*[ ]. The rand( ) function in C is used to generate random numbers. The rand() function is seeded with system time to generate a new set of random numbers each time it is invoked. The value of random number varies between zero and one. The random numbers are used for generation of packets, assigning of the destination output port of switching fabric for packets, and in determination of type of traffic in packets. Every time a random number is accessed a new random number is obtained from next element of array *ran_num*. A new packet is generated at an input link, if the accessed random number is less than or equal to input load. The *input load* is the probability of arrival of packet at an input port in each clock cycle. The generated packet is always accessed by its pointer. The address of new packet is taken from array *pac_add*. The address of the packet is address of element of array *pac*, which contains contents of structure *atm_packet*. A random number is accessed and multiplied by *n*, the integer value of product of these two numbers is the output link of switching fabric to which generated packet is destined. The type of traffic in the packet is determined by comparing random number with percentage of voice traffic in input load. A voice packet is generated when accessed random number is less than or equal to percentage of voice traffic, otherwise a data packet is generated.

The packets move to array corresponding to following stage at the end of each clock cycle. The program checks for elements of array of following stages with the value of *pxx* before switching packets. In case a packet is present in element of array of following stage, the packet at succeeding stage is blocked. When internal blocking occurs we have non-priority, priority and enhanced priority schemes. Whenever a packet is blocked at a stage, the value of respective element of array *blo* is incremented by one. In *non-priority scheme* both packets at input links of the SE have same probability to move forward. The scheme is implemented in simulation program by accessing a random number, if the random number is less than or equal to 0.5, the packet at lower input link of SE is blocked, otherwise the packet at upper link is blocked. The elements of array *blo* indicates whether a packet was blocked in previous clock cycle. The packet is routed depending on bits in variable *dest-add*. '0' or '1' routes packet to upper or lower output link of the SE respectively. The most significant bit in *dest_add* is used for switching the packet at first stage and the least significant bit is used for switching packet at last stage.

Fig 3.1. shows interconnections between different stages of switching fabric. The flow chart of simulation method is shown in Fig. 3.2. In each clock cycle, the simulation program first routes pointers from elements of array for last stage (stage b), then routes pointers from elements of array at stage (b-1), and lastly from array for first stage. After packets from first stage are routed, new packets are generated, and pointers to new packets are copied in elements of an array for first stage. The program

counts total number of packets generated. In case the element of array at stage 1 is occupied by packet, the newly generated packet is lost. The program counts total number of packets lost. In each clock cycle, the values in elements of array *t_bloc* and *c_out* are updated before discarding pointers from array *out*. After routing pointers in last clock cycle, all pointers remaining in arrays corresponding to different stages are routed to array *out[n].* Now the program calculates the value of normalized throughput, normalized delay, normalized standard deviation of delay and probability of packet loss. The formulas used for calculating these parameters are given below.

$$\text{Normalized throughput} = \frac{\sum_{i=0}^{n-1} c\_out[i]}{(\textit{Total number of clock cycles}) \times n}$$

$$\text{Normalized delay} = \frac{\sum_{i=0}^{(10\times b)-1} (i+b) \times t\_bloc[i]}{N \times b}$$

Normalized standard deviation of delay

$$= \frac{1}{b} \sqrt{\frac{N \sum_{i=0}^{(10\times b)-1} (i+b)^2 . t\_bloc[i] - \left(\sum_{i=0}^{(10\times b)-1} (i+b).t\_bloc[i] \right)^2}{N(N-1)}}$$

$$\text{Probability of packet loss} = \frac{\textit{Total number of packets lost}}{\textit{Total number of packets generated}}$$

where N is the total number of packets arrived at output links.

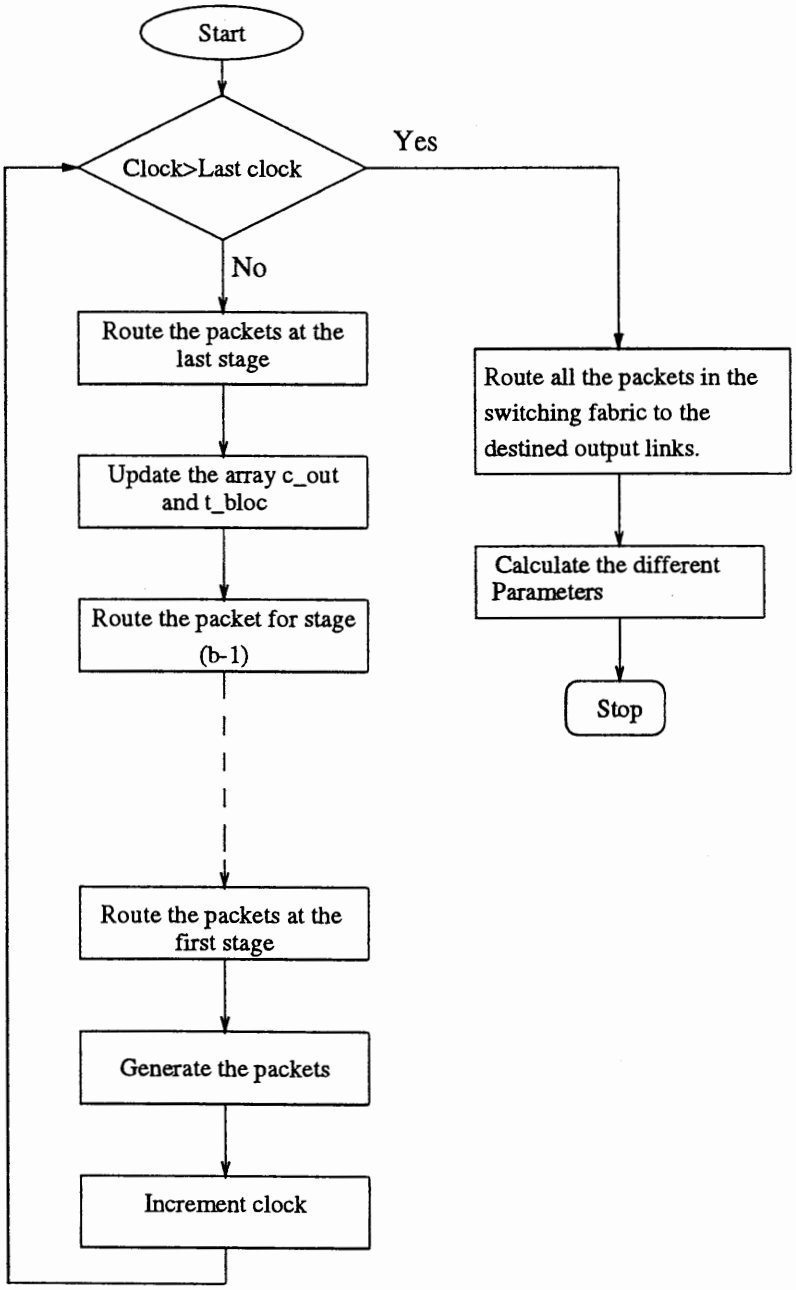

Figure 3.1 Flow chart of the simulation program.

Chapter 4

Comparison of simulation and analytical results

4.1 Introduction

All results are for simulations run for 10^5 clock cycles. We simulated switching fabrics consisting of 4, 6 and 10 stages. The results of simulation run for 10^6 clock cycles for a switching fabric consisting of four stages indicates that the change in value of normalized delay is less than 0.1%, the change in values of normalized throughput and normalized standard deviation of delay is less than 0.2% and 0.6% respectively. The difference in values of parameters obtained from simulating the switch consisting of 6 and 10 stages for 10^6 clock cycles is lesser than the difference obtained for 4-stage switch.

4.2 Comparison of simulation and three-state model results with non-priority scheme

The comparison between three-state model and simulation results with non-priority scheme is shown in figures 4.1, 4.2, and 4.3. The input load is shown on x-axis in all figures. Fig. 4.1 shows that the normalized throughput of fully loaded switching fabrics consisting of 4, 6 and 10 stages is 10% lower than three-state model. The term *fully loaded* indicates an input load of 1.0 on the switch. Fig. 4.2 shows that the normalized delay of fully loaded switching fabrics consisting of 4, 6 and 10 stages

is 2% higher than three-state model. Fig. 4.3 shows that when the switch is fully loaded, there is a difference of 30%, 38%, and 45% in the normalized standard deviation of delay of switching fabric with 4, 6 and 10 stages respectively. The variance of delay obtained from three-state model are higher. The comparison shows that the results of three-state model are optimistic except for variance of delay. At low input loads the analytical results are close to simulation results. The difference between the two results widen with the increase of input load on the switch.

4.3 Comparison of simulation results with non-priority versus priority scheme

We simulated switching fabric with priority scheme after non-priority scheme. CCITT has already recommended the use of priority bit in the ATM cell. The performance improvement in variance of delay from priority scheme versus non-priority scheme is shown in figure 4.4. Fig. 4.4 shows difference in values of normalized standard deviation of delay. When input load is 1.0 for 4, 6 and 10 stage switch the difference is 25%, 21% and 19% respectively. The three-state model [11] predicted increase in throughput by 10% for a 6-stage switch for input load equal to 1.0 with priority scheme. The simulation results confirmed significant reduction of variance of delay with priority scheme, however it did not show any major change in throughput as shown by three-state model. When input load is 1.0, there is 1% difference between results obtained from two schemes for throughput, delay and

probability of packet loss. The delay decreases while throughput increases with priority scheme.

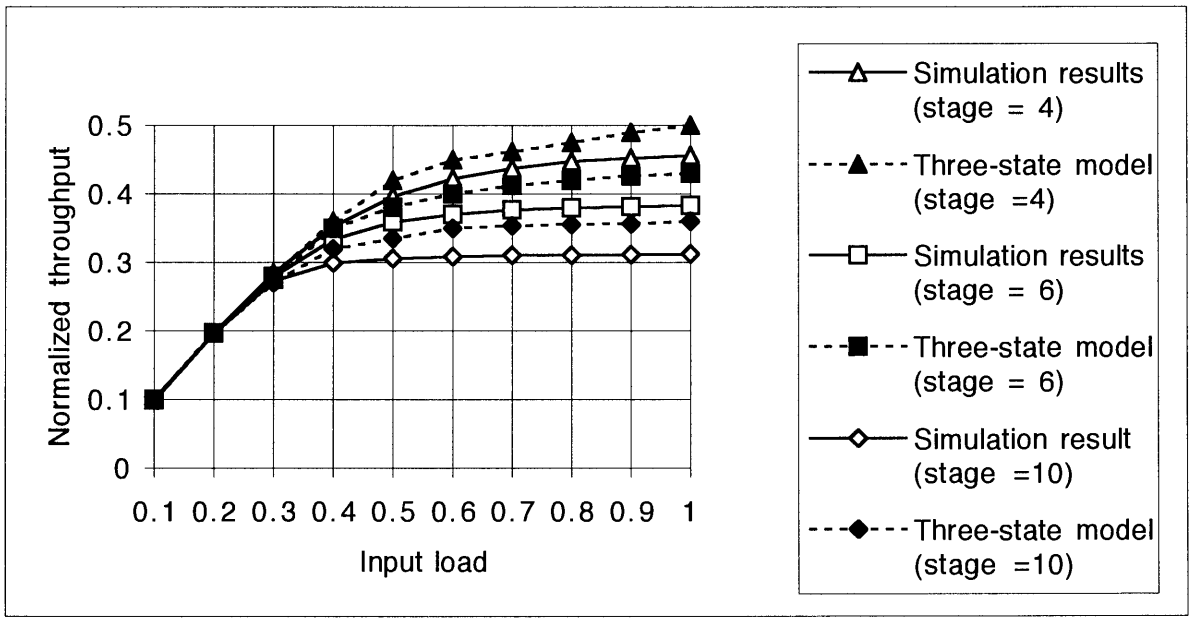

Figure 4.1 Throughput comparison with non-priority scheme

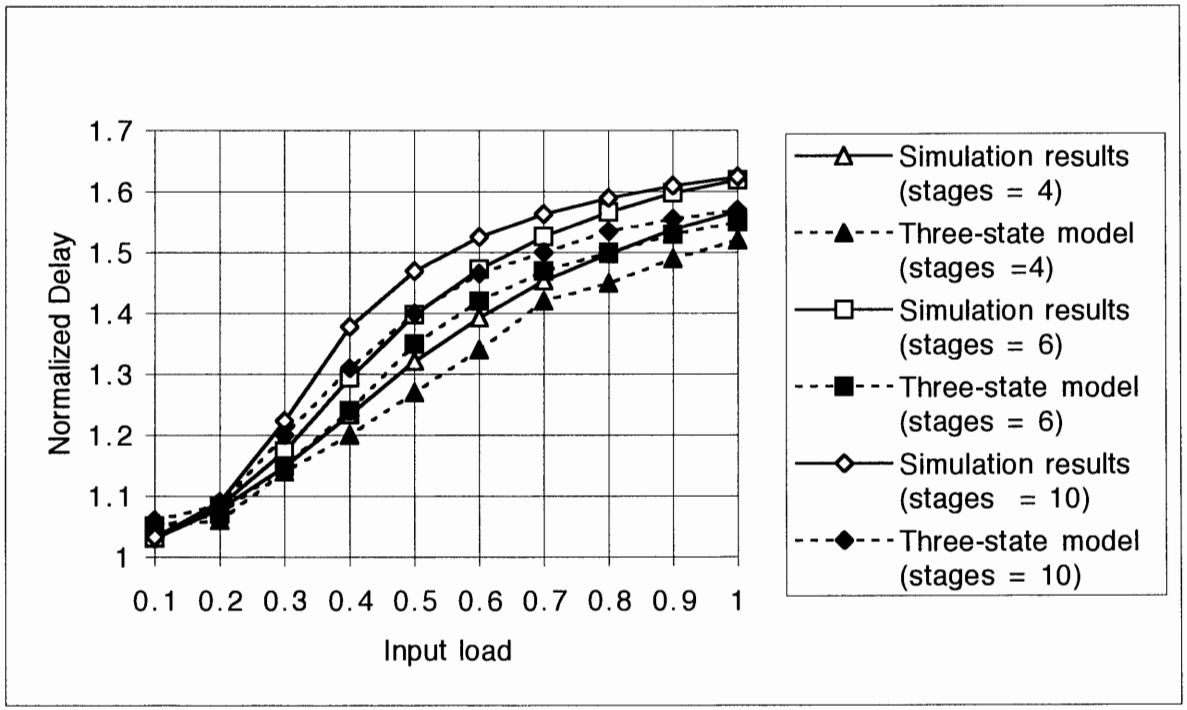

Figure 4.2 Delay comparison with non-priority scheme

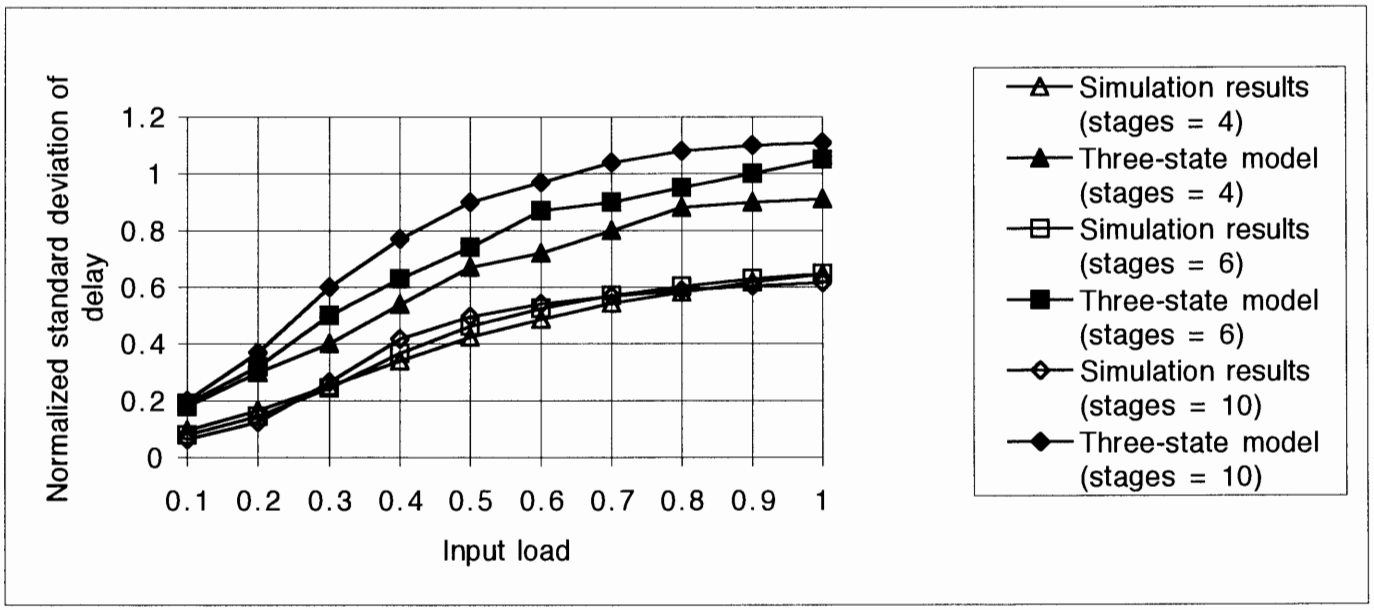

Figure 4.3 Delay variance comparison with non-priority scheme

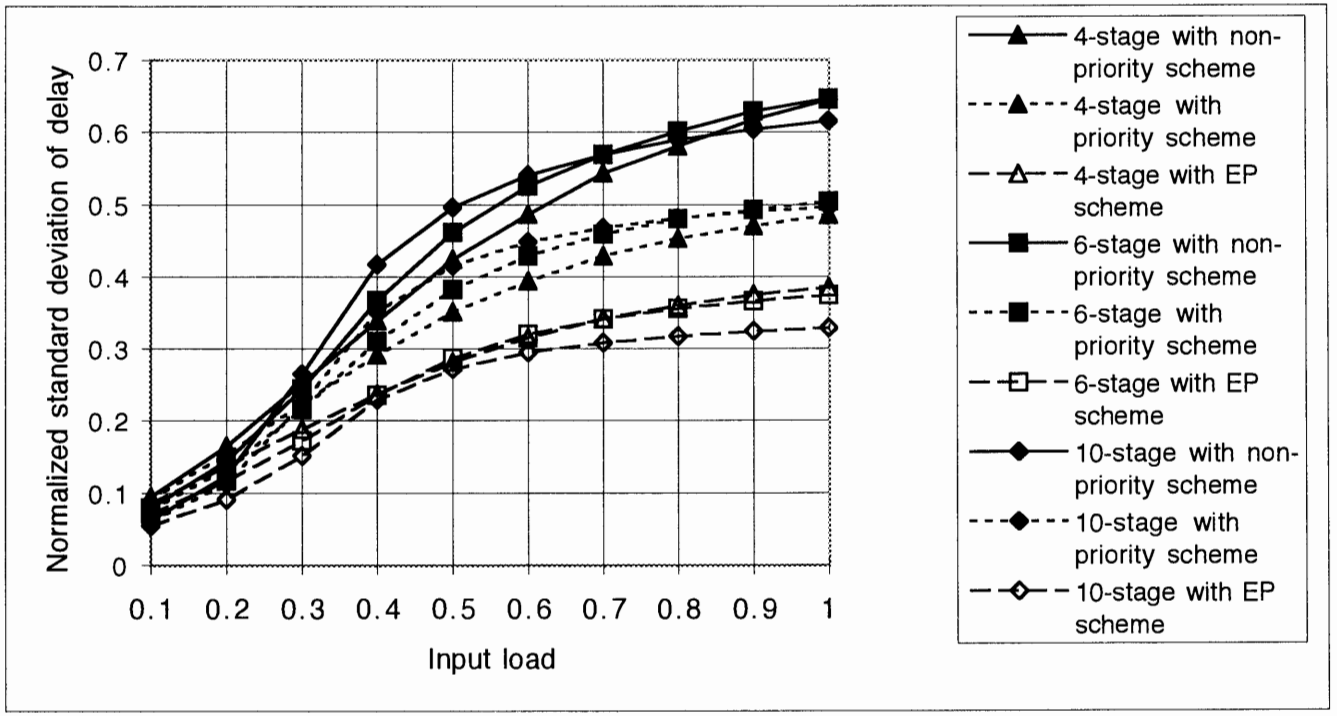

Figure 4.4 Delay variance comparison between non-priority, priority and enhanced priority scheme

Chapter 5

Modification in the switch

5.1 Enhanced priority scheme

Delay and variance of delay are important in case of delay sensitive traffic such as voice and video. We extend priority scheme proposed by Yan and Jenq [11] even further by suggesting enhanced priority scheme. In the *Enhanced priority (EP) scheme* when internal blocking occurs in the SE, priority is given to the packet blocked greater number of times. The simulation results shows that the normalized standard deviation of delay of EP scheme compared to priority scheme, for 4, 6 and 10 stage switch is lower by 20.75%, 25.79 and 33.77% respectively. This is shown in figure 4.4. The results shows that the reduction in variance of delay is higher when the switch is larger. The scheme also provides an increase in throughput by 2% for the 4-stage and 4.5% for 10-stage switch. The EP scheme can be useful in minimizing the variance of delay in the case of non-uniform traffic condition. The EP scheme increases the complexity of SE. The circuitry dedicated to work for EP scheme has to be implemented in SE. Also in the header of the packet, provision for recording number of times the packet was blocked has to be provided. The circuit to increment number of times the packet is blocked has to be implemented in SE.

5.2 Non-blocking first stage (NBFS) switch

In this section we propose a new scheme to improve throughput based on some simulation observations. We define a new term called degree of blocking at a stage of the switch to estimate blocking at each stage of switching fabric. *The degree of blocking at a stage* is defined as the ratio of total number of blockings occurring at a particular stage to total number of packets passing through a stage of the switching fabric. Fig. 5.1 shows the degree of blocking at different stages in the 6-stage switch with priority scheme. The input load is shown on abscissa. The slope of the degree of blocking for first stage increases sharply compared to other stages, when input load is increased above 0.4. When the switch is fully loaded the degree of blocking at stage 1, stage 2 and stage 3 is 1.57, 0.87, and 0.54 respectively. The degree of blocking for stage 1 is almost double that of stage 2. The results shows that the total number of blocking occurring in the first stage are more than the total number of packets passing through the first stage. In the first stage it is easier to avoid internal blocking by routing packets on two different input links of SE just by checking the most significant bit of the header of packet. We call the switching fabric with such an arrangement as a non-blocking first stage (NBFS) switching fabric. The NBFS scheme reduces degree of blocking significantly for first stage, this will allow lesser packets to be dropped, hence results in increase in throughput of the switch. In simulation the scheme is implemented by routing the packet with '0' in the most significant bit of header on the

upper input link of the SE and '1' in the most significant bit on the lower input link of SE. The result shows that the normalized throughput of fully loaded switches with NBFS scheme consisting of 4, 6 and 10 stages increases by 12.14%, 7.06% and 3.95% respectively.

5.3 Switch with NBFS and EP scheme

We simulated switching fabric combining NBFS scheme and EP scheme. Fig. 5.2, 5.3, 5.4 and 5.5 demonstrate difference in throughput, delay, variance of delay and probability of packet loss between this switching fabric and a normal switching fabric with priority scheme. Fig. 5.2 shows that the normalized throughput of the switching fabric consisting of 4, 6 and 10 stages increases by 11.53%, 8.56% and 6.94% respectively. Fig. 5.3 shows that the normalized delay of switching fabric consisting of 4, 6 and 10 stages increases by 3.08%, 6.35% and 8.27% respectively. Fig. 5.4 shows that the normalized standard deviation of delay for 4, 6 and 10 stage switch decreases by 23.88%, 25%, and 29.42% respectively. Fig. 5.5 shows that the probability of packet loss of switching network consisting of 4, 6 and 10 stage decreases by 11.62%, 6% and 3.58% respectively.

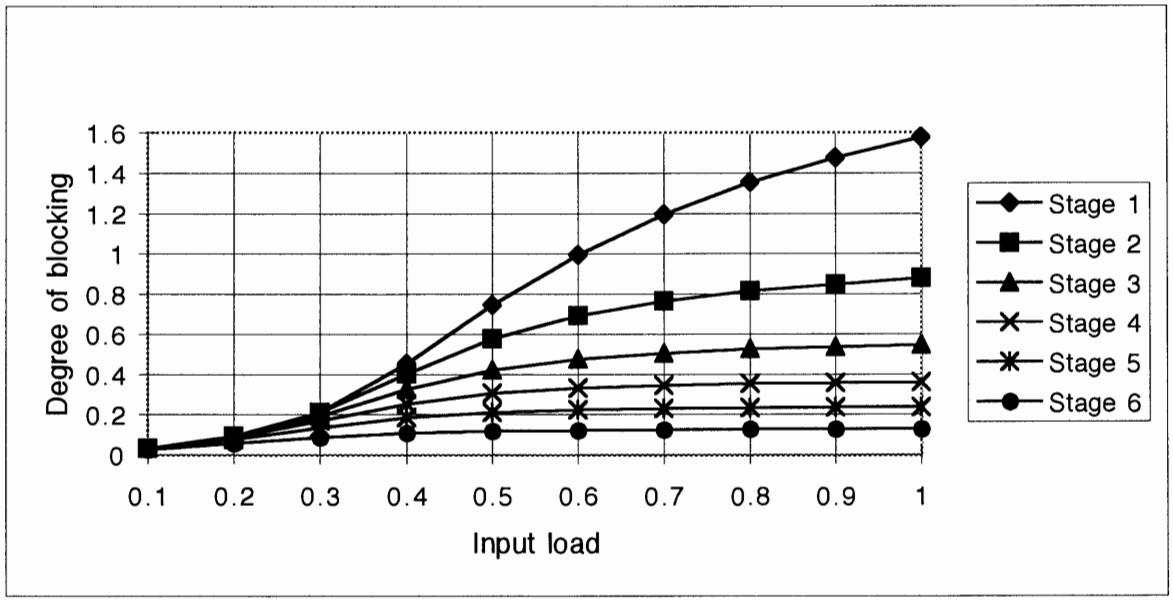

Figure 5.1 Degree of blocking of different stages for 6-stage switch with priority scheme

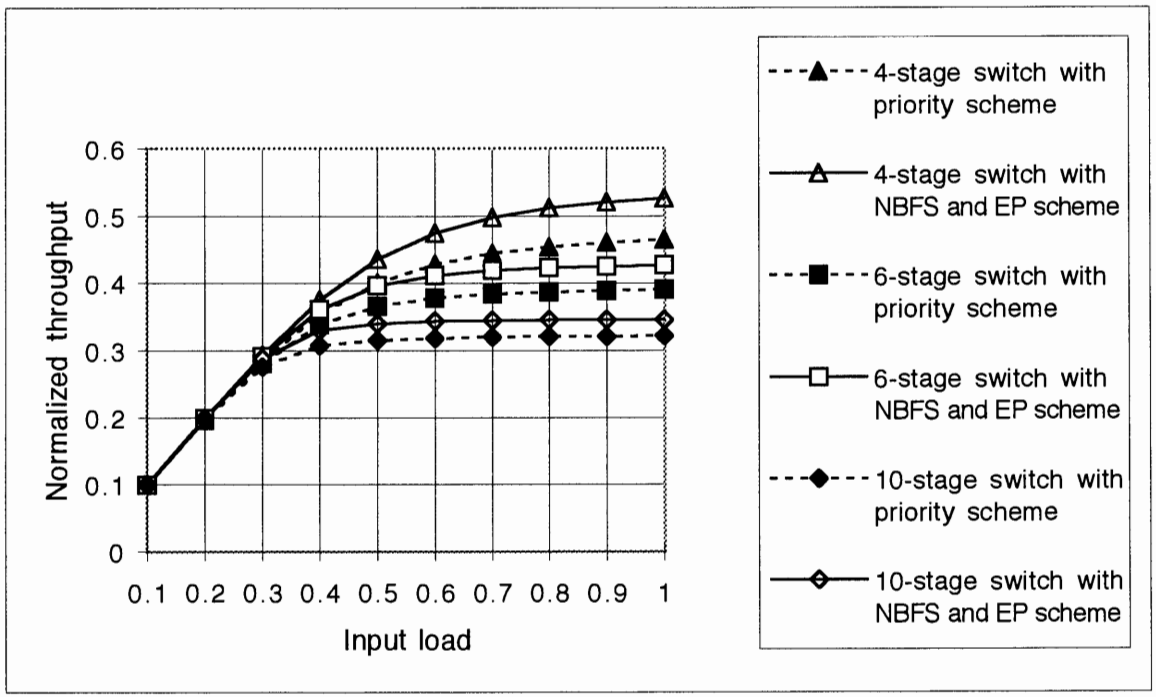

Figure 5.2 Throughput comparison between priority scheme and combined NBFS and EP scheme

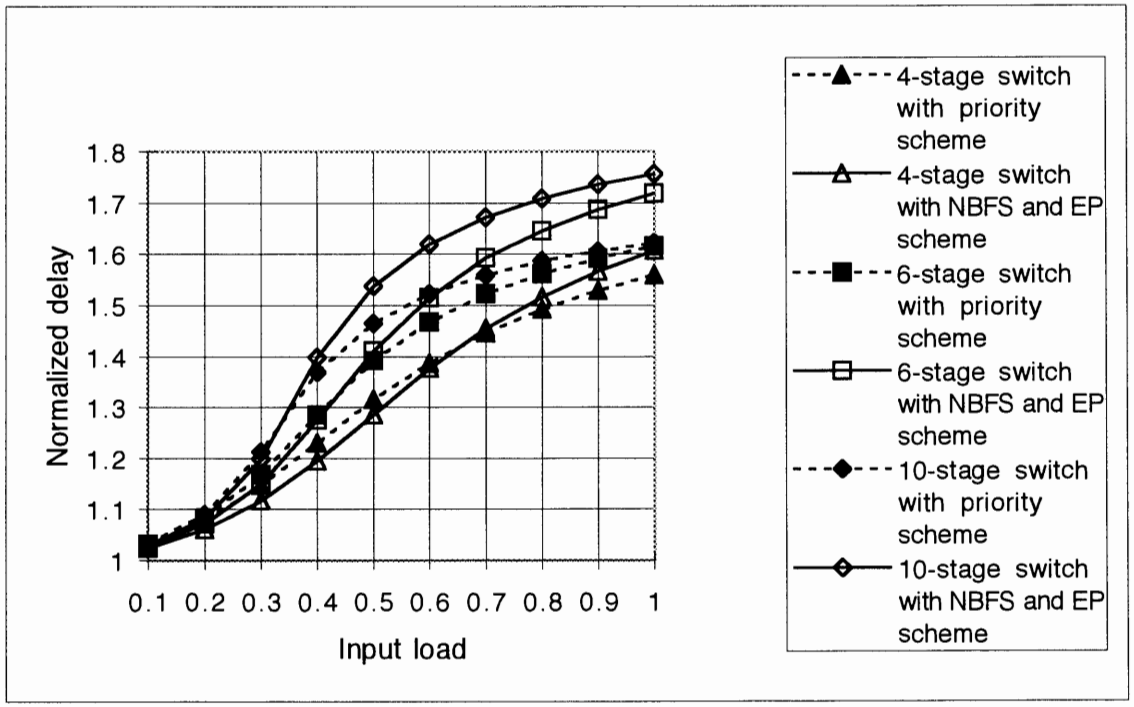

Figure 5.3 Delay comparison between priority scheme and combined NBFS and EP scheme

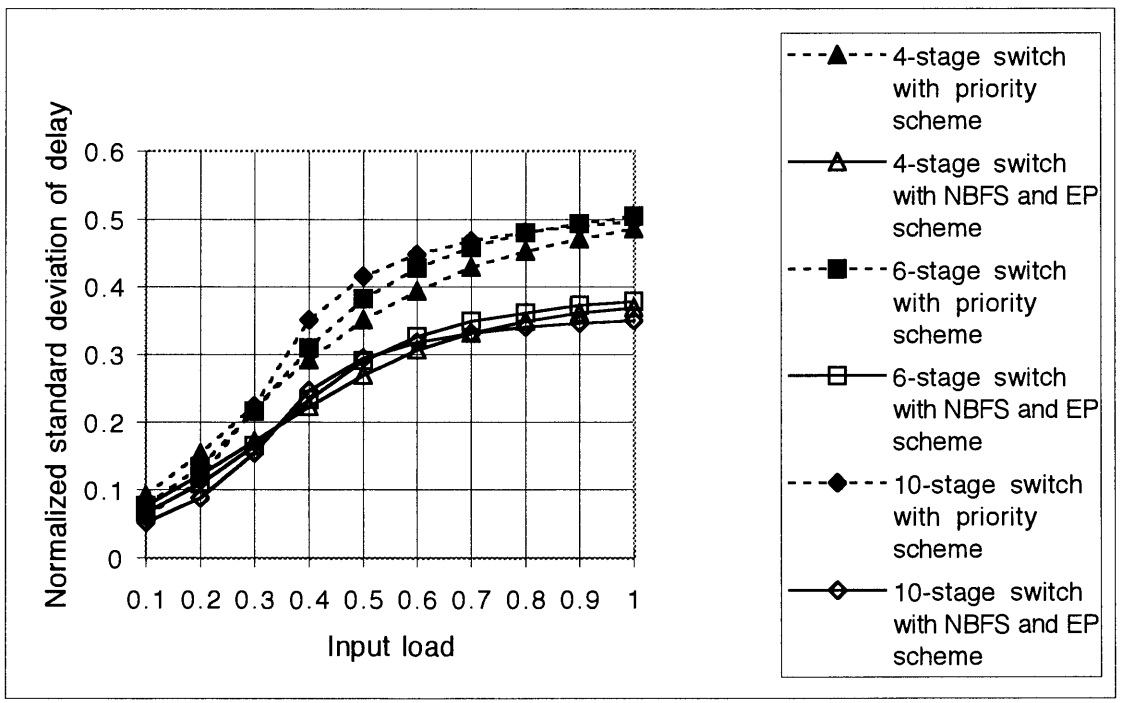

Figure 5.4 Delay variance comparison between priority scheme and combined NBFS and EP scheme

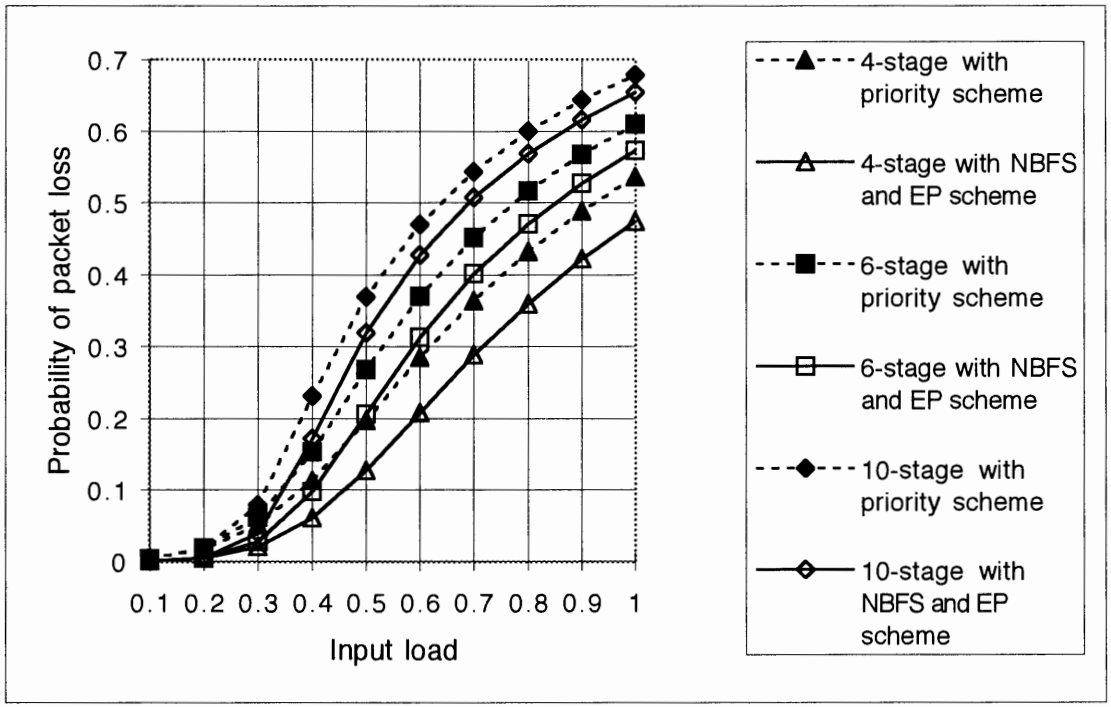

Figure 5.5 Comparison of Probability of packet loss between priority scheme and combined NBFS and EP scheme

Chapter 6

Simulation results of the switch with mixed voice and data traffic

6.1 Delay with mixed voice and data traffic

Different types of traffics will be passing through switch as the purpose of ATM network is to support multimedia traffic on a single network. We simulated the 4 and 6-stage switch with NBFS, EP scheme and mixed voice and data traffic. In case of internal blocking in the SE between a voice packet and data packet, voice packet has priority to advance to next stage as it is more sensitive to delay. When internal blocking occurs due to same type of packet, the packet blocked greater number of times has priority to advance to next stage. The results shows that the throughput of switch remains almost the same, delay and variance of delay depends on the type of traffic. When simulating the switch with mixed traffic, the variables are input load and percentage of voice traffic. The *percentage of voice traffic* is the ratio of voice traffic in input load of the switching fabric. The percentage of voice traffic is shown on abscissa in figures. The performance for different input loads is shown by the different curves in figures. Fig. 6.1 and 6.2 shows normalized delay of voice and data traffic. As expected slope of curve for normalized delay of voice traffic is less than slope of curve for normalized delay of data traffic for given input load. The slope of curve for normalized delay increases with increase of input load and percentage of voice traffic. When input load is 0.4 and percentage of the voice traffic is varied from 10% to 90%,

the normalized delay of voice packet changes from 1.14 to 1.26, the normalized delay of data packet increases from 1.29 to 1.47.

6.2 Delay variance with mixed voice and data traffic

Fig. 7.3 and 7.4 shows the normalized standard deviation of delay of voice and data traffic. When input load is 0.4 and percentage of voice traffic varies from 10% to 90%, normalized standard deviation of delay of voice traffic increases from 0.20 to 0.24, normalized standard deviation of delay of data traffic increases from 0.25 to 0.44. The variance of delay of voice traffic has some interesting behavior. It increases with increase in percentage of voice traffic for input load from 0 - 0.3, whereas for input load of more than 0.4, it is maximum when percentage of voice traffic equals 80%. This is shown in Fig. 7.3. The reason for this behavior can be explained as follows: When the input load is high and priority is given to voice packet, the data packets are more likely to be blocked. The blocking of each data packet causes external blocking of packets in succeeding stages resulting in increase of delay variance of voice and data traffic. However, When the voice traffic is increased above 80%, the data traffic decreases below 20%, there is less external blocking of voice packets due to blocked data packets, hence the variance of delay of voice traffic decreases.

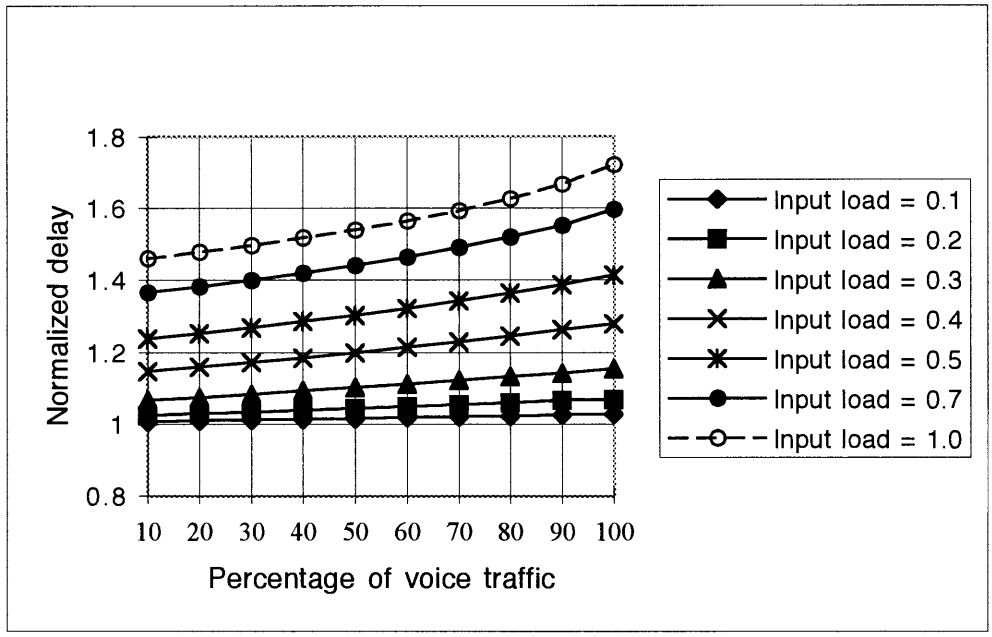

Figure 6.1 Delay of voice traffic for 6-stage switch

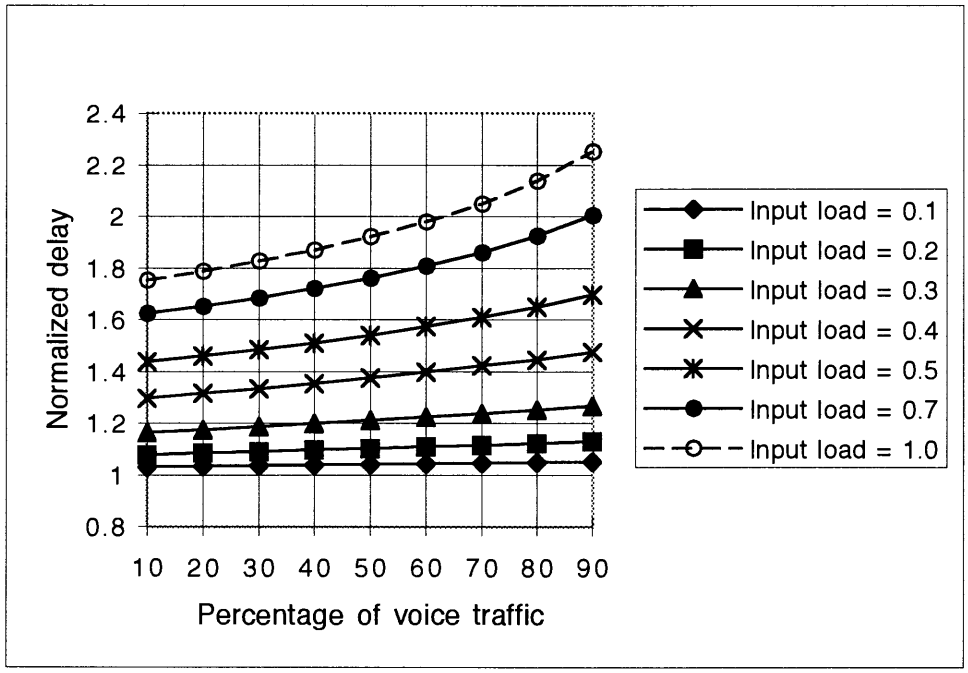

Figure 6.2 Delay of data traffic for 6-stage switch

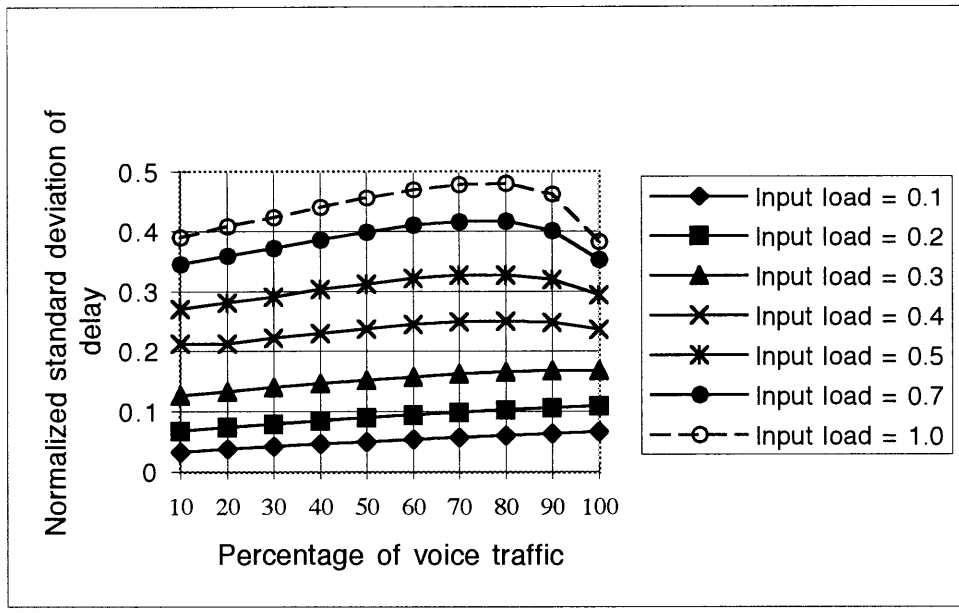

Figure 6.3 Variance of delay of voice traffic for 6-stage switch

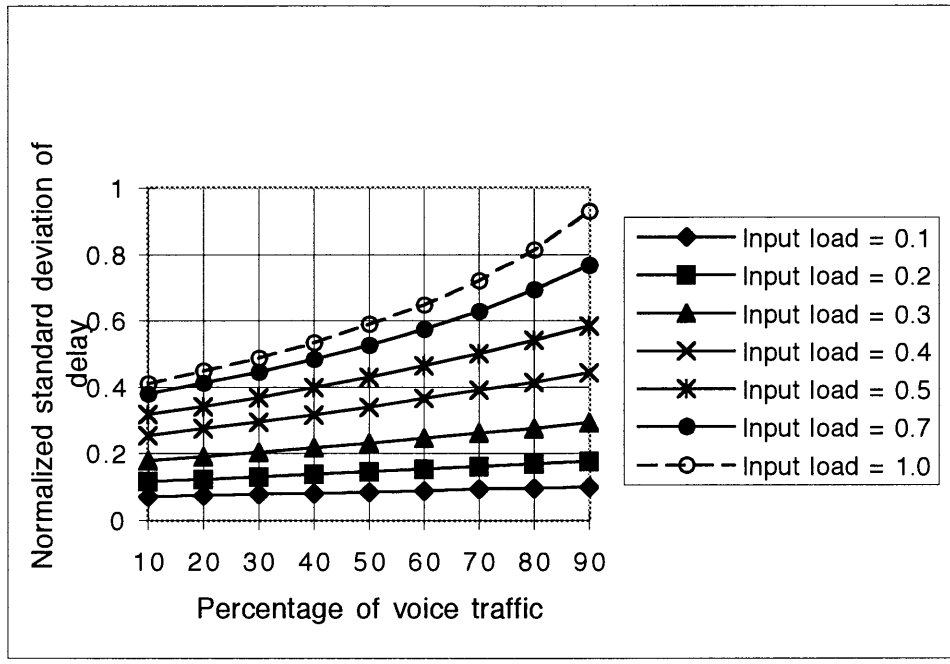

Figure 6.4 Variance of delay of data traffic for 6-stage switch

Chapter 7

Double buffer switching element

7.1 Introduction

We found that the normalized throughput of fully loaded switch with NBFS and EP scheme consisting of 4, 6 and 10 stages is 0.52, 0.42,and 0.34 respectively. In the last chapter we found that, the normalized delay and normalized standard deviation of delay of voice traffic for the fully loaded 6-stage switch, with NBFS and EP scheme, and 10% voice traffic is 1.45, and 0.38 respectively. In order to use the Banyan network efficiently in the ATM switch, the throughput has to increase, and delay and variance of delay has to decrease. In the case of contention between voice and data packet, the data packet is blocked. The blocked data packet will cause externally blocking of the packets in the succeeding stages, this will result in increase in delay voice traffic, and lowers the throughput of network. To reduce external blocking we propose the double buffer switching element.

7.2 Double buffer switching element

Multibuffer SE [5] were proposed to enhance the throughput. Multibuffer SE consist of arbitrary number of serial buffers at each input link of the SE. The problem with the Multibuffer SE is increase in the delay which is not desirable in case of certain traffic sensitive to delay. In the double buffer SE we try to encounter this

problem. The double buffer switching element is the development on single buffer switching element. The structure of 2x2 double buffer switching element is shown in figure 7.1. Each input link of the SE is connected to two buffers through a demultiplexer. The demultiplexer has an additional function of recognizing the empty buffer, and routing the incoming packet to the empty buffer. A multiplexer is placed between buffers and the cross bar switch. The multiplexer is an "intelligent" multiplexer. The multiplexer has the additional function to give priority to a type of traffic in the enhanced priority scheme. In our simulation with voice and data traffic, voice packet is given priority over data traffic. When the packet is blocked, it has the circuit to increment the number of times a packet is blocked.

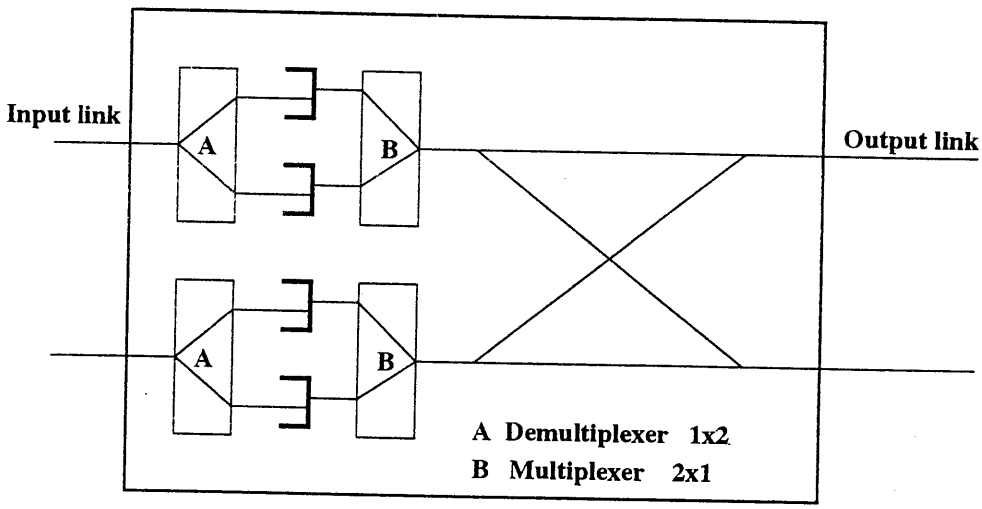

Figure 7.1 Structure of double buffer SE

7.3 Performance analysis of double buffer switching network

The structure and operation of double buffer Banyan switch is similar to single buffer Banyan switch except that the single buffer SEs are replaced with double buffer SEs. We simulated the 4, 6 and 10-stage switch, with NBFS and EP scheme for the input load of 0.1, 0.2, 0.3, 0.4, 0.5, 0.7 and 1.0. The simulation results shows significant increase in throughput, and decrease in delay and variance of delay of voice traffic at the expense of data traffic. In the following sections we compare the results of double buffer 6-stage switch to single buffer switch. Figure 7.10 shows the change in normalized delay and normalized standard deviation of delay of voice and data packet for fully loaded double buffer 6-stage switch in comparison with single buffer switch.

7.3.1 Comparison of throughput

The normalized throughput from the two networks are compared in figure 7.2. The throughput of fully loaded double buffer switch with 4, 6 and 10 stages increases by 12.5%, 23.7%, and 39.4% respectively. The throughput of fully loaded 6-stage double buffer switch is 0.52, whereas the throughput of single buffer switch is 0.42. The throughput of fully loaded 10-stage double buffer switch is 0.48, whereas that of single buffer switch is 0.34. In the figure 7.3, the percentage change in normalized throughput of double buffer switch compared to single buffer switch shown. The input load is shown on abscissa. The change in throughput is larger for bigger switches. The

graph can be divided into three regions. Considering a 6-stage switch, the change in throughput is moderate for input load less than 0.3, the change is significant for the input load between 0.3 and 0.7, the slope of the change is negative for the input load more than 0.7.

7.3.2 Comparison of delay for voice traffic

In figure 7.4 shows the normalized delay of 6-stage double buffer and single buffer switch for different input loads. The percentage of voice traffic is shown on abscissa. As anticipated the change decreases as the percentage of voice traffic increases. When the switch is fully loaded, and 30% is voice traffic, the delay decreases by 12%. When input load is raised above 0.4, at certain percentage of voice traffic the change in normalized delay turns positive. This is alarming when the input load is 0.7, the delay in double buffer network is higher than single buffer network for more than 60% of voice traffic. This condition may be avoided in the ATM switches.

7.3.3 Comparison of variance of delay of voice traffic

The variance of delay of double buffer switch decreases significantly in comparison with the single buffer switch. Figure 7.5 shows the normalized standard deviation of delay of voice traffic of 6-stage double buffer and single buffer switch for different input loads. The percentage of voice traffic is shown on abscissa. The change is maximum for the input load of 0.4. The change decreases as the percentage of voice

traffic increases. When the switch is fully loaded and 30% is voice traffic, the change is negative 15%. The variance of delay of double buffer switch is more than single buffer switch, in case the of voice traffic is more than 90%, and input load more than 0.5.

7.3.4 Comparison of delay of data traffic.

Figure 7.6 shows the normalized delay of data packet for 6-stage double buffer and single buffer switch for different input loads. When the load is less than 0.4, and percentage of voice traffic lesser than 40, the delay in double buffer is lower than single buffer. When the input load is more than 0.5, the change is positive, and it increases drastically with the increases in the percentage of voice traffic. When switch is fully loaded and 30% is voice traffic, the variance of delay of double buffer network is 68% higher than the single buffer network.

7.3.5 Comparison of variance of delay of data traffic

Figure 7.7 shows the normalized standard deviation of delay of data packets for 6-stage double buffer and single buffer switch for different input loads. When the input load is less than 0.4, and percentage of voice traffic lesser than 40, the change is negative. The change is positive for the input load more than 0.5. The variance of delay of data traffic increases drastically for input load of more than 0.5 and percentage of voice traffic in excess of 40%. When the switch is fully loaded and 30%

is voice traffic, the variance of delay of data traffic is 30% higher than the single buffer switch.

7.3.6 Comparison of probability of packet loss

Figure 7.8 shows the change in probability of packet loss for 6-stage double buffer switch in comparison with single buffer switch for different input loads. The percentage decrease in probability of packet loss of double buffer 4, 6, and 10-stage switch is 100% until the load reaches 0.4. The decrease in probability of packet loss is greater for bigger switches. When the switch is fully loaded, the probability of packet loss of double buffer 6-stage switch is reduced by 20%.

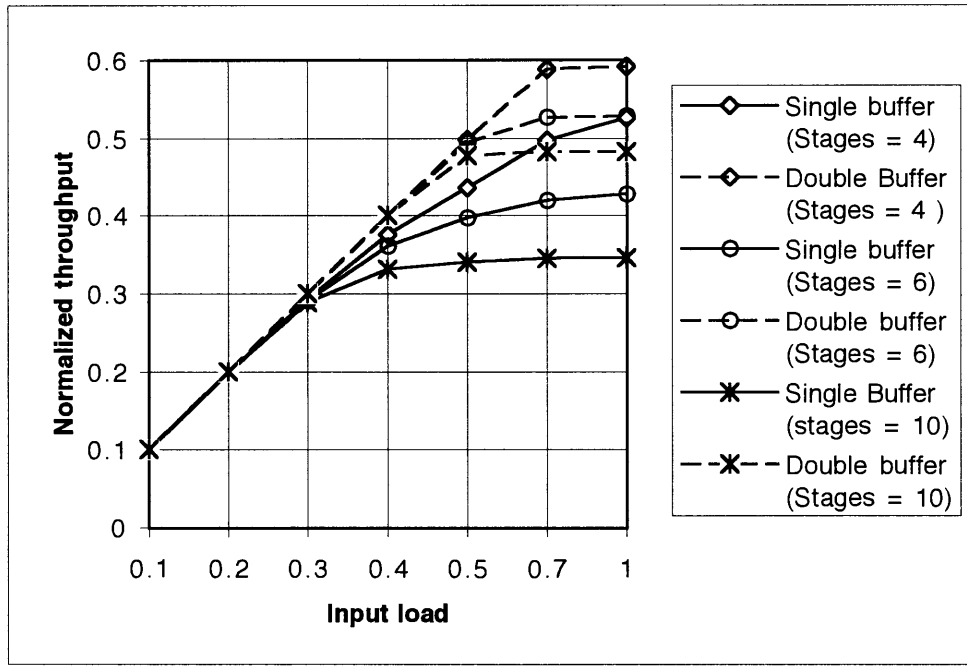

Figure 7.2 Throughput comparison between double buffer and single buffer switch

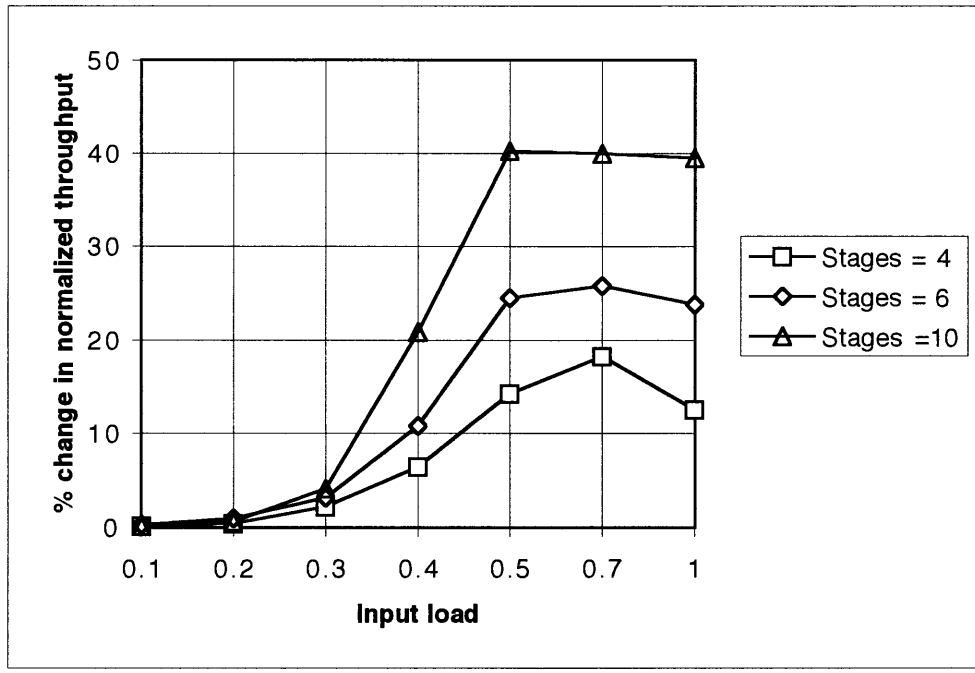

Figure 7.3 Percentage change in throughput for double buffer switch

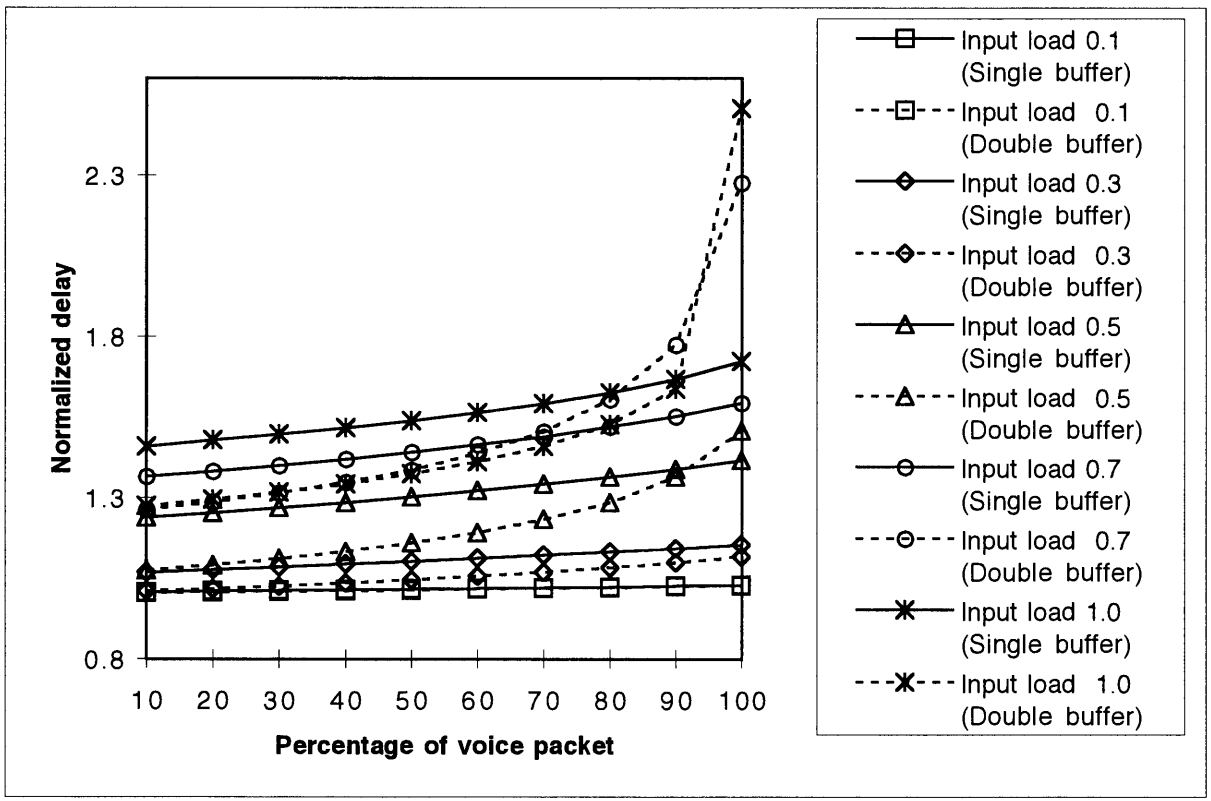

Figure 7.4 Comparison of delay of voice packet between double and single buffer 6-stage switch

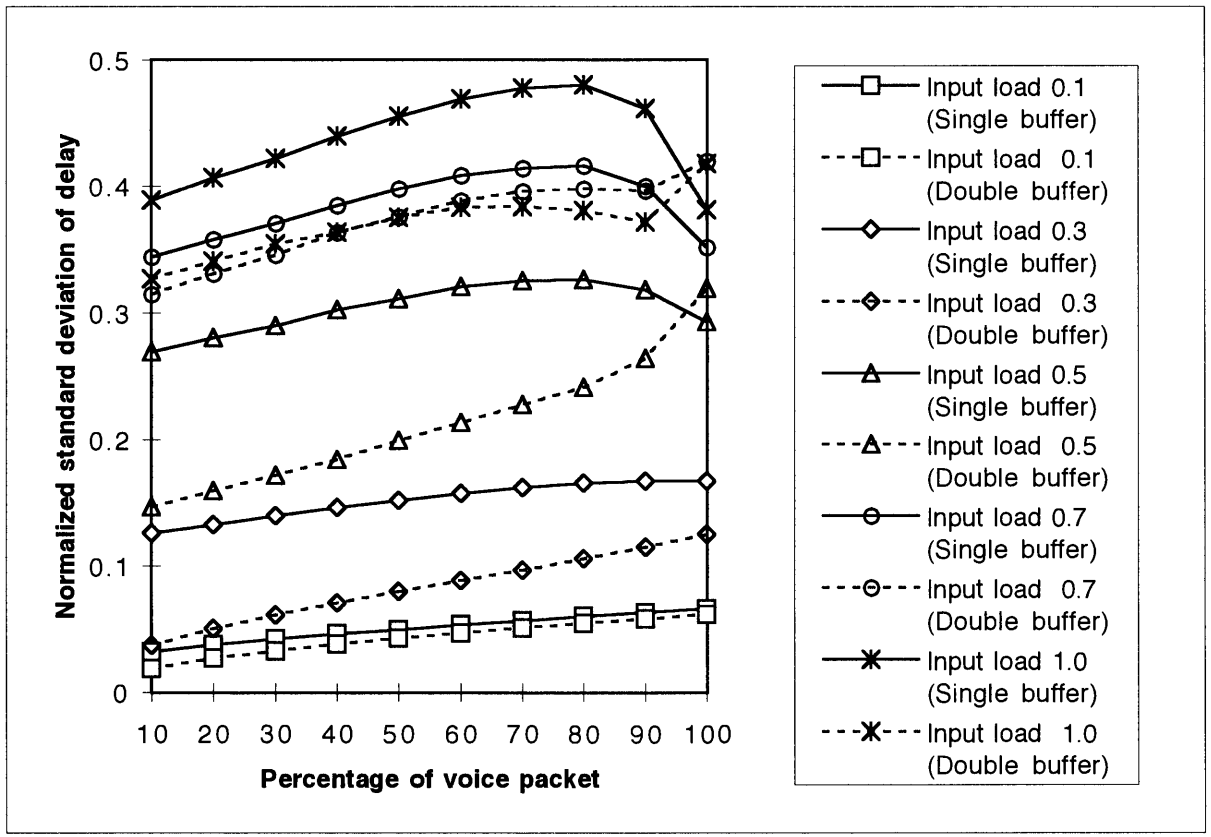

Figure 7.5 Comparison of variance of delay of voice packet between double and single buffer 6-stage switch

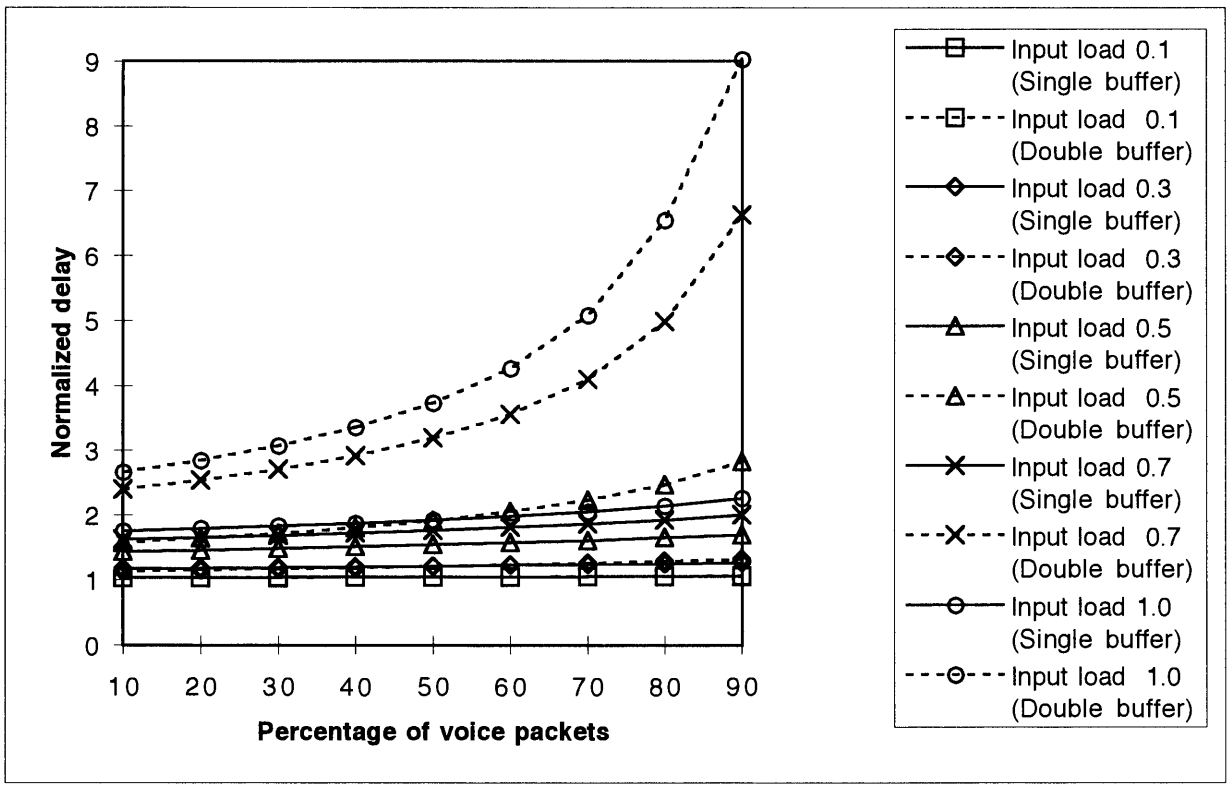

Figure 7.6 Comparison of delay of data packet between double and single buffer 6-stage switch

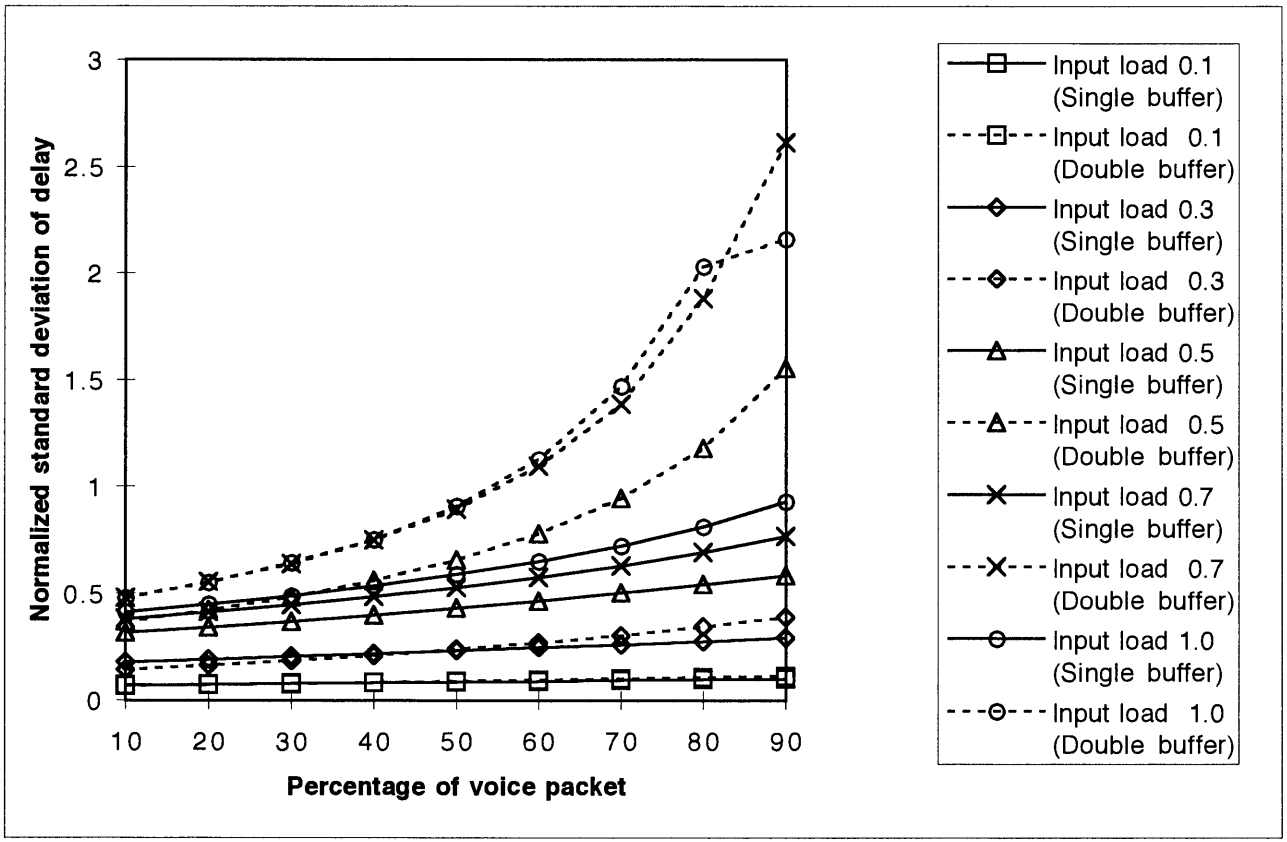

Figure 7.7 Comparison of variance of delay of data packet between double and single buffer 6-stage switch

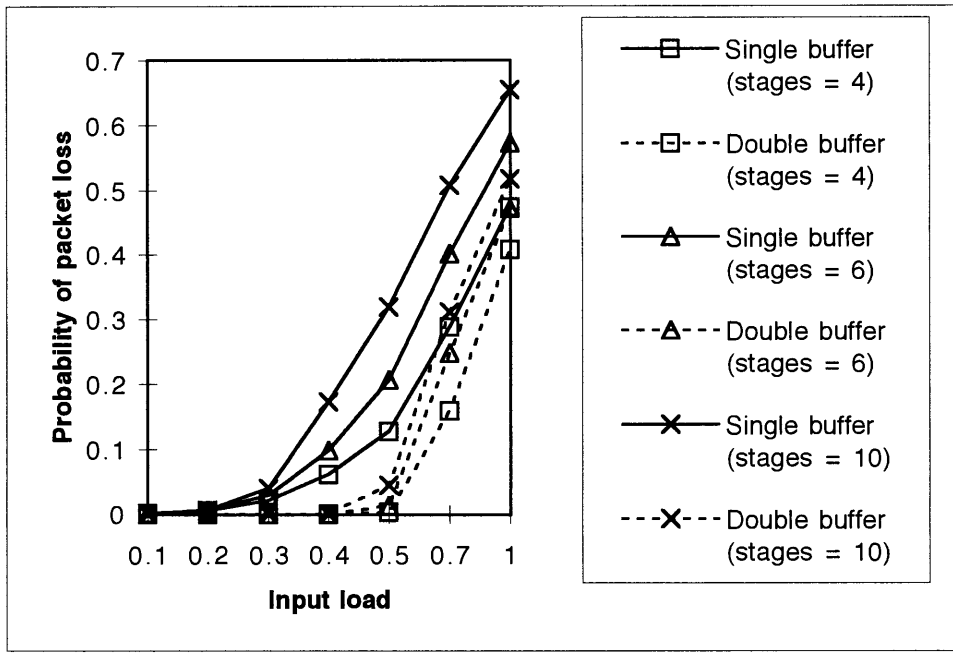

Figure 7.8 Comparison of probability of packet loss between double buffer and single buffer 6-stage switch

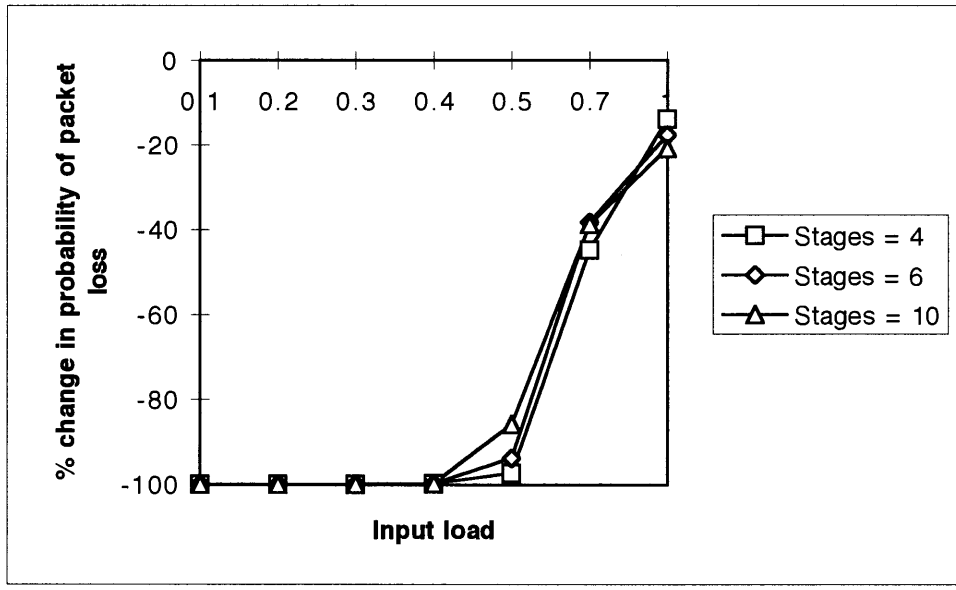

Figure 7.9 Percentage change in probability of packet loss for the double buffer 6-stage switch

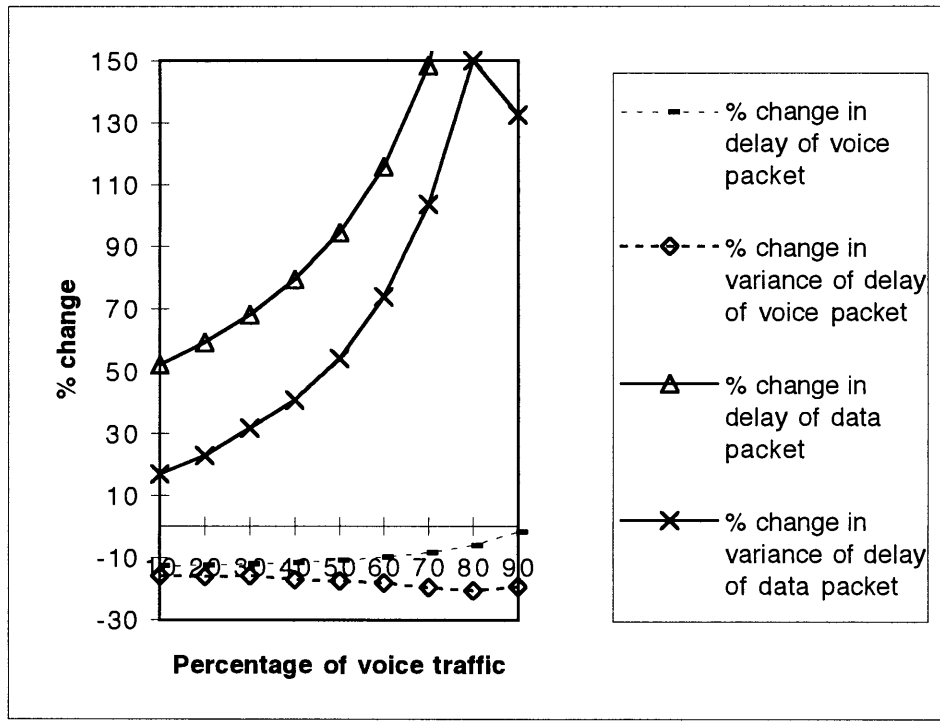

Figure 7.10 Percentage change in delay and variance of delay of voice and data packets for fully loaded double buffer 6-stage switch

Chapter 8

Conclusion

8.1 Summary

In this thesis, we studied the performance of ATM packet switch based on single buffer Banyan network by simulations. We compared the analytical results of three-state model with the simulation results. The maximum normalized throughput obtained from three-state model with non-priority scheme is optimistic by 10% for 4, 6, and 10-stage switch. The simulation results showed that although throughput does not increase with priority scheme, there is a significant reduction in variance of delay.

We introduced two new schemes, non-blocking first stage switch and enhanced priority scheme. It is shown that the EP scheme further significantly reduces the variance of delay, and the NBFS scheme increases the throughput. The EP scheme can be useful in minimizing variance of delay in non-uniform traffic pattern. The typical values of performance parameters for 6-stage fully loaded switch with NBFS and EP scheme are as follows: normalized throughput is 0.4271, normalized delay is 1.718, normalized standard deviation of delay is 0.3782 and probability of packet loss is 0.5728. We obtained the performance of switch with mixed voice and data traffic, where priority is given to voice packet. It is found that for input load greater than 0.4 (which is the supportable throughput of the switch) the normalized standard deviation

of delay of voice traffic reaches its maxima when percentage of voice traffic is about 80%.

In order to increase throughput, decrease delay and variance of delay of Banyan switching fabrics in realistic ATM network traffic condition, external blocking has to be decreased. We proposed double buffer switching fabric to lessen the effects of external blocking. The throughput of fully loaded double buffer 4, 6, and 10-stage switch increases by 12%, 23%, and 39% respectively. The delay and variance of delay of voice traffic of fully loaded 6-stage switch, with 30% voice traffic, decreases by 12% and 15% respectively.

8.2 Future research

In pursuit of the goal of increasing throughput, decreasing delay and variance of delay, the switching fabric with more than two buffers in parallel at each input link of the SE may be studied. Double buffer Banyan switch based on 4x4 switching elements operating in EP and NBFS scheme may be studied. The performance of the switch with increasing buffers in the preceding stages than the following stages, to lower external blocking, to decrease the delay, and to increase the throughput may also be studied.

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