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A PWM Control Method for Reducing Electromagnetic Noise at the Generation Source in Power Electronic Converters

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A PWM Control Method for Reducing Electromagnetic Noise at the Generation Source in Power Electronic Converters

by

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Abstract

Advancements in power semiconductor devices are enabling the design of better electrical power conversion systems. Wide Bandgap (WBG) switching devices using materials like Silicon Carbide and Gallium Nitride can operate at higher temperatures, voltages, and frequencies with faster turn-on/off periods, improving converter performance over silicon devices. However, WBG technologies are still new, and the rapid switching transitions of these devices lead to issues such as voltage overshoots, ringing, and electromagnetic interference, which need to be addressed for widespread adoption. This work introduces a new control method for reshaping the switching voltages, which overcomes the disadvantages of fast transition time without increasing system losses. In fact, the proposed method reduces overall switching losses.

Experimental results on a small-scale prototype have shown that silicon-based devices improved the efficiency of a 380W DC-DC converter from 78% to 87% and reduced noise by 20dB+. A maximum of 9% efficiency improvement was observed in a 220W $100V_{in}$ DC to $100V_{rms}$ three-phase AC converter. Using Silicon Carbide (SiC) devices for 750W DC-DC and DC-AC converters resulted in about 15dB to 20dB+ reduction in electrical noise and about 1% efficiency improvement in the proposed case compared to the conventional switching method. The system Electromagnetic Interference (EMI) performance under proposed and classical switching methods is tested and compared, and results show about

5dB to 10dB reduction in conducted EMI for frequencies above 1MHz to 30MHz range. The proposed control technique allows breaking the relationship between converter efficiency and electromagnetic noise in state-of-the-art solutions, thereby speeding up the adoption of new WBG-based power-switching devices by addressing challenges related to electromagnetic noise, leading to higher power density and efficiency.

Dedication

This work is dedicated to my late mother, Anita Sukumaran, and my loving maternal grandparents, who deeply wish to see me earn a Master's Degree in Engineering.

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"In order to master a field, you must love the subject and feel a profound connection to it."

— Robert Greene, Mastery.

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Acronyms

AC Alternating Current

DC Direct Current

DMM Digital Miltimeter

DUT Device Under Test

EMC Electromagnetic Comptability

EMI Electromagnetic Interference

FPGA field-programmable gate array

GaN Gallium Nitride

HVDC High Voltage Direct Current

IGBT Insulated-gate Bipolar Transistor

LISN Line Impedance Stabilization Network

MMCX Micro-miniature coaxial

MOSFET Metal-oxide-semiconductor Field-effect Transistor

MSO Mixed Signal Oscilloscope

PCB Printed Circuit Board

PWM Pulse Width Modulation

RMS Root Mean Square

Si Silicon

SiC Silicon Carbide

SOT Small-outline Transistor

SPDT single-pole double-throw

SPTT single-pole triple-throw

SVM Space Vector Modulation

THD Total Harmonic Distortion

VA Volt-Ampere

WBG Wide band-gap

ZVS Zero Voltage Switching

1 Introduction

1.1 Problem Statement

The use of power electronic converters dates back several decades, with early developments occurring in the mid-20th century. Since then, they have found widespread use in various sectors, including renewable energy systems, electric transportation, consumer electronics, industrial automation, and grid infrastructure. Today, they are integral to modern energy systems, contributing to efficiency, reliability, and sustainability across diverse industries and applications.

Advancements in the semiconductor industry in the last two decades have been huge, enabling the design of higher-efficiency power converter modules. These power converter modules are used from low-power (tens of Watts) to gigawatt scale systems. These include but are not limited to smartwatches, mobile/laptop charges, and modern electronic gadgets in the low-power category, whereas electric vehicles, solar farms, wind farms, and High Voltage Direct Current (HVDC) transmission systems, to name a few of the high-power applications. Compared to conventional linear power conversion techniques, these solid-state power converters enable higher efficiency performance in DC/DC, DC/AC, AC/AC, and AC/DC conversions.

Improvements in semiconductor technology are allowing better performance of devices

made of SiC and Gallium Nitride (GaN). These devices fall under the category of Wide band-gap (WBG) devices with electron band-gap of about $3.3eV$ and $3.7eV$ for SiC and GaN respectively as compared to Si material with a bandgap of about $1.14eV$ [1]. This means these materials have higher bandgap energy (about $9eV$), which is required to excite electrons from the valence band to the conduction band. Compared to traditional silicon-based devices, WBG materials allow semiconductor devices to operate at higher temperatures, voltages, and frequencies compared to silicon devices. These devices also offer lower on-resistance, reduced parasitic capacitance, and faster transition time (in the range of nanoseconds) that helps to minimize conduction and switching losses, thereby improving the overall device performance and efficiency.

Faster transition edges result in shorter switching times, reducing the duration the device takes to turn on or off (during switching). This minimizes the device's switching power losses and hence improves power electronic circuits' efficiency. Switching frequency and switching losses have a direct relationship. This means the losses in the system start increasing as the switching frequency increases. Hence, to keep the losses in the converter to a minimum, designers must trade-off between efficiency and operating frequency. The disadvantage of operating at a lower frequency is that the size of passive components, such as inductors and capacitors, has to be bigger. With these new WBG devices with inherently lower switching losses, designers can substantially increase switching frequencies, thereby enabling the design of smaller, lighter, and more compact power converters with reduced passive component sizes. This benefits applications where size, weight, and efficiency are

critical, such as mobile devices, electric vehicles, and aerospace systems, to name a few.

Characteristics offered by the WBG devices are necessary to break the barriers in power density, efficiency, and applicability [2]. Since this is a new technology, fabrication complexities are still involved, and the device properties and behavior are not fully understood [3]. The switching nature of converters made of WBG devices can operate at high switching frequencies, and faster transitions can lead to many issues within the system. Significant problems include large voltage overshoot, voltage ringing, and generation of wide-band electromagnetic noise due to the fast transition time. The large voltage swings and ringing can cause self-harm to the device when they exceed the operation parameters of the components. These issues can also influence the control circuitry, leading to false triggering of these switching elements that could lead to short circuits and device damage. The nature of EMI is that it can be both conducted and radiated noise spanning a broad band of frequencies. This noise can interfere with the operation of other surrounding equipment and radio communication. These effects also lead to motor winding failures, bearing currents, high-frequency ground leakage currents, and Electromagnetic Comptability (EMC) issues. To mitigate these noise-related issues, bulky and lossy EMI filters are being used. Overcoming these challenges is crucial to the widespread adoption of SiC and GaN based devices to design power converters with higher power density to meet the increase in electric energy demands [2, 4].

1.2 Objective

This work introduces a new Pulse Width Modulation (PWM) control method to reshape switching voltages to overcome the disadvantages of the fast transition times without increasing switching losses. Instead, the approach reduces switching losses even further. It involves designing and reducing the slope of most of the fast-rising and falling edges of the switching voltage, thereby reducing a significant amount of electromagnetic noise at the source. Zero Volt Switching (ZVS) at several switching transitions reduces losses and enhances converter efficiency. This method can be applied to two-stage converters where the source and the load nodes connect to the intermediate energy storage element using active devices. This work provides analytical details of the approach and is supported by experimental work to verify the proposed concepts.

1.3 Significance

The initial simulation and laboratory-scale experiments confirm the effectiveness of minimizing EMI and switching losses. Reduction in EMI and noise are achieved by tuning the transition edges. This eliminates the need for bulky EMI filters and facilitates the design of converter modules with higher power density. Improvements in overall converter efficiency are achieved by eliminating switching losses. The findings presented in this work confirm the improvement in system efficiency when using the proposed control strategy.

2 Literature Review

The switching frequency and switching transition time of the switches in power electronic converters affect the efficiency of the system and the amount of generated electrical noise. In Figure 2.1, the top half qualitatively represents the contrast between the transition periods of the switching voltage of Si device (in green) and SiC device (in red), and the bottom half represents their impact on the frequency spectrum. The slope of the red trace is greater than the green trace.

Equation (2.1) characterizes the average switching loss calculation in a semiconductor device. In the equation, P_{sw_loss} is the switching power loss for the device, V_{DS} is the blocking voltage across the device, I_{DS} the current through the device, t_{on} and t_{off} are the device turn-on and turn-off time period respectively, and f_{sw} the switching frequency at which the device is operating at. From this equation, it is clear that switching losses have a direct relationship with the device transition time. Hence, SiC devices have inherently low switching losses compared to the Si devices.

Switching Power Loss:

$$P_{sw\_loss} = V_{DS} \times I_{DS} \times (t_{on} + t_{off}) \times f_{sw} \tag{2.1}$$

The bottom half of Figure 2.1 represents the pole voltage spectrum for the two material types. The trade-off of the fast transition is the increased electromagnetic noise generated

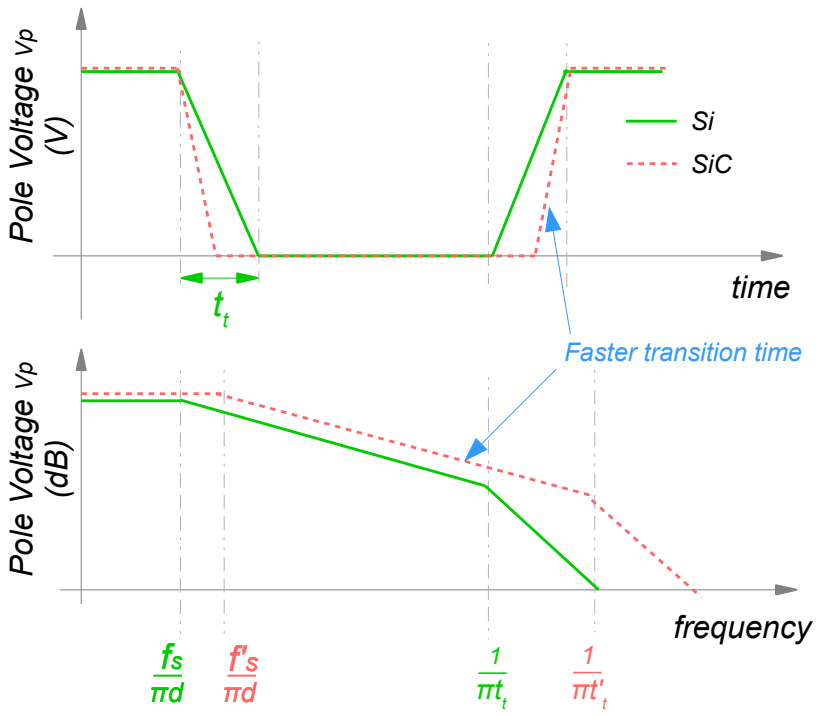

Figure 2.1: Comparing the transition time for Si and SiC devices

from the system due to the switching action. The first corner frequency is directly related to the device switching frequency (f_{sw}), whereas the second corner frequency is associated with the transition duration (t_t) of the switch. Due to the faster transition edge for a SiC device, it generates additional noise when compared to a Si device when operating similar conditions. With any state-of-the-art solution, as converter efficiency increases, so does the electromagnetic noise. This work addresses the prominent issues caused by the fast rise and fall times.

Some of the other prominent issues and challenges caused by these fast transition high voltage signals are as described below:

Device Stress: Considerable voltage or current across the switching device that exceeds

the maximum rated level can cause the breakdown of the semiconductor junctions, leading to damage or degradation of the device [2, 5].

Motor Winding Failures: Motor winding failure due to switching noise can result from voltage spikes surpassing insulation breakdown thresholds, high-frequency currents inducing resistive losses and heating, resonance effects causing mechanical stress, electromagnetic interference disrupting control circuitry, and partial discharge deteriorating insulation [6].

Ground leakage current: This refers to an unintentional transfer of current to the ground. Due to the effects mentioned above, the motor winding insulation can get damaged. This will expose the conductor to touch the metal body of the equipment, thereby creating an undesirable path for the current to flow. Ground leakage poses safety hazards on electrical systems that could lead to electrical shock or damage to the equipment [5, 6].

Wide-band Electromagnetic Noise issues: Wide-band encompasses a large spectrum noise that can interfere with the operation of electronic devices and communications systems, leading to malfunction, reduced signal quality, and decreased performance. It increases background noise, induces cross-talk, and can affect sensitive equipment like sensors. In some cases, prolonged exposure to high levels of electromagnetic noise may have health implications [7, 8, 9].

2.1 State-of-the-art Solutions

Some of the most widely used methods to address the issues mentioned above are the following:

Hardware and design changes: Some of the issues discussed above can be solved by manufacturing modifications and design changes. One way is to increase the insulation strength of the metal cables. This will let the cable withstand high dv/dt issues concerning ground leakage currents. It also enhances safety, improves reliability, and protects against external factors. However, the downsides are increased manufacturing cost, increased bulkiness, increased weight, decreased flexibility, and decreased heat dissipation.

Devices with higher voltage safety margins (1.5x to 1.7x times the operating point) are being adopted to deal with high-voltage swings observed by the device. However, the downside is that these devices will be costly, have a bigger footprint, and have slower switching speeds due to increased parasitic capacitance and inductance [7, 10].

Filters: Advanced filter designs such as LCR filters are a solution for mitigating issues caused by the fast transitions of the switching elements. However, the filter designs typically account for 2-3% of system losses, can occupy up to 30% of the overall system volume, and increase system cost [4, 11, 12, 13, 14].

Active filter designs are another approach to suppressing electrical noise-related issues. They filter out noise by injecting counteracting currents or voltages, thereby canceling harmonic currents or voltages. Even though this method looks attractive, it increases system complexity, design cost, and power consumption as it requires additional power to operate. The active filters can generate their own EMI, leading to failing EMC testing. The limited bandwidth of these filters limits their ability to meet the wide-band nature of the noise generated by SiC devices.

Gate drive approaches: Increasing the gate resistor can solve this issue by showing the switching transition to reduce the voltage overshoots, EMI, and device stress. However, slowing the switching transition leads to an increase in switching losses. Poor choice of gate resistor can risk oscillation, instability, or EMI-related issues due to cross-talk [10, 15].

Lossy Snubbers: Snubber circuits are passive electronic circuits that protect semiconductor devices from voltage spikes and transient overvoltages during switching operations. These circuits are designed to absorb or divert energy from the semiconductor device, reducing the risk of damage or malfunction. However, these circuits increase design complexity, increase cost due to extra components, and increase system losses. [16, 17].

Lossless Snubbers: Soft switching snubber techniques have also been studied for three-phase PWM inverters [17, 18]. These circuits facilitate smoother switching transitions in power electronic devices. Unlike traditional snubbers that focus on suppressing voltage spikes and ringing, soft snubbers aim to reduce switching losses and stress on the switching devices by ensuring that they operate in a soft-switching mode.

These snubbers achieve their purpose by manipulating the voltage and current waveforms during switching events. By carefully controlling the rise and fall times of these waveforms, the soft-switching snubber minimizes the occurrence of abrupt voltage and current transitions, reducing switching losses and EMI in the process. The advantages of this method include reduced switching losses, enhanced reliability, lower EMI, and improved performance.

The downside of these lossless snubbers is they are more complex, costly, and less

reliable. Soft-switching snubbers require careful tuning and may not achieve faster switching frequency. Additionally, they may cause efficiency losses in high-power applications, and the snubber designs are typically specific to certain power converters or topologies.

2.2 Summary

This chapter discusses the use case of different power electronics devices in the industry and their capabilities for high-current and high-voltage applications. It also addresses the challenges and issues associated with these devices, such as high switching and conduction losses, poor thermal performance, and sensitivity to overvoltage and overcurrent conditions. Further, it discusses the progress in newer semiconductor technologies and the potential for power electronics converters made out of these devices to improve power density, efficiency, and applicability. Additionally, it emphasizes the challenges caused by the fast transition of high-voltage signals. It discusses the solutions widely used in the community, including hardware and design modifications with advanced filter designs.

The next chapter discusses the proposed control strategy to mitigate the EMI at the generation source. Using this approach, the inherent shape of the switching transition voltages is modified without slowing down the switching device or increasing switching losses. This approach delinks the direct relationship between converter efficiency and electromagnetic noise established by the state-of-the-art techniques, with near-to-zero switching losses, while simultaneously providing the ability to tune the electromagnetic noise.

3 Design Methodology

Chapter 2 discusses several state-of-the-art techniques and their respective shortcomings with EMI and switching losses within switching power converters. The proposed PWM control strategy enables an attractive pathway to reduce EMI at the source of its occurrence without increasing the switching losses. The proposed control technique can be used in DC-DC and DC-AC converter topologies. The rest of the chapter discusses the converter topologies and the contrast between the traditional and proposed modulation and control techniques. A detailed discussion of the design considerations, including the components' sizing and control implementation, is also provided in this chapter.

3.1 DC-DC Converters

As described in Chapter 1, power electronic systems have been playing a major role in helping to meet the next-generation electrification goals. These systems help harness renewable energy, store electricity in batteries, and increase the efficiency of various applications, from transmission systems to consumer electronics [16]. One of the fundamental building blocks of these electrical systems is DC-DC converters. As the name suggests, these converters help convert current and voltages from one DC level to another and operate these systems optimally. This section covers the topology for the DC-DC converter and how the conven-

tional topology can be modified to accommodate the proposed control approach. Detailed working principles of the modified topologies are also provided.

3.1.1 Conventional Approach

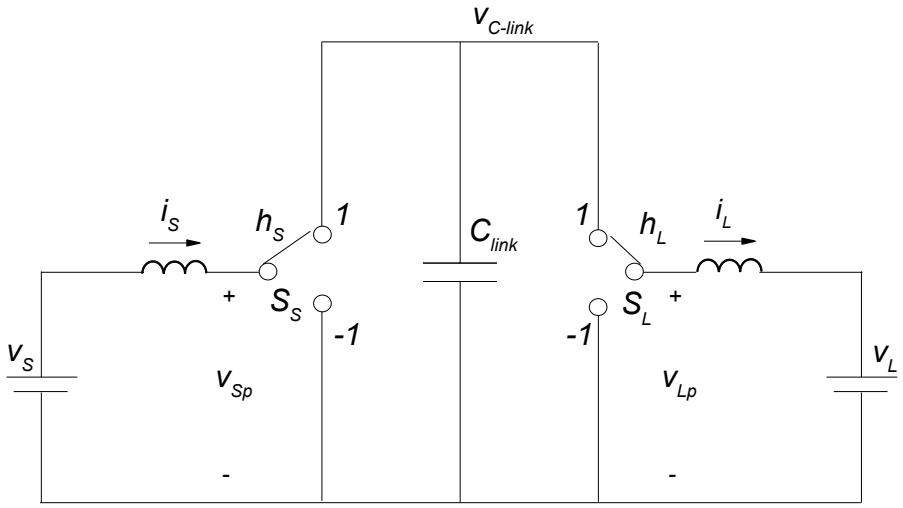

Figure 3.1: Conventional topology for a DC-DC converter example.

Figure 3.1 shows the basic circuit concept behind the conventional DC-DC converter [19]. The conventional two-stage approach uses single-pole double-throw (SPDT) switches to connect the source and the load to the intermediate DC-link capacitor (C_{link}), annotated as S_S and S_L in the figure. The input voltage source is V_s, and the input current is i_S. h_S and h_L signify the source and load-side switch state of the SPDT switches. The active state of the top switch and the bottom switch is represented by "1" and "-1", respectively, in both the half-bridges represented in Figure 3.1. The source and the load-side pole voltages are V_{Sp} and V_{Lp}, respectively. The output current from the load-side is represented as i_L, and

the output voltage is annotated as V_L. The general operation of the circuit is described in the sections below.

3.1.1.1 Converter Operation

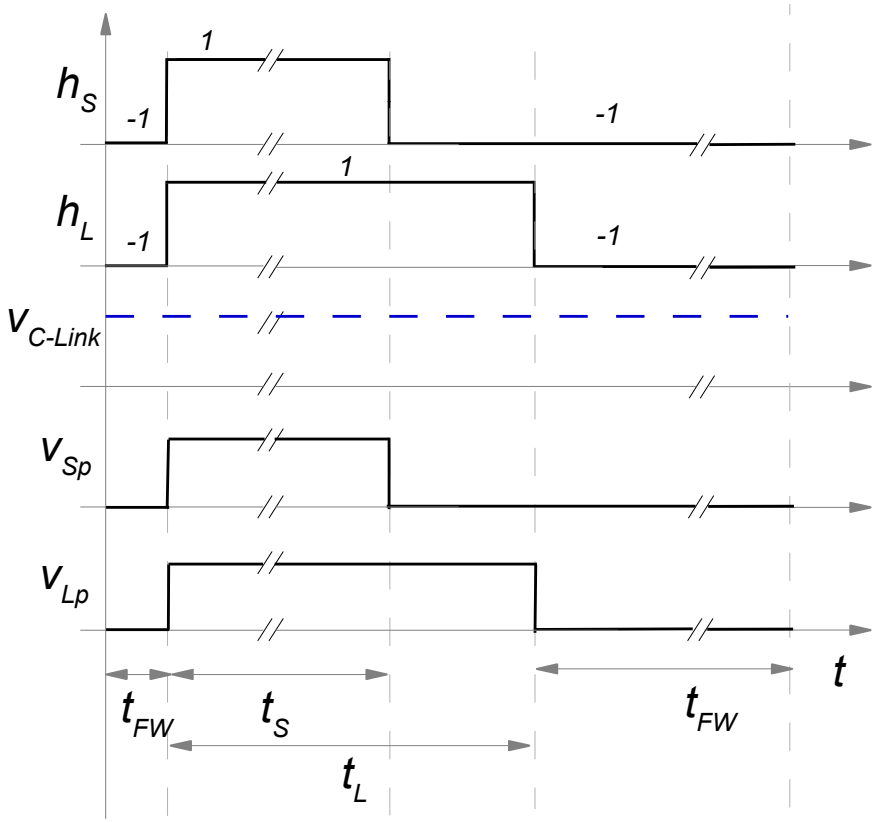

Figure 3.2: Conventional boost mode waveforms of the switching functions (h_S and h_L), Bulk capacitor voltage V_{C-link}, source and load-side pole voltages (v_{Sp} and v_{Lp})

In this classical approach, no synchronization is needed between the operation of the two half-bridge modules. Figure 3.2 and Figure 3.3 show a simple way of operation for both the boost and buck modes of operation. In both figures, average values of h_S and h_L represent the duty ratios, that is, how long each switch is active for a given period. In the boost operation, it can be noticed that the load-side top switch is active for a longer duration when

compared to the source-side top switch. Similarly, the load-side top switch is active for a shorter duration than the source-side bottom switch for the buck mode of operation. V_{C_Link} represents the voltage across the bulk (link) capacitor that interfaces the source and the load-side, as shown in Fig 3.1. V_{Sp} and V_{Lp} represent the voltage waveforms across the source

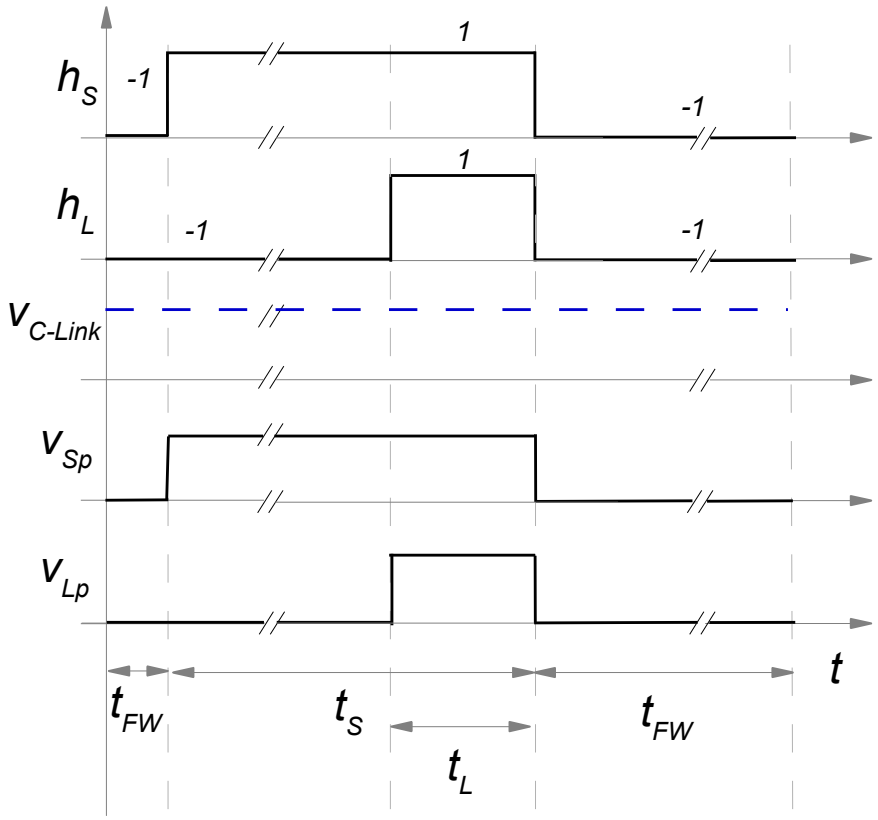

Figure 3.3: Conventional buck mode Waveforms of the switching functions (h_S and h_L), Bulk capacitor voltage V_{C-link}, source and load-side pole voltages (v_{Sp} and v_{Lp})

and load-side bottom switches. t_S represents the time duration for which the source-side top switch is active, and similarly, t_L represents the time period for which the load-side top switch is active. t_{FW} is the time duration for which the converter is freewheeling or in zero state. No power transfer occurs between the source and the load in this state.

The duty ratios of each half-bridge, when the converter operates in either boost or buck

mode of operation, can be calculated from Equations 3.1 and 3.2 for a set operating point. d_S and d_L reperesent the source-side and load-side duty ratios and f_{SW} is the switching frequency of the converter. Note that in Boost mode $t_S < t_L$ whereas in Buck mode $t_S > t_L$.

$$t_S = \frac{d_S}{f_{SW}} \approx \frac{v_S}{f_{SW} V_{C-link}} \tag{3.1}$$

$$t_L = \frac{d_L}{f_{SW}} \approx \frac{v_L}{f_{SW} V_{C-link}} \tag{3.2}$$

For the smooth operation of each of the half-bridges, enough dead time must be provided to ensure that the bulk capacitor voltage V_{C-Link} does not get shorted during the transition period of each switch, potentially damaging the transistors. As a rule of thumb, the dead time should be at least more than the sum of the transistor turn-on and turn-off periods and delay time periods [10].

3.1.2 Proposed Approach

The main idea of the proposed approach is first described with the help of a DC-DC boost-buck converter example. The approach uses single-pole triple-throw (SPTT) switches, instead of the classical SPDT switches, to connect the source and the load to the intermediate DC-link capacitor (C_{link}), annotated as S_S and S_L in the Figure 3.4 [20]. The differences from the conventional case circuit are highlighted in blue traces. The additional throw of the switches, annotated with state "0", connects to a *tiny* capacitor (C_{tiny}) and is used

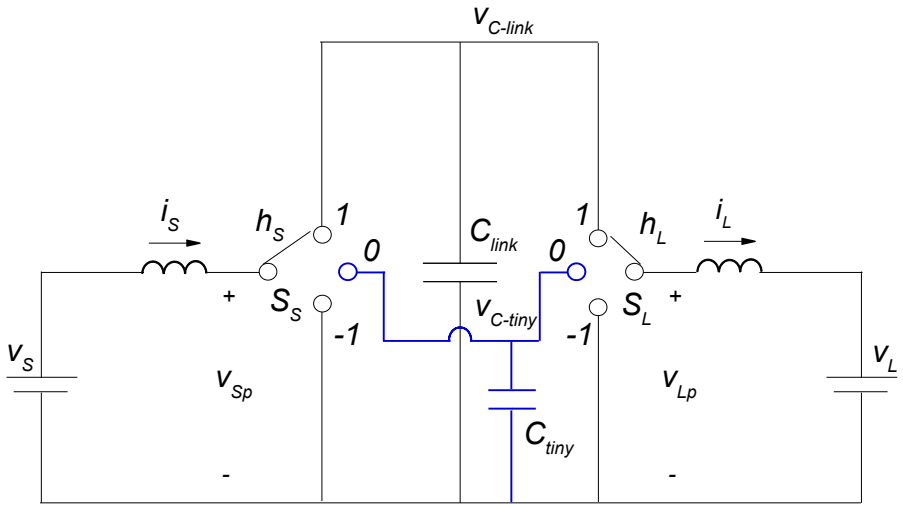

Figure 3.4: Proposed topology for a DC-DC converter example.

to smoothen the fast dv/dt transitions of the switch pole voltages, v_{Sp} and v_{Lp}, without additional switching losses, as described later in the chapter.

3.1.2.1 Boost Operation

In comparison with the conventional PWM approach described above, where the source and load transistors, S_S and S_L, may or may not be synchronized, the transistors of each module are sequenced and synchronized as shown in Figure 3.5. The beginning of the switching interval starts by charging the tiny capacitor (C_{tiny}). During its charge time t_C, the switch poles first connect to throw "0" and C_{tiny}, which is at zero volts. The capacitor gets charged by the net current ($i_S - i_L$), raising its voltage from zero volts to a voltage value that is approximately close to the DC-link voltage V_{C-link}. On the v_{C-tiny} waveform plot, ϵ denotes the difference in voltage between v_{C-tiny} and V_{C-link} after the end of the charge interval of the tiny capacitor. Its magnitude, close to zero, depends on the control and

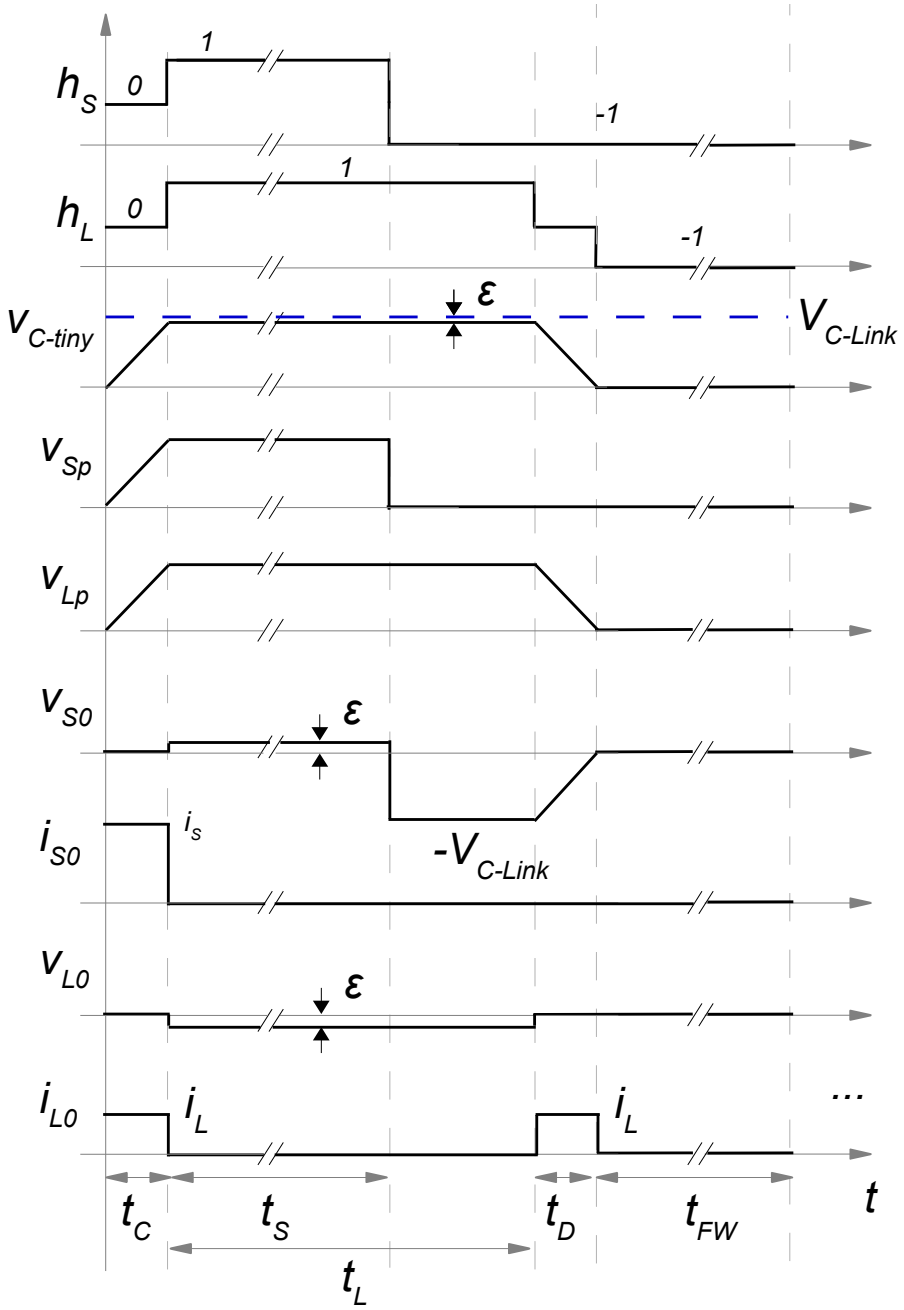

Figure 3.5: Waveforms of the switching functions (h_S and h_L), tiny capacitor voltage (V_{C-tiny}), source and load-side pole voltages (v_{Sp} and v_{Lp}), and voltage, current waveforms of state "0" throws (v_{S0}, i_{S0} and v_{L0}, i_{L0}) during boost mode of operation [21].

hardware implementation. It is this charging action of C_{tiny} that allows the tuning of the switch pole voltages, v_{Sp} and v_{Lp}, enabling a slower rising edge. This feature is highlighted in the v_{Sp} and v_{Lp} waveforms of Figure 3.5. After V_{C-tiny} reaches close to the bus voltage, V_{C-Link}, the transistors transition to a "1" state where they connect to the DC-link capacitor C_{link} for the conventional power transfer operation. During this transition, from state "0" to state "1", ZVS occurs at both the source and the load-side converters as $v_{C-tiny} \approx V_{C-link}$. Similar to the conventional case, the DC-link capacitor is assumed to be large enough, and hence, the DC-link capacitor voltage V_{C-link} features low voltage ripple.

The source-side module transfers power during the t_S duration, and the load-side power transfer occurs for the t_L duration to complete the power transfer process for boost operation. As discussed earlier, these two time intervals are essentially the same as that of the conventional approach. In the boost operation, the source-side switch is active for a shorter interval and goes into an inactive freewheeling state. The source-side half-bridge transitions from the "1" state to the "-1" state. The input inductor charges up when the pole connects to the "-1" state. It is evident from the V_{Sp} waveform that the transition has a high dv/dt rate, which will lead to switching losses and noise generation during this transition.

In contrast, the load-side converter transitions to state "-1" from state "1" through state "0" where C_{tiny} is discharged to zero by the load current i_L. Only the load switch transition edge features a tunable low slope (dv/dt) rate during the active-to-inactive freewheeling state. The remaining time period (t_{FW}) is completed by the inactive freewheeling state where both the source and load remain in the switch state "-1". Note that the time intervals

of the converter's low dv/dt transitions, t_C and t_D, are exaggerated for illustration purposes.

3.1.2.2 Buck Operation

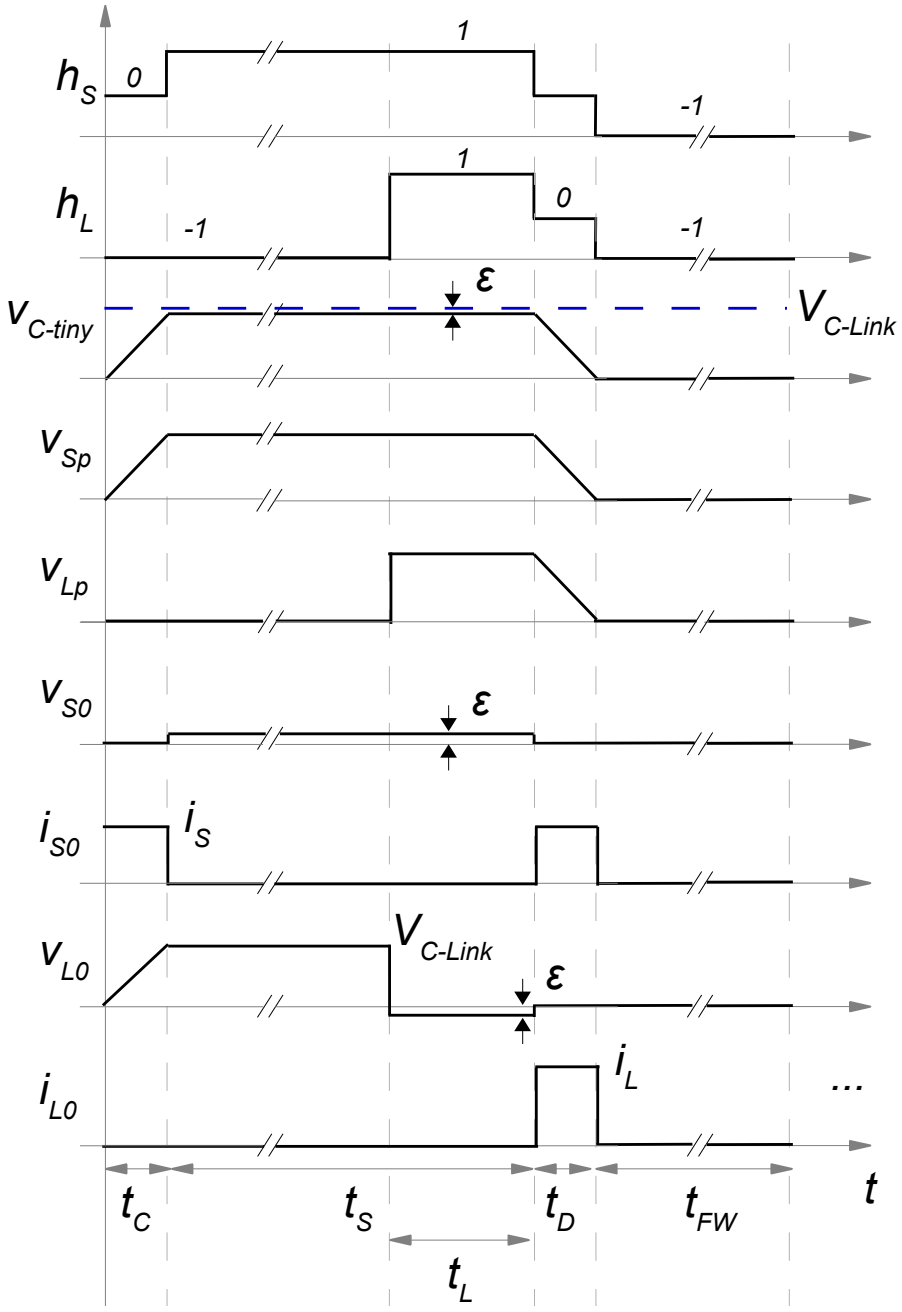

Figure 3.6: Waveforms of the switching functions (h_S and h_L), tiny capacitor voltage (V_{C-tiny}), source and load-side pole voltages (v_{Sp} and v_{Lp}), and voltage, current waveforms of state "0" throws (v_{S0}, i_{S0} and v_{L0}, i_{L0}) during buck mode of operation [21].

The buck mode of operation of the converter is represented in Figure 3.6. In this mode of operation, both the source-side and load-side half-bridges are synchronized. Here, the source switch has a longer active interval than the load switch. The switching interval starts by charging the tiny capacitor (C_{tiny}). Only the source-side pole connects to throw "0" to charge the tiny capacitor. During the charge time interval t_C, the capacitor charges up from zero volts to a value (ε) close to the DC-Link voltage V_{C-link} with a net current of i_S for the duration of t_C. Therefore ε is calculated to be $\varepsilon = V_{C-link} - V_{c-tiny}$. The source-side pole voltage, v_{Sp}, has a slow-rising edge, as highlighted in Figure 3.6. Next, the switch transitions to the "1" state, connecting to the DC-link capacitor C_{link} for the conventional power transfer operation. This transition from the "0" state to the "1" state happens with ZVS as $v_{C-tiny} \approx V_{C-link}$.

The source-side converter transfers power for the duration of t_S, and the load is connected to the DC-link voltage V_{C-link} for t_L duration by the load-side converter. In the transition during which the load gets connected to the bus capacitor, the transistors experience hard switching with a fast slope (dv/dt). Both the source and load-side modules transition to the "-1" state from the state "1" through the "0" state. During this transition, the C_{tiny} is discharged to zero by the net negative current of (i_S-i_L). At the "-1" state, both the converters are freewheeling. The time intervels, t_C and t_D, depicted in Figure 3.6 have been exaggerated for illustration purposes only.

3.1.2.3 Duty Ratio Calculations

Based on the overall application requirements, the slope of the transition edges discussed above can be designed using the proposed approach. Compared with the classical approach, slowing the transition edges does not lead to more switching losses. The time intervals t_C and t_D determine the transition rate of the switching pole voltages (v_{Sp} and v_{Lp}) and can be calculated based on the capacitor equation, $C_{tiny}\frac{dv_{C-tiny}}{dt} = i_{tiny}$, as shown in (3.3)-(3.6) [21].

Boost:

$$t_C = \frac{d_C}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_S - i_L} \tag{3.3}$$

$$t_D = \frac{d_D}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_L} \tag{3.4}$$

Buck:

$$t_C = \frac{d_C}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_S} \tag{3.5}$$

$$t_D = \frac{d_D}{f_{SW}} \approx \frac{C_{tiny} \times V_{C-link}}{i_L - i_S} \tag{3.6}$$

Here, d_C and d_D represent the duty ratios of the charge and discharge time intervals, f_{SW} is the switching frequency, V_{C-link} is the DC-link capacitor voltage, i_S, and i_L are the source and load currents respectively. With a chosen value for C_{tiny}, a range of values for the tuned transition time intervals t_C and t_D are possible, which will also be a function of the operating conditions of the converter. To accommodate t_C and t_D intervals in the source and the load duty ratios, Equations (3.7)-(3.10) can be calculated as shown using linear duty ratio expressions [21].

Boost:

$$t_S = \frac{d_S}{f_{SW}} \approx \frac{v_S}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C}{2}}_{\text{small}} \tag{3.7}$$

$$t_L = \frac{d_L}{f_{SW}} \approx \frac{v_L}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C + t_D}{2}}_{\text{small}} \tag{3.8}$$

Buck:

$$t_S = \frac{d_S}{f_{SW}} \approx \frac{v_S}{f_{SW} V_{C-link}} - \underbrace{\frac{t_C + t_D}{2}}_{\text{small}} \tag{3.9}$$

$$t_L = \frac{d_L}{f_{SW}} \approx \frac{v_L}{f_{SW} V_{C-link}} - \underbrace{\frac{t_D}{2}}_{\text{small}} \tag{3.10}$$

Here, d_S and d_L are the corresponding duty ratios for time intervals t_S and t_L as annotated in Figure 3.5 and Figure 3.6, v_S and v_L are the source and load voltages respectively. The designed time intervals for t_C and t_D are expected to be relatively small compared to (t_S) and the load (t_L) and could potentially be ignored. On rearranging the Equations, (3.3)-(3.6), Equation (3.11)-(3.12) can be obtained, which helps to choose a value for C_{tiny} and hence tune the slop (dv/dt) of the transition time as per the specification of the application under consideration [21].

Boost:

$$C_{tiny} \approx \frac{t_C(i_S - i_L)}{V_{C-link}} \approx \frac{t_D i_L}{V_{C-link}} \tag{3.11}$$

Buck:

$$C_{tiny} \approx \frac{t_D(i_L - i_S)}{V_{C-link}} \approx \frac{t_C i_S}{V_{C-link}} \tag{3.12}$$

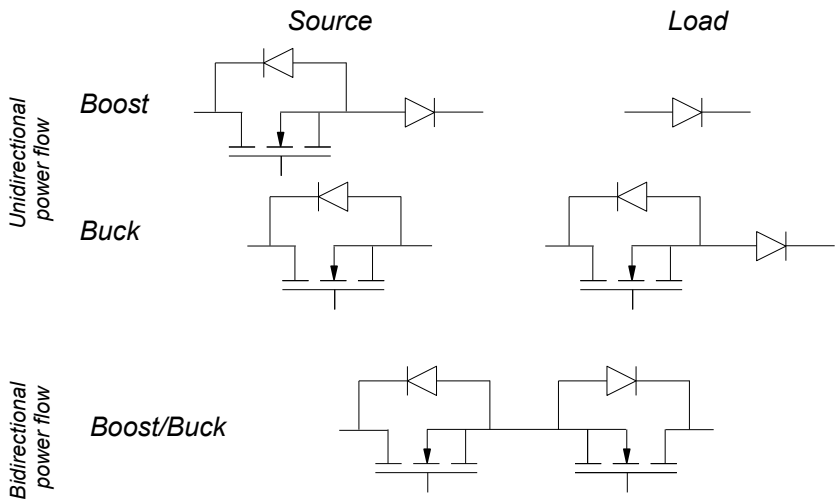

Figure 3.7: Switch realizations for the middle switch for the proposed DC-DC converter. [21]

3.1.2.4 Device Ratings

The new state "0" of the two SPTT switches of the proposed methodology can be realized using conventional semiconductor devices such as Metal-oxide-semiconductor Field-effect Transistors (MOSFETs), Insulated-gate Bipolar Transistors (IGBTs), and diodes with lower overall power rating. Figure 3.5 and Figure 3.6 illustrate the voltage and current waveforms of the throw "0", as annotated by v_{S0}, i_{S0} and v_{L0}, i_{L0} for the source and the load respectively. Figure 3.7 shows the switch realizations for two modes of operation for unidirectional and bidirectional power flow using MOSFETs and diodes. Table 3.1 lists all the additional device peak voltage and Root Mean Square (RMS) current ratings to optimize device Volt-Ampere (VA) ratings.

Considering the boost mode of operation, the source-side throw "0" blocks bidirectional voltage. Therefore, this node can be realized as a combination of a MOSFET and a diode. Here, the diode will be rated for the voltage blocking capability of V_{C-link}, and the voltage

Table 3.1: Peak voltage and RMS current ratings of the switches of the additional throw for boost and buck mode of operation. [21]

Mode		Source throw "0"		Load throw "0"	
		MOSFET	Diode	MOSFET	Diode
Boost	Voltage	$\epsilon \to 0$	V_{C-link}	-	$\epsilon \to 0$
	Current	$i_S\sqrt{d_C}$		$i_L\sqrt{d_C + d_D}$	
Buck	Voltage	$\epsilon \to 0$	-	V_{C-link}	$\epsilon \to 0$
	Current	$i_S\sqrt{d_C + d_D}$		$i_L\sqrt{d_D}$	
Note: $d_C, d_D << 1$					

rating of the MOSFET is $\epsilon \to 0$. However, the load-side throw "0" will witness a negative blocking voltage. Hence, this throw can be realized with a diode with minimal blocking voltage requirements of ϵ, which is $V_{C-link} - V_{C-tiny}$.

In the buck mode of operation, the source-side throws "0" blocks positive voltage of ϵ. This throw can be realized using a single MOSFET. However, since the load-side throw "0" witnesses bidirectional blocking voltage, it requires a MOSFET and a diode connected in series. Here, the diodes are rated for the voltage blocking capability of V_{C-link}. Regardless of the mode of operation, the RMS current ratings of the devices are determined by the source and the load currents. The time interval for which the middle switch remains active is very small compared to the main power transistors, so the RMS currents are smaller than rated current magnitudes. Two transistor devices with antiparallel diodes are necessary if the converter design requires bidirectional power flow, as shown in Figure 3.7. Figure 3.8 illustrates the circuit schematic of the proposed DC-DC converter with buck mode of operation and unidirectional power flow. The modification to the conventional topology is

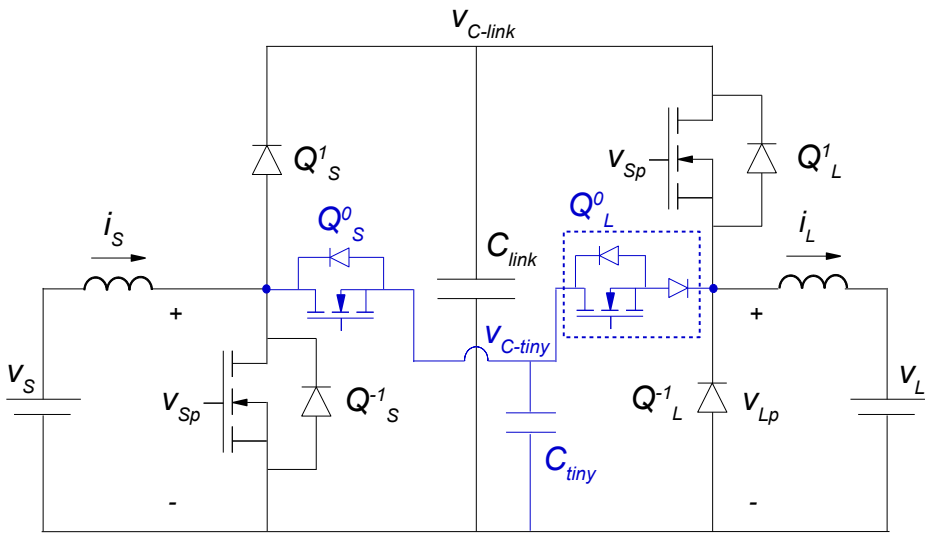

Figure 3.8: Circuit schematic of the proposed DC-DC converter with buck mode of operation and unidirectional power flow. Note that the switch additions are highlighted in blue traces [21].

represented in blue traces. Various other design scenarios can also be derived with the help of Figure 3.7 and Table 3.1.

Table 3.2: VA rating of the semiconductor devices with buck mode of operation per-unitized over the input power [21].

Device	Voltage	Current	VA (p.u.)
Conventional Devices			
Q_S^1	V_{C-link}	$\sqrt{d_S} I_S$	$\frac{1}{\sqrt{d_S}}$
Q_S^{-1}	V_{C-link}	$\sqrt{d'_S} I_S$	$\frac{\sqrt{d'_S}}{d_S}$
Q_L^1	V_{C-link}	$\sqrt{d_L} I_L$	$\frac{1}{\sqrt{d_L}}$
Q_L^{-1}	V_{C-link}	$\sqrt{d'_L} I_L$	$\frac{\sqrt{d'_L}}{d_L}$
Additional Devices			
Q_S^0	ϵ	$\sqrt{d_C + d_D} I_S$	$\frac{\epsilon}{V_S}\sqrt{d_C + d_D}$
Q_L^0	V_{C-link}	$\sqrt{d_D} I_L$	$\frac{\sqrt{d_D}}{d_L}$
			Note: $\frac{\epsilon}{V_S} << 1$, $\frac{d_D}{d_L} << 1$

Table 3.2 details the VA calculation comparison for buck mode of operation by extending

the results obtained in Table 3.1. It lists all the VA ratings of the conventional and the additional devices per-unitized (p.u.) over the input power. Even though the peak voltage ratings of the additional devices can be as high as the DC voltage value, the RMS current ratings will be a fraction of the ratings of the conventional power transistors. Consider a design example where the transition times are tuned to approximately $1\mu s$ for a 15kHz switching frequency. Here, the $\frac{d_D}{d_L} << 1$. Further, $\epsilon \rightarrow V_{C-link}$ Hence, $\frac{\epsilon}{V_S} << 1$. Hence, it is clear that the net VA rating of the additional devices is expected to be a fraction of that of the conventional devices.

3.1.2.5 Commutation Strategies

The main focus of Figures 3.6 and 3.5 is to illustrate the simplified switching function and basic operation of the SPTT switches in Figure 3.4. This section discusses the various PWM signals required to safely let the converter modules transition from one state to another.

Buck Mode Operation

During the buck mode of operation, the switches (MOSFETs) shown in Figure 3.4 get activated based on the input signal provided to the gate pin. Figure 3.9 shows the gate driver signals incorporating dead-time and overlap time durations to avoid commutation issues. Here, Q_y^x refers to device Q with state x, where $x = -1, 0, 1$, and y refers to source or the load-side where $y = S, L$.

Deconstruction of what happens during the commutation is shown in Figure 3.9 step by step. In the buck mode of operation, during t_C, the charge interval of the tiny capacitor, the source-side transistors transition as follows: S_S :"-1" $\rightarrow$ "0" $\rightarrow$ "1". In the conventional

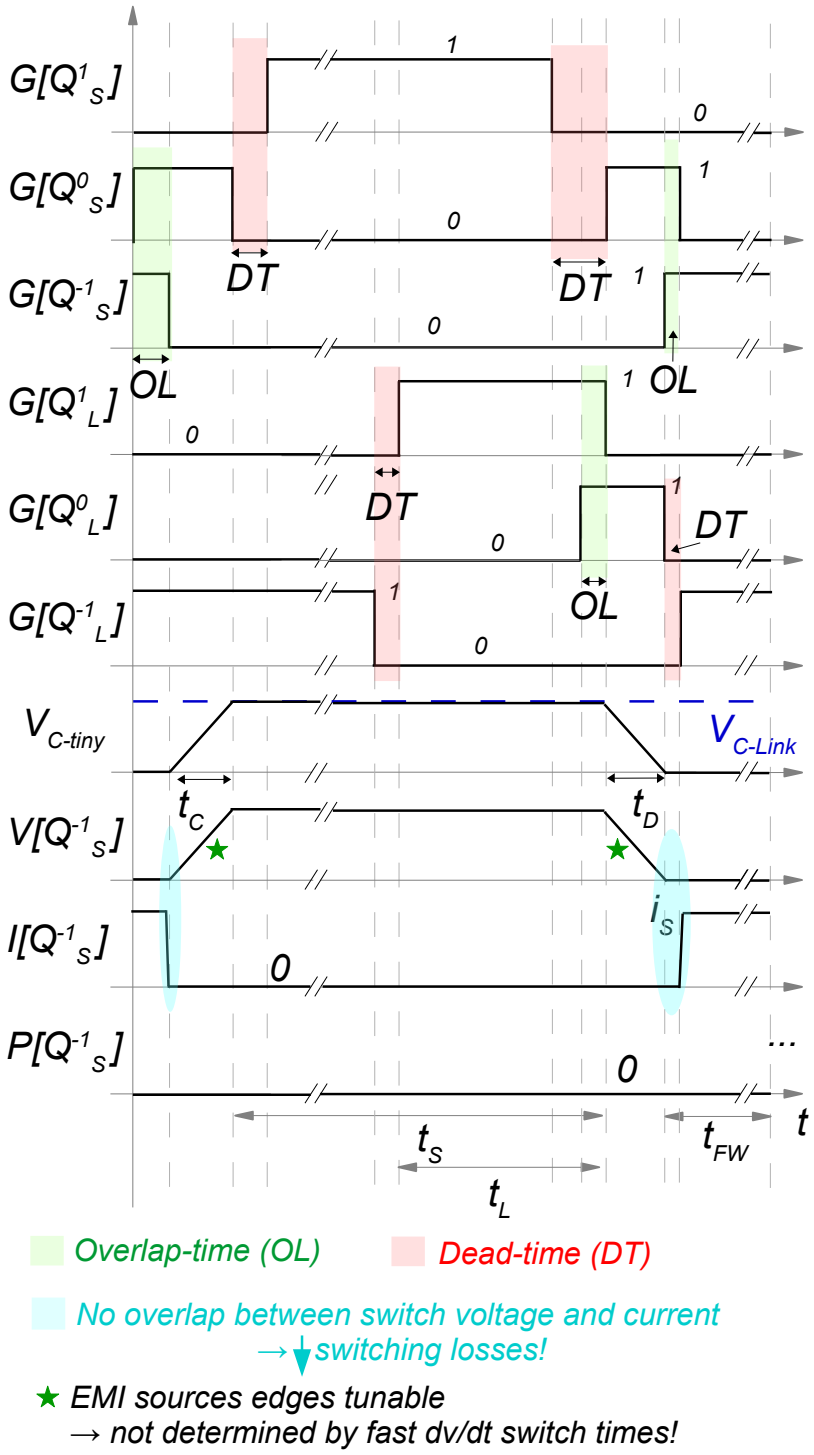

Figure 3.9: Waveforms of the gate signals of the source and load transistors ($G[Q_y^x]$, where $x = -1, 0, 1$ and $y = S, L$), tiny capacitor voltage (V_{C-tiny}), and the voltage, current and power waveforms of the source-side bottom transistor ($V[Q_S^{-1}], I[Q_S^{-1}], P[Q_S^{-1}]$) with buck mode of operation[21].

case, based on the direction of the source current, the bottom transistor Q_S^{-1} turns off, and the antiparallel diode of Q_S^1 turns on. That means, soon after $G[Q_S^{-1}] = 0$, and if the middle transistor (state "0") is not turned on, the antiparallel diode on the top transistor starts to conduct to provide a path for the stiff pole current. As noted in the figure, an overlap time (OL) during the transition from state "-1" $\rightarrow$ "0" is needed to reduce the duration for which this diode is active. The tiny capacitor starts to charge up only after $G[Q_S^{-1}] = 0$. As the tiny capacitor becomes fully charged, which happens When $V_{C-tiny} \approx V_{C-Link}$, the antiparallel diode of Q_S^1 becomes forward-biased and turns on. Hence, to avoid shorting the tiny capacitor, $G[Q_S^1] = 1$ only after a dead-time (DT) interval. This diode's characteristics can affect the switching transition edge quality and lead to unwanted overshoots or undershoots. This is not an optimum situation, which could lead to more losses and heating up of the device. Hence, choosing the appropriate duration of dead time is also crucial.

During the discharge interval of the tiny capacitor (t_D), the transition of both S_S and S_L :"1" $\rightarrow$ "0" $\rightarrow$ "-1" occurs. For the source-side converter, the switch transition involves the turn-off of the top switch. However, the current will still be conducting through the antiparallel diode. Therefore, a dead-time must be provided before activating the middle switch, which is marked in between $G[Q_S^1]$ and $G[Q_S^0]$. When the middle switch ($G[Q_S^0] = 1$) becomes active, the switch diode becomes reverse-biased, and the switch starts to conduct. Finally, during the "0" $\rightarrow$ "-1" phase, where the middle switch turns off, and the bottom switch is activated, an overlap time is provided to provide the turn-on of the top switch antiparallel diode. Here, the discharge interval (t_D) starts with the turn-off of Q_L^1, after

which the load current begins to discharge the tiny capacitor via Q_L^0. When $V_{C-tiny} \approx 0$ marks the end of the discharge phase, the antiparallel diode of the bottom switch turns on and takes over. The main role of the diode of the device Q_L^0 in Figure 3.8 is to block the small voltage difference ϵ when the load-side is in the active state. Next, consider the load-side half-bridge transistor. Here, the device transition involves the turn-off of the top switch and the turn-on of the antiparallel diode of the bottom switch. As soon as the control signal $G[Q_L^1] = 0$, and the state "0" transition is not switched on, the antiparallel diode of the bottom switch starts to conduct to provide a path to the stiff load inductor current. Therefore, this transition from "1" $\rightarrow$ "0" needs an overlap time (OL) as shown in the figure, followed by a dead-time before turning on the bottom switch signal $G[Q_L^{-1}]$. During this entire process, the transition edges of the voltage signal of $V[Q_S^{-1}]$ are being tuned or reshaped and, hence, making it possible to tune the EMI due to the fast transition charastricts of the device used. The transition edges being tuned are marked by a green star symbol in Figure 3.9.

3.1.3 Summary

One of the crucial features of the several switch transitions associated with the proposed state "0" is that they occur under ZVS. Figure 3.9 highlights ZVS operation for the source-side bottom switch, Q_S^{-1}, during buck mode of operation. This ZVS is achieved with the charging and discharging of the tiny capacitor. During the case where the bottom switch is "on," no current transfer happens to the load-side, and the moment this switch turns off, the middle switch Q_S^0 takes over and slowly charges the tiny capacitor from 0V to V_{C-tiny}.

Table 3.3: Zero-voltage switching instances with the proposed approach for boost and buck mode of operation [21].

Mode	State	source-side	load-side
Boost	$S_{-1} \rightarrow S_0$	S_{-1} ZVS off, S_0 ZVS on	
	$S_0 \rightarrow S_1$	S_0 ZVS off, S_1 ZVS on	
	$S_1 \rightarrow S_{-1}$	Hard switching	-
	$S_1 \rightarrow S_0$	-	S_1 ZVS off S_0 ZVS on
	$S_0 \rightarrow S_{-1}$	-	S_0 ZVS off S_{-1} ZVS on
Buck	$S_{-1} \rightarrow S_0$	S_{-1} ZVS off S_0 ZVS on	-
	$S_0 \rightarrow S_1$	S_0 ZVS off S_1 ZVS on	-
	$S_{-1} \rightarrow S_1$	-	Hard switching
	$S_1 \rightarrow S_0$	S_1 ZVS off, S_0 ZVS on	
	$S_0 \rightarrow S_{-1}$	S_0 ZVS off, S_{-1} ZVS on	

The voltage across the tiny capacitor V_{C-tiny} is close to the bus voltage V_{C-bulk}. Next, when the source-side top switch becomes active, the switching transition happens between two nodes with a voltage difference close to 0V, leading to ZVS operation. Similar to the above case, when the tiny capacitor discharges, the source-side bottom switch (Q_S^{-1}) is "off" before the t_D and blocks the bus voltage, V_{C-bulk}. The bottom switch is turned on only after the source and load-side middle transistors discharge the capacitor to 0V. Further, the simultaneous occurrence of the high current conduction and high voltage blocking state is eliminated in this switching instance. This method can be extended to other switching

transitions and modes of operation. Table 3.3 summarizes all the ZVS instances. Note that of all the switching transitions, those that occur between states "-1", "0," and "1" are under ZVS operation. In other words, out of the four fast transitions of the switching voltages V_{Sp} and V_{Lp} of classical operation, three transitions can be tuned to the desired slope rate. In summary, the proposed method reduces switching losses while simultaneously reducing the electromagnetic noise by tuning the fast edge rates. The analytical results obtained from laboratory-scale working prototypes are discussed in Chapter 5.

$$V[Q_S^{-1}] = \underbrace{d_S V_{C-Link}}_{\textit{power transfer}} + \sum_{n=1}^{\infty} 2 d_S V_{C-Link} \left| \frac{sin(n\pi d_S)}{n\pi d_S} \right| \left| \underbrace{\frac{sin(n\pi t_t/T_{SW})}{n\pi t_t/T_{SW}}}_{\substack{\textit{Conv.: } t_t\textit{=rise/fall time} \\ \textit{Prop.: } t_t\textit{=tuned interval}}} \right| cos(n\omega t + \phi) \quad (3.13)$$

Equation (3.13) characterizes the noise spectrum and illustrates the advantages of tuning the transition time intervals [21]. Unlike the conventional case where the transition time t_t is determined by the inherent rise/fall time of the switch, in the proposed control approach, t_t can be tuned. This transition time is indirectly proportional to the magnitude of the voltage spectrum. The longer the transition time, the lower the magnitude for higher frequencies.

3.2 DC-AC Converters

The DC-AC three-phase converter topology is derived from the DC-DC topology in Figure 3.4 presented earlier in this chapter. In Figure 3.10, it is evident that the main difference compared to the DC-DC converter is the addition of two more half-bridge modules. A

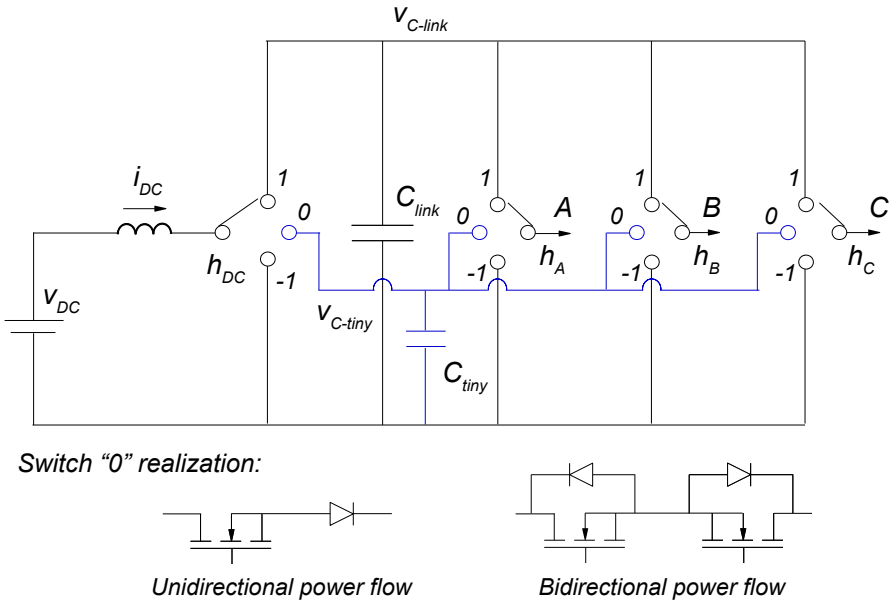

Figure 3.10: The Proposed case DC-AC three-phase topology [21].

DC-AC three-phase converter topology can be assembled with at least four half-bridge modules. The blue trace shows the additional modification needed for the proposed topology in contrast to the conventional three-phase topology. The tiny capacitor is connected to all the half-bridge modules, and all the modules must be controlled synchronously to achieve the proposed control. Based on the application requirements, the middle transistors can be realized for unidirectional or bidirectional power flow, as shown in the bottom part of Figure 3.10. These additional transistors have to be rated for the full DC-link voltage. However, since they are active for only a fraction of time (in the range of 1-4 μs in the design examples considered in this thesis document), the net current rating can be chosen to be a small value compared to the conventional top or the bottom power devices.

A simple circuit schematic for a DC-AC three-phase converter capable of bi-directional power transfer is shown in Figure 3.11. Note that the circuit modifications compared to

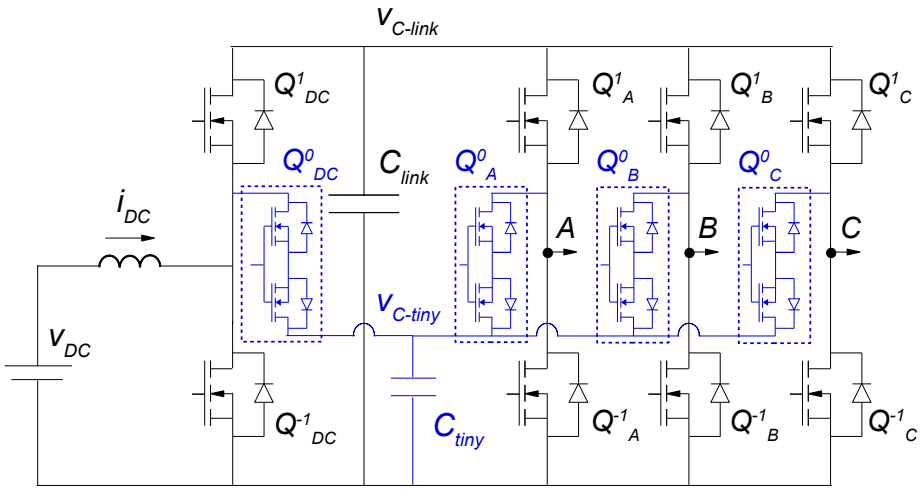

Figure 3.11: Circuit schematic for the proposed DC-AC power conversion [21].

conventional topology are highlighted in blue.

3.2.1 Operation

The control signals for operating all the devices on each model are generated using Space Vector Modulation (SVM). It is one of the widely adopted techniques in the industry. The proposed control implementation can be achieved with minor modifications to the algorithm. The technique is further described in detail in the sections below.

3.2.1.1 Space Vector Modulation

Space Vector Modulation (SVM) is used in power electronics and motor control to generate the switching signals for multi-level inverters. In SVM, the reference voltage vector, which represents the desired output voltage waveform, is synthesized by combining the three-phase inverter voltage vectors. These voltage vectors are described in a mathematical space called the "space vector" plane, where the vectors are positioned to create the desired output

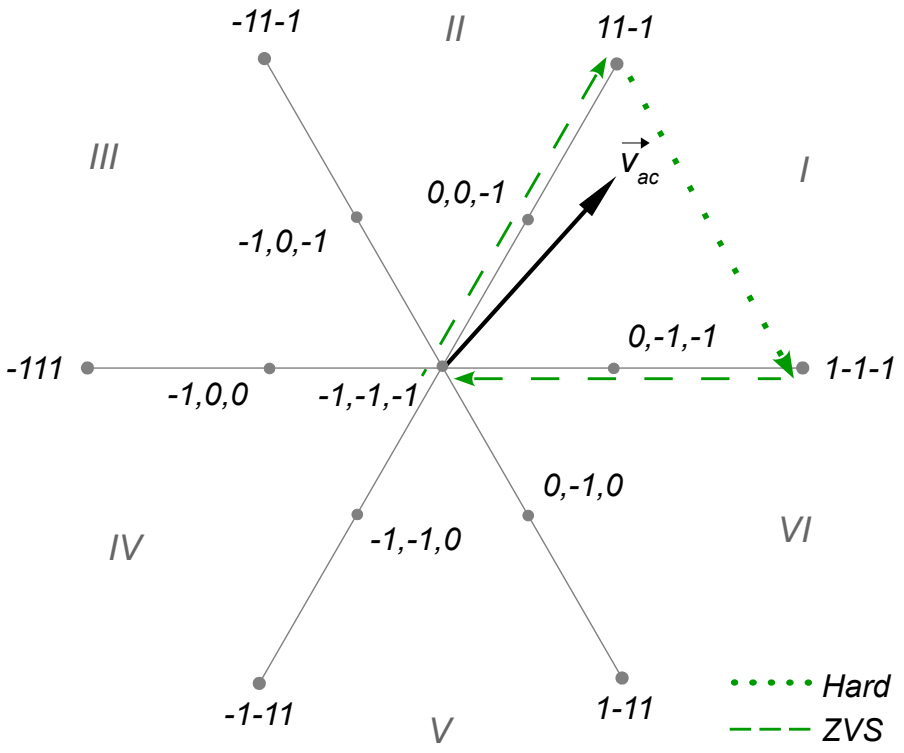

Figure 3.12: Space vector diagram for the AC inverter operation with the proposed PWM method [21].

voltage. SVM offers advantages such as improved voltage utilization, reduced harmonic distortion, and better dynamic performance than other modulation techniques. It is widely used in high-performance motor drives and other applications where precise control of voltage and current is essential.

This principle of SVM can be extended to generate the control signals for the addition of middle transistors (state "0"). Figure 3.12 shows the space vector diagram with the additional state vectors for the proposed case. The entire vector space is divided into six sectors. The Alternating Current (AC) phase A is aligned with the horizontal x-axis of the diagram. The AC vector $\upsilon_{ac}^{\rightarrow}$ is shown in Sector I of operation. The state of each phase for the conventional switching strategy is shown on the outer edge of the with states "1" and

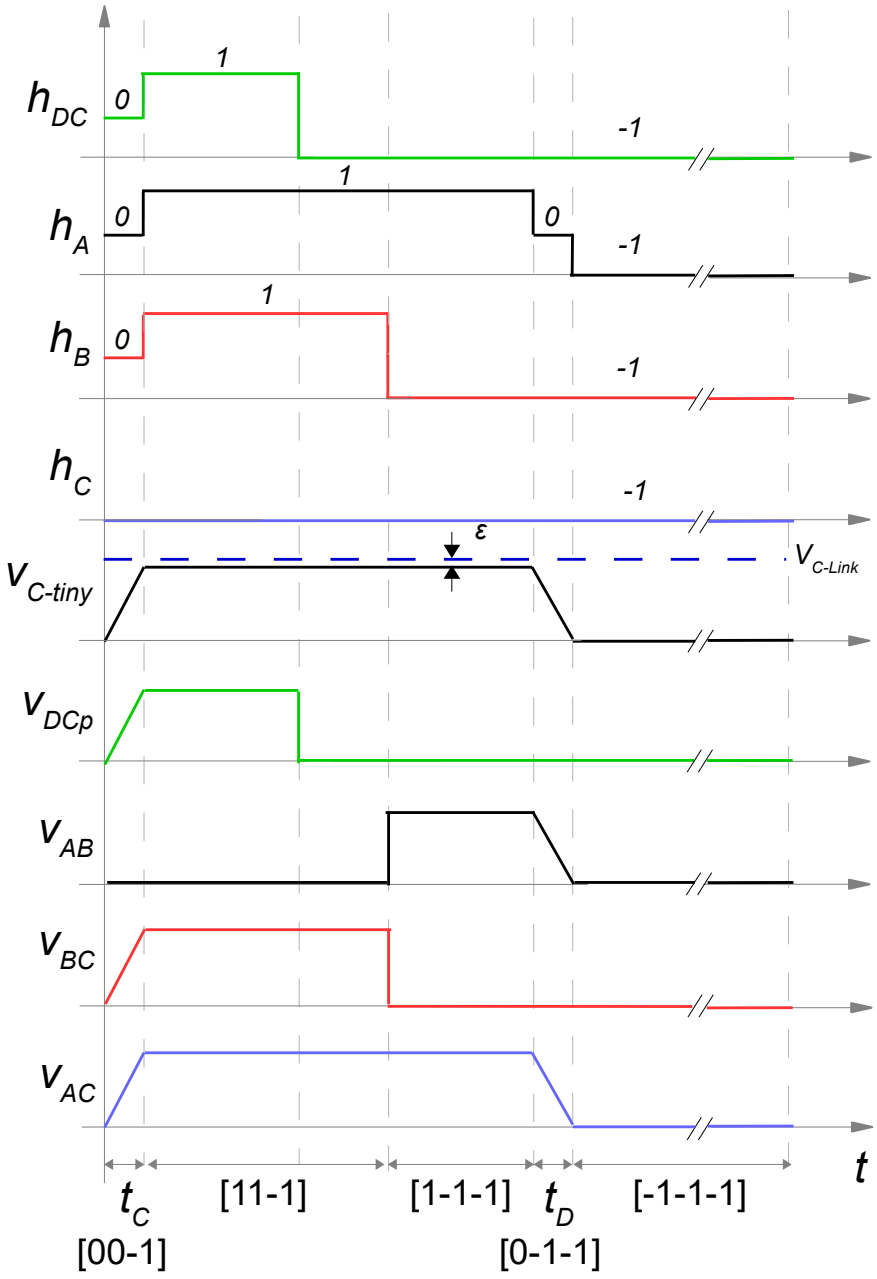

Figure 3.13: Switching waveforms for DC-AC conversion for one sector of operation[21].

"-1" where [A, B, C] is the convention phase followed. Similarly, the proposed space vector states are illustrated in the inner region with the additional state "0". During sector I of conventional operations, the nearest space vectors [11-1] and [1-1-1] are typically chosen.

However, the proposed method adds extra space vectors with a "0" state at the beginning and end of the active space vectors. For example, during sector I, the state vector sequence will have the following sequence: [-1-1-1] $\rightarrow$ [00-1] $\rightarrow$ [11-1] $\rightarrow$ [1-1-1] $\rightarrow$ [0-1-1] $\rightarrow$ [-1-1-1]. The figure highlights the transition between several state vectors using dotted and dashed green arrow lines. The transition on the outer edge is under hard switching conditions, as shown by the dotted line. On the other hand, the remaining transitions have been optimized for the tuned dv/dt rate and ZVS operation. The space vector transitions can be clockwise or counterclockwise and are based on minimizing DC-link capacitor voltage ripple, reactive power minimization, and loss minimization, among other conventional optimized functions.

Figure 3.13 shows the switching functions corresponding to the state vector diagram in Figure 3.12. It also displays the pole voltage of the DC and AC transistors during the first sector of operation. The figure shows how the switch state "0" is combined with the DC and AC phases, where the "0" state is added to the beginning or end of the switching functions (h). Additionally, the AC line-line voltages are illustrated.

Four of the six switching transitions can be tuned using the C_{tiny} capacitor. The DC switching state is sequenced with the first active AC state vector to charge the tiny capacitor C_{tiny}. Similar analysis can be extended to the remaining sectors of the space vector diagram.

3.3 Summary

This chapter discusses the proposed PWM control strategy, which enables the reduction of EMI and switching losses in switching power converters. The chapter also discusses the

considerations and goals for designing laboratory-scale prototypes to confirm the feasibility of the proposed control strategy. A detailed explanation of DC-DC and DC-AC converter topologies and their control implementation are discussed. The conventional approach for DC-DC converters is explained, along with the modified topology to accommodate the proposed control approach. The next chapter discusses the design of an open loop control implementation for experimental verification for all the cases mentioned in this chapter.

4 Results & Analysis

4.1 Experimental Test Setup

The working principle of the proposed control methodology described in the former chapter has been simulated for a DC-AC three-phase topologies in the PLECS circuit simulator environment. The design parameters include power throughput $P = 3kW$, DC voltage $V_{DC} = 200V$, AC voltage $V_{AC} = 208V$ with 60Hz output frequency, DC-link voltage $V_{C-link} = 400V$ and $f_{SW} = 15kHz$. The simulation results are discussed in [20]. The results from the simulation were promising, and to understand the real-world performance of the proposed approach, device behavior in-particular, laboratory-scale prototypes were designed to test both DC/DC and DC/AC converter topologies.

The main goals for conducting the experimental tests are to:

- Evaluate the performance of the proposed control strategy against the conventional switching method for DC-DC and DC-AC power converters.
- Test the performances of the proposed control strategy against the traditional method of switching on converter modules designed using high-power silicon MOSFET.
- Test the performances of the proposed control strategy against the conventional switching method on converter modules designed using a combination of high-power

and low-power silicon MOSFET.

- Test the performances of the proposed control strategy against the conventional switching method on converter modules designed using a combination of high-power WBG devices such as SiC and low-power silicon MOSFET.

- Compare the conducted EMI performance of the new control strategy against the conventional switching method.

- Provide quantitative analysis data on the performance of the proposed control strategy over conventional hard switching for all the cases.

4.1.1 Hardware Implementation

Two sets of laboratory test setups are used to confirm the feasibility of the proposed control strategy. In the first setup, Si devices are used to realize the switches. A detailed explanation can be found in Section 4.3. In the second setup, switches are realized with a combination of SiC and Si devices. The primary switches of the half-bridge are realized using SiC devices, and the additional throw with state "0" is realized using Si MOSFET rated for lower power. Also, note that low power SiC devices with smaller footprints were not commercially available to realize the middle switches during converter design. Using the same devices as the top or bottom switch is not optimal, as the middle switch carries only 1-2% of the total rated current. Hence, using low power MOSFETs with a smaller footprint is preferred.

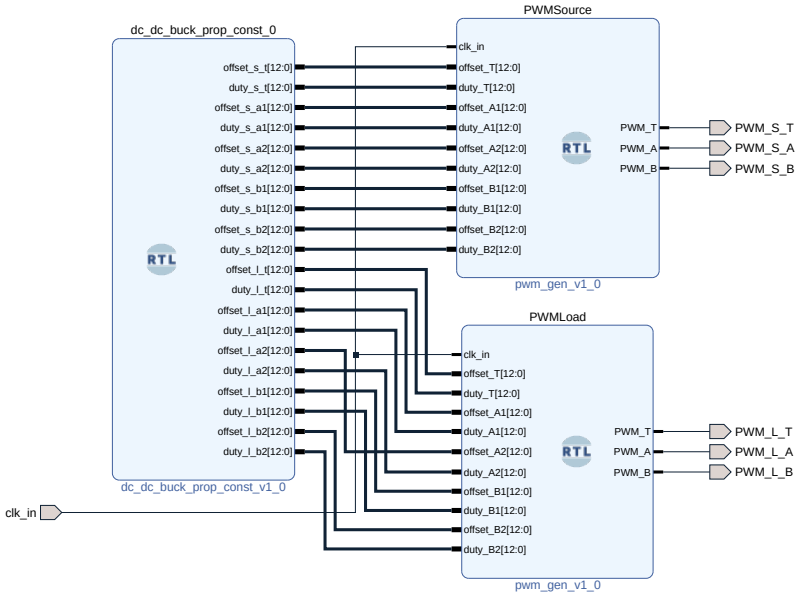

Figure 4.1: Vivado IP integrator Block Diagram for DC-DC Buck mode proposed case setup

4.1.2 Control Implimentation

An open loop control system is implemented on a field-programmable gate array (FPGA) development board to simplify the design and control implementation. A PYNQ-Z2 FPGA development board based on the Xilinx Zinq 7000 SoC is used in both setups. The development board was readily available in the lab and had sufficient I/O pins implementing the open-loop PWM control. Working with an FPGA development board also provides flexibility, reconfigurability, and ease of implementation, as the hardware limitations of a microcontroller won't affect the controller implementation.

The control implementation varies based on how the system needs to be configured. For example, four PWM signals are required for the DC-DC conventional converter system to

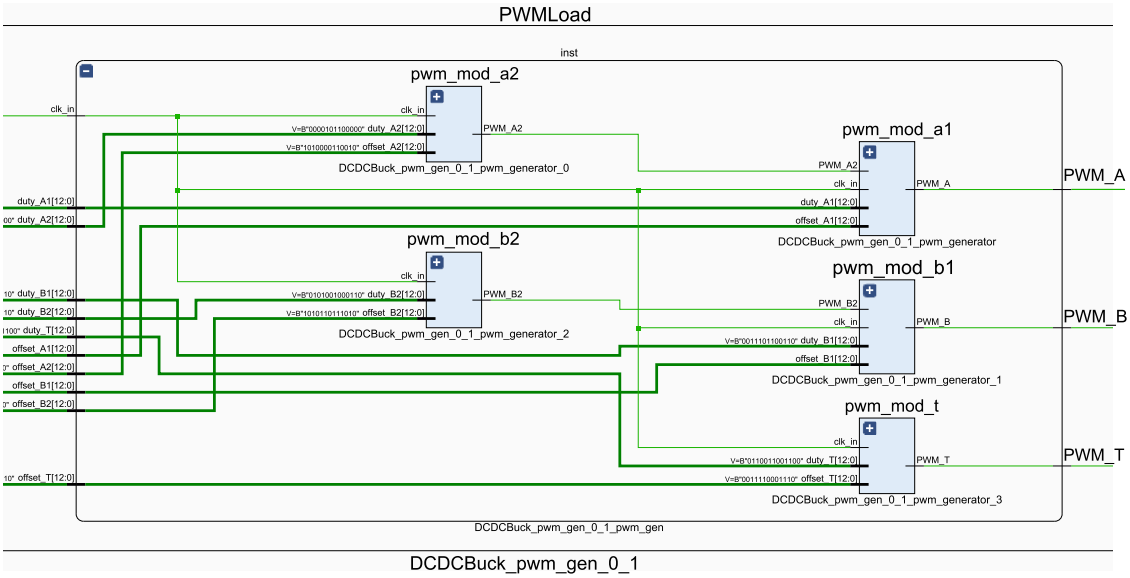

Figure 4.2: Schematic view of proposed case load side PWM generator block

meet the functionality. However, one additional control signal per half-bridge is necessary for the proposed case topology to control the middle transistors.

Figure 4.1 depicts the block diagram for the controller implementation. The implementation uses a hierarchical design flow and using custom module blocks. The module titled “dc_dc_buck_prop_const_0", as the name describes, holds the duty values for the PWM signals that need to be generated. It interfaces with two PWM generation blocks that generate the necessary PWM control signals. Both modules are synchronized using the 125MHz master clock. Here, the PWM control signals labeled "PWM_S_A" control the sources side middle transistor, and "PWM_S_B" control the load side middle transistors. These are the two additional control signals needed in the proposed topology compared to the conventional topology.

Breaking it further down, a second module titled "pwm_gen_v1_0 module" in Figure 4.1

consists of multiple PWM modules as shown in Figure 4.2. Multiple sets of control signals can be designed using the same PWM generator block. The key advantage of using an FPGA is that all these individual PWM bocks run parallelly, leading to precise synchronization among each control signal.

4.2 Experimental Results with Silicon Devices

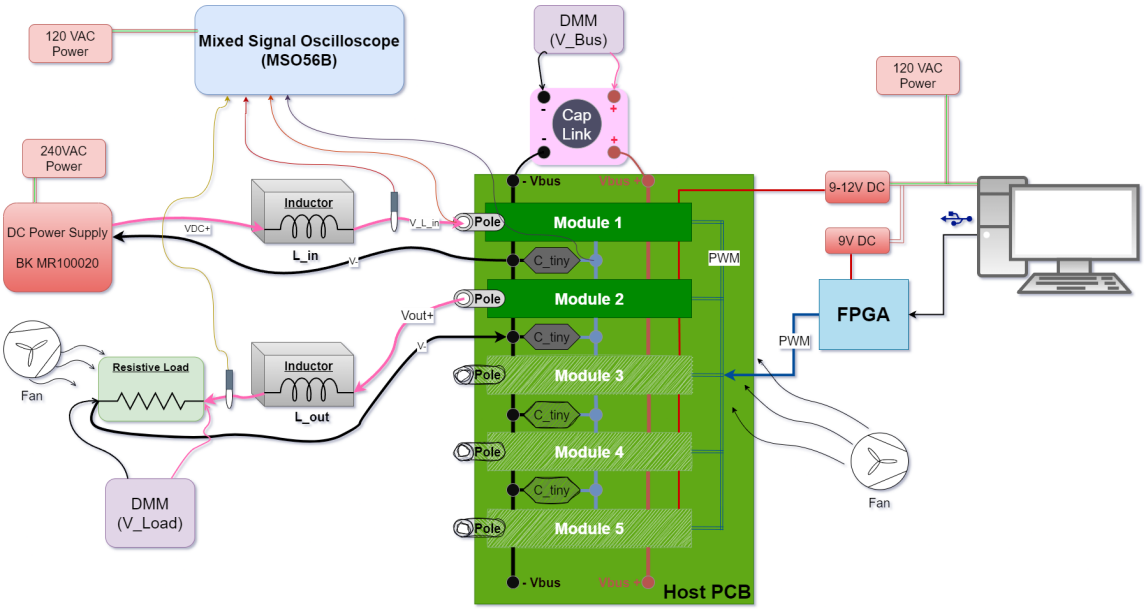

Figure 4.3: Test setup block diagram showing how the system is configured to test a DC-DC converter populated with half-bridges designed using Si MOSFETs.

Figure 4.3 shows the Si test setup architecture. It comprises of the high voltage Direct Current (DC) source, the Device Under Test (DUT) or the power converter setup, which involves half-bridge modules, a host Printed Circuit Board (PCB) for interfacing multiple half-bridge modules, and a controller board for generating the PWM control signals. Wire-wound resistors rated for $1000W$ each provide the resistive load for the setup. A Mixed Signal Oscilloscope (MSO) and Digital Miltimeter (DMM) are used to measure various

Table 4.1: List of power supplies used in the test setup

Item	Manufacture	Model Number	Key Parameters
High Power DC Supply	BK Precision	MR100020	5000W, 1000V, 20A
Auxiliary DC Supply 1	BK Precision	1688B	360W, 1-18V, 0-20A
Auxiliary DC Supply 2	BK Precision	9104	320W, 1-84V, 0-10A
Auxiliary DC Supply 3	Korda	KD3005D	150W, 0-30V, 0-5A
Auxiliary DC Supply 4	Tri-Mag, LLC	L6R36-090	36W, 9V

parameters such as voltages and current signals. Additional low-power bench DC power supplies and wall adaptors provided the auxiliary DC power needed to power the controller board and control logic on the half-bridge modules. The details of various power supplies used in the experimental setups can be found in Table 4.1. Cooling fans ensure a steady air flow to keep the resistors and switching devices from overheating.

The primary input DC source is a BK precision benchtop high-voltage multi-range DC power supply. It can provide $5kW$ power with a max voltage of 1000V or 20A current. It is a versatile power supply used in various research and testing facilities. A modular design approach is taken while designing the power converter prototype, which allows more flexibility in testing and debugging issues. The host PCB is designed to receive multiple daughter cards (half-bridge modules) that can be easily modified to fit the requirement for the topology that needs to be tested. This approach provides a one-fit for all testing rigs that can test conventional and proposed control strategies with minor modifications. The FPGA development board met the desired number of I/O pins to generate all the PWM

signals needed to implement the control strategy. Working with an FPGA provides more flexibility in generating the required PWM control signals. The primary instrument used for measurement is the Tek MSO56B series, a 1GHz bandwidth MSO capable of meeting all the testing requirements. The detailed list of instruments and probes used for the measurement is provided in Table 4.2.

Table 4.2: List of instruments and probs used in the test setup

Item	**Manufacture**	**Model Number**	**Key Parameters**
Oscilloscope	Tektronix	MSO56	6-Channel, 1 GHz 6.25 GS/s
Multimeter	Keithley	DMM6500	6½ Digit Multimeter
Multimeter	Fluke	FLUKE-115	Auto True RMS, 600V, 10A
LISN	COM-Power	LI-125C	150 kHz - 30MHz, 50 Ohm, 50 uF 25A, 400V
Current probe	Tektronix	TCP0020	Current clamp probe 50MHz
Voltage probe	Tektronix	THDP0200	HV differential probe 200 MHz
Voltage probe	Tektronix	TPP0850	1000 V 800 MHz passive probe
Voltage probe	Tektronix	TPP1000	300V 1GHz passive probe
IsoVu Probe	Tektronix	TPVP02	Optically Isolated, 200MHz
Logic Probe	Tektronix	TCP058	8 channel Logic prob

4.2.1 DC-DC Testing

The host board is populated with two half-bridge modules to test the performance for a DC-DC boost-buck or a boost-boost topology, as shown in Figure 4.3. It is designed so that either of the daughter modules (half-bridge modules) can operate as a source-side converter,

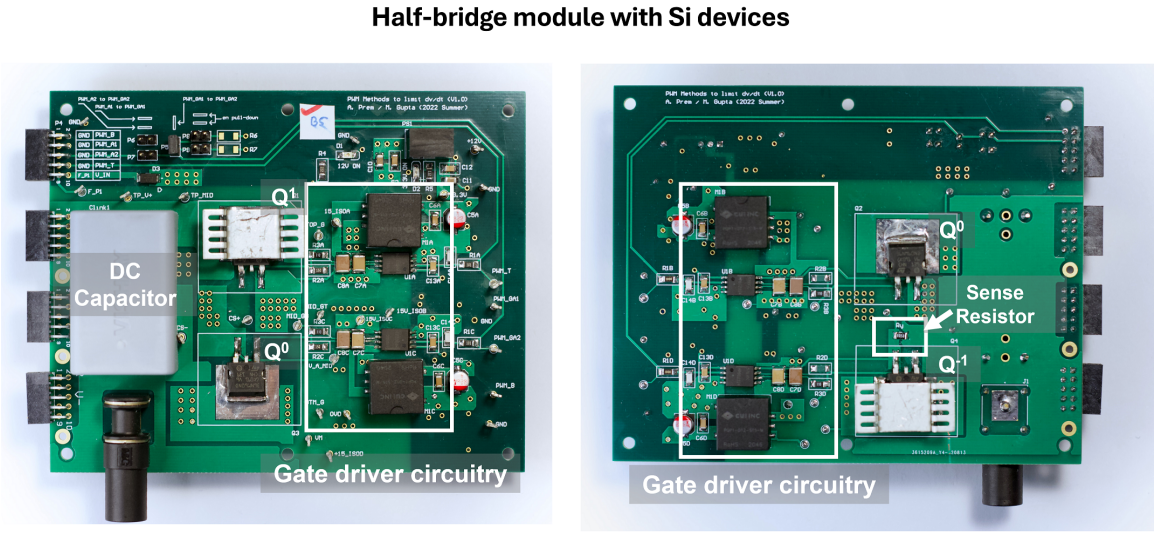

Figure 4.4: The prototype half-bridge module using Si devices

and the second module acts as a load-side converter based on probing convenience. The conventional and proposed PWM modulation approach is run on the converter setup.

The close-up view of the top and bottom sides view of one of the half-bridge modules with Si devices is shown in Figure 4.4. The top side device Q^1 is placed on the top side of the PCB, whereas the bottom side switch Q^{-1} is on the bottom side of the PCB. The middle switch is realized using two MOSFETs marked as Q^0. Notice that these two devices do not have a heatsink as it transfers only 1-2% of the total power handled by the other two (Q^1 and Q^{-1}) primary devices. A DC-link decoupling capacitor is also placed close to the devices to eliminate as much ringing as possible. The list of key components used is listed in Table 4.3.

Table 4.3: List of the manufacturer part numbers used in the laboratory-scale prototype 1 with Si bases half-bridges

Parameter	Manufacturer Number	Key Ratings
Si MOSFET	STB36NM60ND	650V, 29A, $R_{DS} = 0.11\Omega$, $t_r = 53.4ns$, $t_f = 61.8ns$, $t_{rr} = 175ns$
Gate Driver	NCD57090CDWR2G	Isolated, 6.5A Output
Bulk Capacitor	ALA7DA331CE500	500VDC, 330μF
C-link Decouplning	MKP1848SE61090JP4F	900VDC, 10μF
Tiny Capacitors	R76TF12705050J	650VDC, 2.7nF
Filter Inductors	C-59U	10mH, 12.5A

Figure 4.5 to Figure 4.8 show the experimental results from the converter under buck mode of operation, handling roughly $400W$ to $420W$, respectively. The converter switching frequency is about $f_{SW} = 15kHz$, and a 22Ω resistor, rated for 1000W, is used as the output load. The bus voltage measured across the link capacitor is about $V_{C-link} = 350V$, and the measured operating parameters for both proposed and conventional cases are provided in Table 4.4.

Figure 4.5 shows the contrast between the rise time and fall time for conventional and proposed approaches measured across the source side bottom switch Q_S^{-1} during the switch turn-off and turn-on event. In the proposed approach plot (shown in green), the switch transition time is *tuned*. The figure shows that the slope rate is designed to be 350V/1μs, whereas in the conventional case, the slope falls at 350V/50ns and rises at 350V/52ns, which is determined by the inherent device properties along with the default gate driver circuitry. These parameters are close to the inherent transition characteristics provided by the device manufacturer's datasheet. The effects of these fast transitions can be easily observed in the Pole Current (bottom Figures of 4.5). It is clearly visible that in the proposed case (green

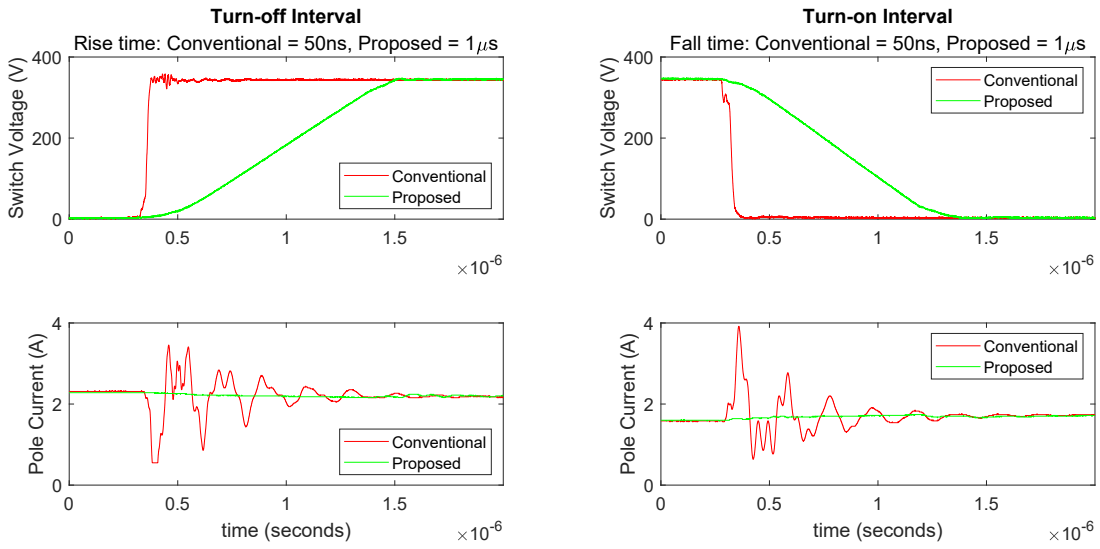

Figure 4.5: Experimentally measured Q_S^{-1} switch turn-off (left) and turn-on (right) transition with the conventional (red) and the proposed (green) approach where the voltage transition time is 50ns and 1μs respectively. The bottom waveforms illustrate noise propagation to the pole current (i_S) with the conventional (red) and the proposed (green) PWM method [21].

plot), the signal is significantly less noisy in contrast to the conventional switching method.

Figure 4.6 and Figure 4.7 illustrate the Fourier spectrum of the source-side switch voltage (Q_S^{-1}) and the pole current (i_S) during the DC-DC Buck mode operation of the converter. The operating points for the setup are the same as mentioned earlier in the section. The contrast between conventional switching (red plot) and the proposed switching strategy can be observed in both plots. Observing the source side pole voltage (also the voltage across Q_S^{-1}) spectrum plot, Figure 4.6, for the conventional case, the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\frac{1}{\pi t_t}$ (roughly 6.4MHz). This corresponds with the inherent transition time, roughly 50ns, of the Si switching device. In contrast, the proposed control method transition time is tuned to $1\mu s$. Hence, it can be observed that the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\approx$ 310kHz. Figure 4.7 shows the Fourier spectrum of the source side pole current, i_S, of Figure 4.5 (bottom plots). The noise

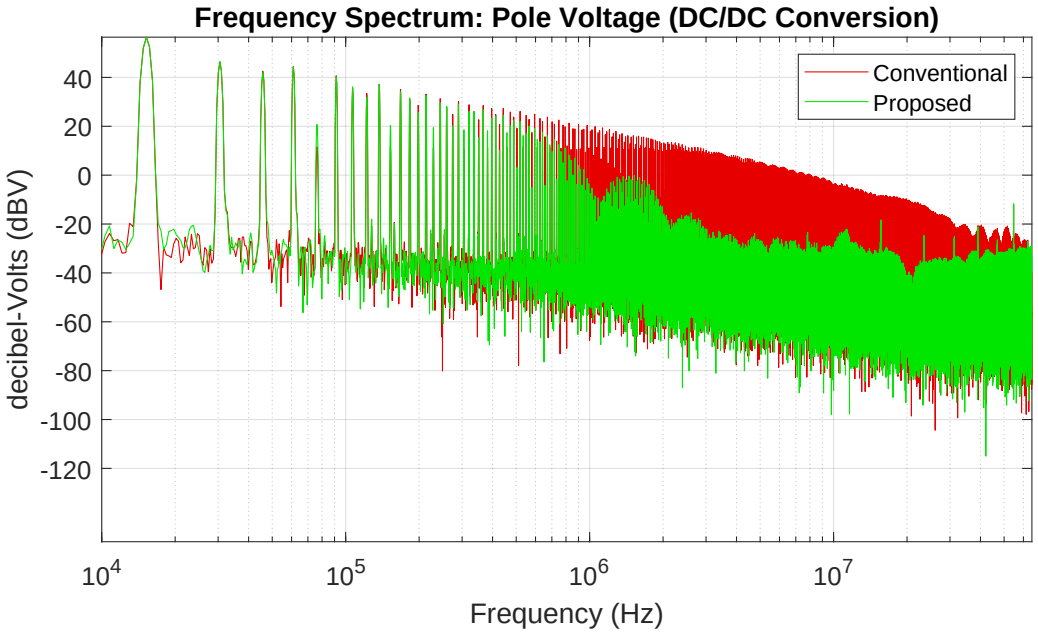

Figure 4.6: Experimentally measured frequency spectrum of the trapezoidal-shaped switch voltage (green) compared against the conventional case (red) [21].

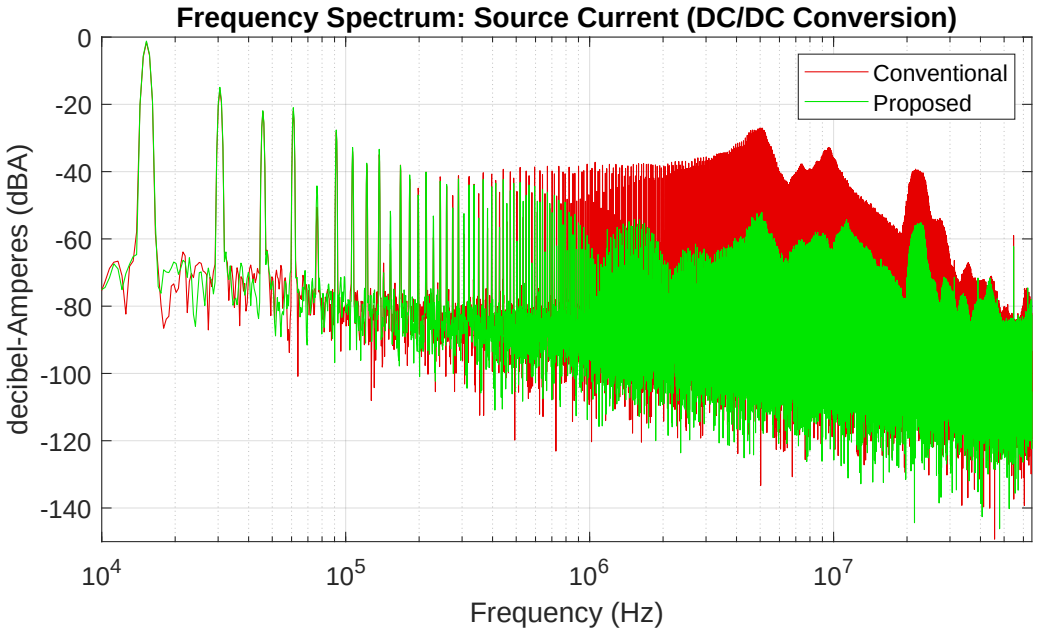

Figure 4.7: Experimentally measured frequency spectrum of the source current with trapezoidal-shaped pole voltages (green) compared against the conventional case (red) [21].

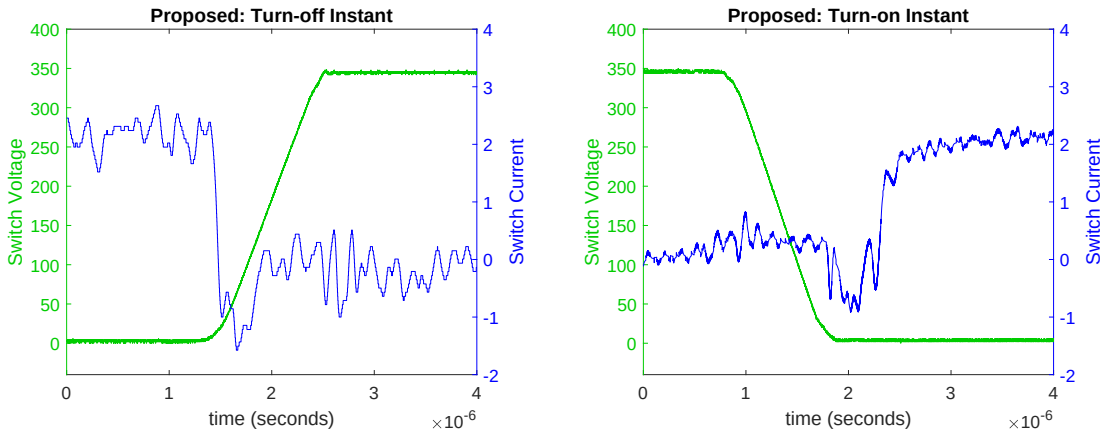

Figure 4.8: Experimentally measured switch voltage (green) and current (blue) waveforms during turn-off transition (left) and turn-on transition (right) illustrating zero-voltage switching operation on the silicon device test setup [21].

reduction observed in the time-domain waveforms from Figure 4.5 is readily confirmed from its Fourier spectrum plot. In summary, from these results, a 15dB to 20dB+ reduction of electromagnetic noise is observed in both pole voltage and pole current spectrum plots in the frequency range of 1MHz to 20MHz range in the proposed control approach compared to the conventional switching approach.

Unlike traditional EMI mitigation methods that increase system losses, the proposed approach can reduce switching losses through ZVS operation. The ZVS can be observed in the experimental waveform illustrated in Figure 4.8. The switch voltage is measured using a high bandwidth (1GHz) passive probe, and the switch current is measured with the help of a sense resistor. The voltage across the resistor is measured using an isolated probe. Since the resistance is a known value, the equivalent current can be calculated or observed on the scope. During the turn-off instance of the switch, it transitions from the conduction state to the blocking state with voltage support from the tiny capacitor. During this transition

instance, the pole current charges up the tiny capacitor first before the top switch becomes active. Since the current gets discharged to the capacitor quickly before the actual switching happens, the current and voltage waveforms do not cross each other during the switching, thereby reducing switching losses. Similarly, during the turn-on instance, the switch voltage transitions from the voltage-blocking state to the conduction state using the tiny capacitor. Again, during the transition instant, the pole current flows through the tiny capacitor (and the switch current is zero), eradicating any time instant simultaneously featuring both high current and high blocking voltage.

Table 4.4: List of measured parameters during buck mode of operation on Si DC-DC test setup.

Parameters	**Proposed**	**Conventional**
Vin	210 V	210 V
Iin	1.916 A	2.04 A
Pin	402 W	428 W
Vout	88 V	86.2 V
Rout	22 Ohm	22 Ohm
Iout	4 A	3.92 A
Pout	352 W	338 W
Measured Losses	*50 W*	*90 W*
Efficiency	*88 %*	*79 %*

The parameters measured during the DC-DC buck mode operation for both conventional and proposed switching methods are listed in Table 4.4. The total measured power loss for the whole setup for the conventional case is 90W with a conversion efficiency of 79%. Here, a net efficiency improvement of 9% with an overall converter efficiency of 88% for the proposed case scenario is observed.

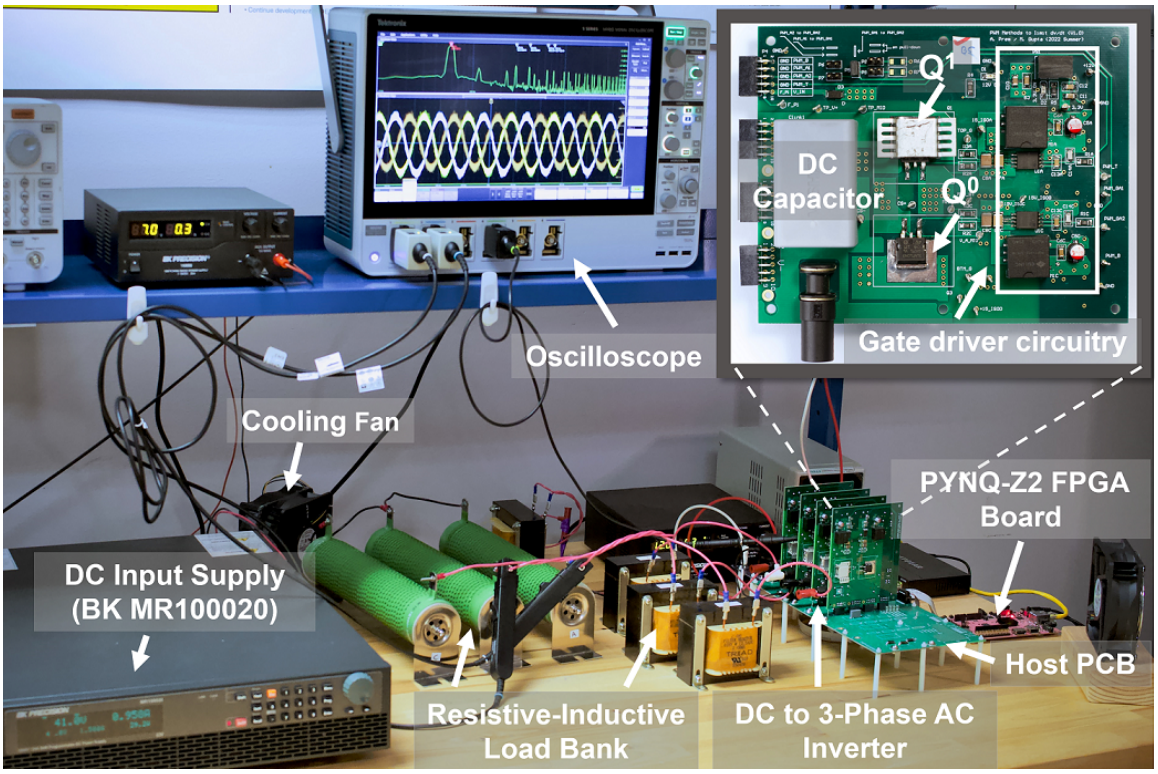

Figure 4.9: The prototype setup to test DC to 3 phase topology using Si devices [21].

4.2.2 DC-AC Testing

As mentioned in Chapter 3, the DC-DC topology can be easily ported to a 3-phase converter topology, as shown in Figure 3.10. Four half bridges need to be connected to the host PCB to configure the DC to 3-phase converter topology. In addition, some minor modifications, such as adding more C_{link} and C_{tiny} capacitors, are also needed on the host PCB. The FPGA development board is programmed to generate the appropriate PWM signals using SVM. The setup is optimized to operate at an input voltage of $v_S = 100V$, bus voltage $V_{C-link} = 200V$, AC output RMS voltage of $100V$, and switching frequency, $f_{SW} = 15kHz$. Figure 4.9 shows the setup configured to test the 3-phase topology.

The three-phase AC currents with the conventional (top plots) and the proposed (bottom

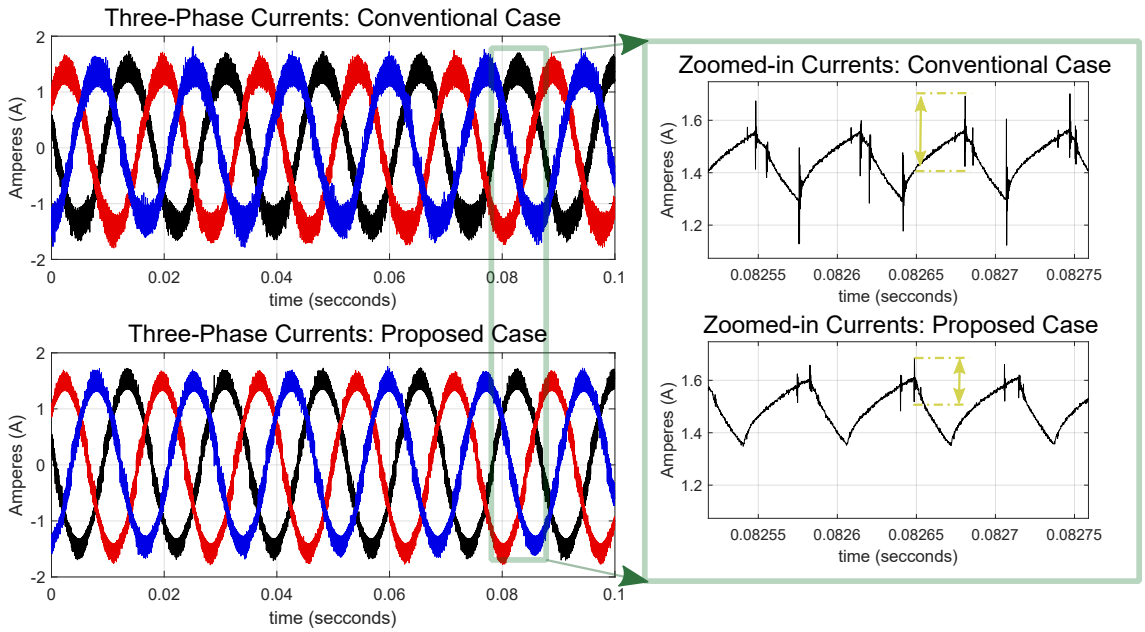

Figure 4.10: Waveforms of the three-phase AC currents with the conventional (top) and proposed (bottom) modulation strategy. [21]

plots) modulation strategies are presented in Figure 4.10. The zoomed-in version of a section of one of the phase currents (on the right) reveals that the current quality (less noisy) is improved for the proposed case, unlike the conventional case. This quality factor is quantitatively measured as Total Harmonic Distortion (THD), calculated using Equation 4.1, and the AC currents are measured to be 8.9% and 8.4% for the conventional and the proposed case, respectively.

$$THD = \frac{I_{RMS\_without\_fundamentals}}{I_{RMS\_fundamental}} \times 100 \tag{4.1}$$

This also confirms that the effects of EMI noise due to the tuning of the pole voltage transitions reduce the high-frequency noise in the pole current during the switching instances.

Figure 4.11 illustrates the Fourier spectrum of an AC side switch voltage for the entire switching period of 60Hz with the conventional space-vector PWM (red) and the proposed

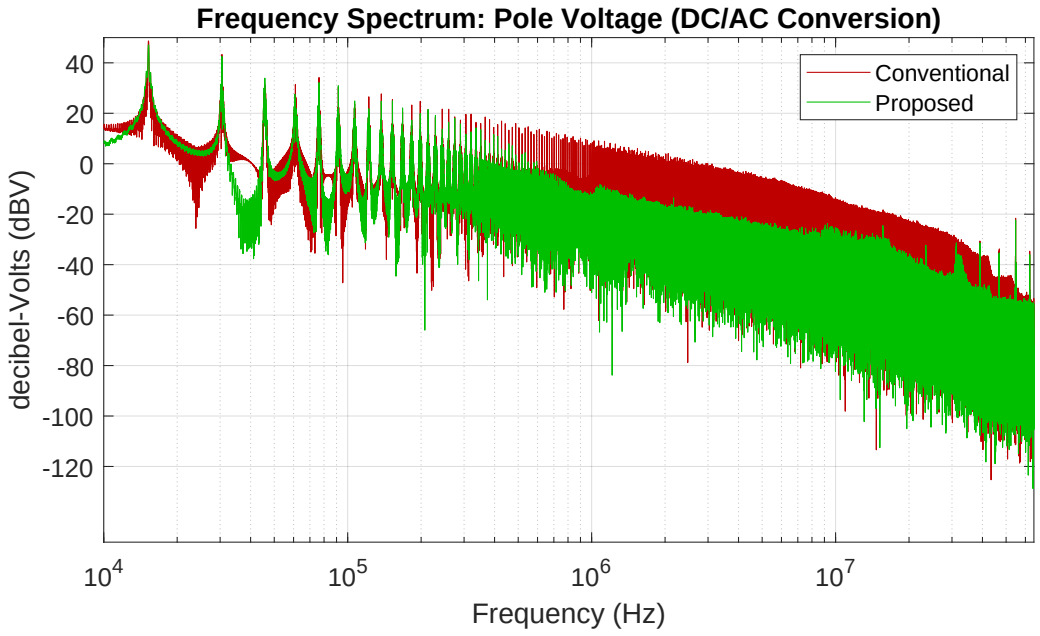

Figure 4.11: Experimentally measured frequency spectrum of the trapezoidal-shaped switch voltage (green) compared against the conventional case (red) [21].

space-vector PWM method (green), respectively. Similar to the DC-DC case, the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\frac{1}{\pi t_t}$ (roughly 6.4MHz). On the other hand, with the proposed space-vector PWM method, the AC pole voltages feature pseudo-trapezoidal or trapezoidal shapes, as discussed in Section 3.2.1.1. Here, the spectrum is about 10dB to 20dB quieter in 800kHz to 20MHZ frequencies for the proposed case compared to the conventional case.

4.2.3 Summary

While 75% of the edges are tuned in DC-DC conversion, 62.5% of the edges are tuned in DC-AC conversion. Hence, higher efficiency improvements with DC-DC conversion are expected. However, there is a slight variation in the power levels and operating points at

Table 4.5: List of measured parameters and efficiency calculation for the DC-AC conversion operation of the test setup with half-bridges realized with Si MOSFET

Parameters	**Proposed**	**Conventional**
V_{in}	100 V	100 V
I_{in}	2.2 A	2.26 A
P_{in}	220 W	226 W
R_{L_A}	56.33 Ohm	56.33 Ohm
R_{L_B}	54.69 Ohm	54.69 Ohm
R_{L_C}	54.94 Ohm	54.94 Ohm
I_{out_A}	1.03 A	1.06 A
I_{out_B}	1.08 A	0.99 A
I_{out_C}	1.11 A	1.05 A
Pout (total)	191 W	177 W
Measured Losses	*29 W*	*49 W*
Efficiency	*87 %*	*78 %*

which the DC-DC and DC-AC are tested. The efficiency improvement observed in both cases is comparable. The parameters measured from the DC-AC setup are listed in Table 4.5.

From the above experiment setup, about 8-9% improvement in overall converter efficiency in both DC-DC and DC-AC topology is observed along with about $15 - 20dB+$ reduction of noise in the frequency range of $1MHz$ to $20MHz$ in both pole voltage and current frequency spectrums. This opens an avenue for testing with other commercially available devices such as IGBT devices and WBG devices such as SiC and GaN devices. The WBG devices can operate at high temperatures, voltages, and frequencies with faster turn-on/off periods, improving converter performance over Si devices used in conventional system designs. So, with this proposed control method, SiC based converter system should yield even higher performance and mitigate EMI issues due to the reduced dv/dt rates.

During the tuning process of the fast transitions, the middle switches are active only for a

brief period. Hence, these switches can be realized using devices rated for lower power and smaller footprints. This opens up another way to test how well the converter would perform when using low-power and inexpensive transistor devices. To understand their feasibility, a pair of half-bridges were assembled, and the middle switches were realized using a low power MOSFET. With careful tuning and optimization, the test ran successfully.

4.3 Experimental Results with Silicon Carbide Devices

Drawing from the experience gained by designing and testing with the Si device-based setup, a revised PCB is designed. The second set of the test setups is designed to understand how the new control method would impact the performance of the converter when SiC switches are used instead of regular Si MOSFETs. A new set of components was selected to fit the requirement of the SiC switches. A list of the key components used is listed in Table 4.6.

As discussed in the earlier chapter, there are two kinds of EMI that are commonly tested, conducted, and Radiated EMI. To better understand the noise performance of the new setup when the new switching methodology is used, measuring the conducted EMI performance will help source a contrast between the conventional and proposed switching methods. To measure conducted EMI, Line Impedance Stabilization Network (LISN) units are used. The working principle of LISN and its application has been described in detail in [22]. The detail of the LISN used in the experiment can be found in Table 4.2.

Figure 4.12 shows the line diagram of setup configuration for testing the performance of a DC-DC converter setup. This setup can be configured to test all the different topologies

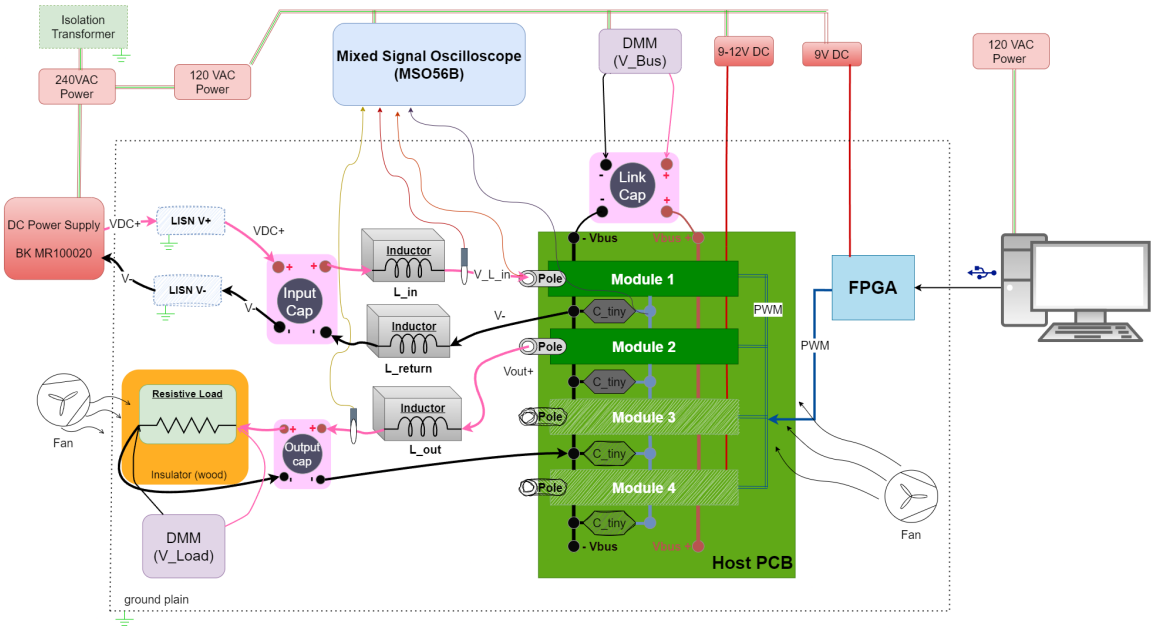

Figure 4.12: SiC DC-DC Test Setup block diagram

discussed in this work. Note that all the measurement equipment and power supplies are connected to the same power source to minimize the noise from unwanted ground loops. The black dotted section shows the ground plain where the LISN devices are mounted. In this configuration, the LISN devices are placed in between the input power source and the source-sided converter modules. This permits the measurement of the conducted EMI returning to the power source. This setup aims to perform a comparative study on how the system EMI performance concerns conventional and proposed switching strategies. A combination of multiple tests, measurement instruments, and probes are used to measure various parameters from the test setup. When the passive probes for the MSO are being used, the LISNs device is bypassed. Similarly, when the conducted EMI measurement is taken from the LISN, no additional passive probes must be used to take any measurements from the test setup. This protocol is followed to ensure that no unintended current loops exist

between the scope and the DUT, ensuring that the front end of the MSO is not damaged.

When measuring conducted EMI, due to the presence of a high inductance value, if there are any sudden changes in current, there is a high likelihood of occurrence of high voltage spikes on the measurement channel that could destroy the sensitive input ports of the instruments. Hence, a combination of a transient suppressor and bandpass filter is used. When testing switching devices rated for high power, it is a highly recommended device recommended by the instrument manufacturers.

4.3.1 DC-DC Testing

The new experimental setup is first configured to test DC-DC Boost Buck conversion. Two of the newly designed half-bridge modules are connected to the host PCB, where the first module acts as a boost converter, and the second module performs the buck operation connected to the resistive load network. Both the conventional and the proposed PWM modulation strategies are tested using this setup. The new setup is designed to handle about $1000W$ compared to the setup that used Si MOSFET, which is about $500W$. After conducting preliminary setup debugging and testing, the operating parameters for the converter setup are chosen as follows.

The input voltage $v_S = 300V$, input current $i_S = 2.5A$, capacitor voltage $V_{C-link} = 500V$, output voltage $v_L = 200V$, and switching frequency, $f_{SW} = 15kHz$. A 56 Ω, 1000W rated resistor is used as the output load. Each pair of $10mH$ is connected separately from the source and load sides. A pair of $470\mu F$ capacitors are connected in parallel at the input side to provide a stiff input voltage signal. Similarly, the same type of capacitor configured

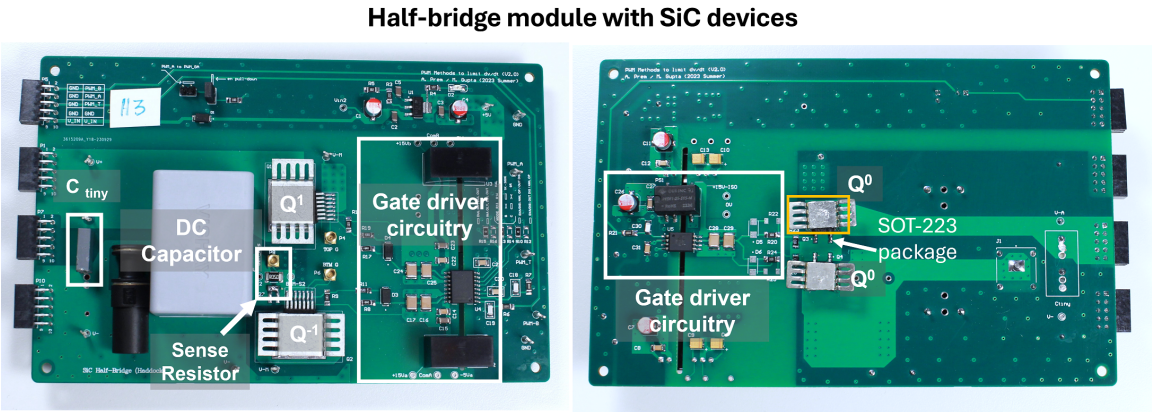

Figure 4.13: The prototype half-bridge module using SiC devices

in series was connected in parallel to the load to filter out some of the high-frequency voltage noise. For these experiments, an optically isolated probe (TIVP02), with the 10X probe tip, is used to measure the voltage across the shunt resistor placed in series with the bottom switch to measure the amount of current flowing through the source side bottom device of the half-bridge module. Using the IsoVu probe with the high bandwidth coaxial probe time and the Micro-miniature coaxial (MMCX) connector as a test point offers high bandwidth and common mode rejection compared to using the differential probe. The close-up images of the half-bridge modules are shown in Figure 4.13. The major changes to note in comparison with the former design in Figure 4.4 are layout, the addition of C_{tiny} on the board, the top and bottom devices on one side of the PCB, and the use of MOSFETs rated for lower power with smaller footprint Small-outline Transistor (SOT)-223 package. The list of key components and their details are provided in Table 4.6.

Table 4.6: List of the manufacturer part numbers used in the laboratory-scale prototype 2 with SiC bases half-bridges

Parameter	Manufacturer Number	Key Ratings
SiC MOSFET	UF3C120150B7S	$R_{DS} = 0.15\Omega$, $t_r = 5ns$, $t_f = 7ns$, $t_{rr} = 24ns$
Si MOSFET	IPN95R2K0P7ATMA1	950V, 4A, $R_{DS} = 2\Omega$, $t_r = 13ns$, $t_f = 18ns$, $t_{rr} = 337ns$
SiC Gate Driver	NCP51561BADWR2G	Isolated, 4.5-A/9-A
SiGate Driver	UCC5304DWVR	Isonalte, 4A/6A
Bulk Capacitor	Chemi-con 19XH4M	400VDC, 470μF
C-link Decouplning	MKP1848SE61090JP4F	900VDC, 10μF
Tiny Capacitors	R76TF12705050J	1600V, 2.7nF
	R760F1100SE00J	1000V, 1nF
	R76QF056050H0J	1000V, 560pF
Filter Inductors	C-59U	10mH, 12.5A

Figure 4.14 illustrates the contrast in voltage and current signals between the rise and fall time for the conventional and proposed control strategies measured across the source side bottom switch Q_S^{-1} during the switch turn-off and turn-on events. Unlike the transition trend observed in the conventional case of the Si test setup in Figure 4.5, the SiC device has a pseudo-trapezoidal switching characteristic. In other words, one of the transition edges is much slower than the other transition edge. Further investigation revealed that this is happening due to the device characteristics under the low current scenarios. After running the conventional case at 2.5x the planned operating power by decreasing the load resistance by about 2.5x times, the voltage signal had a symmetric behavior, and the observed rise and fall time agreed with the values provided in the device datasheet. More optimization and investigation were unnecessary as it was beyond this project's scope.

From the same set of voltage plots in Figure 4.14, it can be observed that the transition

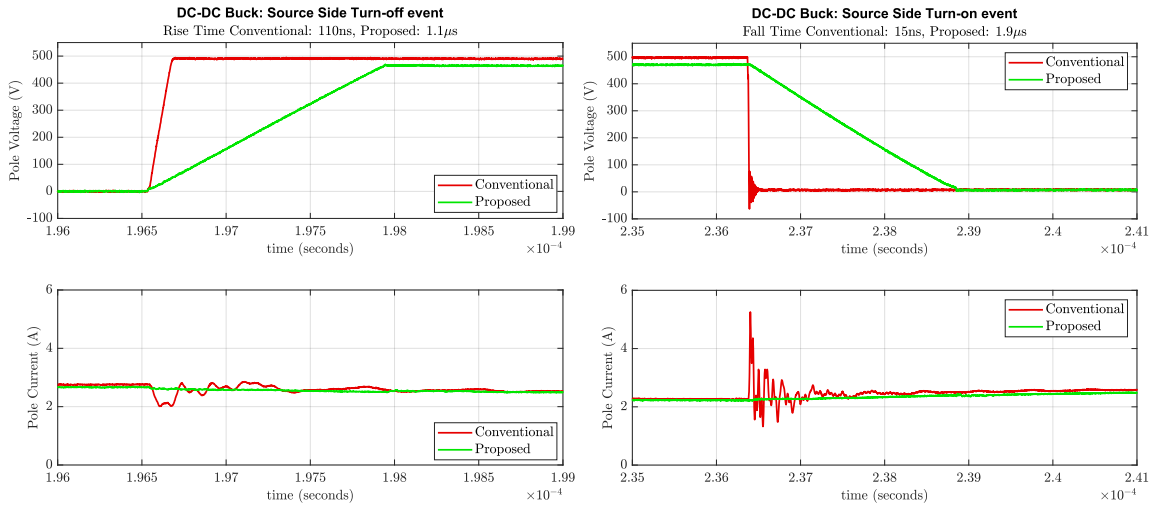

Figure 4.14: Experimentally measured Q_S^{-1} switch turn-off (left) and turn-on (right) transition with the conventional (red) and the proposed (green) approach where the voltage transition time is 110ns and 1μs respectively. The bottom waveforms illustrate noise propagation to the pole current (i_S) with the conventional (red) and the proposed (green) PWM method.

edges for the proposed case (green trace) are tuned as compared to the conventional case transition edges (red trace). The proposed case voltage signal rises with a slope of $500V/1\mu s$ and falls with $500V/1.9\mu s$. In contrast, in the conventional case, the rising slope is about $500V/110ns$ and falls much faster at $500V/15ns$ respectively. Some ringing is observed in the conventional case falling edge, as the fall transition is much faster than the rising transition. As evident from the pole current signals, just like in the case of Si test setup, the noise in the current waveform is eliminated in the proposed case scenario. In comparison, in the conventional case scenario, the current signal has more high-frequency noise components at the transition edges. From these plots, it is evident that the proposed case signals are significantly less noisy in comparison to the conventional switching method.

Figures 4.15 and 4.16 shows a comparison of the Fourier spectrum of the pole voltage (Q_S^{-1}) and current (i_S) during the DC-DC Buck mode operation of the converter for the

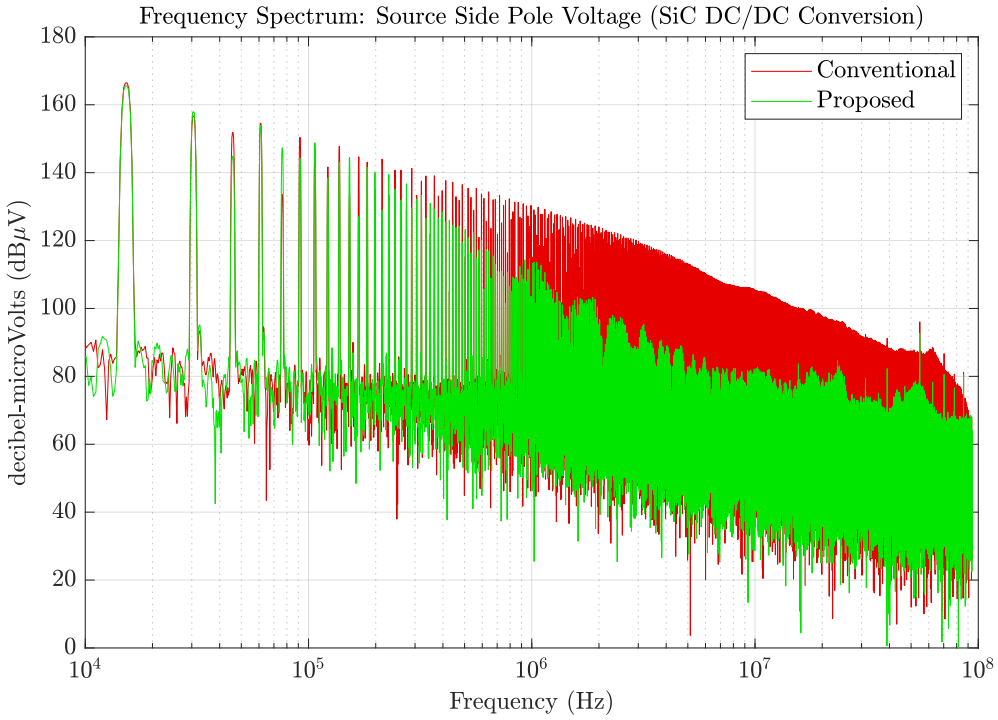

Figure 4.15: Source Side Bottom Device Pole Voltage Spectrum obtained from SiC test setup

same operating point as mentioned earlier in the section. Observing the difference between the conventional switching (red plot) and the proposed switching (green plot) strategy, approximately 15-20dB+ reduction in noise is observed in the proposed case plot for frequencies ranging from 1MHz to 10MHz. On observing the source side pole voltage across Q_S^{-1}) spectrum plot in Figure 4.15, there is about 20dB+ noise reduction in the range of 1MHz to 10MHz frequencies. Based on how the edges are tuned in the proposed case, the spectrum falls at 20dB/dec until 200kHz, then drops at 40dB/dec. However, for the conventional case, the spectrum begins to fall at 40dB/dec after the cut-off frequency of $\frac{1}{\pi t_t}$ (roughly 30.4MHz).

Figure 4.16 showcases the Fourier spectrum of the source side pole current, i_S, of Figure

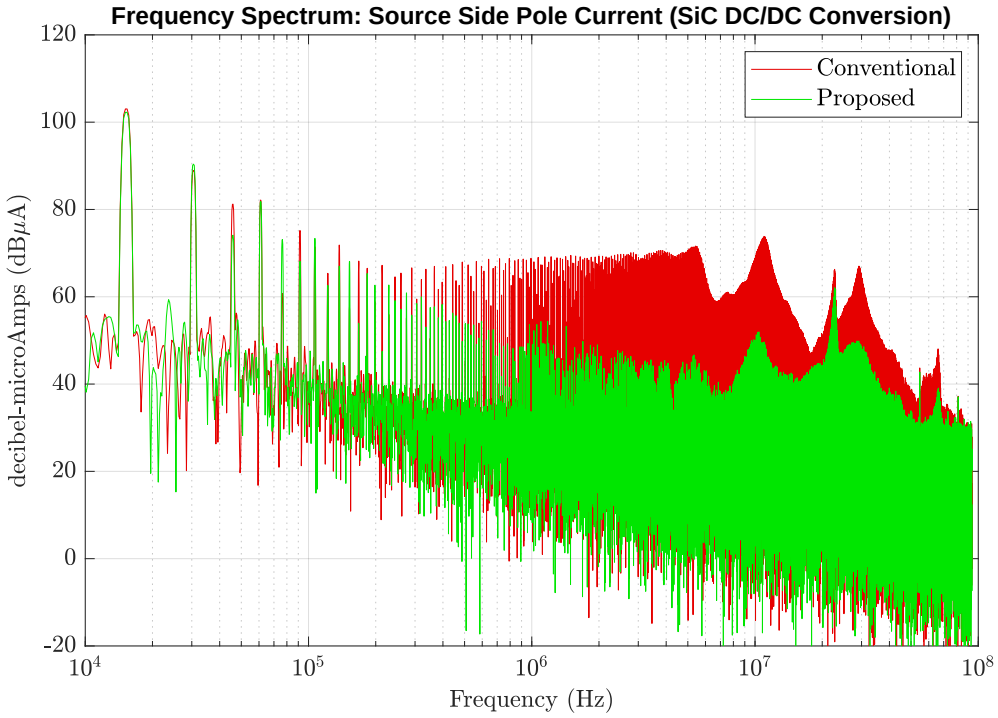

Figure 4.16: Source side pole current frequency spectrum obtained from DC-DC buck converter setup

4.14 (bottom plots). The noise reduction observed in the time-domain waveforms is readily confirmed from its Fourier spectrum plot with a difference of about 20 to 30dB between the proposed and conventional cases. From Figure 4.17, it is evident that ZVS is achieved during the proposed case operation.

The overall performance of the DC-DC Buck converter is summarized in Table 4.7. From the experimental results, SiC devices have performance improvement over Si based MOSFETs. With the conventional case switching method, an overall 92% efficiency, whereas for the proposed case, an overall efficiency of 93% is achieved. Here, the measured efficiency improvement in SiC is lower than Si because SiC has much lower switching losses, and the converter was running at a lower switching frequency of about 15kHz. Higher gains

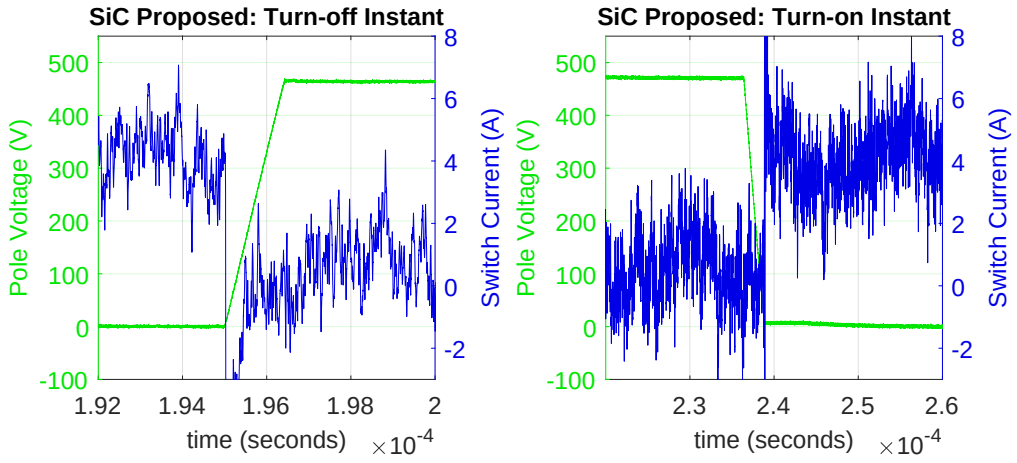

Figure 4.17: Experimentally measured switch voltage (green) and current (blue) waveforms during turn-off transition (left) and turn-on transition (right) illustrating zero-voltage switching operation on the SiC device test setup during DC-DC buck operation

are expected when a faster switching frequency is selected.

Table 4.7: List of measured parameters during buck mode of operation of the SiC test setup

Parameters	**Proposed**	**Conventional**
Vin	300 V	300 V
Iin	2.41 A	2.48 A
Pin	723 W	744 W
Vout	193.7 V	196 V
Rout	56.33 Ohm	56.33 Ohm
Iout	3.42 A	3.46 A
Pout	662.5 W	678.2 W
EMI Noise Spectrum	up-to 20dB quieter	Baseline
Measured Losses	*60.5 W*	*65.8 W*
Efficiency	*93 %*	*92 %*

Figure 4.18 shows the contrast between the measured conducted EMI spectrum of the conventional (red or orange waveforms) and the proposed (green waveform) switching strategies for the range of 100kHz to 40MHz. The pair of LISN devices are placed between the source side converter and the input high-power DC supply, MR100020. The spectrum is obtained by plotting the spectrum view of the time domain signal measured using the

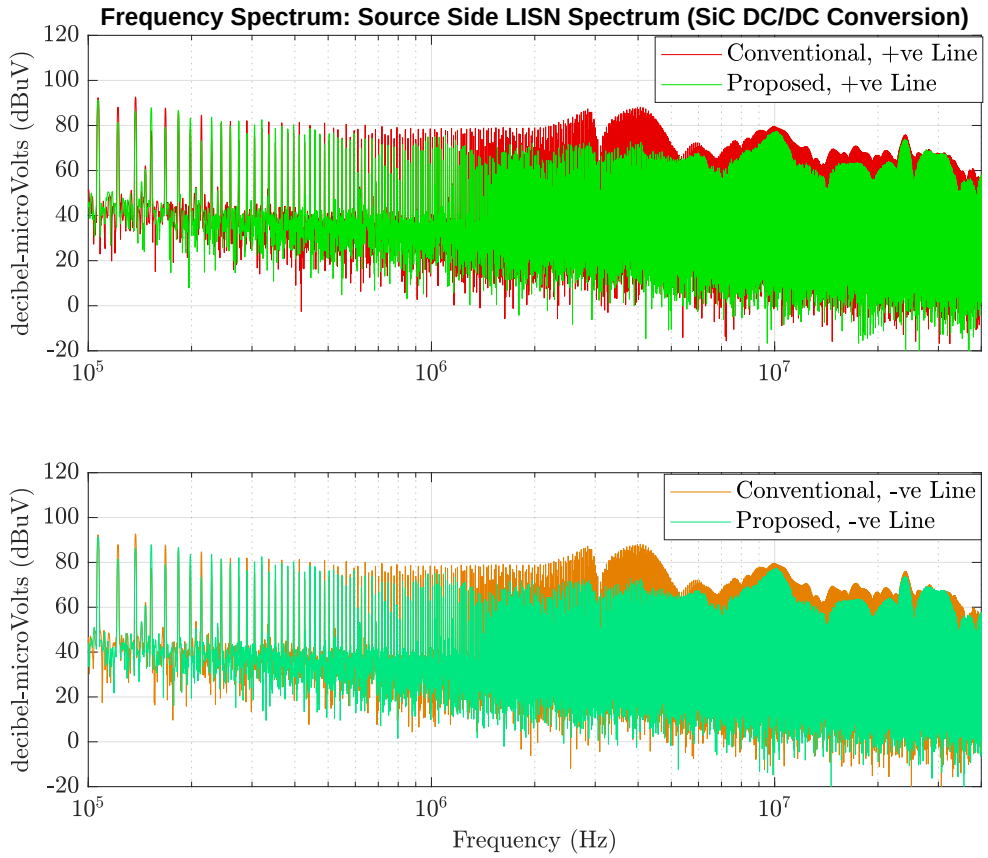

Figure 4.18: Source side LISN Spectrum comparison for DC-DC Buck operation on the SiC test setup

oscilloscope. The top figure presents the measured spectrum across the positive input line, and the bottom figure presents the spectrum measured across the return path. In both positive and negative current plots, there is a reduction in conducted EMI in almost all frequencies. For the frequencies in the range of 1MHz to 20MHz, there is about a 5dB to 20dB reduction in noise for the proposed case compared to the proposed case in both the positive and negative lines. A similar signature can be observed in the source side pole current spectrum in Figure 4.16, which further strengthens the claim that the proposed PWM control strategy has great potential to reduce electric noise right at the generation source.

4.3.2 DC-AC Testing

DC-AC topology is more practical for traction and grid-connected electric power conversion applications. The working principle of DC-AC topology is described in detail in Section 4.2. The DC-DC test setup can be easily upgraded to a DC to AC topology by adding two more half-bridge modules to the host PCB. Figure 4.19 shows the experimental test setup assembled in the lab. The setup is more complex compared to the setup that was used to

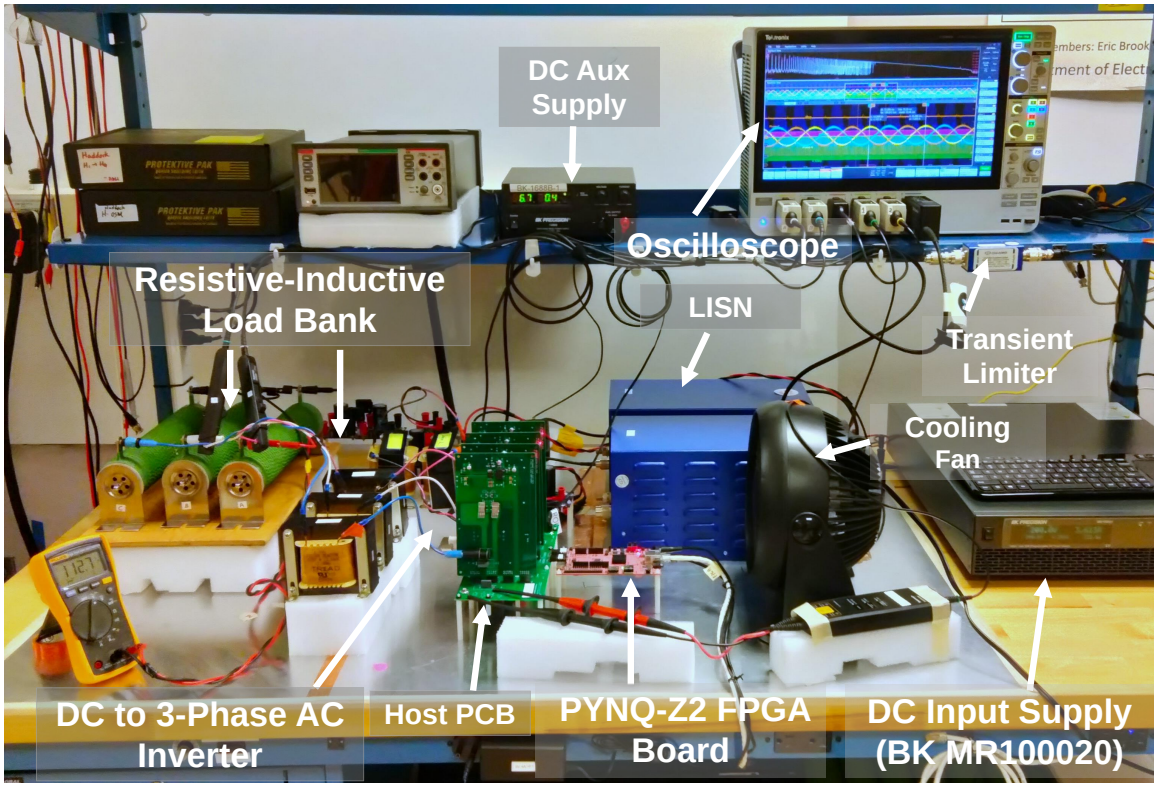

Figure 4.19: The prototype converter setup for DC to 3 phase AC topology using SiC devices

test and compare the switching strategy performance of the power converter setup based on Si MOSFETs as shown in Figure 4.9. The resistors used in the setup are configured in a star configuration. Inductors are placed in series with each phase to ensure a stiffer current output.

The control implementation used for the system is very similar to the approach used for the Si setup, with some minor design and implementation changes and bug fixes. The host PCB is also slightly modified, where the equivalent C_{tiny} capacitor value is about $6nF$ instead of the $6.5nF$ equivalent capacitance present in the DC-DC converter setup. For both DC-DC and DC-AC test cases, the tiny capacitor value is deliberately kept close, and operating parameters are chosen in such a way as to keep the i_s and i_l consistent across the source side and load side half-bridge modules for both DC-DC and DC-AC conversion setup. This way, the voltage transition characteristics of the device are similar. However, for the DC-AC setup, as the output current is alternating, as we are using an open-loop controller implementation, the tuning parameters of t_c and t_d from Figure 3.13 have to account for the edge case scenarios. The control PWM signals are optimized to run the DC-AC converter for an input voltage $v_S = 200V$, bus voltage $V_{C-link} = 400V$, AC output RMS line to neutral voltage of $110V$, and switching frequency, $f_{SW} = 15kHz$ and line frequency of about 60Hz.

The three-phase AC currents measured from the experimental DC-AC setup with the conventional (top plots) and the proposed (bottom plots) modulation strategies are presented in Figure 4.20. Observing these two waveforms (left top and bottom), there is a noticeable difference in the noise present in the current waveforms. To emphasize further, the zoomed-in current waveform when Phase-C is at its peak, the difference in noise is clear, and the worst-case amplitudes are marked in orange for both cases.

Figure 4.21 shows the contrast between the conventional case (red waveform) and the

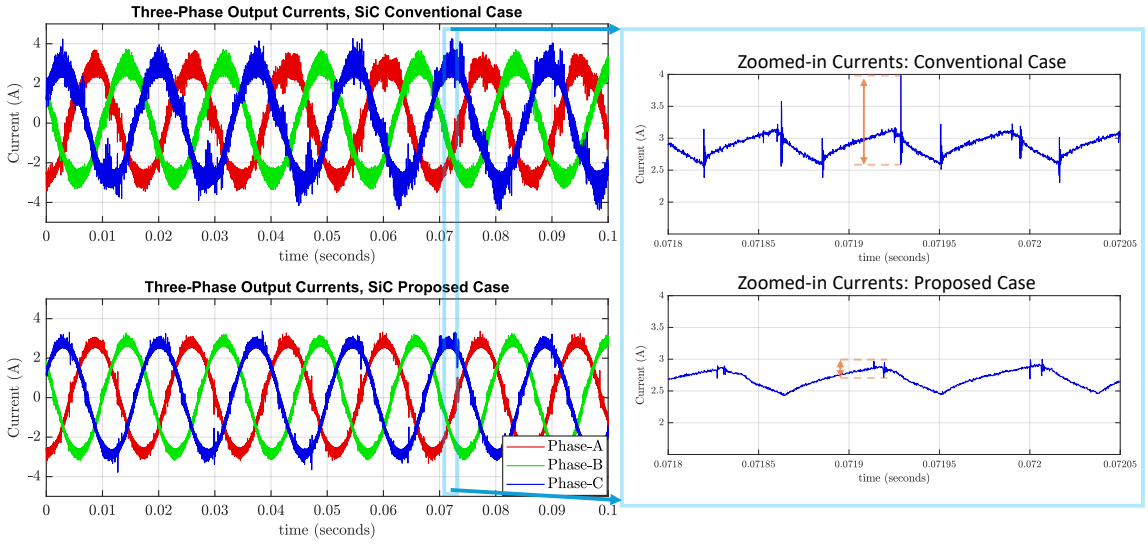

Figure 4.20: The three-phase AC waveforms with the conventional (top) and proposed (bottom) modulation strategy from SiC DC-AC converter

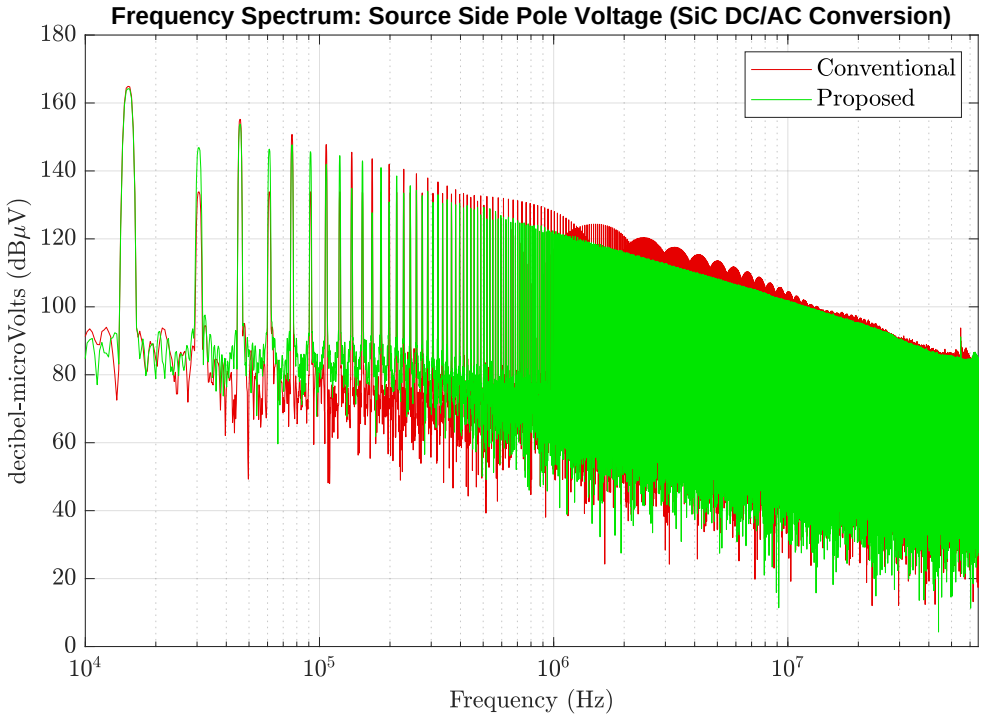

Figure 4.21: The frequency spectrum of the trapezoidal-shaped source side switch voltage (green) compared against the conventional case (red).

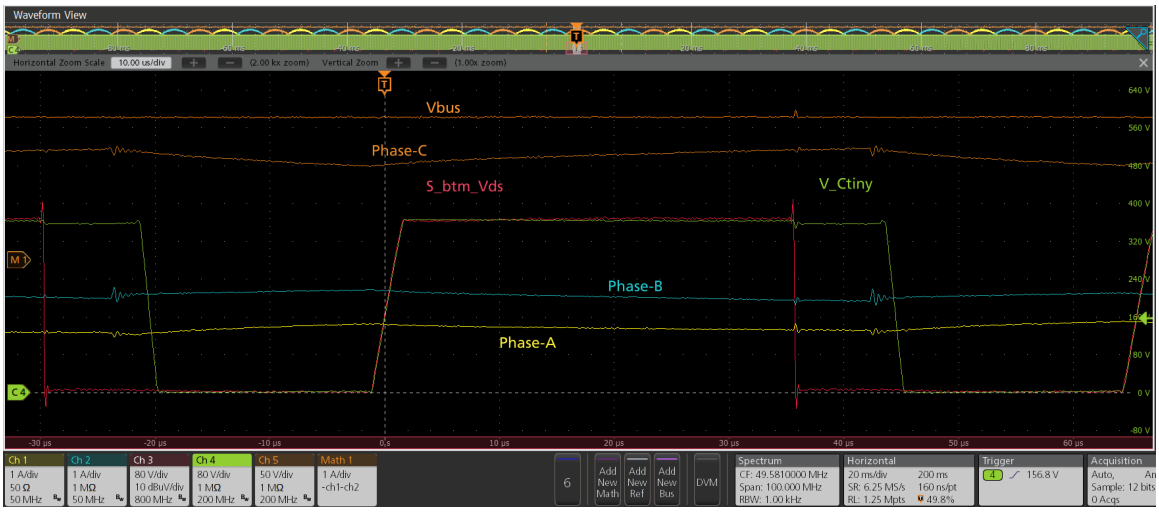

Figure 4.22: The waveform snippet obtained from the MSO for the DC-AC proposed case focusing on source side bottom switch, Q_{DC}^{-1}, the voltage on CH3, C_{tiny} voltage on CH4, the three-phase output current waveforms on CH1, CH2 and Math1, and Bus Voltage on CH5 respectively.

proposed case (green waveform) source side pole voltage (Q_{DC}^{-1}) frequency spectrum. There is some noise reduction in the frequency range of 800kHz to 1MHz for the proposed case compared to the conventional case. However, it is not that significant compared to the result obtained from the DC-DC converter setup, as shown in Figure 4.15. In the DC-AC case, only the rising edge of Q_{DC}^{-1} is getting tuned, as clearly visible in 4.22. Due to the fast-falling transition, $t_f = 110ns$, a bit of ringing is observed at the transition beginning and end. However, the ringing is less noise than the Q_S^{-1} voltage transition portrayed in Figure 4.15. Only 50% of the transition edges of the source side half-bridge are getting tuned. Despite that, there is still noise reduction observed in the Q_{DC}^{-1} voltage spectrum of the proposed case in comparison with the conventional case Q_S^{-1} voltage spectrum from the DC-DC converter setup.

The comparison of experimentally measured proposed case frequency spectrum of Phase-A pole voltage is compared against the conventional case provided in Figure 4.23.

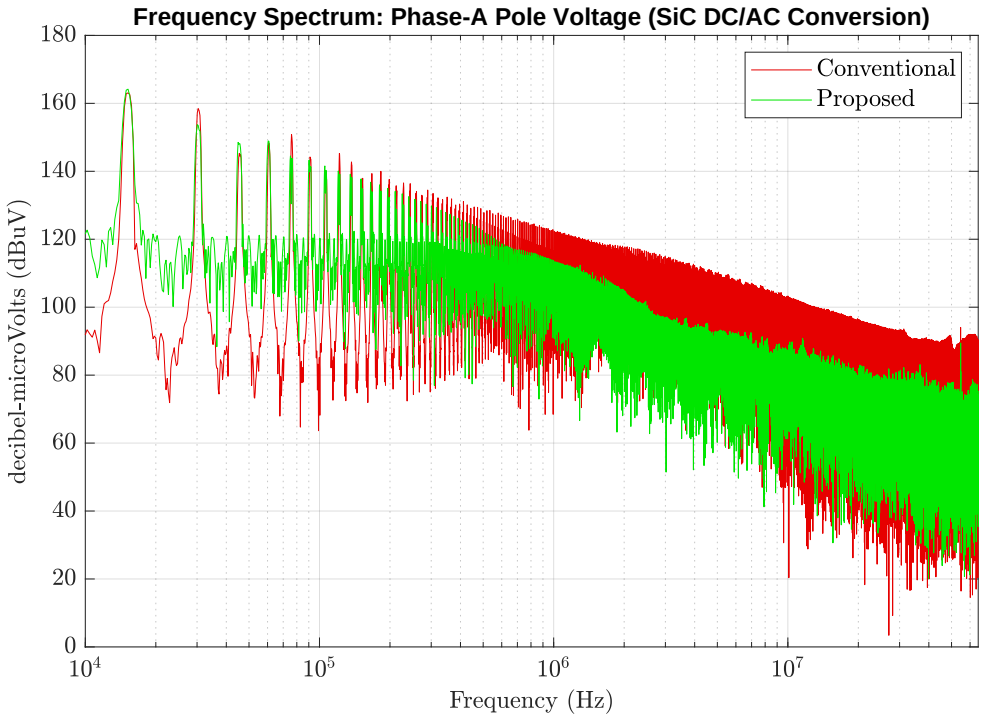

Figure 4.23: The proposed case frequency spectrum of Phase-A pole voltage (green) compared against the conventional case (red).

In the proposed case spectrum plot (in green), the signal is much quieter at frequencies above 600kHz compared to the proposed case spectrum in Figure 4.21. The load side device voltage transitions are tuned roughly 75% of the time compared to the load side. Further, about 50% of the time, when the switches are active, both the rising and falling edges are tuned. This is evident from both 4.23 and the channel 3 waveform in Figure 4.24. Overall, the load side phase voltage spectrum is about 15 to 20 dB+ quieter than the conventional case for frequencies ranging from 1MHZ to about 30MHz. The cutoff frequency can be shifted based on how the voltage transition edges are tuned. For the proposed case spectrum, it falls by 20dB/Dec to about 300kHz, and from there, it starts falling by 40dB/dec as compared to the conventional case, where it starts to fall by 20dB/Dec until 40MHz+ consistently.

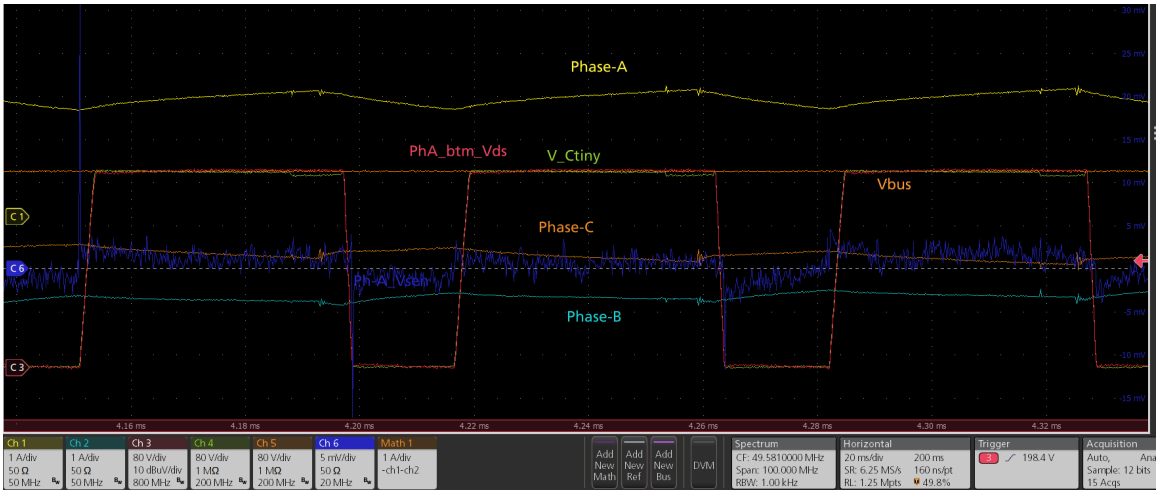

Figure 4.24: The waveform snippet obtained from the MSO for the DC-AC proposed case portraying ZVS.

The experimentally measured voltage and current parameters for efficiency calculation for proposed and conventional switching cases are compiled and presented in Table 4.8. Based on the calculations, the proposed case has better efficiency over the conventional switching strategy with an overall conversion efficiency of about *94%* for the proposed case and *93%* for the conventional case switching, respectively.

Table 4.8: List of measured parameters and efficiency calculation for the DC-AC conversion operation of the test setup with half-bridges realized with SiC MOSFETs

Parameters	**Proposed**	**Conventional**
V_{in}	200 V	200 V
I_{in}	3.56 A	3.81 A
P_{in}	711.4 W	762.4 W
V_{out}	112 V_{rms}	115.8 V_{rms}
R_{L_A}	56.33 Ohm	56.33 Ohm
R_{L_B}	54.69 Ohm	54.69 Ohm
R_{L_C}	54.94 Ohm	54.94 Ohm
I_{out_A}	1.99 A	2.055 A
I_{out_B}	2.02 A	2.064 A
I_{out_C}	2.01 A	2.079 A
Pout (total)	668 W	708.33 W
EMI Noise Spectrum	*up-to 20dB quieter*	*Basline*
Measured Losses	*43 W*	*54 W*
Efficiency	*94 %*	*93 %*

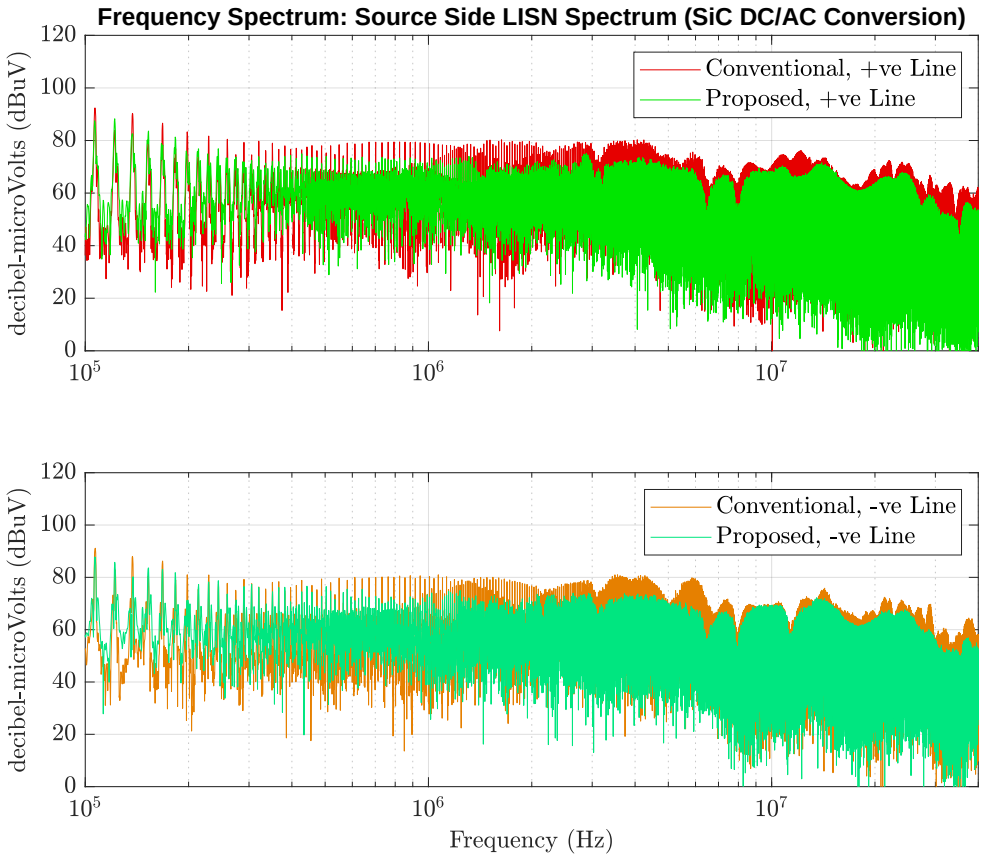

Figure 4.25: Source side LISN Spectrum Comparison for DC to three-phase AC converter

Figure 4.24 portrays the occurrence of ZVS of the Q_A^{-1} switch for the DC-AC proposed case scenario. The signals shown are the three-phase output current waveforms on CH1 (yellow), CH2 (light blue) and Math1 (brown 1), source side bottom switch (Q_A^{-1}) voltage on CH3 (Red), C_{tiny} voltage on CH4 (green), Bus Voltage on CH5 (brown 2), and sense resistor voltage measure across Phase-A half-bridge module on CH6 (dark blue) respectively. This is the instance where Phase-A current is positive. Hence, the current is flowing out of the pole. Here, the current flows out of the positive reference as we measure the voltage across the shunt resistor placed in series with (Q_A^{-1}). Hence, the voltage measured across

the shunt is inverted with respect to the reference voltage. The C_{tiny} voltage also appears to be following the active phase bottom switch (Q_A^{-1}) voltage as well, which also proves the feasibility of the proposed PWM control approach. There is negligible noise on the current signals due to the slow transitions. However, some noise is observed when other half-bridge switches undergo hard switching.

The conducted EMI of the DC-AC three-phase inverter measured at the DC input side is presented in Figure 4.25. The top plot compares the proposed and conventional case of the conducted EMI on the positive input line. In contrast, the bottom plot showcases the comparison of EMI for these two cases on the return path. In both the top and bottom plots, the proposed switching method has better EMI performance over the conventional switching strategy. However, in comparing this plot with the EMI performance of the DC-DC system shown in Figure 4.18, more noise is conducted from the DC-AC as there are more switching event occurrences. In both cases, the LISN spectrum is not compared against any standards as it is beyond this project's scope.

4.4 Summary

This chapter presents the experimentally measured observations from two sets of test setups. Half-bridge modules realized using Silicon-based devices in Boost-Buck configuration are tested in the first setup. An improved converter efficiency from 78% to 87% without additional optimizations was observed with the conventional and proposed cases, respectively. A 20dB to 35dB reduction in the switching noise is also observed. The same control technique

was extended to a DC to three-phase AC converter topology, and about 9% efficiency improvement was observed with the proposed approach compared with the conventional case. A similar 20dB+ switching noise reduction in pole voltage and current is observed.

The second set of test setups tested the possibility of extending the proposed control approach on the same converter topology but using silicon carbide MOSFETs. These devices have higher efficiency due to low conduction loss and switching losses. The testing results on a DC-DC Boost-Buck and DC-AC three-phase configuration setups showed about a 20dB+ reduction in noise at higher harmonic frequencies without adding any passive filters. The EMI performance of the converter with the SiC bases half-bridge modules was also tested, resulting in better performance with the proposed control approach. The proposed topology also shows a 1% efficiency improvement compared to the classical switching approach. With the chosen set operation point, an average converter efficiency of about 94% was achieved with the proposed DC-AC three-phase converter configuration. The main focus is to compare how well the proposed PWM switching method performs against the classical switching method. All the experimental measurements validate that the proposed control method outperforms the conventional switching method in the performance metrics of converter efficiency and EMI. Most noise mitigation filters can occupy about 30% of the converter volume. This means that with further optimization, we can extract better efficiency from these power converters, dramatically improving power density and better thermal performance.

5 Conclusions and Future Work

5.1 Conclusions and Contributions

5.1.1 Intellectual contribution

The primary contribution of this work is to present a new PWM control technique for DC-DC and DC-AC power converter topologies to reshape switching voltages to overcome the disadvantages of the fast transition times without increasing switching losses. In the traditional approach, the slow transition edge of the switching device leads to higher switching losses as the switching frequency increases. However, with WBG, devices with much faster transitions lead to lower switching losses, enabling the converter to operate at a higher frequency, thereby allowing the use of a smaller filter size and increasing power density. The downside is the drastic increase in switching noise. The conventional barriers are overcome with the proposed control approach as the new topology allows faster switching, slow transition edges, lower switching noise, and higher density.

With the presented experimental results, the proposed approach can be used in designs with both Si and SiC devices. With Si devices, an efficiency improvement of about 8% to 9% with noise reduction of 20dB+ is achieved, whereas with SiC devices inherently being more efficient, still observed an improvement of 1% to 2% improvement in efficiency and about 20dB+ noise reduction as well.

5.1.2 Anomalies and Weakness

In this work, the performance of the switching converter operating under the proposed control technique is evaluated only for a set operating point with constant loading conditions. The thesis aims to characterize and assess the performance of the proposed approach and compare it against the classical control technique. Using a constant value for tiny capacitors also limits the power range at which the converter would perform well.

For the proposed control technique to work correctly, precise synchronization among multiple modules is required, which can further increase the design complexity in the real world. The development of faster and cheaper microcontrollers and control drivers enables more precise control of these elements. The PCB layout and controller design complexity of the proposed topology is slightly higher compared to the classical half-bridge topology. This can increase the time required to design, test, and debug the system.

5.2 Future work

5.2.1 Optimization

An optimized implementation of the control technique must be pursued for this technique to be fully adopted in an embedded system. The cost implications of the additional switches and filter requirements and system-specific and application-specific cost-benefit analyses must be considered in future studies. The proposed control strategy cannot tune all the switching transitions; looking into solutions for tuning all the switching transitions of the

modules will be highly effective in improving the efficiency and more or less drastically reducing EMI related issues.

5.2.2 Closed-loop Control

Implementing a closed-loop control would be attractive, opening the avenue for evaluating more complex testing cases with variable loading conditions. Investigating electrically tunable capacitors would be another practical approach to testing and evaluating performance, aiding closed-loop control. At the current stage, the converter works best at chosen optimal operating conditions, and all the testing presented in the work only performs single-directional power transfer for the DC-DC topologies. However, source-to-load bidirectional power transfer for all the topologies is an attractive path to pursue, which would add a bit more complexity to the control system.

5.2.3 Monolithic Integration – A Long Term Vision

Another attractive path to pursue is to monolithically integrate the additional low-power circuitry (middle switch) that handles <2% rated power of the active switches along with the tiny capacitor into a single half-bridge device package design. There are already single-package half-bridge modules available in the market, and it is a matter of time and persistence before this design idea can be integrated into a single package. This is a multi-disciplinary undertaking; however, if it can be successfully pulled off, it takes away the design complexity of component placement and signal routing complexities on the PCB. Most parasitic inductance-related issues with the PCB layout can be avoided, and more

precise control capability can be achieved. This will drastically improve the switching converters' overall efficiency and noise performance.

5.3 Summary

This thesis presents a new control method for reshaping the switching voltages, with minor modifications to the classical converter topology, which overcomes the disadvantages of fast transition time without increasing the system's losses. The theory behind the implementation is discussed, and quantitative practical experiments are carried out to prove the improvement of the overall converter with the proposed control technique compared against the classical control approach on the same system. Some of the anomalies and limitations of the proposed work that need to be addressed are also discussed, along with the actual contributions of the thesis. Finally, some of the future works that are attractive to pursue have also been put forward.

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Appendix A: Design Files

A.1 Project Repository

https://github.com/abhijeet8prem/psu-ms-thesis-design-files